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Optimization of p-$CuInSe_2$/n-CdZnS Solar Cells

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ABSTRACT

$CuInSe_2$ wafers cut from melt-growth ingots were supplied by K. Bachmann under SERI subcontract #XL-4-04041. CdS was deposited onto the wafers to make $CuInSe_2$/CdS heterojunctions. Some wafers were treated in an Se atmosphere to lower the resistivity and to homogenize properties through the wafer. Devices of over 4% efficiency with open circuit voltages over 0.45 V were made. Not all wafers were found to be single crystal.

SUMMARY

The goal of this research program was to fabricate $CuInSe_2$/CdS solar cells on well-characterized $CuInSe_2$ single crystal wafers in order to improve the understanding of thin-film polycrystalline devices. $CuInSe_2$ wafers were supplied by K. Bachmann of North Carolina State University under subcontract #XL-4-04041. The wafers were characterized in terms of resistivity, carrier type, composition and crystallographic structure. $CuInSe_2$/CdS cells were made with efficiencies over 4% and V_{OC} over 0.45 volts. The limited number of wafers and their quality limited the device performance achievable within the scope of this effort.

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1. INTRODUCTION

Shay, Wagner and Kasper(1) in 1975 reported a single crystal $CdS/CuInSe_2$ heterojunction solar cell with a conversion efficiency of ~ 12%. This was a small area cell (area = 0.79 mm^2) that had a V_{oc} of about 0.5 V. Devaney et al.(2) has reported thin-film (CdZn)S/$CuInSe_2$ solar cells with ~ 12%. These devices have high short circuit currents (the quantum efficiency appears to be greater than 90%), but the V_{oc} is about 0.44 V. Recently, Potter et al. has reported a thin film $CuInSe_2$/CdS/ZnO cell with V_{oc} = 0.487 and = 11.2%(3).

The goal of this research program was to fabricate $CuInSe_2$/CdS solar cells on well-characterized $CuInSe_2$ single crystals in hopes of developing a better understanding of the operation of this device. The program had limited success since a considerable effort was spent characterizing the restricted number of $CuInSe_2$ crystals and trying to modify their properties for optimum device performance.

2. CHARACTERIZATION OF CRYSTALS

Six $CuInSe_2$ wafers were received from Dr. K. Bachmann. Four of the wafers were from the same crystal growth and the remainder from two other growths. The wafers were characterized at IEC in terms of resistivity, carrier type, composition and crystallographic structure.

Four point and hot probe measurements were made on both sides of each wafer with the results summarized in Table 2.1. Wafers 84-1 to 84-4 are from the same crystal growth. The free surface of the #84 ingot is apparently n-type but below the surface the $CuInSe_2$ is p-type. Wafers 84-1 and 84-2 are assumed to be representative of the bulk properties of this ingot.

Table 2.1

Electrical Properties of $CuInSe_2$ Wafers

Wafer #	Thickness cm	Resistivity/Type side 1 Ω-cm	side 2 Ω-cm
84-1	0.122	0.65/p	0.66/p
84-2	0.120	0.55/p	0.53/p
84-3	0.125	1.21/p	0.19/p
84-4	0.213	0.72/p	$2x10^3$/n
85-1	0.147	36/p	53/p
85-2	0.129	intrinsic	

The composition of the wafers was determined using EDS, and the results are summarized in Table 2.2. The EDS measurement is made using thin-film $CuInSe_2$ standards, and thus there may be some error in the absolute value of the composition. The relative error in the measurement is estimated to be about 6%.

Table 2.2

Composition of $CuInSe_2$ Wafers

Wafer #	% Cu	% In	% Se
84-2	27.2	25.6	47.3
85-1	27.6	25.9	47.5
85-2	27.2	25.6	47.2

All the wafers appear to be about the same composition and are slightly Cu rich. This is somewhat surprising in light of the variation in resistivity.

The crystallographic orientation and perfection has been examined on four wafers, 84-1, 84-4, 85-1 and 85-2 using back reflection Laue and X-ray diffractometer techniques. The Laue patterns obtained on sample 84-1 suggested that the wafer was not single crystal and an X-ray diffraction scan therefore was run with the results summarized in Table 2.3. The diffraction peaks due to planes other than (110) show conclusively that this wafer is not a single crystal. Similar results were obtained on wafer 85-2 and the XRD data is also presented in Table 2.3.

Table 2.3

X-ray Diffraction Analysis

d (A)	I/I_o	d	h k l
Wafer 84-1			
3.34	22	3.34	112
2.046	100	2.04	204;220
2.012	13	1.90	301
1.743	9	1.743	116;312
1.328	30	1.327	316;332
Wafer 85-2			
3.33	50	3.34	112
1.480	100	1.480	305;323

The Laue pattern obtained from the free surface of wafer 84-4 (free surface) gave an appropriate symmetry pattern for the (110) plane, however, the axis was tilted ~ 10° from the surface. (see Reference 4). The diffraction spots were neither sharp nor well-defined raising questions about the perfection of the wafer. The observed pattern shows distinct split spots, implying sub-grains with misorientations of ~ 0.5°. A diffraction scan from the free surface confirmed the essential (110) orientation with a FWHM of 0.4° for the (220) reflection.

Wafer 85-1 gave a Laue pattern that could reasonably be interpreted as from a single crystal. A standard X-ray diffraction scan using Cu k-alpha radiation yielded only one peak, the (211) at 35.8° (2.51A). This plane is 22° from the two-fold axis, (110), and visual inspection of the Laue does indicate a two fold axis ~ 22° from the center of the Laue. No further x-ray analysis was considered to be justified on this wafer.

3. DEVICE PREPARATION

Wafers were prepared for the CdS deposition using the following procedure:

1. Polish using 600 grit paper and rinse in DI water.
2. Polish using 1 μm alumina slurry and rinse in DI water.
3. Polish using 0.5 μm alumina slurry and rinse in DI water.
4. Clean ultrasonically in DI water.
5. Rinse in DI water followed by CH_3OH.
6. Etch in Br/CH_3OH (1% solution) for ten seconds.
7. Rinse in CH_3OH and blow dry with argon.

This procedure replaced the aqua regia etching reported in the Interim Report(4).

To form the CdS/$CuInSe_2$ junction, an undoped layer of CdS (~ 0.5 μm) was deposited followed by an In-doped CdS layer. In one case the entire CdS layer was doped with In. A substrate temperature of 200°C and CdS growth rate of nominally 0.5 μm/min was used for all wafers. ITO was used as the top contact to the CdS and the 3x3 mm^2 device area defined using a photolithography and etching technique.

A back contact to the cells was formed by first etching the surface in aqua regia and then depositing two gold dots. This allowed measurements between the gold dots to check that the contacts were ohmic. If a non-linear I-V was measured, the dots were removed and new contacts were formed.

4. RESULTS

4.1 Effect of Heat Treatments

Wafer 84-4 showed resistivities of 5 Ω-cm and $2x10^3$ Ω-cm on sides 1 and 2 respectively. The wafer was cut into two pieces, 84-4a and 84-4b. Wafer 84-4b was heat treated in air for 32 hours at 200°C and 22 hours at 400°C. Table 4.1 summarizes the effect of the air heat treatments on the resistivity; the 200°C heat treatment has little or no effect. After the 400°C heat treatment the resistivity of the crystal appeared to be uniform throughout at ~ 140 Ω-cm.

Table 4.1

Air Heat Treatment of Wafer 84-4b

Heat Treatment Temperature °C	Time hr	Resistivity/type Side 1 Ω-cm	Side 2 Ω-cm
as received		5/p	$2x10^3$/n
200	8	8/p	$2x10^3$/n
200	24	43/p	930/n
400	22	140/p	148/p

Wafer 84-4a was sealed in an evacuated ampoule with Se (see Appendix for description of procedure) and heat treated at 600°C for 24 hours. The Se over pressure in the ampoule was computed to be 100 torr. After the heat treatment, a Se deposit was found on the wafer surface and was removed by polishing and etching. The measured resistivity was 0.3 Ω-cm on both sides of the wafer and the conductivity was p-type.

4.2 $CuInSe_2$/CdS Devices

Nine $CuInSe_2$/CdS devices were made and the results are summarized in Table 4.2. The two best devices were made on wafers that had been treated in Se resulting in a resistivity of less than 1 Ω-cm. The best V_{OC} measured was 0.46 volts but this was on a sample with bad contact behavior as can be seen in Figure 4.1. The spectral response for this cell is shown in Figure 4.2. The response is flat over the entire wavelength range and there is no change with light bias, indicative of a good quality sharp heterojunction.

Table 4.2

$CuInSe_2$/CdS Cell Results

Wafer	V_{oc} (V)	J_{sc}* mA/cm^2	FF (%)	n (%)	Comments
84-1	0.38	22	37	3	Heat treated in Se (initial) = 0.7 Ω-cm (final) = 0.1 Ω-cm
84-2	0.32	7.6	<25	0.5	Problems with contacts: see Interim Report(4)
84-3	0.32	6.3	32	0.7	See Interim Report(4)
84-4a	0.46	~28	41	~6	$CuInSe_2$ Heat treated in Se; Problem with contacts
	0.28	30	46	4.4	After new contacts
84-4b	-	-	-	-	Air heat treatment - nearly linear I-V
85-1	-	-	-	-	In doped CdS; linear I-V;
	0.22	21	44	2.3	CdS removed; heat treated in Se
	0.25	28	26	2.1	2 hr, 200°C air heat treatment
85-2	-	-	-	-	Linear I-V; No change after 200°C heat treatment
	-	-	-	-	CdS removed; Heated in Se linear I-V

* ELH simulation at 87.5 mW/cm^2

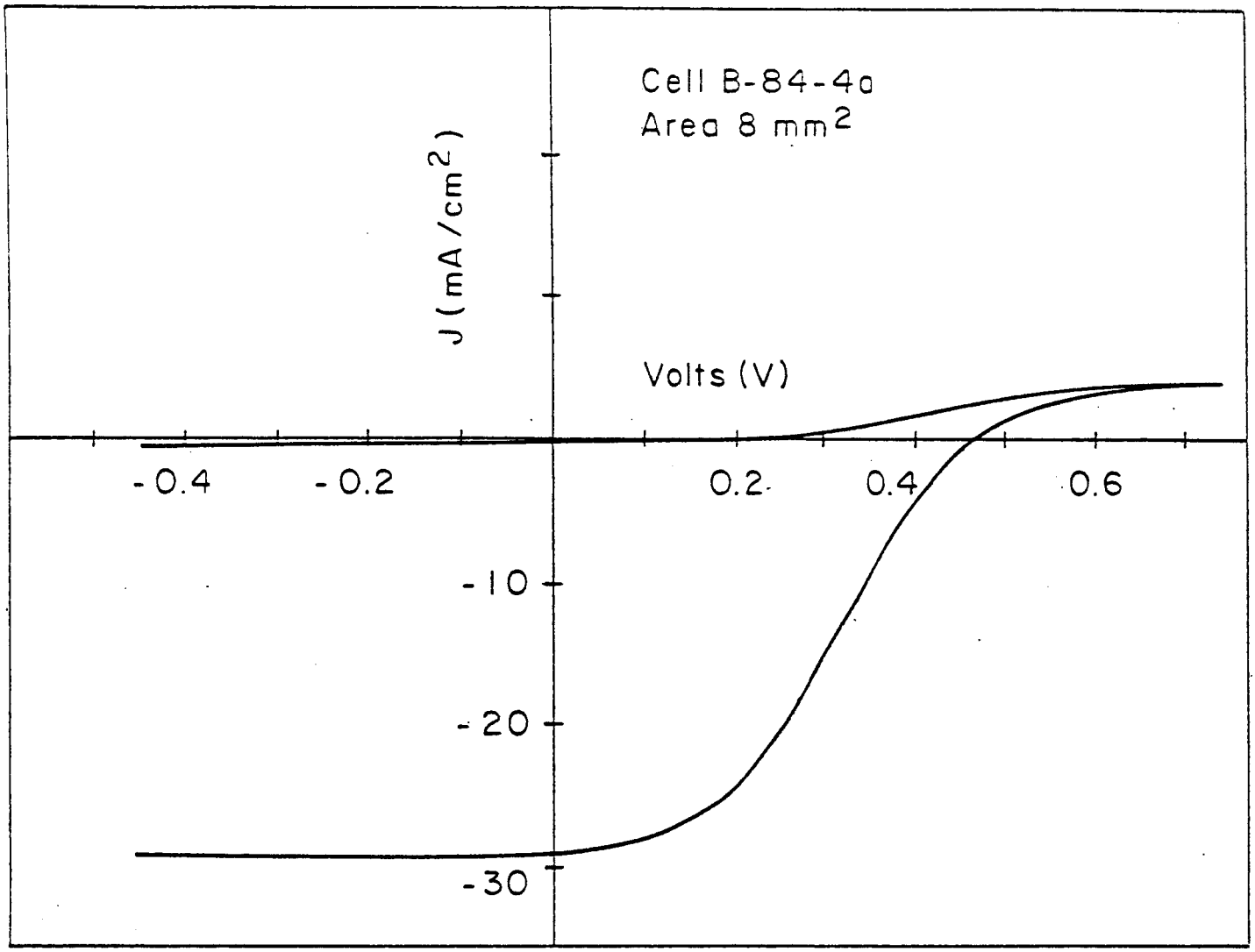

Figure 4.1. Current-Voltage response of $CuInSe_2$/CdS single crystal cell B-84-4a.

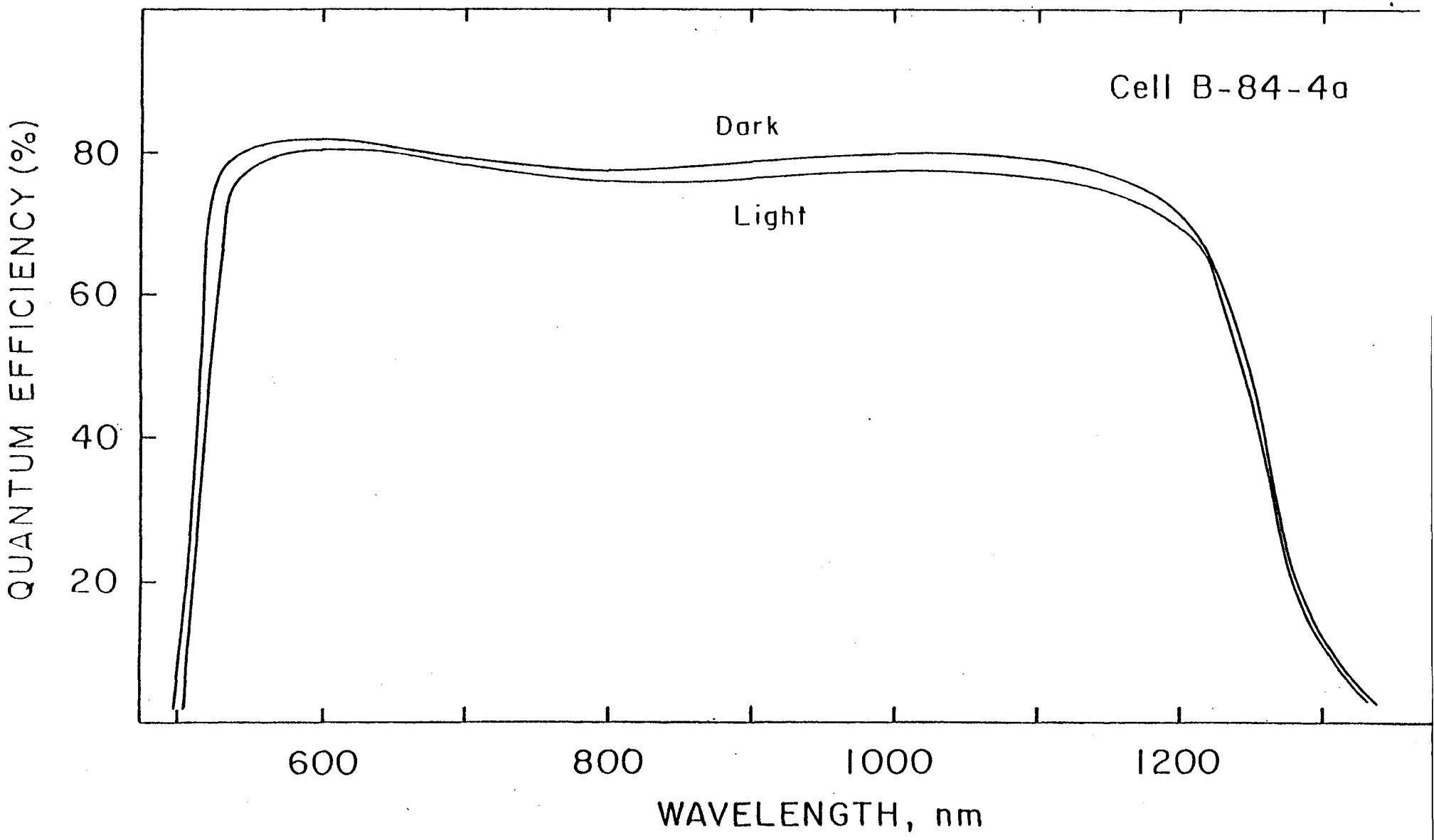

Figure 4.2. Spectral response of cell B-84-4a at short circuit current.

5. CONCLUSIONS

$CuInSe_2/CdS$ single crystal devices were made with efficiencies over 4% and V_{OC} over 0.45 volts. The limited number of crystals and the poor quality of the wafers supplied (most were not single crystals) severely limited the quality of devices which could be made. Most of the effort was spent characterizing the wafers and trying to modify their electronic properties. For future work to be successful an adequate supply of high quality crystals should be available at the beginning of the contract period.

6. REFERENCES

1. J.L. Shay, S. Wagner and M.M. Kasper, Appl. Phys. Lett., 27, 89 (1975).

2. W.E. Devaney, R.A. Mickelsen and W.S. Chen, Proceedings 18th IEEE Photovoltaic Specialists Conference, Las Vegas, (1985), to be published.

3. R.R. Potter, C. Eberspacher and L.B. Fabick, Proceedings 18th IEEE Photovoltaic Specialists Conference, Las Vegas (1985), to be published.

4. IEC Interim Report, Solar Energy Research Institute, Subcontract #XL-4-04060-1, December 1984.

APPENDIX - Procedure for Annealing $CuInSe_2$ Wafers in a Selenium Atmosphere

1. A two chamber quartz ampoule with an extension rod is prepared from 15 mm (ID) x 18 mm (OD) stock. See Figure A-1.

2. The ampoule is cleaned in aqua regia, etched in hydrofluoric acid, rinsed and dried.

3. Se pellets (5N purity) are placed in the small chamber; the $CuInSe_2$ crystal is loaded in the large chamber.

4. The ampoule is evacuated to ~ $5x10^{-5}$ torr and sealed leaving an 8 cm specimen chamber. The crystal is kept cool during sealing by water cooling that region of the ampoule.

5. The ampoule is loaded into a tube oven such that $CuInSe_2$ is held at 600°C with the Se melt being ~ 10°C cooler to minimize condensation of Se on the wafer during cool down. At 590°C, the selenium pressure in the tube is computed to be ~ 100 torr.

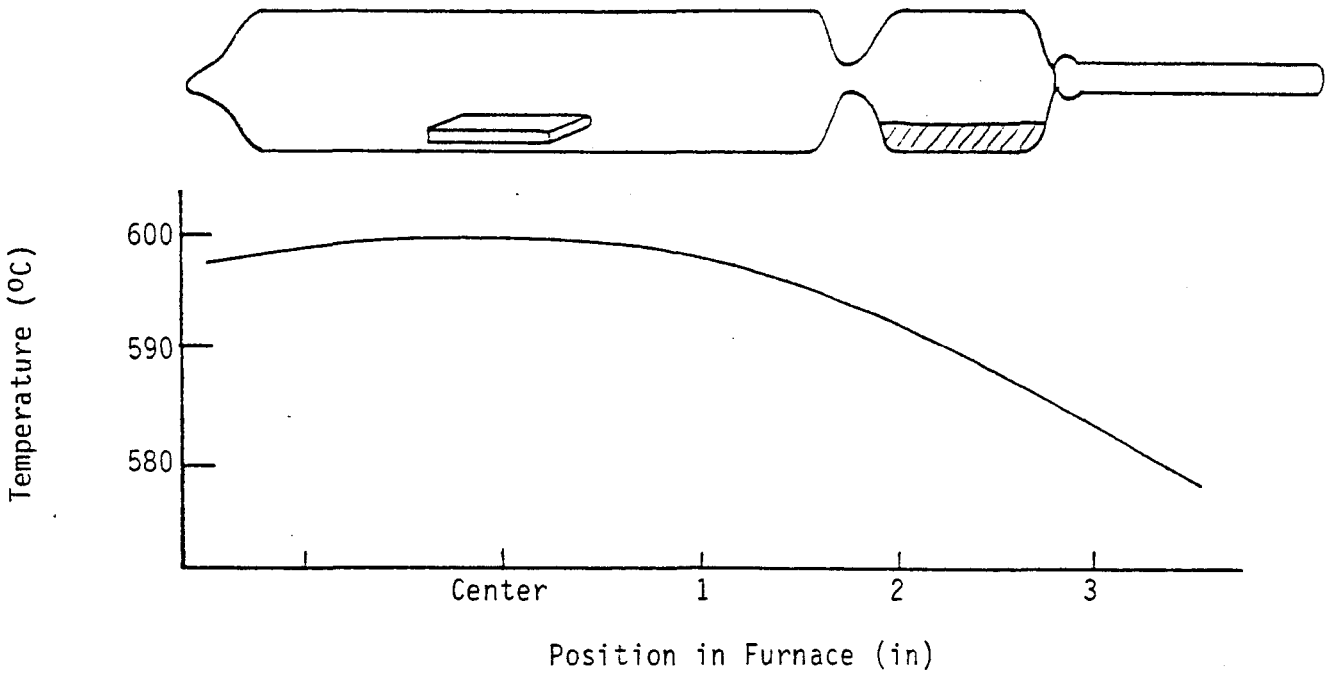

Figure A-1 Ampoule for treatment in Se atmosphere and temperature distribution in the furnace.