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MWPC DATA ACQUISITION IN THE BROOKHAVEN FASTBUS

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Introduction

For Brookhaven AGS Experiment #749, a data acquisition system to accommodate 12, 256 wire multiwire proportional chambers (MWPCs) has been built in the context of the Brookhaven FASTBUS. Information about wires hit or continuous clusters of wires hit is encoded as the centroids of the clusters and number of wires in those clusters. The encoded information is stored in a stack memory in a FASTBUS module where it can be accessed by a FASTBUS Master. Encoding time is less than 4 microseconds. Also, information (in the form of front panel outputs) as to the nature of the data is available in less than 200 nanoseconds.

System Overview

The system is made up of three components: a board which amplifies, discriminates, digitally delays, latches, and does parallel to serial conversion of the hit information in the MWPCs (latch, 16 per chamber), a module which encodes the serial data (encoder), and a simple interface board which controls communications and data flow between the latches and the encoder (interface). The latch boards are PC layout (17" × 24", with 54 ICS), the interface is a small wirewrap card (36 IC locations), and the encoder module is wirewrapped on the Brookhaven FASTBUS multi-purpose card. The system is built entirely from 10,000 series ECL components.

The latch and interface boards reside on the MWPCs themselves. Each latch board accomodates 16 wires. The encoder modules reside in a 130 pin water-cooled FASTBUS crate segment. Each module has 3 channels, that is, can encode information from 3, 256 wire MWPCs. The latch boards present, through the interface (1 per chamber), data in serial form. The encoder then performs serial to parallel conversion to obtain information in the form of centroids of clusters and the width of those clusters. This information is stored in a stack memory in the encoder module where it is available to FASTBUS masters.

Latch and Interface

Each discriminated signal is delayed in a 6 bit serial-in serial-out shift register whose shift frequency is determined by an external clock. Timing is done by adjustment of this clock frequency. For this experiment the frequency was 50 megahertz, giving about 300 nanoseconds of delay.

The outputs of these delay shift registers (16 per board) are input to a 16 bit parallel- in serial-out shift register. 16 latch boards are then daisy-chained together via twisted pair lines to form a 256 bit parallel-in serial-out shift register, which, then accommodates one chamber (extensions to more wires are trivial). The interface sits on the end of this chain.

Upon receiving a trigger from the interface, information from adjacent wires is latched (parallel entered) in adjacent bits in this register. The serial data is then shifted out by the interface by a 100 MHz clock. The interface synchronizes the clock and data and passes them, along with a control line, to the encoder via a mass-terminated ribbon twisted pair line.

Encoder Module

When the interface asserts the enable line, signifying the beginning of encoding, the encoder counts clock cycles in an 8 bit counter. When the data line is asserted, the contents of this counter (i.e., the first wire) are latched and a 3 bit counter is enabled. The latter counter registers the number of cycles for which the data line is asserted (i.e., the number of wires). A flip-flop is set if the width exceeds the capacity of the counter, that is, if more than 8 contiguous wires are hit. When the data line drops, the 8 bit wire number, the 3 bit width, and the status of the overflow bit are written to a 16 by 12 bit stack memory. If more than 16 hits are accumulated, a flag bit (stack overflow) is set. All these operations are performed sychronously with the 100 MHz clock.

The centroid of the cluster is obtained at FASTBUS readout time. To obtain the centroid, the contents of the top of the stack are input to an adder circuit which adds to twice the wire number minus one the width minus one. Then the centroid is defined as

$$\text{Centroid} = 2*(\text{first wire \#} - 1) + (\text{width} - 1)$$

so that for 256 wires there are 511 centroids. For example, if two adjacent wires are hit, the centroid is defined as the position between the wires.

There are 3 such devices in each FASTBUS encoder module. The outputs of the adder circuits along with the width information and the flag bits are multiplexed to the FASTBUS address/data lines.

In addition, the encoder gives fast information concerning the nature of the data. This is given as front panel outputs. One "ABORT" output is asserted if more than a preselected number of clusters are found in a chamber. This number is set by hardware switches. If the stack pointer is found to exceed this number during encoding the event can be aborted. Also, "VETO" outputs are asserted if there are not hits in a chamber or if there is not at least one hit in each half-plane of a chamber. These are done by allowing the encoder, via the interface, to "SPY" on the data as it moves through the 256 bit shift register in the latch boards. Every fourth bit in each half of this register is ORED together and these ORS are passed to the encoder via the ribbon twisted pair. By observing these lines the encoder can determine in the first 4 clock cycles if any data is present in each half plane. This information, then, is available in less than 200 nanoseconds after a trigger.

FASTBUS Access and Data Format

The encoder modules perform as FASTBUS slaves according to the Brookhaven FASTBUS protocol. The address of each channel is selected independently of the others by hardware switches. The individual channels are selected by decoding the 4 least significant bits of the address (AD 0-3).

To a FASTBUS master each address accesses a read-only FILO stack. The contents of the stack are the cluster centroid and width, the channel address, and the overflow flag bits. After each FASTBUS read of the stack, the stack pointer is automatically bumped. When the stack pointer reaches the bottom, a "LAST VALID" bit is returned with the data telling the master it has just emptied the stack. Note that the stack can be read through only once. There is no external stack pointer control.

After this last read the channel initializes itself and is immediately rearmed for the next trigger. If a trigger has not been received since the last trigger or if no clusters were recorded in the last encoding a 32 bit word of zeros is returned on a FASTBUS read, and the channel initializes. The module also initializes in the same way in response to a FASTBUS initialized (IT=1), broadcast clear, broadcast abort, or a front panel clear.

A valid FASTBUS read during encoding time is ignored but acknowledged by a busy acknowledge (BK=1). An invalid request is acknowledged by a negative acknowledge (NK=1). A FASTBUS initialize, broadcast abort or clear, and front panel clears are always obeyed immediately.

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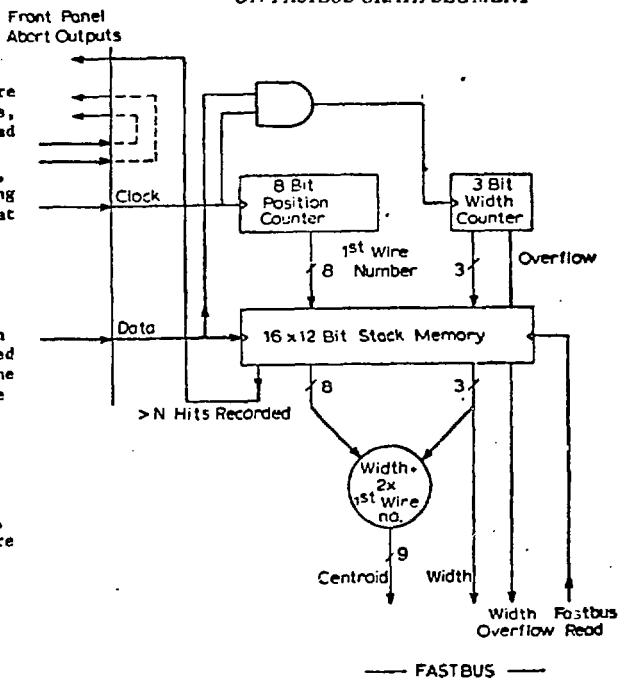
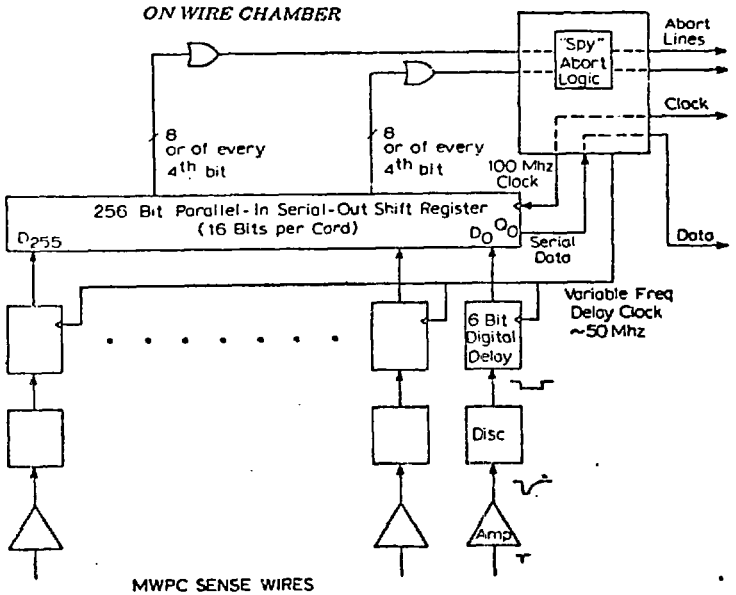
References

1. L.B. Leipuner, et al., "A Five Segment Brookhaven Fastbus System", paper presented at the Conference on Real-Time Computer Applications in Particle and Nuclear Physics, May 1983. To be published in the IEEE proceedings.

ON FASTBUS CRATE SEGMENT



ON WIRE CHAMBER



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