Multi-layer Enhancement to Polysilicon Surface-Micromachining Technology

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Abstract

A multi-level polysilicon surface-micromachining technology consisting of 5 layers of polysilicon is presented. Surface topography and film mechanical stress are the major impediments encountered in the development of a multi-layer surface-micromachining process. However, excellent mechanical film characteristics have been obtained through the use of chemical-mechanical polishing for planarization of topography and by proper sequencing of film deposition with thermal anneals. Examples of operating microactuators, geared power-transfer mechanisms, and optical elements demonstrate the mechanical advantages of construction with 5 polysilicon layers.

Introduction

MicroElectroMechanical Systems (MEMS) manufactured by technologies which leverage the infrastructure for silicon integrated circuit fabrication are rapidly expanding into a multi-billion dollar industry (1,2). Polysilicon surface-micromachining (3) is typically or ordinarily hindered in further growth by the limitation of the number of layers available for design. Thus, analogous to design with multiple integrated circuit (IC) metalization layers, the complexity of the devices that can be fabricated in a polysilicon surface-micromachining technology scales super-linearly with the number of layers. In addition to broadened design space for potential innovative designs, additional polysilicon layers readily bolster device reliability and robustness.

To clarify nomenclature, we count the initial electrical interconnect layer plus 4 mechanically active polysilicon layers and designate the process as a 5-level polysilicon surface-micromachining technology. This is consistent with nomenclature used for an externally available polysilicon surface-micromachining process (4). Here, we present a methodology which extends Sandia's currently available 4-level SUMMiT process to 5-levels, significantly enhancing our ability to create complex micro-assemblies (see Fig. 1). Examples of batch-fabricated devices fabricated by the 4-level process can be found elsewhere (5,6,7,8). This 5-level process allows the design of extremely complex micromechanical systems, with significant concurrent increase in device reliability and robustness.

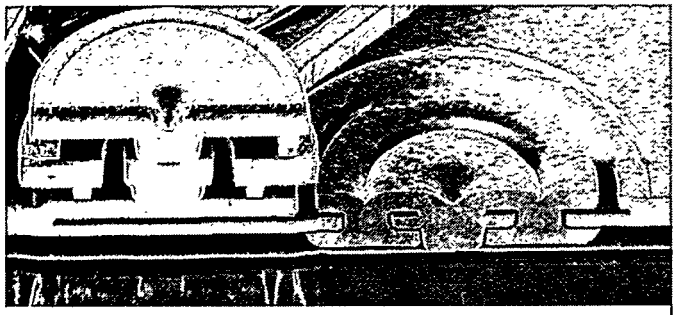

Figure 1. This SEM cross-section was formed by focused ion beam (FIB) milling through a 5-level device area. The polysilicon layers are the light films, while the dark spaces are where the sacrificial oxide films existed prior to the release etch. Nominal thickness of mechanical polysilicon layers and sacrificial oxide layers range 1-2 microns.

The 5-level process development was based on the continued extension of advanced IC process techniques to micromechanical device fabrication. For example, consistent yield and high reliability with 3 (or greater)-level polysilicon surface-micromachining benefits from planarization of surface topography. This topography, which arises from the repetitive cycle of deposition and selective removal of films used to construct the micromachines, severely curtails advancement beyond a 3-layer process. In fact, 5-layers would be virtually impossible without planarization. Chemical-mechanical polishing (CMP), which is widely used in multi-level metalization for high-density, sub-micron integrated circuits, has been successfully incorporated into polysilicon surface-micromachining for planarization (5).

To expedite process development while true 5-level microsystems were being laid out, the final level of an existing 4-level design was reproduced as the 5th polysilicon layer. This resulted in a working 5-level process that produced functional devices as demonstrated by a multi-level geared transmission with redundant top-level gears (see Fig. 2). Details on the functional improvements to these devices are provided in the section on impact on future devices.

Process Development

This 5-level technology has, as its basic process module, the repetitive cycle of deposition and definition of 2 primary films, a sacrificial silicon dioxide film and a structural polycrystalline silicon film. The deposition, photolithography, and etch processes are based on those used in standard IC fabrication, but modified for thicker, mechanically-optimized films. Thus low-pressure chemical vapor deposition (LPCVD) of polysilicon and silicon dioxide films, and reactive ion etch for film definition are used. A 5-level process in essence repeats this base sequence a minimum of

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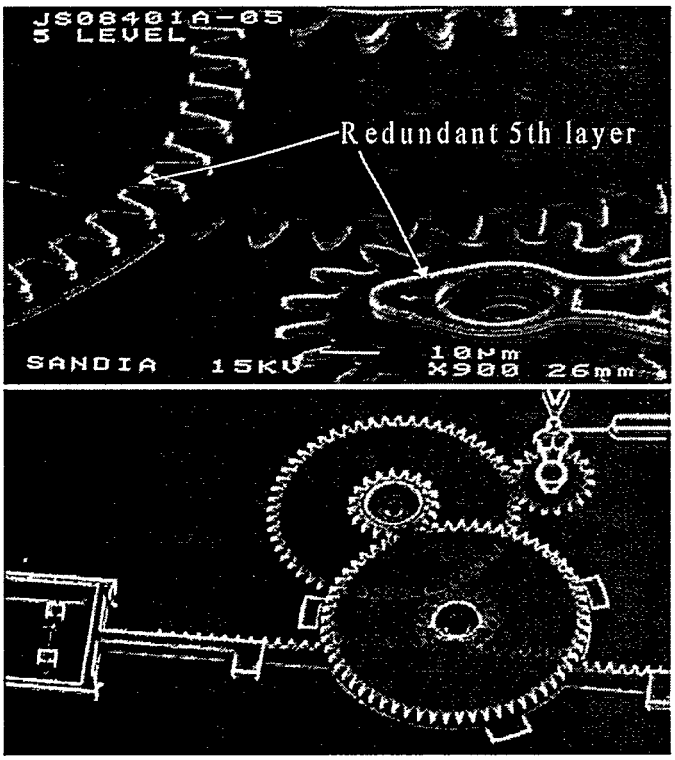

Figure 2. These SEM images show parts of a geared microactuation mechanism, a linear geared-rack, and part of a fold-up mirror (6). The top image is a close-up of the torque conversion unit, showing multi-level gears and specifically the redundant top gear layer which demonstrated the 5-level process.

5 times. Details of rudimentary polysilicon surface micromachining are described by Howe (3), while details of the Sandia 4-level polysilicon surface micromachining technology are described by Garcia and Sniegowski (5,6,9). The 5-level technology presented here is based on this 4-level technology. Key advantages of polysilicon surface-micromachining are that the process is a batch-fabrication technology that does not require piecepart assembly and that it utilizes the IC infrastructure which is capable of large-scale production. Thus, completion of the fabrication cycle entails a final release step which removes all sacrificial films to provide hundreds to thousands of ready-to-operate devices.

Surface topography and film mechanical stress were the major impediments successfully overcome by the development of a multi-layer surface-micromachining process.

A. Vertical Topography

Vertical topography is introduced by the repetitive deposition and etching of multiple films. The etches create film steps that normally are retained through the remainder of the process. This topography can produce mechanical interference between moving parts and complicates subsequent process steps. For example, mechanical interference arises when interconnecting links must pass over a structure's edge. Fig. 3 illustrates how these steps ordinarily cause mechanical interference. The subsequent film used to create an interconnecting link deposits conformally over these steps producing an overhang feature. This artifact can protrude far enough into the lower levels to create mechanical interference. Without planarization of the surfaces, link/gear interference must be accommodated by design.

In addition to the above design constraint, two significant process difficulties arise from severe topography. One results from the use of highly anisotropic plasma etch processes for the definition of the polysilicon layers. The anisotropy is necessary to obtain the desired vertical sidewalls of the polysilicon structures. However, the very anisotropy of the etch prevents the etch from completely removing the polysilicon layer from along the bottom edge of a step. This leaves behind long slivers of polysilicon along these edges, often referred to as stringers. Stringers can also produce mechanical interference or even electrical shorts. The second difficulty is problematic definition of subsequent layers over severe topography. Photoresist, the photosensitive polymeric coating used to transfer the design into the physical films, becomes difficult to apply, expose, and develop, leading to loss of resolution and definition.

The addition of chemical-mechanical polishing (CMP) planarization to the 4- and 5-level technologies is a major process enhancement from both the design and process perspectives (5). The benefits of CMP for surface-micromachining are three-fold. It eliminates the link/gear interference problem illustrated in Fig. 3. It eliminates the artifact of anisotropic etching of conformal polysilicon films over edges, i.e., stringers, since there are no steps on a planar surface. Thirdly and most critically, CMP enables evolution to a multi-level technology such as the 5-level process by eliminating the topography and associated photolithographic problems.

B. Mechanical Stress

The second critical area involves control of the overall mechanical stresses present in the wafer due to the multiple film stack. The primary concern ordinarily being wafer

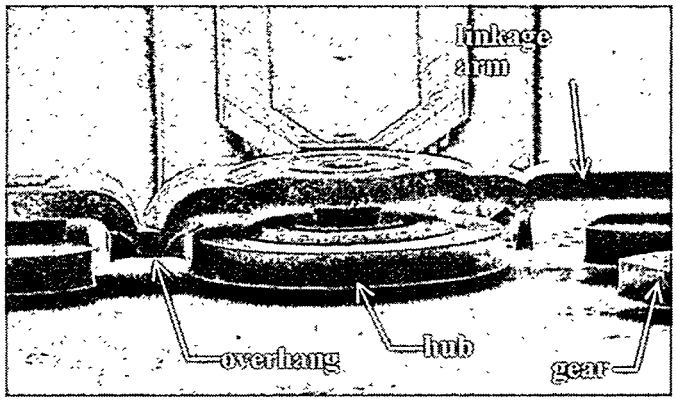

Figure 3. This SEM illustrates the artifacts generated by the conformal nature of the polysilicon depositions over prior topography (indicated by arrows).

breakage and excess wafer deformation. Although breakage is clearly catastrophic, excess wafer deformation in the form of bow or warp could preclude continued processing of the wafer as well.

The Resulting Process

Referring to Fig. 1, the cross-section of a device designed for the 5-level process clearly depicts all levels and illustrates planarization by CMP prior to polysilicon levels 4 and 5. Total stack height from the substrate is 12.5 μm, (see lower image in Fig. 4) while the greatest device thickness that can be produced is 12.0 μm. In contrast, single-level processes normally consist of polysilicon film thickness on the order of 2 μm. Thus, the stack is roughly a factor of 6 thicker which, from simple elastic beam theory, implies roughly a cubic increase in out-of-plane stiffness, i.e., greater than a factor of 100 increase in out-of-plane stiffness.

In addition, the 5th layer continues to display the same degree of extremely low film stress-gradient which leads to film curl in released structures. One of our polysilicon film processes exhibits a film curl having ≤ 150 nanometer out-of-plane deflection at the tip of a singly-clamped cantilever beam with a length of 1000 μm. This measurement is done using an interferometric technique (10). Film distortion at this extremely low level is very acceptable in optical mirror applications. Further, net in-plane stress is at the limit of our current stress diagnostic structures which detect film stress at the tens of megaPascal level (11). This implies that structures having extremely large in-plane dimensions, such as the gears in Fig. 2, continue to be viable in the 5th level of polysilicon. This is very critical to many micromechanical sensor and actuator elements.

Impact on Future Device Design

In the first processing run, the devices designed for the 4-level process continued to demonstrate full functionality despite not being specifically designed for the 5th layer. More importantly, actuation elements, such as the electrostatic comb drive (12) in Fig. 4, display the improvement in performance expected from the addition of another layer.

A. Mechanical Film Thickness

The use of thin films (2-4 μm) has often been cited as a major limitation to polysilicon surface-micromachining. Benefits resulting from increasing film thickness include greater out-of-plane mechanical stiffness which is a cubic function of device thickness, and larger in-plane actuation or transduction which are proportional to thickness. Stacking polysilicon levels provides this desirable increase in film thickness. The lower image in Fig. 4 illustrates the use of film stacking to create a central truss on the comb-drive which is orders-of-magnitude stiffer than if it were comprised of a single level. This applies to both the out-of-plane direction and in-plane deformation as well. The effect for this actuation device is that significantly higher drive voltages, and consequently larger output forces, can be obtained because the device no longer deforms to the point of electrical failure by shorting.

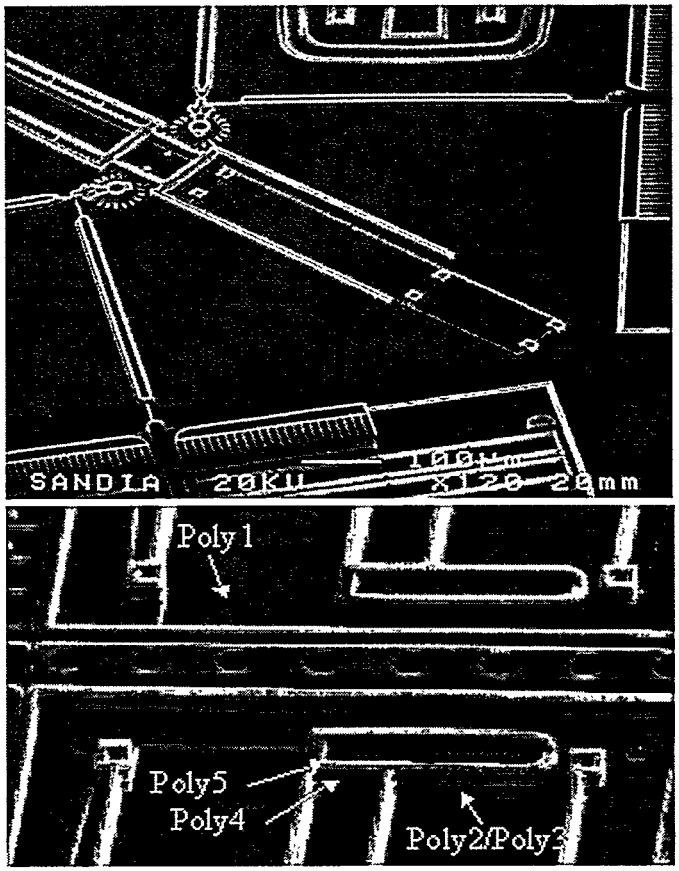

Figure 4. SEM images of dual microengines driving a geared-rack connected to a pop-up mirror. The drivers to the microengines are linear electrostatic comb drives seen in the lower-left and upper-right of the image on the top. The image on the bottom is a closer view of the elastic elements supporting the comb drives. The poly layers are numbered from 0, the ground poly, to Poly4, the uppermost, for a total of 5-levels. One sees that the effective thickness of these elements is greatly enhanced with the additional layer. The total device height above the substrate is 12.5 μm.

The out-of plane stiffness also contributes to better fabrication yield. Device yield improves because the additional stiffness aids significantly in overcoming both release and in-use stiction (13). Stiction, as used in micromechanics, refers to the tendency of micromechanical structures to adhere to themselves or their supporting substrate. This occurs often in MEMS due to the scaling of surface phenomena forces as the surface-to-volume ratio increases. Much effort is being expended to address the surface phenomena, however, a proven approach is to reduce the surface-to-volume ratio by simply increasing the volume of the structures which effectively stiffens the structures against surface forces. Additional polysilicon layers can be used to accomplish this. We are observing increased reliability in proportion to the increase of out-of-plane stiffness.

Sensors, such as accelerometers, benefit from both the stiffness and output transduction increase. The additional stiff-

ness reduces cross-axis response in many sensor structures. This occurs due to a decrease in the sense element response to cross-axis forces or due to a decrease in mode coupling between the desired sense axis and the cross-axis.

B. Novel Designs

The designs currently being fabricated primarily make use of the 5th level for its increase in robustness and reliability, with some use of innovation in the connectivity between structures. However, the potential utility of the 5-level polysilicon/oxide stack is depicted in Fig. 5. This technology allows a designer to consider stacking complex, moving structures on top of movable structures. This, in essence, allows micromechanisms to be conveyed about the surface of the substrate to interact with each other or with the environment. For example, we are developing lock elements which when unlocked enable other operations on the wafer by insertion of geared elements for power transfer. Fig. 5 is a portion of a recently fabricated 5-level design which illustrates the potential complexity of next generation devices (14).

Summary

In summary, a 5-level polysilicon surface-micromachining technology that has extremely desirable mechanical attributes and expands the available mechanical design space has been developed. Out-of-plane curl of released polysilicon layers over a millimeter span is less than 150 nanometers. Residual in-plane stress is less than 10 megaPascal. Initial results also show that the addition of the 5th level of polysilicon provides both significant improvement in device reliability and robustness, and new design space. Specifically, the increase in out-of plane stiffness contributes to both better fabrication yield and better design.

This new 5th level will permit the creation of considerably more sophisticated devices, and the potential for novel designs with 5 levels.

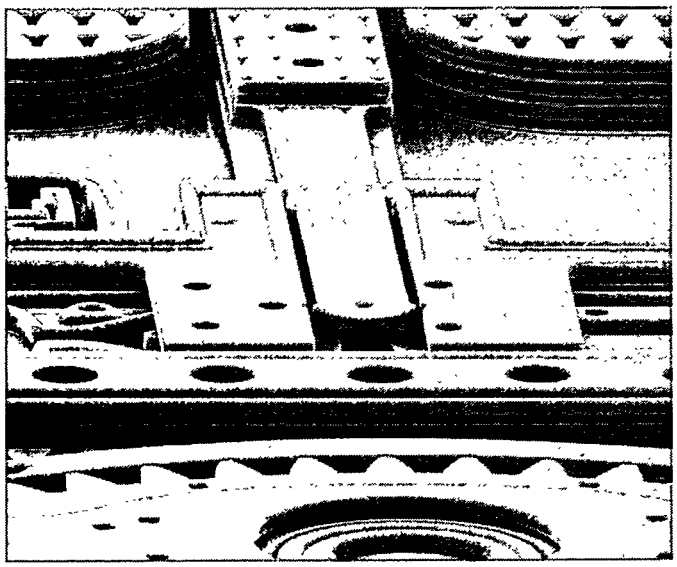

Figure 5. This SEM illustrates the degree of mechanical complexity that can be fabricated in this 5 level surface micromachining technology.

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(14) Results are pending and will be submitted to a future MEMSconference by M. S. Rodgers and J. J. Sniegowski.

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