SLAC-PUB-4904
UH-511-598-86
October 1986
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RADIATION HARDNESS AND ANNEALING TESTS OF A CUSTOM VLSI DEVICE*

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SLAC-PUB--4104

DE 89 013985

ABSTRACT

Several NMOS custom VLSI ("Microplex") circuits have been irradiated with a 500 *rad/hr* ^{60}Co source. With power off three of four chips tested have survived doses exceeding 1 *Mrad*. With power on at a 25% duty cycle, all chips tested failed at doses ranging from 10 to 130 *krad*. Annealing at 200°C was only partially successful in restoring the chips to useful operating conditions.

Introduction

We are planning to use a custom very large scale integrated circuit ("Microplex")[1-4] as a multiplexing readout for silicon strip detectors to be used in the Mark II experiment at the SLAC Linear e^+e^- Collider. Several studies of the radiation hardness of silicon strip detectors have been done[5-9], showing that no significant damage is to be expected from the anticipated levels of radiation of tens of *rads* per year; however, the radiation hardness of the Microplex chip needed to be tested. In addition, if radiation damage occurred, we wanted to see if annealing at relatively low temperatures (~200°C) could be used to restore the chips to working order. We cannot raise the temperature much higher since that would damage other parts of the detector

Description of Tests

The Microplex chip uses 5 μm NMOS technology. All the chips tested were produced at the Stanford Integrated Circuits Laboratory. The chip integrates and stores the charge from 128 input channels in parallel and multiplexes them using a shift register onto a single output channel. Two versions, referred to as I and II, have been produced. Microplex I... several improvements, including double correlated sampl... and hold circuitry which improved the signal-to-noise ratio. A further description and details of the performance of this chip may be found in references 1-4. Power must be pulsed on the analog section during beam crossings when the chip will be exposed to radiation; however, power to the digital readout section will be applied only afterwards when no radiation is present.

Two sets of irradiation tests were done, the first with no power applied (power off), and the second with power to the analog section pulsed at a 25% duty cycle (referred to as power on), but no power applied to the digital section. We used 25% instead of a higher duty cycle to avoid possible damage due to heating from power dissipation.

The chips were irradiated with a ^{60}Co source which was calibrated twice during the course of the tests. Its average strength was measured to be 489±24 *rad/hr*. At various intervals the chips were removed from the ^{60}Co source well and electronically tested. One characteristic of the second version (Microplex II) is that it requires a negative bias voltage to be applied to the substrate in order for the digital section to function properly. The minimum value for this substrate bias voltage was found to increase as the radiation dose increased. As can be seen in figure 1, this increase is a non-linear function of the dosage and is independent of whether or not power was applied to the analog section during irradiation.

For most of the chips, at some level of radiation, their performance began to degrade, *e.g.*, the gains of some or all of the channels decreased. The exact criterion used to define chip failure evolved with time as the testing procedures became more quantitative. For most of the chips, the test consisted of looking on an oscilloscope at the amplified output of the Microplex circuit from input calibration pulses equivalent in charge to that of a minimum ionizing particle traversing a 300 μm thick silicon strip detector (approximately 24000 electrons). At this stage, chip failure was defined rather qualitatively as the point at which the gains of some of the channels decreased by roughly a factor of five from their initial values.

* Work supported by the Department of Energy, Contracts DE-AC03-76SF-00515, DE-AA03-76SF00034, and DE-AC03-83ER-40103

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Presented at the Nuclear Science Symposium and Symposium on Nuclear Power Systems
Washington, D.C., October 29-31, 1986

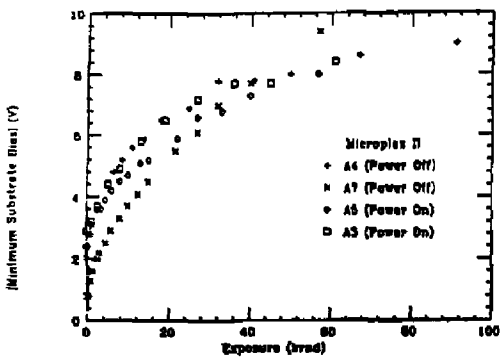

Figure 1. Absolute value of the minimum substrate bias voltage necessary for proper performance of the Microplex II chip as a function of the exposure for four chips, two with power applied at a 25% duty cycle to the analog section and two with no power applied.

After these initial studies of chip performance as a function of radiation dose, we saw a need to make more quantitative measurements, particulary to measure the signal-to-noise ratio and to choose more restrictive criteria to define chip failure. We improved the test setup by digitising the output voltages for each of the 128 channels of the Microplex chip using a CAMAC BADC[10]. The data acquisition used a standard CAMAC system coupled to an LSI-11/73 minicomputer. A series of six runs of approximately 500 pulses each was done. The first was a pedestal run (no calibration lines on), followed by runs in which each of the four calibration lines was in turn switched on, and the last was also a pedestal run. The data were analyzed to extract the pedestal values, the pedestal-subtracted calibration signals (the mean of the distribution), and the noise (defined as the rms width of the calibration signal distribution), from which the signal-to-noise ratio was calculated. The average for all working channels of the calibration signal, the noise, and the signal-to-noise ratio is shown in figure 2 as a function of radiation dose for chip D8. The error bars represent the rms spread over the 121 working channels in this chip. The most notable result is that the noise level increases dramatically above 50 krad, while the signal (i.e. the gains of the amplifiers in the chip) decreases only slightly, causing a steep decline in the signal-to-noise ratio. For the purposes of our silicon strip detector, if the signal-to-noise ratio decreases to below some fraction of its initial value, then that channel will become less useful. Therefore, the criterion for chip failure became the point at which the average signal-to-noise ratio dropped below 70% of its initial value. This more quantitative criterion is roughly a factor of two more strict than the previous qualitative criterion based on observations on the oscilloscope.

These results are summarized in table 1 and figure 3. For a given criterion for failure, the level at which failure occurs has an uncertainty of approximately 30%. Three of the four

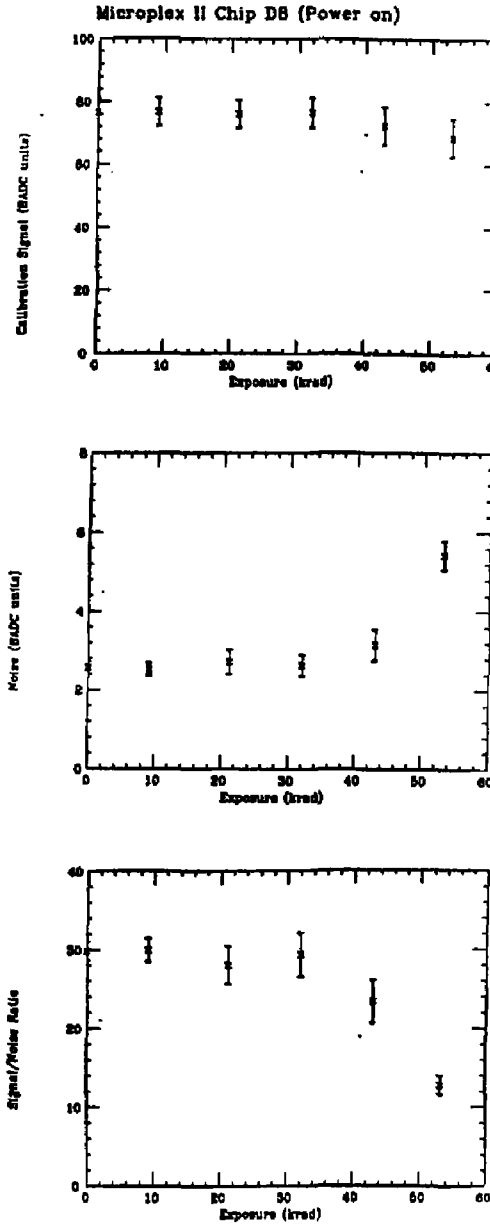

Figure 2. Calibration signal, noise, and signal-to-noise ratio as a function of radiation dose for chip D8. The points are the average values for the 121 working channels in the chip with the error bars representing the rms spread in the distribution over the 121 channels.

DISCLAIMER

Table 1

Summary of Irradiation and Annealing Tests

Dosages at which chip failure occurred. The > sign indicates that the chip was still working. The asterisk indicates that the chip was Microplex I, the rest are Microplex II. Errors on these numbers are discussed in the text. Chips in the D series had a more strict criterion to be declared "dead" than the others.

Chip Number	"Lethal" Dose (*krad*)	
	Before Anneal	After Anneal
Power off		
7B*	> 2165	
A7	74	
A4	> 1615	
B1	> 1353	
Power on		
6K*	11	
A5	74	46
A3	78	33
B2	53	24
B4	45	18
B3 (PEP)	> 77	
D2	128	12
D9	10	
D8	43	

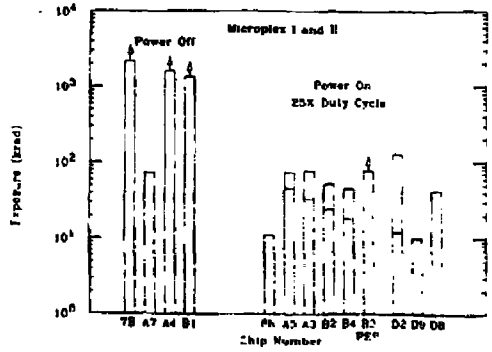

Figure 3. Summary of the results of the irradiations of thirteen chips. Upward pointing arrows indicate that the chip was still working at that dose level. For chips A5, A3, B2, B4, and D2, a second line at a lower value indicates at what dosage the chip failed after having been annealed. Chips D2, D9, and D8 had a more strict criterion for failure than did the rest of the chips (see text).

chips irradiated with power *off* survived exposures exceeding 1 *Mrad*; however, all of the chips irradiated with power on failed at exposures in the 10 to 130 *krad* range. Note that for chips D2, D9, and D8 failure was defined by a criterion different (and more strict) than that of the other chips.

There was some concern that a similar dose of synchrotron radiation, *off*-energy electrons, etc. present in the environment of an e^+e^- storage ring might be more damaging to the chip. To test this hypothesis, one chip (B3) with power on the analog section at a 25% duty cycle but no power applied to the digital section was placed on the beam pipe near interaction region 12 of the PEP storage ring at the Stanford Linear Accelerator *Center*. Thermoluminescent dosimeters placed in close physical proximity to the chip were used to monitor the amount of radiation exposure. During a four month period, the chip was removed and tested three times. The gains of the channels remained constant to within 10% of their initial values. Thus, no significant radiation damage was found after an exposure of 77 ± 15 *krad*. This result is also summarized in table 1 and figure 3.

Annealing tests were performed on six (power on) chips which had severe radiation damage. Annealing was not attempted for chips 6K and D9 which had failed after their first 10 *krad* exposure. Chips were placed in an oven through which dry nitrogen gas was circulated to get a roughly inert atmosphere. The chips remained in the oven during the entire heating and cooling cycle. They were removed when the temperature dropped below roughly $70°C$. A typical temperature profile as a function of time is shown in figure 4. We define

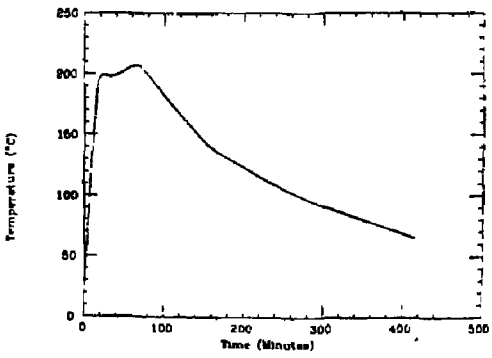

Figure 4. Typical temperature profile as a function of time for a $200°C$ anneal. In this case the chip was removed from the oven after 415 minutes.

the annealing time and temperature as the length and average height of the plateau. For annealing times of 1 hour, we tried annealing temperatures of 100, 150, 180, 200, and 210°C. For temperatures below 200°C, no improvement in the chips' performance was found, whereas for annealing temperatures of 200°C and higher, the performance of five of the six chips for which annealing was tried improved to usable levels. However, for chip D8, the noise level did not decrease enough to pass the more strict signal-to-noise ratio criterion used to define chip failure. We then re-irradiated these chips using the same ^{60}Co source and above-described procedures. The level of radiation which produced similar damage to the previous irradiation was markedly lower as shown in table 1 and figure 3; i.e., 10% to 70% of the previous levels. Re-annealing at 200°C did not succeed in returning the chips to usable performance levels. Attempts at 300°C destroyed the chips; however, the exact nature of the damage was not determined.

Discussion and Conclusions

The results of these radiation hardness tests give a good qualitative picture of the radiation tolerance of the Microplex chip. Large chip-to-chip variations and the small number of chips tested preclude making more quantitative conclusions, but several general observations may be made. With no power applied, the radiation tolerance exceeds the 1 *Mrad* level with the caveat that one chip was found to fail after only 74 *krad*. With power on the analog section at a 25% duty cycle, failure occurs in the 10 to 130 *krad* range. If we extrapolate this to 100% duty cycle, as will be the case in the Mark II experiment, this range is 2.5 to 32 *krad*. This is at least two orders of magnitude greater than calculated levels due to synchrotron radiation during normal operation of the SLAC Linear Collider. Thus it appears that the radiation tolerance of the Microplex chip is sufficient for our purposes. Low-temperature annealing was only partially successful in restoring the performance of the chip to usable levels. In all cases, the performance was not completely restored and subsequent irradiation produced chip failure at much lower levels than initially. In addition, after a second irradiation, annealing at 200°C did not succeed in making the chips usable. Higher temperatures (300°C) destroyed the chips.

In summary, the radiation tolerance of the Microplex is adequate for use at the SLAC Linear Collider. Low-temperature annealing does not appear to be a practical means of restoring chip performance if failure occurs due to a gradual buildup of radiation damage. Further tests of radiation hardness of a commercially produced NMOS version of the Microplex circuit are underway to determine in a more quantitative way the radiation tolerance of the chips which will be used in the silicon strip vertex detector for the Mark II experiment.

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