Processing Issues and Technologies for Optoelectronics-Integrated Circuits and Devices (Invited)

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ABSTRACT

The influence of processing on the design of optical devices and optoelectronic integrated circuits is discussed. Process compatibility of devices used as the basis of a complete optoelectronic integrated circuit will be discussed along with some potential optoelectronic integrated circuits employing only phase modulators and couplers. Specific examples of the application of reactive-ion-beam etching in the formation of passive optical waveguide phase modulators, optical interconnects, turning mirrors, and output couplers in GaAs/AlGaAs are given.

1. INTRODUCTION

Photonic integrated circuits (PICs) have not yet evolved to the level of sophistication of electronic integrated circuits. One primary impediment to the development of a wide variety of PICs for many applications is the difficult design and fabrication process required of every new PIC. Development of a fully functional PIC requires careful consideration of the application requirements, the detailed behavior of each device used, and the interaction of all the devices with the others. Generally, custom processing is required in order to build the circuit, requiring the engineer designing the circuit to have a full understanding of the process capabilities and limitations. This is in sharp contrast with the electronic integrated circuit field where well established device, and circuit, design rules based on proven-reliable process technology allow engineers to easily lay-out integrated circuits. The engineer requires only a minimum understanding of the actual operation of the devices in the circuit and the process technology required to manufacture the circuit. This ease of design and the ability of the designer to view the manufacturing process as a black box from which good parts emerge, provided he adheres to the design rules, has allowed a wide diversity of electronic integrated circuits to flourish in the marketplace.

In order for PICs to become widely accepted as viable solutions in a variety of applications the huge overhead cost associated with custom design and manufacture of each circuit must be minimized. One way to minimize costs is to follow the example of the electronic integrated circuit industry and establish a fixed set of mutually compatible devices with well-established design rules governing their placement in the circuit in such a manner as to assure an operating PIC. This paper will discuss, in detail, one potential optical device set and covers several application circuits which could be realized with the technology. Constraints on selection of the device set due to fabrication issues such as regrowth and etching will also be covered.

2. PROCESS TECHNOLOGIES SUITABLE FOR PICs

Photonic integrated circuits are typically designed from the top down. An application is selected. An optical circuit is designed to achieve the desired result. A method is found to fabricate the required circuit. This design method, when successful[1], generally results in a very high-performance and costly circuit. The reason for this is that circuit function and performance are considered paramount over manufacturability and cost.

A more practical approach, and indeed one which may result in a greater diversity of circuit applications from a given PIC technology, is to reverse the order and first select those process

technologies which are expected to be controllable, reproducible, and high yield. Then the set of optical devices which can be fabricated using only the selected desirable process technologies is determined. Finally, functional application circuits are defined which can be assembled out of the allowed set of devices. The concept is to select a minimum number of processes best suited for PIC fabrication and then decide what kinds of devices can be made with only those few processes in such a manner that all the devices may be interconnected into a functional PIC using a set of reasonably simple design rules. If this selection process is done correctly, the result should be a manufacturable PIC technology. It should be noted, however, that in the corporate environment the application (or general class of application) is often specified first and may dictate that certain types of devices, such as lasers or detectors, be included in the device set. This fact will necessarily influence the set of allowed processes. In our PIC application, a need was identified for a generic collection of circuits suitable for coherent optical processing. Complete integration of light source, optical circuit, and detector was not a requirement. These facts allow a very simple technology based on phase modulation, without optical sources and detectors.

The evaluation of process technologies is not very tedious. An evaluation for coherent-optical signal processing applications is summarized below. Two clearly unavoidable technologies are metalization for electrical contact and etching for definition of waveguides, gratings, and mirrors. Both of these are included in our set. Metal will be applied by evaporation and lift-off or selective-area plating. (Etching of metal is not desirable due to undercut problems and the possibility of the metal etchants attacking the III-V compound semiconductor.) Wet chemical etching of the semiconductor will not be used since it does not offer much control of wall angle. Dry plasma etching processes which allow smooth vertical walls or walls of arbitrary angle for waveguides, reflective facets, and gratings are prefered. Chlorine reactive-ion-beam etching (RIBE) is an ideal technique for etching of waveguides and facets due to its smooth morphology, extreme anisotropy, and variable angle of incidence. Conventional reactive-ion-etching (RIE) would also be useful but does not offer easily-variable wall angle. Ion milling offers adjustable wall angles but cannot simultaneously etch two walls, facing opposite directions, at the same angle. Chemically-assisted-ion-beam etching (CAIBE) is nearly as good as RIBE except for shadowing effects of the injected reactive gas and greater process complexity. Lithography methods will include all standard contact and projection exposures as well as electron-beam direct write. Electron-beam exposure is required for highly accurate and smooth patterning of curved and intersecting optical waveguides and gratings. Dielectric layers of SiO_2, SiN_x, or polyimide will be used as needed and etched by conventional isotropic, parallel-plate, dry methods.

Regrowth of heteroepitaxial material and ion implantation require special consideration. If it is desired to integrate active light-emitters and absorbers with passive components it may be required that one or both of these technologies be added to the list. Lasers and detectors can be integrated without these methods[2] but severe performance limitations often result. The case against regrowth is that it is difficult and requires very high temperatures which may damage other portions of the circuit. Therefore, if a useful technology can be found which does not employ regrowth, the odds of creating low-cost, high-yield PICs are much higher. At the expense of omitting active sources and detectors from our PIC, regrowth will not be used in our process. The relative merits of ion implantation are less clear. Use of proton implantation for electrical isolation is reliable but sensitive to the moderate (~400°C) processing temperatures used in contact alloying. Disordering of quantum wells by ion-implantation has been used to blue-shift the absorption edge of quantum-well waveguides, this allows integration of active sources with disordered passive devices but makes fabrication of biased pn-junction modulators difficult. Ion implantation will be held in reserve for future consideration.

3. SET OF DEVICES USING THE ALLOWED PROCESS SET

Having decided which process steps will be permited in our PIC fabrication (optical and electron-beam lithography, RIBE, lift-off metalization and selective area plating, SiO_2, SiN_x, polyimide dielectrics, and dry-etch for dielectric window etches), the task of selecting the devices that will make up

our set of parts from which to assemble PICs is now possible. The constraints are simple. A sufficient variety of devices is needed such that useful PICs may be assembled, and all of the devices must be designed for interchangability and process compatibility. However, an excessive quantity of different device structures may complicate the final design-rules without adding a proportionate amount of additional potential function to the PIC. For this reason, it is preferred to minimize the number of different devices in our PIC technology.

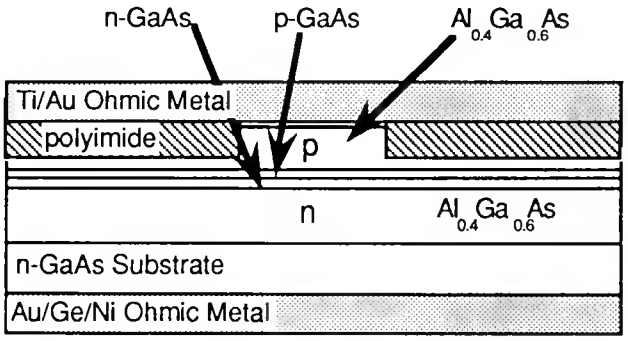

FIGURE 1: Cross section view of ridge waveguide phase modulator.

From a processing viewpoint, one of the most simple devices to fabricate in integrated form with passive, low-loss, optical waveguide interconnects is the waveguide phase modulator[3]. Phase modulators of the depletion-edge-translation type fabricated in GaAs/AlGaAs have low insertion loss, $<2.5\ cm^{-1}$, and high modulation efficiency, >81°/V-mm, at 1.06μm wavelength. Furthermore, the device may be fabricated in a ridge optical waveguide form well-suited for passive optical waveguide interconnection between devices (figure 1). Thus, if the epitaxial material is grown as a GaAs/AlGaAs waveguide with a doped pn-junction designed for optimum phase modulation efficiency under reverse bias, the ridge waveguides used to define the phase modulator may simply be extended, without metalization, for use as interconnects. In this scheme, the only difference between a phase modulator and an interconnecting waveguide is that modulators have ohmic contacts on the rib. The entire PIC will then have the same optical loss as the phase modulator, $2.5\ cm^{-1}$ at 1.06μm wavelength.

Optical waveguide amplitude modulators form another potentially useful class of PIC devices. There are, however, a number of drawbacks to the use of these structures in PICs. Most recent amplitude modulators in III-V semiconductors employ multi-quantum-well waveguides and the Quantum Confined Stark Effect (QCSE) under reverse bias of the waveguide layers[4]. These devices only operate at wavelengths near the excitonic absorption edge of the quantum wells such that under an applied electric field the waveguide absorbs more light due to the stark-shift of the n=1 exciton. The on-off ratio of these devices can be quite large with low applied voltages but the insertion loss is necessarily large as well since the operating wavelength is very close to the band-edge of the unbiased quantum wells. The large insertion losses of $>50cm^{-1}$ inherent in the design of QCSE modulators make them unsuitable for any PIC application where regrowth or implantation will not be used to shift the absorption edge of the interconnecting waveguides. Vertically-integrated waveguides such as the Integrated Twin Guide[5] and other vertical coupled-mode schemes[2] could be used to shift the optical signal up into the modulator, but these add process complexity and will not be considered further.

As already mentioned, rib waveguides are well suited to our process technology and work well as interconnections between devices. Waveguide bends and branches are also very important in the layout of PICs. Bends are needed for alignment and routing of signals while branches allow splitting and recombining of signals. Bends are implemented in our process at the mask-layout level with little

difficulty while splitters and combiners require careful process control but are otherwise compatible with our process set. One type of splitter/combiner is the waveguide directional coupler. This configuration requires only that three rib waveguides be placed side-by-side such that power is split from the single input guide to the two output guides, or vice versa, by evanescent mode coupling. The degree of power transfer is fixed by the etch depth of the waveguide ribs and the spacing between them. Although the process steps are simple, the tolerances are tight. In order to fabricate a -3dB splitter without added metal pads to adjust the split ratio after fabrication, it is expected that 0.1μm linewidth and 0.05μm etch control are needed. Electron-beam direct-write lithography is capable of maintaining these linewidth tolerances while RIBE with careful *in-situ* etch monitoring may be capable of the etch control required. An alternative approach is to use conventional y-junctions as are commonly seen in lithium niobate waveguide circuits. Here fabrication tolerances for the etch depth are somewhat relaxed but efficient mode splitting still requires precise control of the linewidth and shape of the branch section. Either of these splitter/combiners is adequate for our PIC.

Compact PICs will require sharp waveguide bends for signal routing. Since radiation losses of a uniform radius bend do not allow sharp bends, total-internal-reflection turning mirrors are prefered[6]. These can be fabricated using a self-aligned process of two RIBE steps resulting in highly accurate mating of a shallow-etched rib waveguide with the deeply-etched 45° turning mirror. Figure 2 illustrates a rib-waveguide directional coupler with output to a turning mirror.

Output and input coupling to PICs may be performed at cleaved facets with butt-coupled fibers but some circuit configurations might require input/output normal to the chip surface. For these applications, gratings can be etched across the rib waveguide such that the first-order diffraction is surface-normal.

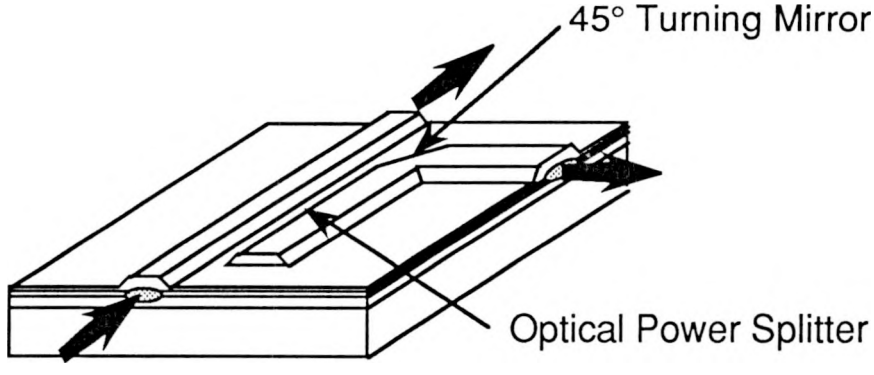

FIGURE 2: Rib waveguide directional coupler power splitter integrated with 45° turning mirror. Epitaxial layers are identical to Fig.1.

4. LOGICAL FABRICATION SEQUENCE

All of the above mentioned devices are suited to our set of process technologies and can, with relatively few constraints, be placed in any order within the PIC. Single mask level, self-aligned processes are preferred when attempting to align individual devices such as modulators, waveguides, turning mirrors, and gratings. One very useful result of our limited selection of processes is that all of the devices are fabricated primarily by one or two RIBE etch steps and all of them share the same initial waveguide etch. This allows one etch step to define the geometry of the entire PIC in the first process step. Based on this self-aligned approach, the process sequence is as follows. First the wafer is masked with a tri-level dry-etch mask of hard-baked photoresist, titanium, and a top layer of electron-beam resist patterned for the fundamental waveguide circuit complete with couplers, turning mirrors,

gratings, branches, and phase modulators. Electron-beam direct write lithography is used for this most critical step in order to maintain control of waveguide linewidth, coupler spacing, branch shape, and grating size. Chlorine RIBE and oxygen RIBE are now used in sequence to transfer the electron-beam resist pattern into the hard-bake photoresist. Another chlorine RIBE step is used to etch the rib waveguide to the correct depth. As the depth of this etch is critical for correct operation of the directional-coupler-type power splitters, *in-situ* optical interferometry is used to determine the real-time etch rate and depth. Leaving the hard-baked resist in place, another layer of photoresist is patterned by conventional lithography with openings for the deep turning-mirror etch. The openings will self-align to the hard-baked resist used to define the actual mirror surface, this mask level may also include any deep etches needed for electrical or optical isolation. Chlorine RIBE is again used to complete the deep turning-mirror etch and both mask levels are removed. With just two etch steps, all the optical structures are complete. The wafer is now coated with a dielectric of SiO_2, SiN_x, or polyimide, openings are etched over the waveguide where phase modulators are needed, and ohmic metal deposited by lift-off or plating for contact to the phase modulators. After application of the substrate ohmic contacts, the PIC is complete.

This very simple straight-forward process sequence is the direct result of minimization of process types, minimization of device types, omission of active sources and detectors, and designing each device to fit the same process sequence as all the other devices. As a result, it is expected that PICs designed to use this technology will have a relatively high manufacture-yield and low cost.

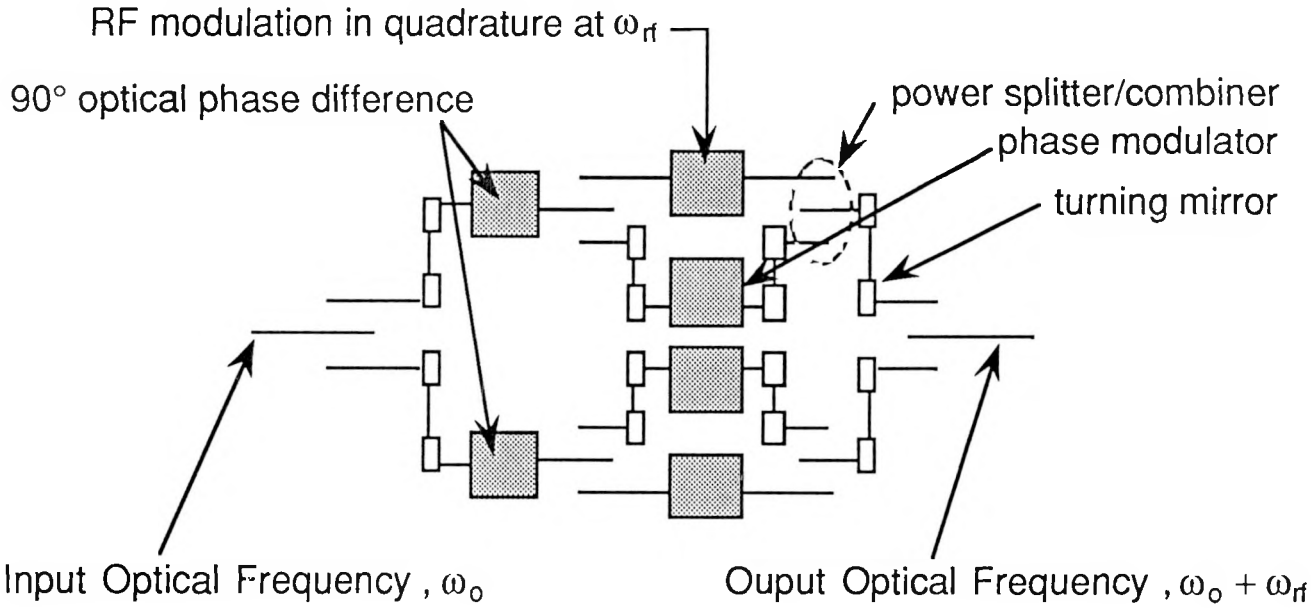

FIGURE 3: Schematic diagram of integrated optical frequency shifter using only phase modulators as active elements. Required amplitude modulation is achieved using a pair of Mach-Zehnder interferometers which appear vertically stacked in the middle of the circuit.

5. A SELECTION OF POTENTIAL PICs

The question now arises, "With such a low diversity of devices and no active elements, what possible PICs can be built with this technology?" The answer is, "Surprisingly many!" The common denominators of any PIC designed for a technology with no active sources/detectors, whose only active devices are phase modulators, are that laser sources and detectors must be located off-chip, coupled in by optical fiber, and all optical processing will be coherent optical heterodyne or homodyne. These

circuits will fill a need for a number of different coherent optical signal processing applications. Some examples are: Optical frequency shifter for FM modulationas well as local oscillator or beat-frequency generation (figure 3); Tunable optical filters (MUX, deMUX); Secure optical links; Generation and control of phased-array antenna signals[7] (figure 4).

All of these PICs use an optical power supply consisting of a single-frequency, narrow-linewidth laser whose fabrication and packaging are optimized for the requirements of a high-performance laser.

6. CONCLUSIONS

In conclusion, a new approach has been outlined for the development of photonic integrated circuits with an emphasis on ease of fabrication and low cost. By selecting high-yield, reliable, process technologies and limiting the number of devices, it is expected that the cost of PIC technology will drop, allowing a greater number of applications to be considered. A phase-modulator-based PIC technology with a very simple, self-aligned process, has been outlined. This approach is an optical analog to the successful electronic integrated circuit practice of limiting the device diversity to not more than two different transistors, even resistors are fabricated using transistors. Just as with electronic integrated circuits, where selection of the number and type of transistors influences the application, the selection of the active optical elements in the PIC limits the applications due to variable functionality, power dissipation, and cost. The phase-modulator-based technology has applications in coherent optical processing and communications where use of a remote, fiber coupled, laser source is either desirable or, at least, not problematic. Even with these constraints, a number of applications have been identified ranging from optical frequency modulation to control of a complete phased-array antenna from a single PIC.

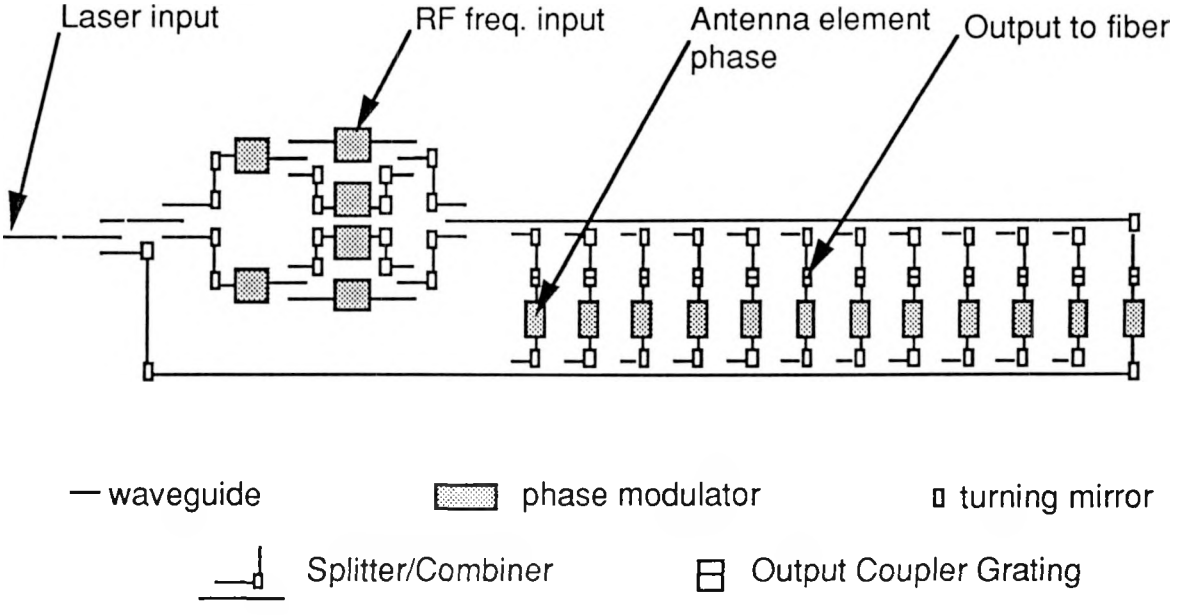

FIGURE 4: Schematic diagram of PIC for generation and control of multiple-element phased-array antenna. Complete description of the circuit is provided in reference 7.

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