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# THE E802 DATA ACQUISITION COMPLEX

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## Abstract

The data acquisition architecture planned for experiment E802 is described. A VAX 11/785 will be front-ended by a VME-based array of 68000-family microprocessors, which will be used as intelligent CAMAC crate controllers, event builders, and to augment the computing power of the VAX for on-line analysis of the data.

## Introduction

E802 will be one of the first experiments to study relativistic nucleus-nucleus collisions using the 15 GeV-A heavy ion beams available at the Brookhaven AGS starting late 1986. E802 centers around a single-arm magnetic spectrometer designed to study events with charged-particle multiplicities as large as 20; thus its detector subsystems will all be highly segmented. These subsystems include 32 planes of tracking detectors (drift chambers), the largest of which contain over 200 wires, a segmented Cerenkov array (125 elements), and a time-of-flight stop detector comprised of 225 elements. The number of elements to be read is of order 10000. A typical event is expected to contain 5000 bytes.

The E802 data acquisition architecture will rely on distributed intelligence, located principally in VME crates, to perform sparse data scans. Non-zero descriptors will be read into VME buffer memories by intelligent crate controllers designed for efficient block transfers and list processing. A dedicated processor residing in the VME crates will format the events for transmission to the VAX 11/785 [1] host, where the data will be recorded on magnetic tape or optical disk.

Reconstruction of events with large multiplicity using largely projective geometry in the tracking chambers is a task which consumes enormous amounts of computing power. Our present estimates, based on Monte Carlo simulations of real events, indicate that data acquired in ten weeks of running will require on the order of ten years of VAX 11/785 CPU time to analyze completely. We will, therefore, augment the power of the VAX with that of an array of processor elements residing in the VME crates. Each processor element will have approximately the power of one VAX 11/780. The price of each processor element and 1 Mbyte of associated memory is about $10K. Processor-memory communication takes place over a private (VMX) bus, so that a large number of these processors can be connected with a gain in processing power linear with the number of elements (i.e., no saturation due to limited bandwidth of the global bus). The present goal is to implement an array of processors with a power of 10x VAX 11/780.

The list of applications to which such an array can be applied is large. It is crucial that we have enough computing power to subject a non-trivial sample of the data stream to a complete on-line analysis. It is also important, given the complexity of the experiment, to be able to monitor the performance of each detector subsystem independently during the experiment. Finally, software cuts will be necessary to reduce the hardware trigger rate (about $10^3$ sec$^{-1}$) to an event rate which can be recorded (about 50 sec$^{-1}$). It is anticipated that, during the experiment, roughly half of the processors in the array will be histogramming data for diagnostic purposes and generating live displays of these histograms while the remaining processors will be either implementing these software cuts or running a full-blown analysis program. After the beam time, all of the processor elements are available for analysis of the data.

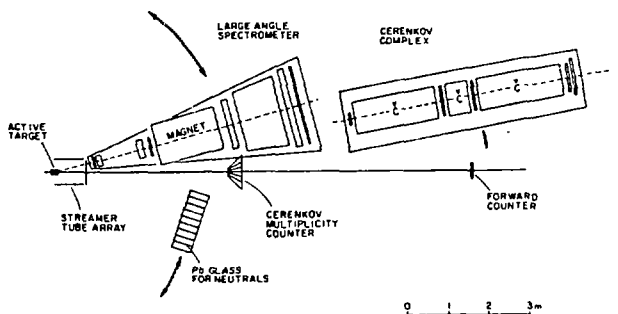


Fig. 1. A simplified layout of the E802 detector hardware. See text for details.

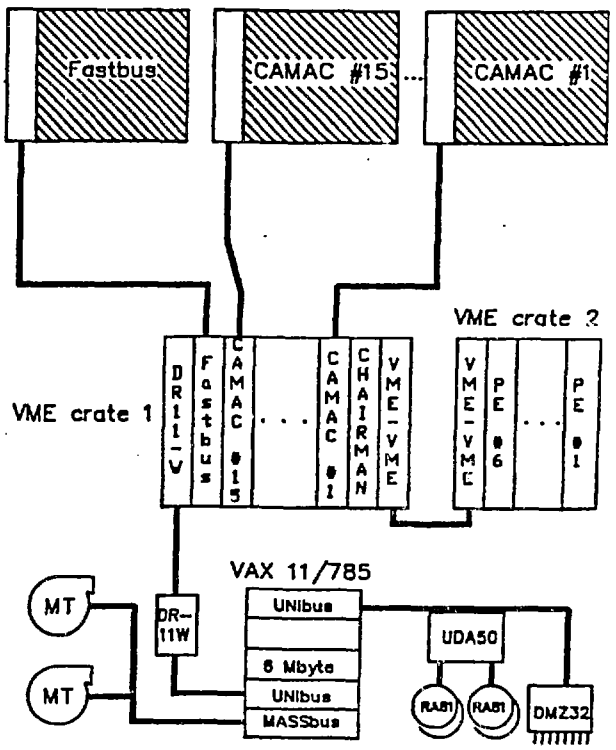


Fig. 2. The E802 data acquisition hardware.

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## The VAX 11/785

The VAX 11/785 will be configured with 6 Mbyte of memory, dual magnetic tape transports interfaced to the SBI, and two UNIbuses: One will be used to support the disk controller, the serial ports, and an Ethernet connection to other VAX installations at BNL. The second will be dedicated to the acquisition of data from the VME crates.

The connection to the VME crates is made via a DR11/W-type device connected to the UNIbus and a similar device residing in the master VME crate. Data is transferred to/from the VAX memory by DMA block transfers controlled by these devices.

## Management of the VME Crates

The VME subsystem is managed by a microcomputer ("the Chairman") based on the 68010 processor. It is accompanied by a 512 Kbyte dual ported (VME-VMX) memory. Both boards are manufactured by DataSud Systems. In the E802 system, the Chairman is responsible for all movements to/from the VAX as well as for synchronizing the activities of the various crate controllers and of the processor elements.

## CAMAC Crate Controllers

Approximately 15 CAMAC crates will be used in E802. Estimates of the times necessary to read out these crates using, for example, 3 parallel branch highways, led to the conclusion that this approach would not be fast enough. This is due, in part, to the slow speed of the branch highway, as well as to the need to read 5 crates sequentially. It was decided, therefore, to interface each CAMAC crate to an intelligent controller. The approach to be described is predicated on the presence of a bit register in each crate; the bit pattern allows the crate controller to read only the relevant devices for each event.

The CAMAC interface utilizes a Kinetic Systems Model 3920 crate controller connected to a XYCOM XVME-080 intelligent prototype module with interface circuitry under design at BNL. The XVME-080 is based on a 10 MHz 68000 microprocessor; it includes address decoding and handshake signals for custom circuitry to be supplied by the user. The BNL interface will memory-map the NAFs for the crate into a portion of the 68000's address space. It is meant to be optimized for executing lists of 16 bit CAMAC reads. Such a list can be executed at 1.3 μsec/transfer. This is accomplished by asserting DTACK at CAMAC S1 time, allowing the transfer of the CAMAC data to 68000 memory in parallel with the remainder of the CAMAC cycle. The cost of both parts of the crate interface will be about $3K.

The CAMAC interface will be activated by a front panel interrupt (event trigger). It then reads the bit register(s), uses a resident table to construct a list of CAMAC commands (memory-mapped) and a list of MOVE.W instructions terminated by a branch or jump. There are more than 100 μsec available to do this for any of the CAMAC devices foreseen for E802. After testing for the appropriate LAMs, it begins blindly executing its list. A missing Q- or X-response interrupts the processor, so that checking after every command is avoided.

Finally, all devices in the crate are cleared, the Chairman is notified that data is available in the interface's memory, and the interface awaits the next event trigger.

## Fastbus Interface

There will be one or two Fastbus segments in E802 to accommodate the pipeline TDCs necessary for the drift chambers. A typical event will require 500 descriptors to be read from these segments. It is clear that the approach used (programmed transfer) for the CAMAC crates will not be suitable for the Fastbus readout: several hardware DMA transfer methods are being considered.

## Assembly of an Event

The time scale for one type of event assembly is shown in Fig. 3. The time scale for CAMAC readout is determined by the use of high density ADCs which require approximately 300 μsec to convert and readout. Fastbus readout cannot begin until the pipeline TDCs have completed data formatting (400 μsec). The time shown in Fig. 3 for Fastbus readout assumes programmed transfer (1.2 μsec/word). The event fragments collected in the local memories of the crate/segment interfaces are then assembled and formatted in the memory of the Chairman. The entire event is then transmitted to the VAX by the DR11/W link. The elapsed time for this transfer is under 2 μsec; however, large portions of this process can be overlapped with the acquisition of subsequent events.

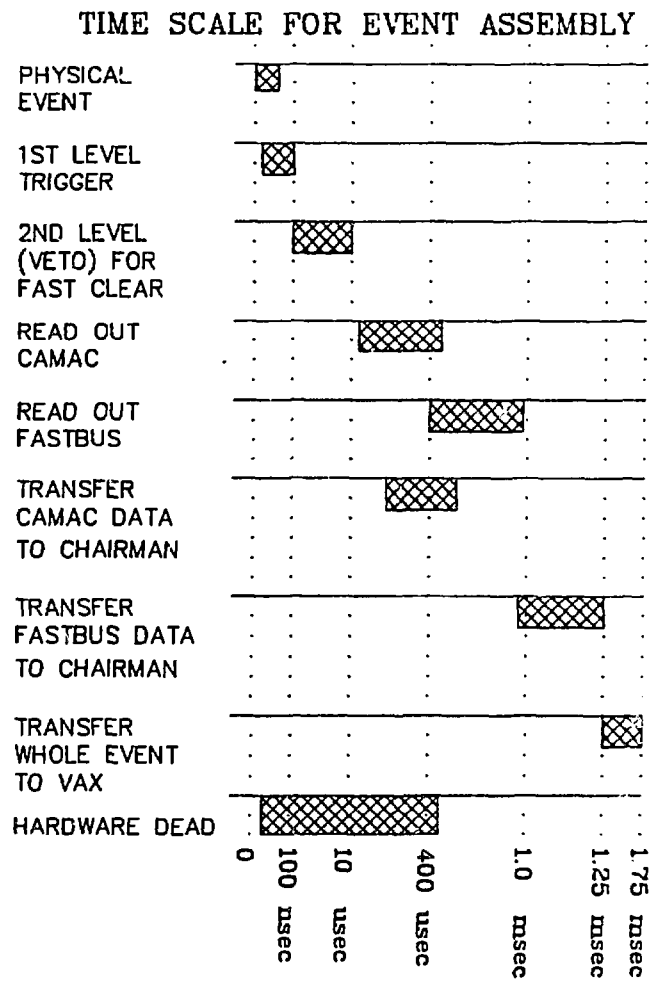


Fig. 3. Time scale for a typical event to be read, formatted, and transmitted to the VAX.

## The Processor Elements

The criteria for the selection of the processor elements were:

1) On-board floating point hardware available.
2) Cross-compilers for higher-level languages, preferably Fortran, must be available.
3) Adequate memory (~1Mbyte) with a private (VMX) connection to the processor must be available.

Based on these criteria, the Motorola MVME130-MVME204 board set was chosen. The CPU is a 68020 microprocessor, for which there is now available a floating point co-processor. The MVME204 is a 1Mbyte dual-ported memory. The 68020 has been benchmarked [2] by the CERN EF-Division, without a floating point co-processor. For integer benchmarks, the 68020 was at least as powerful as a VAX 11/780. The MVME130 includes memory management hardware, which is a necessity for the stability of any multiprocessor array.

An important consideration in this choice was the availability of an appropriate language. The real-time Fortran [3] developed for the 68000 family of microprocessors by the UA1 experiment at CERN was extremely attractive in this sense, since it is largely an implementation of VAX Fortran with some important extensions for real-time use. Extension of this cross-compiler to take advantage of the enhanced instruction set of the 68020 is in progress.

## Software

We anticipate implementing two major data analysis programs for on-line use: HBOOK will exist on both the VAX and on the processor elements in a somewhat smaller version. In addition, LULU [4] will be used on the VAX as a debugging facility for subroutines to be run in the processor elements as well as for data analysis. Discussions are underway to find a smaller incarnation of LULU which can run effectively in the processor elements as well.

## Summary and Present Status

The E802 data acquisition architecture relies heavily on distributed processing to read a large number of devices and to provide on-line analysis necessary for the monitoring of experimental hardware.

The system described is under contruction; although most hardware decisions have been made, much of the hardware has yet to arrive at BNL. It is expected, however, that a first implementation will be operative by early 1986.

## References


[1] VAX is a trademark of the Digital Equipment Corporation.

[2] A. Marchioro et al., CERN Mini and Micro Computer Newsletter No. 7, April 1985.

[3] H. von der Schmitt, DD Division, CERN, private communication.

[4] H. J. Crawford and P. J. Lindstrom, "LULU Analysis Program", IEEE Trans. Nucl. Sci. NS-30, No. 5, October 1983.

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