

2

UCRL- 82967
PREPRINT

CONF-791102--109

MASTER

MFTF SUPERVISORY CONTROL AND DIAGNOSTICS
SYSTEM HARDWARE

DAVID N. BUTNER

This paper was prepared for submittal to the
8th SYMPOSIUM ON ENGINEERING PROBLEMS OF
FUSION RESEARCH; IEEE; SHERATON HOTEL,
SAN FRANCISCO, CA., NOVEMBER 13-16, 1979

11-12-79

 Lawrence
Livermore
Laboratory

This is a preprint of a paper intended for publication in a journal or proceedings. Since changes may be made before publication, this preprint is made available with the understanding that it will not be cited or reproduced without the permission of the author.

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This book was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. References herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

MFTF SUPERVISORY CONTROL AND DIAGNOSTICS SYSTEM HARDWARE*

David N. Butner
Lawrence Livermore Laboratory, University of California
Livermore, California 94550

Summary

The Supervisory Control and Diagnostics System (SCDS) for the Mirror Fusion Test Facility (MFTF) is a multiprocessor minicomputer system designed so that for most single-point failures, the hardware may be quickly reconfigured to provide continued operation of the experiment. The system is made up of nine Perkin-Elmer computers - a mixture of 8/32's and 7/32's. Each computer has ports on a shared memory system consisting of two independent shared memory modules. Each processor can signal other processors through hardware external to the shared memory. The system communicates with the Local Control and Instrumentation System, which consists of approximately 65 microprocessors. Each of the six system processors has facilities for communicating with a group of microprocessors; the groups consist of from four to 24 microprocessors. There are hardware switches so that if an SCDS processor communicating with a group of microprocessors fails, another SCDS processor takes over the communication. Operator commands to control the MFTF experiment are entered through eight consoles that use color graphic displays. Peripheral equipment includes 11 disk drives, two magnetic tape drives, two printers, and one card reader.

Introduction

The MFTF is a large magnetic fusion experiment that includes a superconducting magnet in a large vacuum vessel, a cryogenic system to cool the magnet, plasma streaming guns to start a plasma experiment, approximately 80 kV, 80 A neutral beams to build and maintain the plasma, a set of plasma physics diagnostics, and other support systems.

During operation, the magnet current must be gradually increased to the operating level, which must be maintained for several days or weeks while plasma experiments are performed. Once the magnet current and vacuum are at the desired levels, the goal is to perform a plasma experiment every 5 min.

The SCDS is responsible for coordinating the activities of the various MFTF subsystems, for accepting data from the plasma diagnostics system, and for archiving all data relative to the operation of MFTF.

Supervisory Control and Diagnostics System Design

The system is conceptually designed as a hierarchy, shown in Fig. 1. The system supervisor coordinates the activities of all subsystems. The vessel and facilities supervisors oversee the operation of the vacuum, cryogenic, magnet, getter, safety interlock, and power subsystems. The injector supervisor oversees the operation of the plasma streaming subsystem and the neutral beam subsystems. The diagnostic data processor receives data from the plasma diagnostics system. The data

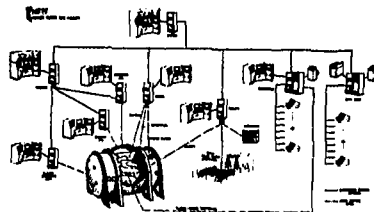


Fig. 1. Supervisory Control and Diagnostics System Design

base manager is responsible for archiving the data. The diagnostic data processor and the data base manager also run the software development systems. The plasma streaming supervisor, the startup neutral beam supervisor, and the sustaining neutral beam supervisor are subordinate to the injector supervisor.

The SCDS communicates with the Local Control and Instrumentation System, which consists of approximately 65 microprocessors. As shown in Fig. 1, the facilities and vessel supervisors communicate with three microprocessors. The plasma streaming supervisor communicates with one to five microprocessors, the startup supervisor with 20, and the sustaining supervisor with 24.

Operators of the MFTF experiment communicate with the SCDS using eight consoles. Most communication is through touch-sensitive panels mounted on color CRT displays. Each console has three or six additional color CRT displays used to present information to the operators.

Each computer in SCDS has a designated backup machine, which must perform identical functions. The overall system performance is allowed to be degraded if any machine is operating in the backup mode. Backup machine designations follow:

Primary computer	Backup computer
System supervisor	Injector supervisor
Injector supervisor	System supervisor
Plasma streaming supervisor	Injector supervisor
Startup supervisor	Injector supervisor
Sustaining supervisor	Injector supervisor
Vessel supervisor	Facilities supervisor
Facilities supervisor	Vessel supervisor
Data base manager	Diagnostics data processor
Diagnostics data processor	
Data base manager	

Hardware Design

The hardware configuration is shown in Fig. 2, and consists of nine Perkin-Elmer computers - a mixture of 8/32's and 7/32's. Each computer has ports on a shared memory system consisting of two

*Work performed under the auspices of the U.S. Department of Energy by the Lawrence Livermore Laboratory under contract number W-7405-ENG-48.

independent shared memory modules. Each processor can signal other processors through hardware external to the shared memory. The system supervisor and the injector supervisor can also send a signal to each machine, which causes the receiving machine to load an operating system from disk (bootstrap).

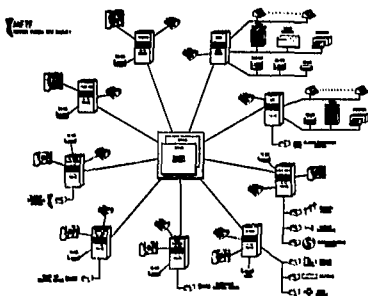


Fig. 2. MFTF Control Diagnostics System

The system hardware has almost no hierarchic structure; any machine may easily communicate with any other machine. Thus, our configuration allows more flexibility in the internal design of the software system. However, the system appears to be a hierarchy to the MFTF operators.

Each computer can address 1 Mbyte of memory in any combination of local and shared memory. The amount of core memory on each computer is shown in Fig. 2. We plan to increase the size of shared memory and the amount of memory on each computer. The shared memory will be doubled to two, 128-kbyte memories. The memory on each computer will be as follows:

Computer	Memory
System supervisor	512 kbyte
Injector supervisor	768 kbyte
Data base manager	768 kbyte
Diagnostics data processor	768 kbyte
Plasma streaming supervisor	512 kbyte
Startup supervisor	704 kbyte
Sustaining supervisor	704 kbyte
Vessel supervisor	640 kbyte
Facilities supervisor	640 kbyte

Each machine has either a 10-Mbyte disk or an 80-Mbyte disk. The data base manager has one each of these disks plus a 300-Mbyte disk to be used for data base storage. The data base manager and the diagnostics data processor have a 75-in., 800/1600-bit/in. magnetic tape drive and a 600-line/min Versatec printer/plotter. In addition, the data base manager has a card reader. Each computer has single- and double-precision floating-point hardware.

Each computer has a hard-copy typewriter used as a computer console, internal clocks for time-of-day and interval scheduling, a digital input/output board for signaling other computers, a hardware interrupt board for receiving signals from other computers, and a hardware bootstrap board.

Communication with the local control computers is performed using RS232C interfaces connected to the supervisor computer through the memory access multiplexer, which is a multichannel direct memory access device. The communication rate with each local control computer is 9600 baud.

Backup Capability

One of the major design considerations in the hardware is the backup capability. In case of failure of any computer, the SCDS can still communicate with all the local control computers to process data and output data to magnetic tape. Several hardware I/O bus switches are in the system, shown in Fig. 3. The system is constructed so that the local control computers normally connected to either the facilities or vessel supervisor may also be connected to the other. Thus, if either of these computers is down, the other communicates with six local control computers. The bus switch is activated either manually or under computer control. Normally, the switching occurs automatically, but if one computer failure made it impossible for the other to automatically assume control, a manual switchover would occur.

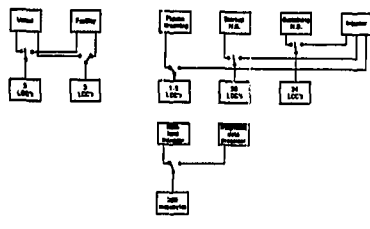


Fig. 3. Supervisory Control and Diagnostics System I/O Bus Switches

Similarly, the local control communication functions of the plasma streaming supervisor, the startup supervisor, or the sustaining supervisor can be assumed by the injector supervisor. The hardware design precludes the injector supervisor from assuming communications from two or more lower computers.

The other bus switch in the system allows the 300-Mbyte disk, which holds a large amount of the data base data, to switch from the data base manager to the diagnostics data processor. If the disk is inoperative, the data base information can be put directly on tape on two machines. There are two tape drives on two different machines; thus, a single point failure will not prevent data from being stored on tape.

In case of some of these failures, notably in the 256-Mbyte disk, a serious degradation in performance of the system could occur, but the system would still operate.

NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Department of Energy, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately-owned rights.

Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.