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PHASE 2 OF THE ARRAY AUTOMATED ASSEMBLY TASK FOR THE LOW COST SILICON SOLAR ARRAY PROJECT

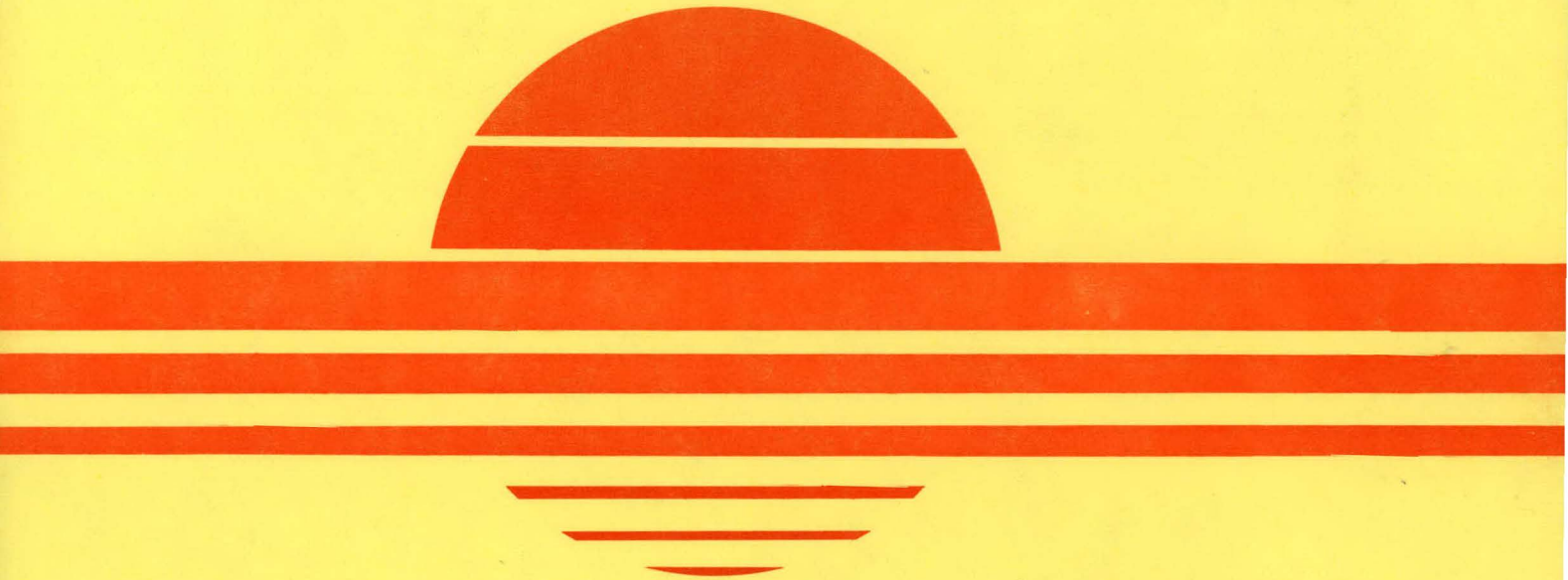
Fifth Quarterly Report

By
Raymond C. Petersen
Jack R. Anderson

January 1980

Work Performed Under Contract No. NAS-7-100-954854

Solarex Corporation
Rockville, Maryland



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FIFTH QUARTERLY REPORT

JANUARY, 1980

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"The JPL low-cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

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SUMMARY

Work in this first quarter of the program extension comprised portions of the first three experimental tasks. The task to study nickel plating on silicon oxide films has been initiated but has not yet been completed. The environmental stress testing of electroless nickel contacts has been formally completed; data and conclusions are presented. The study of nickel penetration of silicon is well under way. These three tasks are scheduled for completion in the next quarter.

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1. INTRODUCTION

This program is a supplement to the original process program. It focuses attention on one key step of a proposed process sequence for mass production of inexpensive silicon solar arrays for terrestrial use. The process step of concern is the metallization of the solar cell.

Solarex has proposed that the metallization be accomplished by a single electroless plating of nickel followed by a dip in molten solder, and Solarex manufactures solar cells using this procedure. Motorola has recommended a process which includes the electroless nickel plate and solder dip of the Solarex process, but which precedes these steps with a number of additional steps of palladium plating, cleaning and annealing. Motorola has claimed that these additional steps are necessary to assure proper ohmic contact with the silicon while at the same time avoiding excessive nickel penetration into the silicon.

This program comprises a technical comparison of the Solarex and Motorola processes, and at the same time it incorporates studies of some of the underlying processes which are important to the understanding and controlling of

the total plating process. The work includes five experimental tasks: the first four of these tasks are studies of some physical processes which are fundamental to the overall metallization process, while the fifth task is a direct comparison of the Solarex and Motorola plating processes.

Work has been conducted on three of these tasks; each is scheduled for completion during the next quarter. The remaining two tasks, the study of the effect of the nickel plating solution on solar cells, and the direct comparison of the Motorola and Solarex processes, will be started in the next quarter.

1.1 Effects of Surface Oxide Thickness and Sintering Temperature

Surface oxides on silicon solar cells are recognized as a potential source of difficulty in applying contact metallization to the cells. Fabrication processes include etching and cleaning procedures designed to remove surface oxides from the silicon, but these procedures are not perfect, and some oxide, of undetermined and perhaps variable thickness, will usually be carried over to the metallization step. This oxide may be the cause of poor adhesion, poor ohmic contact, or both, and may lead to poor reproducibility in the metallization process.

Cells are usually sintered after the metallization step, sometimes at high temperatures, sometimes at relatively low temperatures, in an effort to improve the adhesion and electrical contact properties, presumably through diffusion of the contact metal through the oxide and into the silicon.

The first experimental task in this program is an assessment of the influences of silicon surface oxide thickness and sintering temperature on the adhesion and electrical characteristics of electroless nickel plates on oxidized silicon.

1.2 Environmental Testing of Electroless Nickel Contacts

The Solarex metallization process under study here employs an electroless nickel plating followed by a dip in molten solder. The quality of the bond produced depends upon the quality and cleanliness of the silicon surface being plated, upon the quality of the electroless nickel plate itself, and upon the effectiveness of any sintering action.

The bond produced by this process appears adequate for many solar cell applications, but it may be weaker than bonds formed by some other metallization processes. While

the initial construction generally exhibits perfectly adequate properties, there is some concern as to whether it will perform adequately over an extended period of cell operation under a variety of adverse environmental conditions.

The second experimental task of the program is a study of the integrity of the silicon - metal bond during environmental stress tests. No accelerated stress regimen has yet been demonstrated to be a reliable or useful predictor of solar cell lifetime behavior, but four relatively demanding stress tests have been selected which might be predicted to have some deleterious effect on the silicon - metal bond.

Electrical characteristics of the cells are compared before and after the stresses, and pull tests are conducted on the cells after stress and also on a group of control cells.

1.3 Nickel Penetration of Silicon

Metallized solar cells are usually heated, under conditions ranging from mild to severe, to improve the contact between the silicon and the metallization. A critical concern in the case of nickel metallization is

the possibility of nickel diffusion at elevated temperatures through the front junction of the solar cell, an occurrence which would create paths of high current leakage and could effectively destroy the solar cell.

This task is a study of nickel penetration into silicon as a function of sintering temperature and time in a range that might be experienced in solar cell manufacture. Detection of nickel diffusion will be accomplished by microprobe analysis.

2. EFFECTS OF SURFACE OXIDE THICKNESS AND SINTERING TEMPERATURE

The first phase of this task comprises the growth of oxide films on silicon in thicknesses ranging from 20 to 200 Angstroms, measurement of the oxide thicknesses by ellipsometry, electroless plating of nickel, sintering for one minute at various temperatures from 200°C to 600°C, soldering of interconnect tabs, and testing of adhesion by tab pull tests.

In a second phase of the task, solar cells will be made from silicon specimens having surface oxide films, and electrical characteristics will be measured.

Preliminary experiments were conducted on surface cleaning, growth of oxide films, and measurements of film thickness. Nickel has been plated by the electroless process on a number of specimens having oxide thicknesses up to 100 Angstroms. Good adhesion has been obtained with sintering, but no tab pull tests have been conducted yet.

It appears that it will be difficult, perhaps impossible, to plate nickel directly on silicon oxide films much thicker than 100 Angstroms, and sintering at the higher temperatures may also prove to be useless.

3. ENVIRONMENTAL TESTING OF ELECTROLESS NICKEL CONTACTS

Four environmental stress tests have been selected to test the integrity of the silicon - nickel bond produced by the electroless nickel plating process. The tests include thermal cycle and thermal shock stresses as well as a 1,000 hour test at 150°C and a 1,000 hour bias - temperature - humidity test.

3.1 Cells

Solar cells have been constructed for the stress tests using the Solarex process in which nickel is plated directly on the silicon cell by the electroless plating method, with the cell then being dipped in molten solder. The cells are 2 cm squares cut from larger wafers and have a bus, about 1 mm wide, parallel to and close to one edge. Silicon used was Monsanto CZ 100, P type, boron dopant, 1-25 ohm-cm.

3.2 Tab Soldering

A procedure for soldering tinned copper tabs (70 mils wide, 2 mils thick) across the bus has been developed which uses minimum temperature and time in order to avoid

influencing the silicon - nickel interface. This soldering procedure is detailed in Appendix A. Electrical measurements made on representative samples before and after soldering showed no change, indicating that the tab bonding procedure was not substantially affecting the Si - Ni bond.

3.3 Cell Preparation for Stress Tests

On most of the cells, two tabs were soldered to the front bus, thus providing two data points from each cell. Area of the bond to the front bus could be reproduced within reasonably narrow limits, while bonds made to the back solder varied somewhat in area. It was also more convenient to measure electrical characteristics with no tab on the back.

The cells to be used for the bias - temperature - humidity (B-T-H) test required electrical connections to the backs, so a group of thirty cells had one tab soldered to the front bus and one near the back center. These cells are pictured in Figure 1.

3.4 Electrical Characteristics of the Cells

Electrical characteristics of the cells were measured before and after the stress tests. Current - voltage curves

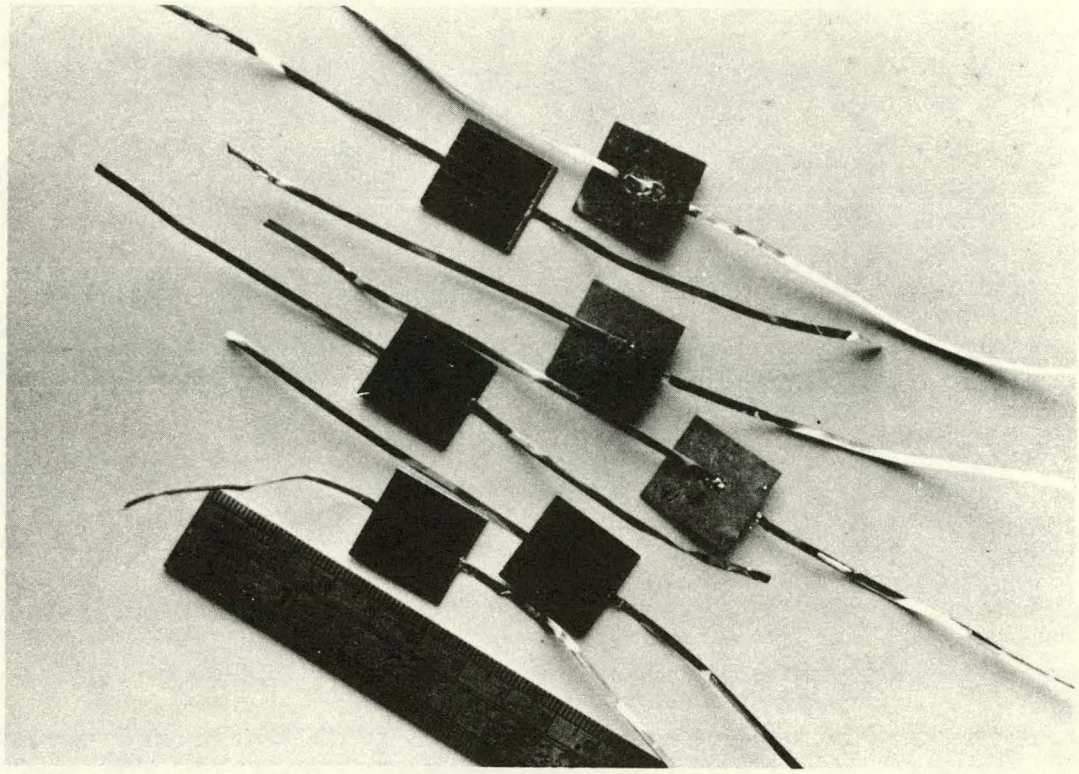

Figure 1 Bias - Temperature - Humidity Test Cells

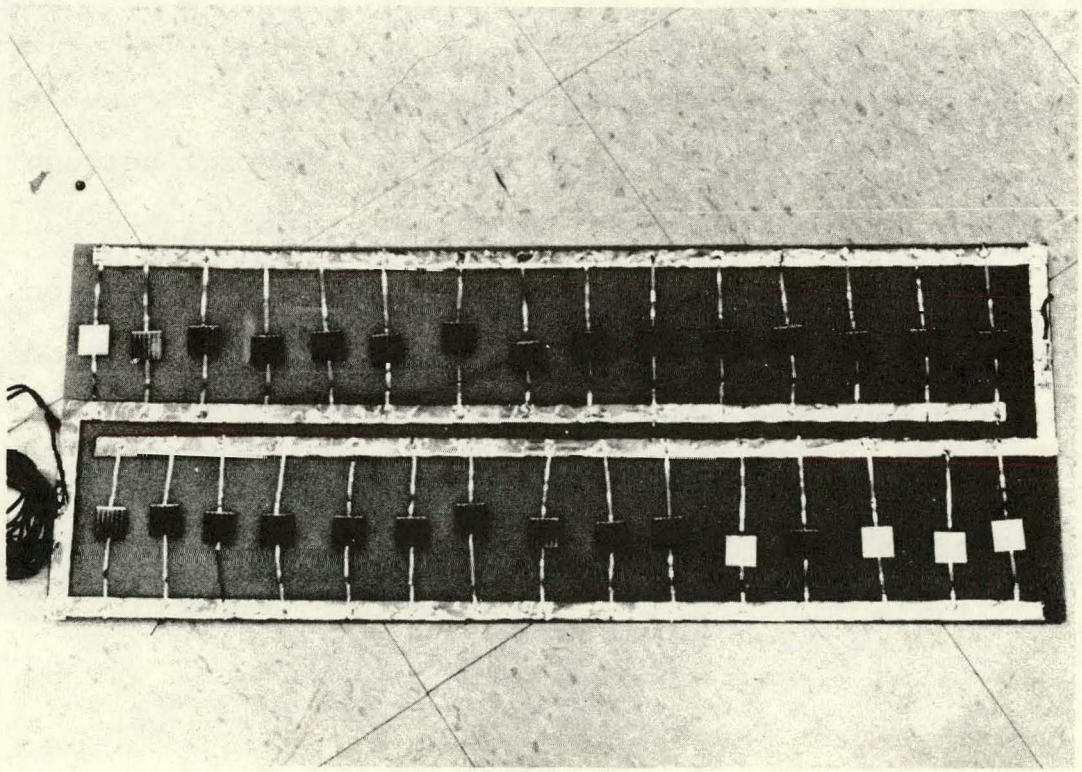

Figure 2 B- T- H Test Cell Array

were recorded at AMO for full sun and with red and blue filters using a solar simulator for illumination. Calibration of the equipment was checked periodically with a standard cell.

Open circuit voltage (V_{oc}), short circuit current (I_{sc}), maximum power (P_m) and series resistance (R_s) were obtained from the current - voltage curves. In addition to these parameters, shunt resistance (R_{sh}) was also determined. This was done by measuring dark leakage current across the cell under reverse bias of 1.000 volt. The shunt resistance is then the ratio of the bias potential to the leakage current.

Series resistance could be a significant parameter in assessing the quality of the electrical contact between the silicon and the nickel, while shunt resistance should provide a direct indication of any junction penetration by nickel. The other electrical parameters are influenced in a less direct manner by these factors.

3.5 Stress Tests

3.51 Bias - Temperature - Humidity Test

Thirty cells for the B-T-H test were mounted by

soldering to a printed circuit board, after a suitable pattern had been etched in the copper conductor of the board and the remaining copper had been tinned with solder. The assembly, pictured in Figure 2, was then placed in a temperature - humidity chamber at 85°C and 85% relative humidity, and the cells, connected in parallel, were biased at 0.45 volt in the forward direction. This stress was continued for 1,074 hours.

The temperature - humidity chamber is a Blue M Electric Co. Model FR-256PBX equipped with temperature and humidity sensing, regulating and recording devices. The regulated biasing power supply was a Model 2015-R from Power Designs, Inc.

3.52 High Temperature Test

For the high temperature stress test, a group of thirty cells was placed in a thermally regulated oven at 150°C in air, and was left there for 1,008 hours. The oven was a Wylie Temperature Test Chamber Model C106-640.

3.53 Thermal Shock Test

For the thermal shock stress test, the high temperature bath was a stainless steel beaker of about 3.75

1 capacity containing 2 1 of fluorocarbon FC-40. It was heated on a hot plate whose heating rate was adjusted such that the liquid temperature (measured by an ordinary mercury bulb thermometer) would increase slowly at 150°C.

The low temperature bath was a stainless steel beaker of about 1.25 1 capacity containing about 0.8 1 of fluorocarbon FC-77. This beaker was immersed in a mixture of dry ice and iso-propyl alcohol in a larger stainless steel container of about 7.5 1 capacity. The larger container was insulated by one inch of polyurethane foam. Temperature was measured by a thermocouple.

The cells under test were held in a small Teflon cassette with a capacity of 24 cells. The cassette containing the cells was placed in the high temperature bath with the temperature near 155°C, held there for five minutes, transferred to the low temperature bath, whose temperature was near -70°C, left for five minutes, then transferred again to the high temperature bath. This procedure was continued for 25 cycles, and two sets of cells were run to achieve a total of 29 cells. Transfer time was typically 4-6 seconds. Measured temperature of the cold bath typically rose about four degrees when the hot cassette was introduced

to the cold bath, while temperature variation in the hot bath was smaller than this when the cold cassette was introduced into it.

3.54 Thermal Cycle Test

A group of thirty cells was subjected to a thermal cycling stress in which they were first placed in a chamber at low temperature (-65 to -70°C) for ten minutes and then in a chamber at high temperature (150 to 155°C) for ten minutes, after which the cycle was repeated for a total of 100 cycles. Cells were contained in a Teflon cassette, and transfer time was less than 15 seconds.

The high temperature chamber was a Blue M Electric Company oven Model SW-17TA, and the low temperature chamber was a Wylie Temperature Test Chamber Model C106-640 using chilled nitrogen as the coolant.

3.55 Control Cells

Cells for a control group were stored in a cabinet at room temperature with a nitrogen atmosphere.

3.6 Results of Environmental Stress Tests

3.61 Results of Bias - Temperature - Humidity Test

A group of thirty cells was subjected to 85% relative humidity at 85°C under forward bias of 0.45 volt for 1,074 hours. At the end of the test these cells were unchanged in appearance, showing no visible evidence of corrosion or of contact deterioration.

Electrical characteristics, shown in Table 1, changed only slightly, with average V_{OC} increasing by 1.4%, I_{SC} decreasing by 0.7%, P_m increasing by 0.9%, R_S decreasing by 11.2% and R_{Sh} increasing by about 30%. With the exception of the small decrease in short circuit current, all of these changes are in desirable directions. The relatively large increase in shunt resistance may be a result of elimination by oxidation of microscopic metallic shunts at cell edges.

Tab pull strengths after the stress, shown in Table 2, averaged 257 grams on the front (bus) tabs and 474 grams on the back solder tabs, with four failures at the tab joint and the remaining 56 failures occurring at the metal-silicon interface. No silicon damage was apparent in any instance. Tab pull strengths on the control cells averaged 177 grams.

Table 1

Electrical Characteristics of B-T-H Test Cells

Cell	V_{oc} (mV)	I_{sc} (mA)	P_m (mW)	R_s (ohm)	R_{sh} (ohms)
11	563(563)	137(130)	53.0(51.5)	.315(.320)	194(228)
12	560(562)	139(139)	55.0(55.0)	.348(.341)	131(168)
13	569(579)	140(138)	56.5(55.5)	.353(.453)	1159(1522)
14	537(545)	135(131)	50.5(51.0)	.328(.290)	132(204)
15	541(553)	135(139)	54.5(56.5)	.319(.313)	840(1075)
16	532(535)	133(131)	49.5(49.5)	.315(.283)	122(141)
17	534(544)	133(135)	52.0(54.0)	.331(.299)	286(357)
18	572(580)	142(140)	56.0(56.0)	.340(.302)	173(243)
19	569(576)	138(135)	54.5(54.5)	.400(.434)	309(394)
20	565(572)	140(138)	54.0(54.0)	.357(.327)	478(565)
21	532(541)	135(130)	53.0(54.0)	.381(.315)	6667(6410)
22	565(573)	139(138)	56.5(57.5)	.333(.295)	980(1647)
23	545(552)	138(136)	51.0(52.0)	.398(.350)	265(344)
24	575(579)	140(136)	58.0(56.0)	.414(.387)	1250(1901)
25	566(566)	143(140)	54.5(55.0)	.385(.304)	193(260)
26	530(539)	134(136)	52.0(53.5)	.322(.291)	980(1328)
27	569(580)	138(137)	54.5(55.0)	.392(.310)	193(226)
28	577(580)	138(142)	57.0(58.5)	.304(.299)	403(552)
30	530(538)	136(136)	52.0(53.0)	.381(.335)	1887(2212)
31	560(571)	134(135)	54.0(55.5)	.255(.204)	333(348)
32	530(540)	135(134)	51.5(52.5)	.351(.242)	980(1274)
35	560(572)	132(130)	51.0(53.5)	.416(.240)	3571(3984)
36	571(577)	135(127)	54.0(52.0)	.350(.298)	124(161)
37	566(580)	138(142)	56.0(58.5)	.320(.300)	1299(1841)
38	556(561)	137(137)	50.5(52.0)	.439(.361)	1515(1318)
39	569(580)	133(133)	53.0(54.0)	.391(.312)	187(240)
40	559(573)	133(135)	52.0(54.0)	.413(.381)	585(725)
43	560(568)	135(136)	56.0(57.0)	.336(.279)	352(571)
44	567(575)	126(123)	52.0(51.5)	.365(.298)	735(826)
45	555(557)	136(133)	56.0(54.5)	.324(.317)	233(3356)
Mean	556.1 (563.7)	136.2 (135.1)	53.7 (54.2)	.356 (.316)	885 (1147)
S.D.	15.5 (15.4)	3.4 (4.3)	2.2 (2.2)	.041 (.051)	1310 (1377)

Data before and (after) 1,074 hours at 85°C and 85% relative humidity biased at 0.45 volt in the forward direction.

Table 2

B-T-H Stress Tab Pull Strengths

	Pull Strength (g)			Pull Strength (g)	
Cell	Front	Back	Cell	Front	Back
11	573	488	26	179	420
12	0	417	27	332	71
13	198	539	28	184*	590
14	99	227	30	454*	516
15	335	252	31	113	505
16	0	445	32	312	765
17	403	221	35	371	598
18	454	323	36	337	706
19	235*	610	37	264	513
20	309	652	38	139	221
21	227	346	39	283	289
22	312	507	40	431	235
23	164	516	43	43*	624
24	326	1264	44	417	627
25	173	289	45	45	451

Front Mean 257 S.D. 145

Back Mean 474 S.D. 225

* tab failure; all others failed at metal-silicon interface.

3.62 Results of High Temperature Stress Test

A group of thirty cells was subjected to 150°C temperature for 1,008 hours. Most of these cells showed severe degradation of electrical characteristics, as shown in Table 3, and also exhibited visible lifting of the metal contacts.

Five of the cells (numbers 143, 144, 157, 170, 183) showed very little change in electrical properties, and four of these five also appeared perfect to visual inspection, while the fifth showed a small amount of contact lifting.

Tab pull strengths, shown in Table 4, averaged 124 grams, with many showing near zero strength. For the five cells listed above as showing little change in electrical properties, tab pull strengths averaged 90 grams, essentially the same as for the group as a whole. In all cases the failures occurred at the Si - Ni interface with no evidence of silicon damage.

It is possible that the performance observed at 150°C is not a fundamental property of the nickel - silicon bond,

Table 3

Electrical Characteristics of 150°C Test Cells

Cell	V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
113	543(534)	138(79)	51.5(16.0)	.482(4.14)	5263(4831)
130	580(570)	135(140)	54.0(40.0)	.330(1.64)	1587(1121)
135	586(563)	133(71)	55.5(14.0)	.312(4.33)	3508(1935)
136	575(582)	133(139)	53.0(47.0)	.328(1.18)	1447(1451)
137	565(*)	128(*)	52.5(*)	.230(*)	1664(*)
138	581(578)	136(143)	56.0(38.0)	.275(1.91)	1295(1067)
139	578(570)	131(51)	51.0(**)	.288(**)	1812(1715)
140	578(576)	136(131)	53.5(35.0)	.524(2.52)	529(500)
142	563(585)	128(130)	55.5(43.0)	.214(1.27)	1270(1451)
143	544(541)	130(137)	52.0(53.0)	.272(.329)	833(699)
144	565(574)	127(135)	52.0(52.0)	.343(.640)	971(990)
146	570(565)	136(77)	54.0(14.0)	.196(4.69)	862(1015)
147	562(515)	136(91)	51.5(17.5)	.326(3.33)	926(947)
152	583(565)	133(132)	56.0(33.5)	.270(2.29)	794(645)
153	565(543)	135(38)	50.0(**)	.489(**)	1992(1618)
155	568(557)	132(138)	54.0(43.0)	.264(1.31)	15873(15384)
156	560(572)	111(131)	44.5(42.0)	.443(1.29)	667(595)
157	550(548)	123(126)	49.5(49.5)	.293(.347)	2463(2194)
159	575(576)	137(131)	55.0(37.0)	.309(2.12)	1337(962)
161	579(543)	136(60)	56.0(**)	.285(5.59)	870(923)
162	563(567)	133(134)	55.5(37.0)	.261(2.91)	1610(1041)
163	565(556)	131(86)	53.0(18.0)	.304(4.21)	3937(3584)
168	576(566)	129(131)	52.0(45.0)	.234(.694)	575(826)
170	570(574)	134(143)	54.5(55.5)	.300(.487)	1534(1481)
172	587(576)	128(104)	54.5(27.0)	.246(3.12)	1015(943)
175	575(570)	126(132)	50.5(44.0)	.201(.963)	1026(794)
177	580(578)	124(75)	51.0(14.0)	.236(4.93)	578(571)
183	570(571)	135(142)	54.5(55.0)	.297(.467)	1163(719)
185	584(583)	124(123)	54.0(33.0)	.199(2.70)	719(641)
189	585(581)	124(74)	54.0(14.0)	.259(5.39)	826(704)
Mean	570.8 (564.8)	130.7 (111.2)	53.0 (35.3)	.300 (2.40)	1965 (1771)
S.D.	11.6 (16.6)	5.8 (32.4)	2.5 (14.1)	.084 (1.67)	2834 (2778)

Data before and (after) 1,008 hours at 150°C.

* cell broken in handling; ** too poor to measure.

Table 4

150°C Stress Tab Pull Strengths

	Pull Strength (g)			Pull Strength (g)	
Cell	Tab #1	Tab #2	Cell	Tab #1	Tab #2
113	193	391	155	198	145
130	0	*	156	116	*
135	57	71	157	0	335
136	0	*	159	60	*
137	0	*	161	85	96
138	23	*	162	11	113
139	57	*	163	198	*
140	0	0	168	204	*
142	0	*	170	139	136
143	0	57	172	369	*
144	147	*	175	278	193
146	145	145	177	119	*
147	411	255	183	0	0
152	113	357	185	57	*
153	170	*	189	0	*

Mean 124 S.D. 119

* bus peeled with first tab

All failures occurred at metal-silicon interface.

but rather that it is a result of contamination of the silicon surface from some process step preceding the nickel plating. Any masking technique, for example, can introduce contamination on the silicon surface which may be very difficult to remove, because cleaning techniques designed to guarantee removal of such contamination are likely to attack the chemically similar masking material as well.

3.63 Results of Thermal Shock Stress Test

A group of twenty-nine cells was subjected to 25 cycles of the thermal shock test; electrical characteristics of these cells are shown in Table 5, and results of tab pull tests are shown in Table 6.

It can be seen from the few cases in which contacts appeared to be intact that the electrical properties changed very little, even though the tab pull tests showed clearly that these contacts had, in fact, been weakened considerably. This observation suggests that the tab pull test is a more sensitive indicator of metallization integrity than are the electrical measurements.

One major point to note is the evidence of silicon damage in most of these cells, unlike the total absence of such

Table 5

Electrical Characteristics of Thermal Shock Test Cells

Cell	V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
191	559(565)	122(131)	50.0(41.0)	.304(1.839)	1427(1385)
192	558(*)	123(*)	49.0(*)	.339(*)	1042(*)
193	555(*)	124(*)	48.0(*)	.396(*)	855(*)
194	566(*)	127(*)	52.0(*)	.334(*)	704(*)
195	574(577)	129(131)	50.0(34.0)	.313(2.360)	521(452)
196	580(582)	126(133)	52.0(54.0)	.288(.336)	442(263)
197	548(553)	119(125)	46.5(46.0)	.339(.581)	137(123)
198	530(*)	120(*)	44.5(*)	.516(*)	295(*)
199	565(*)	127(*)	44.5(*)	.574(*)	543(*)
202	516(*)	112(*)	39.5(*)	.518(*)	1299(*)
203	548(*)	116(*)	43.5(*)	.259(*)	49(*)
204	546(552)	122(126)	50.0(36.5)	.264(2.522)	379(347)
206	573(584)	126(132)	51.0(44.5)	.302(1.305)	254(181)
207	551(552)	121(118)	50.0(33.0)	.241(2.462)	195(185)
208	553(*)	124(*)	48.0(*)	.441(*)	806(*)
211	548(*)	123(*)	47.0(*)	.526(*)	575(*)
212	558(*)	124(*)	45.5(*)	.416(*)	220(*)
214	579(*)	130(*)	53.5(*)	.329(*)	1250(*)
219	522(*)	119(*)	45.0(*)	.405(*)	2000(*)
220	552(569)	124(131)	49.0(46.0)	.358(.802)	1190(820)
222	549(556)	117(124)	47.0(45.5)	.278(.648)	100(99)
224	528(530)	121(111)	47.0(29.0)	.287(2.337)	1389(1393)
226	542(540)	114(109)	43.0(36.0)	.241(.794)	81(84)
227	545(*)	122(*)	47.5(*)	.405(*)	232(*)
233	546(*)	121(*)	47.0(*)	.406(*)	220(*)
236	570(*)	126(*)	52.5(*)	.278(*)	362(*)
238	578(*)	134(*)	52.0(*)	.371(*)	855(*)
239	544(*)	119(*)	45.5(*)	.464(*)	266(*)
242	580(*)	135(*)	55.0(*)	.357(*)	4545(*)

* unable to measure

Data before and (after) Thermal Shock Stress.

Table 6

Thermal Shock Stress Tab Pull Strengths

	Pull Strength (g)			Pull Strength (g)	
Cell	Tab #1	Tab #2	Cell	Tab #1	Tab #2
191	28	---*	211	---*	---*
192	---	---*	212	---	---*
193	---	---	214	---*	---*
194	---*	---	219	0*	85*
195	28*	---*	220	28*	99*
196	170*	0*	222	0*	---*
197	28*	0*	224	---*	57*
198	43*	---	226	0*	0*
199	---*	---*	227	---*	---*
202	---*	---	233	---	---*
203	---*	---*	236	---	---
204	0*	---*	238	---*	227*
206	---*	28*	239	---*	---*
207	0*	---*	242	---*	---*
208	---*	---*			

--- bus lifted at tab during thermal shock cycling.

* silicon damage evident; all others failed at silicon - nickel interface.

Some degree of lifting of back solder was evident in fifteen of the cells.

damage in the cells subjected to the high temperature and bias - temperature - humidity stresses, and the fact that this silicon damage occurs during the thermal shock cycles without the application of any external mechanical stress.

Another group of cells, fabricated using a different masking technique, was also subjected to the thermal shock test, and the results were essentially identical.

In an additional experiment, buses were formed on diffused and alloyed silicon using Kapton tape as a masking material for the nickel plating. Using this technique, the masking process does not contaminate the surface of the silicon to be plated. The tape was removed prior to solder dipping. These specimens were then subjected to the thermal shock test.

Nearly all of the buses lifted during the thermal shock stress, and in every case the silicon was damaged over the entire area under the bus. Silicon damage in the regular cells was not that extensive, suggesting that the masking process does contribute some degree of contamination to the silicon surface.

3.64 Results of Thermal Cycle Stress Test

A group of thirty cells was subjected to a thermal cycle stress alternating between -65°C and +150°C in air for 100 cycles. In every case the bus peeled 100% or nearly 100%. In some cases the contact failure was evident early in the test.

No electrical measurements or tab peel tests could be conducted on these cells after the stress test.

In general the metal separation occurred at the Si - Ni interface, with evidence of some separation at the nickel - solder interface in eight cells, and some silicon damage, ranging from a single small pit to about 70% of the bus area, was apparent in twenty-one of the cells.

3.65 Results of Control Cells

A group of 100 cells was stored in nitrogen at room temperature for about ten weeks as a control group. Electrical data from these cells are shown in Table 7.

Tab pull strengths of these cells averaged 177 grams. Of the 200 tabs, 7 failed at the tab - solder joint, 32

Table 7

Electrical Characteristics of Control Cells

Cell	V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
50	591(586)	129(135)	52.5(54.5)	.306(.297)	78(78)
51	576(568)	133(137)	56.0(55.5)	.216(.294)	323(300)
53	563(558)	129(132)	40.0(40.0)	.100(.059)	9(9)
54	573(564)	132(135)	52.5(52.0)	.327(.351)	870(408)
55	550(538)	126(127)	50.0(49.0)	.261(.233)	100(95)
56	581(570)	135(130)	54.5(54.5)	.377(.261)	746(680)
57	579(569)	138(141)	55.0(56.5)	.464(.288)	654(617)
58	555(542)	130(127)	39.0(33.5)	.211(.487)	17(16)
59	590(580)	137(136)	57.5(56.5)	.361(.312)	2336(1828)
60	546(536)	131(135)	52.0(52.0)	.308(.274)	294(234)
61	576(565)	128(130)	54.0(53.0)	.235(.253)	478(420)
62	581(571)	133(134)	55.0(55.0)	.265(.265)	166(160)
63	563(550)	133(137)	48.0(48.0)	.297(.392)	45(43)
64	585(573)	134(138)	52.5(54.0)	.424(.332)	6993(1592)
65	572(563)	134(135)	53.5(53.0)	.315(.344)	806(538)
66	589(580)	127(128)	53.5(52.0)	.239(.316)	7874(8197)
67	550(539)	122(124)	50.5(50.0)	.248(.205)	585(546)
68	565(553)	133(136)	52.5(52.0)	.321(.317)	1709(1294)
69	573(570)	129(138)	52.0(54.0)	.241(.300)	588(442)
70	578(570)	137(140)	56.5(57.0)	.312(.314)	184(172)
71	548(538)	132(134)	53.0(53.0)	.261(.284)	472(410)
72	595(584)	125(128)	54.0(54.0)	.288(.265)	472(448)
73	571(565)	127(132)	55.0(56.0)	.213(.233)	2732(2525)
74	581(575)	122(131)	50.0(52.0)	.238(.262)	56(53)
75	577(573)	128(137)	53.0(56.0)	.261(.266)	234(227)
76	573(569)	119(127)	50.0(53.0)	.287(.262)	2618(2053)
77	586(585)	123(130)	52.0(54.0)	.259(.286)	787(714)
78	568(566)	125(131)	47.5(47.0)	.213(.379)	45(43)
79	551(548)	131(139)	46.5(49.5)	.299(.296)	30(29)
80	545(536)	120(127)	47.0(49.0)	.351(.316)	244(230)
81	543(536)	127(135)	50.5(51.5)	.268(.264)	694(595)
83	577(571)	121(132)	51.0(55.0)	.229(.269)	862(725)
84	573(565)	119(126)	50.5(52.0)	.257(.267)	303(291)
85	534(527)	133(141)	44.5(46.0)	.701(.709)	146(142)
86	572(567)	131(139)	52.5(54.5)	.285(.334)	820(662)
87	579(575)	124(132)	52.0(52.0)	.247(.474)	171(163)
88	585(580)	122(127)	49.5(51.5)	.291(.280)	86(83)
90	570(562)	117(126)	49.0(52.0)	.272(.286)	667(641)

Electrical Characteristics of Control Cells

Cell	V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
91	572(562)	125(129)	52.5(52.5)	.324(.332)	1020(980)
92	573(566)	127(127)	53.0(52.0)	.274(.276)	1282(990)
93	549(538)	124(122)	51.0(48.0)	.206(.333)	315(286)
94	579(570)	128(130)	51.5(51.0)	.312(.318)	2083(1538)
95	583(581)	129(132)	54.0(54.5)	.310(.361)	1064(1068)
96	565(556)	122(125)	48.5(48.0)	.378(.402)	800(714)
97	548(538)	126(127)	51.0(50.0)	.294(.287)	259(243)
98	573(566)	136(135)	56.0(54.0)	.274(.301)	606(532)
99	574(566)	126(127)	52.5(51.5)	.258(.280)	5525(3401)
100	579(572)	140(143)	56.0(56.0)	.302(.317)	662(613)
115	585(576)	135(141)	57.0(57.0)	.341(.323)	314(298)
116	575(569)	136(141)	55.0(55.5)	.300(.340)	1730(1285)
117	582(572)	128(132)	52.5(52.0)	.252(.248)	158(149)
118	580(574)	125(130)	52.5(53.5)	.277(.252)	1043(877)
119	582(577)	130(135)	54.5(55.0)	.207(.237)	556(400)
120	578(568)	135(141)	52.0(53.0)	.424(.485)	690(581)
121	565(557)	129(131)	40.5(40.0)	.391(.411)	34(33)
122	579(576)	131(140)	51.0(54.0)	.329(.337)	108(99)
123	595(589)	132(138)	57.5(58.5)	.298(.290)	1247(1034)
124	581(575)	128(131)	53.0(52.0)	.272(.310)	314(299)
126	540(538)	135(141)	48.0(49.0)	.522(.545)	60(58)
128	579(577)	126(134)	54.0(56.5)	.246(.256)	441(490)
129	576(573)	126(129)	50.0(50.0)	.339(.305)	125(121)
131	577(570)	128(131)	53.0(53.0)	.240(.282)	250(234)
133	586(576)	126(129)	51.5(51.5)	.253(.250)	212(195)
145	588(582)	127(130)	52.0(52.0)	.251(.267)	75(70)
148	570(563)	132(136)	52.0(54.0)	.412(.353)	3257(2841)
149	565(558)	135(139)	53.0(53.0)	.239(.275)	680(599)
150	578(568)	126(132)	54.0(54.0)	.245(.201)	232(221)
151	566(560)	133(135)	52.0(51.0)	.281(.262)	197(181)
154	580(576)	132(137)	55.0(54.5)	.257(.269)	170(166)
158	570(569)	133(138)	52.0(54.0)	.401(.290)	334(316)
160	567(567)	131(134)	51.0(51.0)	.307(.311)	306(267)
164	580(573)	130(133)	54.5(54.0)	.243(.240)	3322(1795)
165	590(583)	137(141)	57.0(58.0)	.332(.336)	3759(2941)
166	546(542)	122(122)	50.5(49.5)	.225(.237)	439(385)
167	592(581)	128(134)	57.0(57.0)	.172(.188)	4237(2551)
169	595(586)	129(134)	56.5(56.0)	.282(.278)	1949(1276)

Electrical Characteristics of Control Cells

Cell	V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
171	564(555)	133(135)	51.0(49.0)	.327(.299)	60(55)
173	574(573)	136(142)	55.5(56.0)	.326(.307)	503(364)
174	587(575)	130(129)	56.0(54.0)	.222(.226)	377(364)
176	579(569)	133(135)	53.0(51.0)	.289(.347)	413(345)
178	568(561)	126(123)	42.0(39.5)	1.006(1.023)	51(53)
179	569(565)	125(128)	50.5(50.0)	.266(.340)	397(327)
181	563(558)	135(138)	52.0(52.5)	.307(.287)	322(302)
182	579(577)	134(137)	54.5(54.0)	.373(.312)	307(266)
184	559(550)	138(143)	55.0(55.0)	.342(.371)	532(500)
188	560(557)	130(134)	45.0(43.5)	.346(.315)	286(278)
190	568(563)	121(124)	50.5(50.0)	.253(.269)	200(184)
1101	572(560)	132(134)	56.0(55.0)	.258(.277)	6369(4425)
1102	564(551)	138(139)	51.0(50.0)	.458(.444)	1502(1290)
1103	568(558)	132(137)	52.5(53.5)	.358(.306)	1553(1466)
1104	581(573)	125(126)	49.0(48.5)	.364(.298)	109(104)
1105	587(577)	136(137)	57.0(56.0)	.280(.301)	909(709)
1106	582(571)	133(138)	54.0(54.0)	.310(.321)	505(459)
1107	557(548)	139(142)	54.5(54.0)	.366(.378)	1116(1024)
1108	560(549)	135(138)	42.0(42.0)	.279(.120)	15(14)
1109	588(576)	130(130)	55.0(53.0)	.249(.290)	2933(2000)
1110	572(564)	126(129)	51.0(52.0)	.334(.292)	571(490)
1111	590(575)	143(136)	60.5(56.5)	.364(.385)	1244(1157)
1112	588(577)	129(133)	53.0(54.0)	.355(.280)	4808(2558)
1135	557(546)	139(142)	52.0(51.5)	.356(.353)	3509(3257)
Mean	572.4 (564.9)	129.8 (133.4)	52.0 (52.1)	.307 (.314)	1047 (798)
S.D.	13.4 (13.7)	5.3 (5.3)	3.8 (4.1)	.104 (.106)	1530 (1134)

Data before and (after) approximately ten weeks storage at room temperature in a nitrogen atmosphere.

failed at the nickel - solder interface, and the remainder failed at the silicon - nickel interface. There was no apparent silicon damage in any case.

3.7 Summary of Environmental Stress Tests

The cells survived the bias - temperature - humidity test perfectly.

The temperature extremes of -65°C and +150°C are too severe for these cells.

In several cases, where tab pull strengths showed that adhesion had degraded substantially, electrical measurements showed no change.

Different modes of failure were observed with different kinds of stress. In cells from the bias - temperature - humidity and high temperature test, as well as in the control group, failure was almost exclusively at the Si - Ni interface with no evidence of silicon damage. Cells from the thermal cycle test failed predominately at the Si - Ni interface, with some showing evidence of silicon damage, while failures in the thermal shock group occurred predominantly in the silicon.

4. NICKEL PENETRATION OF SILICON

In this task silicon specimens processed as solar cells and then sintered at various temperatures and times will be examined by electron microprobe to detect diffusion of nickel into silicon.

4.1 Silicon Preparation and Plating

Silicon wafers typical of those used for producing solar cells with electroless nickel plating have been processed (etch, phosphorus diffusion, aluminum alloy on back) and then have been plated with nickel using the Solarex electroless nickel plating process (but with no pattern on the front surface).

4.2 Sintering

Several 1 cm squares have been cut from the processed wafers and have been sintered in an inert atmosphere (He or N_2) for varying times at temperatures from 200°C to 400°C. Small decreases in measured shunt resistances suggest the possibility of some nickel diffusion in most of these specimens, but the changes were small and do not indicate any significant junction damage.

Specimens sintered at 350°C and higher, cooled in the inert atmosphere, then exposed to air, peel when exposed to air. Nickel is adhering tightly when first exposed to air, and then peels gradually around the edges with time. Measurements of the surface resistivity of the silicon after peeling show very low values of resistivity, indicating that the remaining surface probably contains some nickel.

A phase change is reported to occur at 325°C in plated nickel films containing phosphorus.(1) The initial state is reported to be a highly disordered solid solution of phosphorus in nickel, while heat treatment above 325°C produces two crystalline components, tetragonal Ni_3P and fcc Ni.

4.3 Specimen Preparation for Microprobe Analysis

A procedure was developed for mounting and angle lapping specimens for microprobe analysis. Specimens have been mounted in Buehler Castolite (a polyester) and have been lapped at an angle of 3.5° using successively finer grits down to 0.05 micron alumina for the final polishing.

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(1) Hedgecock, Tung, and Schlesinger, J. Electrochem. Soc. 122, 866 (1975).

Several specimens were delivered to Tousimis Research Laboratory for microprobe analysis, but the return of data has been substantially delayed by an equipment failure.

5. Conclusions

In the environmental stress tests, cells performed well for 1,000 hours at 85°C, 85% relative humidity, and 0.45 volt forward bias, but the temperature extremes of -65°C and +150°C were too severe for these cells.

At least two different failure mechanisms were operating in these tests, as evidenced by the two different modes of failure prevailing with the different kinds of stresses. This observation implies that at least some of these tests are not valid as accelerated predictors of lifetime behavior, because an accelerated life test procedure, to be valid, must not alter the failure mechanism. These stress tests may, however, be valuable in characterizing the silicon - metal bond.

The thermal shock test comparison between cells fabricated using a resist ink mask and specimens plated using Kapton tape masking suggests that the ink masking introduces some contamination on the silicon surface. This contamination will vary depending upon the specific masking material used, but in any case it may be virtually impossible to remove it completely without also damaging the mask,

since the masking material and the surface contaminant will be chemically very similar. The test results also indicate that the more intimate silicon - nickel contact provided with the Kapton tape mask may also be the more vulnerable to thermal stresses.

6. RECOMMENDATIONS

It is recommended that: 1) tape peel tests and tab pull strength measurements, rather than electrical measurements, be the primary diagnostic tools used in comparing the Solarex and Motorola Nickel plating processes; 2) that most of the plating be done without patterns on the cell fronts, and that when narrower segments are desired, bus patterns be formed using Kapton tape, or by some other method which will not contaminate the silicon surface; and 3) that thermal shock stresses, not necessarily at -65°C and +150°C, be used as an additional diagnostic tool to aid in characterizing the contact adhesion.

The first recommendation stems from our observation that the mechanical strength of the bond is at least as sensitive an indicator of contact integrity as are electrical measurements.

The second recommendation seeks to avoid contaminating the silicon surface by the masking process, and also recognizes that Solarex and Motorola use different masking techniques, while it is our purpose to compare the two plating methods with each other independent of complications and variations which might be introduced by the masking processes.

The third recommendation takes advantage of the fact that the thermal shock stress is a very severe one, and, as such, it may be a sensitive indicator of differences between the products of the different plating techniques.

7. WORK STATUS

The task to study the effect of oxide thickness and sintering time on nickel plating, scheduled for completion at the end of January, was delayed, and its completion will probably be about one month late.

The task to study environmental effects on the contacts, originally scheduled for completion in early March, has been formally completed.

The task to study nickel penetration of silicon, scheduled for completion in mid January, is currently being delayed by an equipment failure at the electron microprobe laboratory.

On balance, the program can be considered to be proceeding on schedule.

APPENDIX A

TAB SOLDER PROCEDURE FOR ENVIRONMENTAL STRESS TESTS

Soldering to Bus:

1. Erase AR coating, using ordinary pencil eraser, from bus area to which tab will be soldered.

2. Place cell on a heat sink (e.g. Al slab, 1/4" thick).

3. Place a small amount of solder paste (about 1 cu mm) on bus area to be soldered (solder paste = SCM Corp. ESP-150).

4. Place tab (70 mil wide, 2 mil thick, about 2" long tin-plated soft copper) across bus at point to be soldered so that the end of the tab is aligned with the center of the bus.

5. Press tab to cell with tip of soldering iron (Hexacon Thermotrac Model 1002 with 1/16" chisel tip - regulated at 600°F). Use quick strokes to avoid heating the cell excessively. Wipe soldering iron tip on a damp sponge prior to each application.

6. Place tabbed cells in an ultrasonic bath containing flux cleaner (Alpha Metals, Inc., #564) for five minutes, then rinse for five minutes in clean iso-propyl alcohol, and finally air dry.

Soldering to Back:

Follow the above procedure with the following modifications: step 1 can be eliminated; in step 3 add a little solder paste to the end of the tab; for step 4 place the end of the tab near the center of the back; in step 5 use a 1/8" chisel tip at 650°F and make the length of the bond approximately equal to the width of the chisel tip.

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