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AUTOMATED ARRAY ASSEMBLY, PHASE II

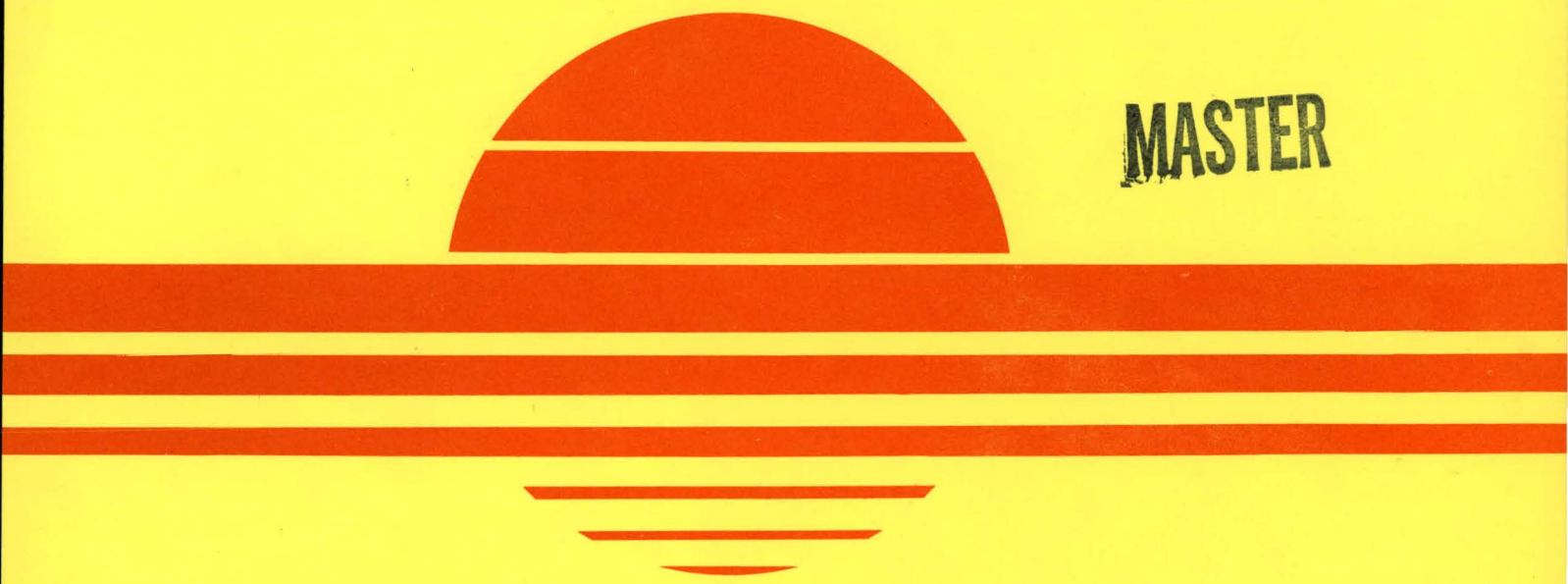
Quarterly Report No. 7

By
R. V. D'Aiello

October 1979

Work Performed Under Contract No. NAS-7-100-954868

RCA Laboratories
Princeton, New Jersey



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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, under NASA Contract NAS7-100 for the Department of Energy.

The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

Prepared Under Contract No. 954868 For

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California 91103

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PREFACE

This Quarterly Report, prepared by RCA Laboratories, Princeton, NJ 08540, describes the results of work performed from July 1, 1979 to September 30, 1979, in the Energy Systems Research Laboratory, B. F Williams, Director; Materials and Process Laboratory, Solid State Division, Somerville, NJ, R. Denning, Manager; and at the Advanced Technology Laboratory, Government and Commercial Systems, Camden, NJ, F. E. Shashoua, Director. The Project Scientist is R. V. D'Aiello and the Project Supervisor is A. H. Firester, Head, Process and Applications. Others who participated in the research and writing of this report are:

E. C. Douglas	-	Ion implantation
J. Murr	-	Screen printing
W. Kern E. Tracy	-	Spray-on AR coating
R. Daniel	-	Cost analysis
G. Lazzery R. Coyle	-	Interconnect and panel assembly
L. Guarino	-	Processing
G. Nostrand	-	Cell testing and test system design

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SECTION I

SUMMARY

During this period, work continued on studies of three manufacturing sequences for solar cells based on ion-implanted junctions, furnace annealing, screen-printed contacts, and spray-on antireflection (AR) coatings. The starting material has been primarily "solar-grade," n- and p-type 3-in.-diameter wafers; in addition, a small quantity of dendritic web has been received. A total of 1500 solar cells has been fabricated and evaluated.

As a result of this work, two problems areas have been identified relating to materials and process compatibility.

First, screen-printed thick-film inks do not contact ion-implanted junctions as well as diffused junctions. Previously we had demonstrated screen-printed contacts and determined suitable ink formulations and firing techniques on diffused-junction solar cells. We now find that when identical techniques are used with ion-implanted junctions, contact resistance problems typically occur on the ion-implanted cells. In most cases, the performance of diffused-junction solar cells is good immediately after the screen-printed inks are fired. In contrast, the AM-1 characteristics of ion-implanted solar cells are quite poor immediately after firing. They require an HF acid treatment and typically are not as good as diffused-junction cells. In addition, we have also noted degradation of the contact characteristics after spray AR coating.

Second, we have found that the previously determined optimum ion implantation/anneal process must be modified to accommodate the starting silicon material.

Discounting the above compatibility problems, we made evaluations and comparisons of the three manufacturing sequences with regard to the performance data accumulated for each sequence and its effect on cost-effectiveness. In cell interconnection and panel assembly, a solder reflow process has been demonstrated in which the cells are individually tabbed and then placed in an array which is soldered by means of a bank of infrared lamps which traverse the array. With the present system, this latter process is accomplished at a rate of 1 linear ft of array/minute.

SECTION II

INTRODUCTION

In our previous work, we identified candidate cost-effective processes for large-scale silicon solar cell and panel production, brought those processes needing development to a state of technological readiness, and verified such processes by experimental production of solar cells and panels. To obtain a selling price of less than $500/kW requires that these processes be assembled to form a manufacturing sequence possessing both material and interprocess compatibility with the capability of operating at high throughput and yield.

In the present program, the three manufacturing sequences shown in Figs. 1 and 2 are under investigation to evaluate their overall cost/performance effectiveness. This evaluation is being performed by studying the production flow and the performance of each sequence; it involves the processing and testing of 1500 solar cells, which are then used in the fabrication of solar panels. Two major objectives of this work are to test the performance of these sequences when low-cost forms of silicon are used for starting material and to assess the internal compatibility between process steps. The reason for this approach is two-fold in that low-cost processes have been used successfully with high-quality Czochralski silicon wafers and on the other hand, most low-cost silicon forms have not been subjected to these specific low-cost sequences. Two forms of silicon being used in the present program are 3-in.-diameter "solar-grade"* wafers and dendritic web** silicon.

Although almost all of the cells fabricated to date have been made with "solar-grade" wafers due to delays in the delivery of web, both material- and process-related compatibility problems have been experienced. The specific processes affected are noted in Figs. 1 and 2 and are discussed in detail in Section III.

*"Solar-grade" silicon is a product of the Monsanto Corp., St. Louis, MO. These are 3-in.-diameter n- and p-type, 1/2 to 2 Ω-cm, round silicon wafers, received in a "saw-cut" form.

**Purchased from Westinghouse Research and Development Center, Pittsburgh, PA.

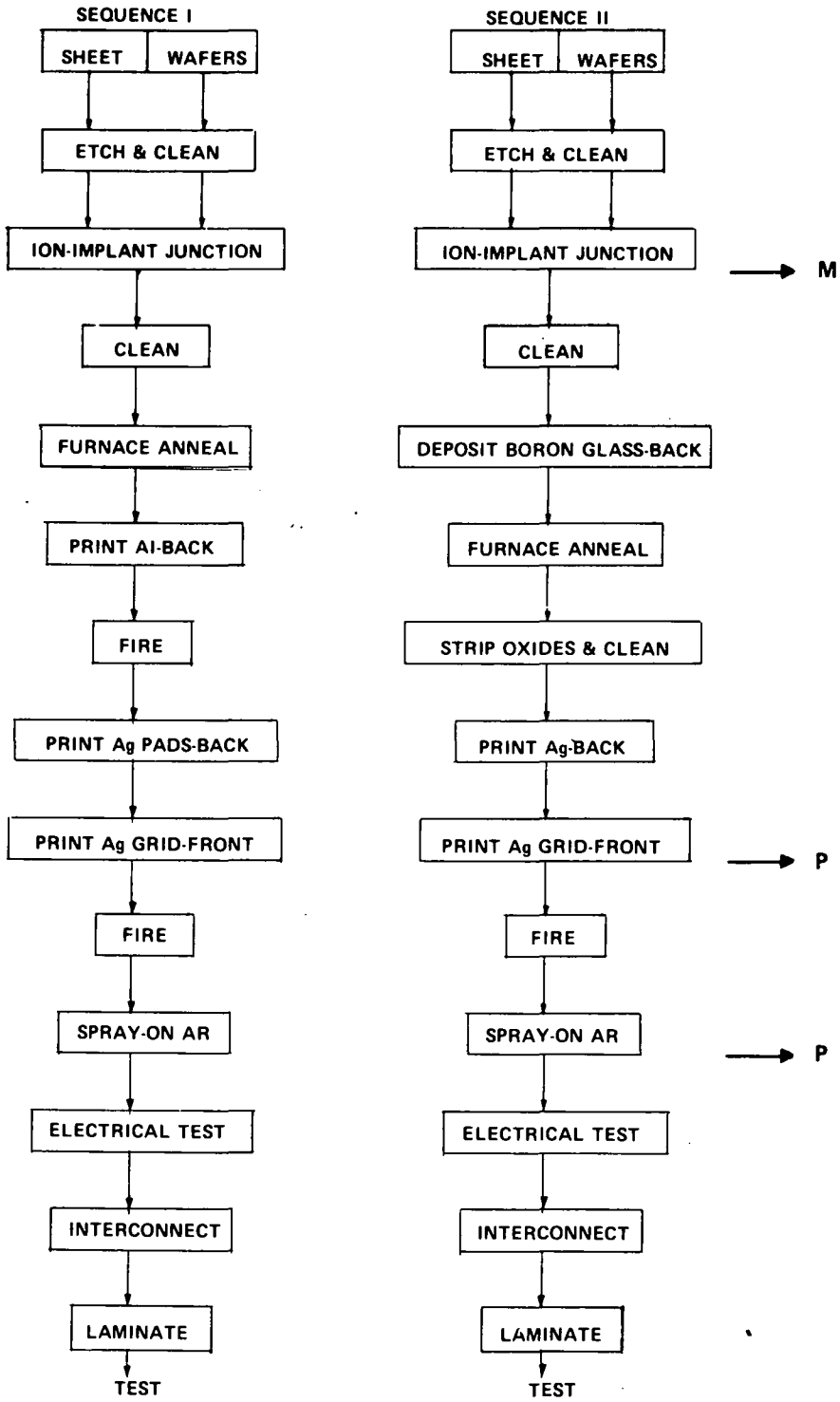

Figure 1. Manufacturing sequences I and II. Arrows indicate steps at which either material (M) or process (P) compatibility problems were experienced.

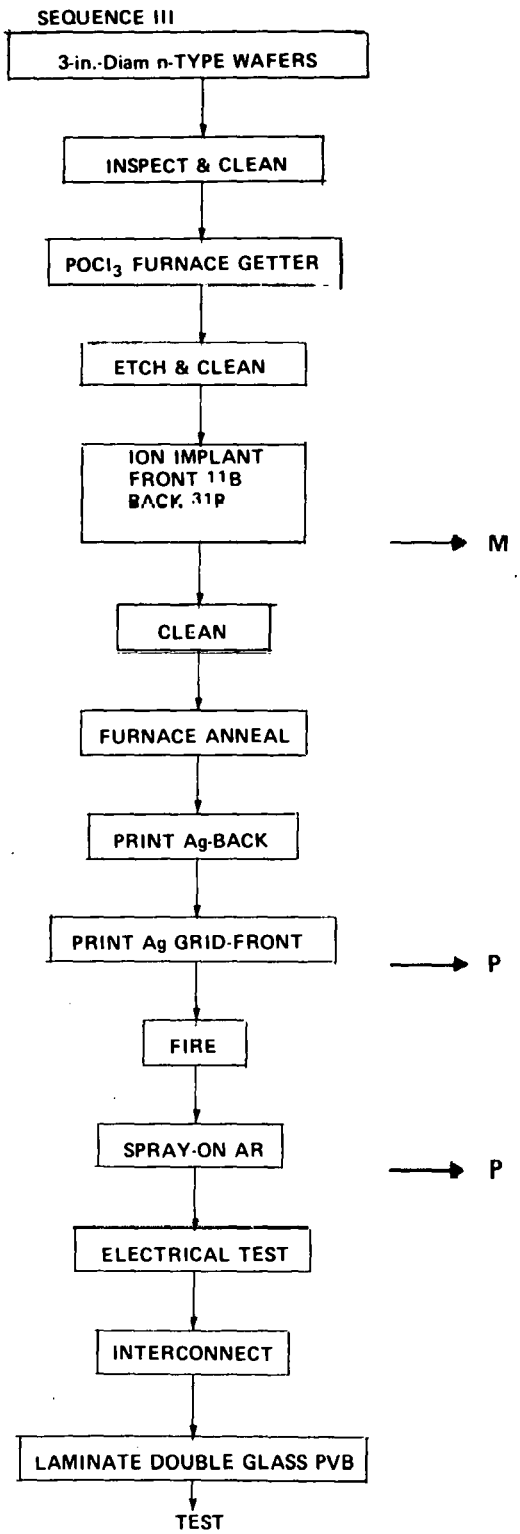

Figure 2. Manufacturing sequence III. Arrows indicate steps at which either material (M) or process (P) compatibility problems were experienced.

SECTION III

MATERIAL AND PROCESS COMPATIBILITY PROBLEMS

As a result of the examination of the data accumulated in the fabrication of about 500 solar cells with "solar-grade" starting wafers used in each of the three manufacturing sequence categories, two problem areas have been identified relating to materials and process compatibility. First, we have found that previously determined optimum ion-implantation and furnace-anneal parameters must be modified to accommodate the "solar-grade" wafer as a starting material. Second, presently used screen-printed thick-film inks do not contact ion-implanted junction layers as well as layers formed by gaseous diffusion.

This problem, although partially eliminated by the addition of a dilute hydrofluoric (HF) acid rinse, manifests itself again after the spray-on AR coating process.

A. MATERIAL-RELATED PROBLEMS

Some details of the problems related to the use of etched "solar-grade" wafers in conjunction with the ion-implantation and anneal parameters for sequence I processing were given in Quarterly Report No. 6 [1]. Data illustrating this problem are summarized in Figs. 3 and 4. These data show that unacceptably high values and a wide range of sheet resistances result when the ^{31}P implant dose is 2×10^{15} cm^{-2} and the high-temperature portion of the furnace anneal is 850°C. Furthermore, when screen-printed contacts are formed on such layers, the resultant solar cells exhibit low values of fill-factor with a decline following the increasing sheet resistances as shown in Fig. 4. Examination of the cell characteristics shows that the low fill-factors are caused almost entirely by excess series resistance.

To investigate this problem further, an experimental test matrix was formed involving a combination of starting wafers, implant and anneal conditions, and the addition of junction layers formed by $POCl_3$ diffusion. The conditions for this experiment are shown in Table 1 along with the post-anneal values of

1. R. V. D'Aiello, Automated Array Assembly, Phase II, Quarterly Report No. 6, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-79/6, June 1979.

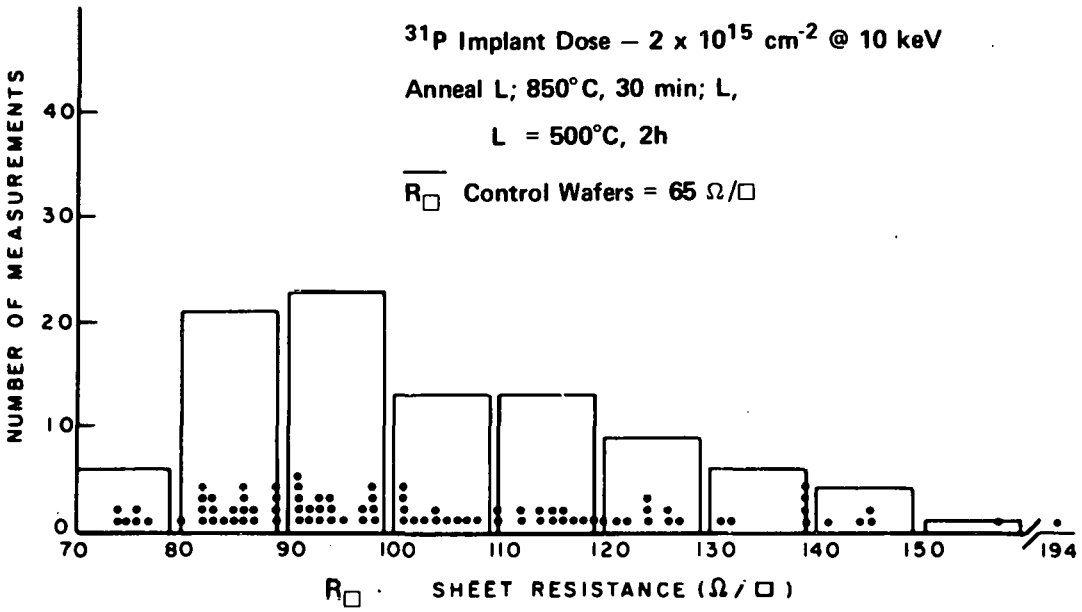

Figure 3. Distribution of measured sheet resistances for three lots of solar-grade wafers. Implant and anneal conditions given in the inset.

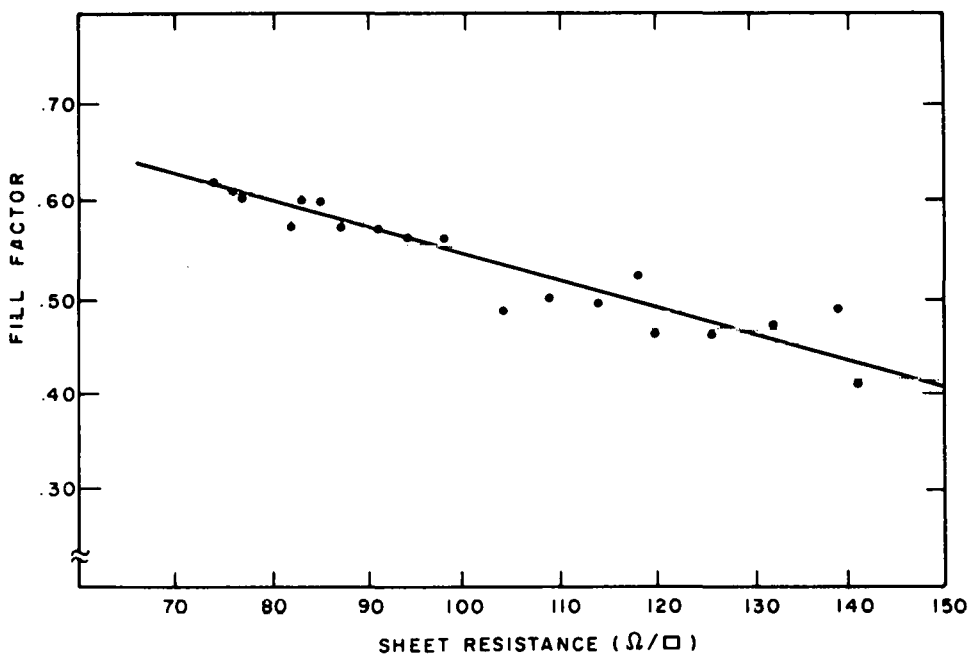

Figure 4. Measured fill factor as a function of sheet resistance for solar cells fabricated from wafer lots shown in Fig. 3.

TABLE 1. TEST-MATRIX CONDITIONS

Lot, Material	Wafer Surface	Wafer Resistivity (Ω-cm)	^{31}P Implant Dose (cm^{-2})	Furnace Anneal	Sheet Resistance (Ω/□)	Screen-Print Ink Front	Screen-Print Ink Back
910P, SG*	Etched	2	$2x10^{15}$	L** 950°C 30 min L	52	TFS 3347	Al/Ag
107P, SG	Etched	2	$4x10^{15}$	L 850°C 30 min L	58		
106P, SG	Etched	2	$4x10^{15}$	L 950°C 30 min L	34		
121, Wacker CZ	Polished	1.5	$4x10^{15}$	L 950°C 30 min L	25		
123, Monsanto CZ	Etched	12	$4x10^{15}$	L 950°C 30 min L	27		
115m, Monsanto CZ	Etched	1.5	$POCl_3$ diffusion	850°C 60 min -	30		

*SG = Solar Grade
** L = 500°C, 2 h

average sheet resistance for each lot of 25 wafers. Solar cells were completed for each lot by screen-printing and firing with the ink combinations given in the last two columns of Table 1.

The average AM-1 solar-cell parameters measured for each lot are listed in Table 2. From these results, the following conclusions can be drawn:

(1) For ^{31}P ion-implanted junctions, the 950°C anneal and 4 x 10^{15} cm^{-2} dose are preferred for best cell parameters.

(2) $POCl_3$ diffused-junctions yield the best overall solar-cell performance.

(3) Under the same implant and anneal conditions, the resultant sheet resistance is higher for solar-grade wafers than for polished or etched CZ wafers.

(4) Even when the sheet-resistance values obtained with ion-implanted solar-grade wafers approach those for $POCl_3$ diffused junctions, the solar-cell parameters (V_{oc} and FF) are not equally as good.

TABLE 2. RESULTS OF TEST MATRIX

Lot	$R_\square$ ($\Omega/\square$)	$\overline{J_{sc}}$ (mA/cm^2)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$	$\overline{\eta}$* (%)
910P	52	20.5	560	0.700	8.0
107P	58	21.7	552	0.659	7.9
106P	34	20.7	557	0.710	8.2
121	25	19.3	553	0.743	7.9
123	27	19.6	518	0.698	7.1
115m	30	20.7	580	0.761	9.2

* No AR coating.

Based on these results, we increased the ^{31}P dose to 4 x 10^{15} cm^{-2} and changed the high temperature anneal to 950°C, 30 min for all subsequent process lots in sequences I and II. This is a compromise in favor of forming lower resistance screen-printed contacts to the n^+ layer since higher short-circuit current is expected, and does result (see lot 107P in Table 2) from a lower temperature anneal. In addition to a possible reduction in cell efficiency which implies greater cost per watt, the requirement for increased implant dose would require implanters of higher beam current or greater capacity to attain the same throughput.

B. PROCESS COMPATIBILITY PROBLEMS

When the implant and anneal parameters indicated above were made, process compatibility problems were noted which are intimately related to the screen-printed metallization process. First, we have consistently observed that screen-printed, thick-film inks do not contact ion-implanted junctions as well as diffused-junction layers. Previously [2] we had demonstrated screen-printed contacts and determined suitable "in-house" and commercial ink formulations and firing techniques on diffused-junction solar cells. We now find that when identical techniques are applied to ion-implanted junctions, such excessive contact resistance is experienced that an additional process step consisting of dilute hydrofluoric acid (HF) rinsing is required after firing, and that even with the addition of this step, cell fill-factors seldom exceed 70%. In contrast, in most cases, the performance of $POCl_3$ diffused-junction solar cells is good immediately after the screen-printed inks are fired. This situation is illustrated in Figs. 5 and 6 for both ion-implanted and diffused-junction cells.

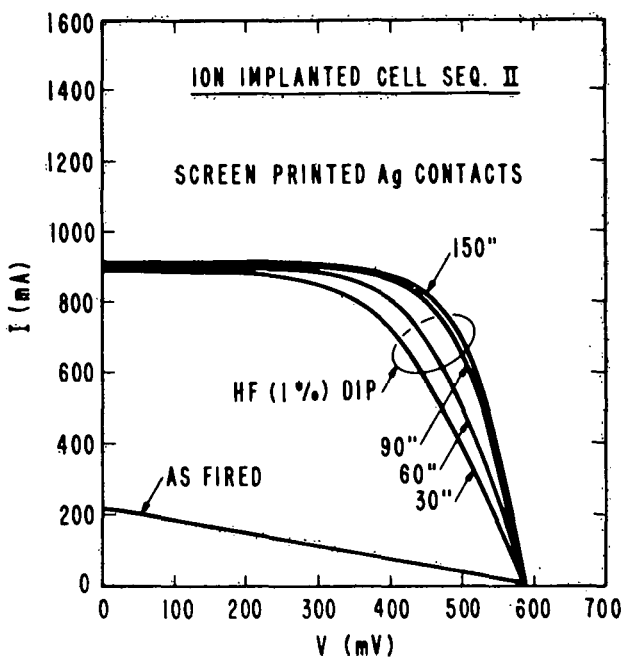

Figure 5. Performance of sequence II ion-implanted cells.

2. R. V. D'Aiello, Automated Array Assembly, Phase II, Interim Report, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-79/1, January 1979.

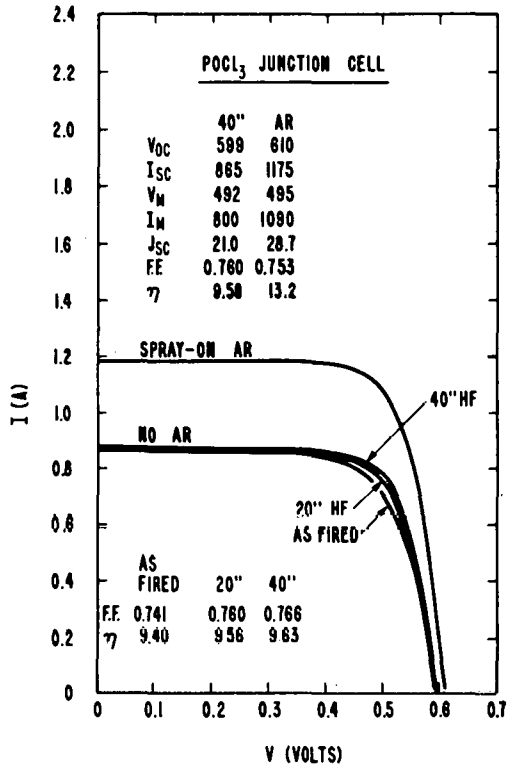

Figure 6. Performance of $POCl_3$-junction cells.

For the diffused-junction cells, a small improvement in fill-factor does result from HF dipping for 30 s. Beyond 30 s very little increase in fill-factor was noted.

The situation shown in Fig. 5 is typical of the ion-implanted cells in that the fill-factor is very low ($\lesssim$30%) after firing, with a large increase in fill-factor resulting from the HF dipping process. The improvement in fill-factor is largest for initial dipping times of from 10 to 30 s; however, in some cases continued increases in fill-factor were measured for dipping times up to 3 min. Dipping for times in excess of 3 min generally results in staining of the silicon surface and ultimately in peeling of the printed metallization.

Because of this, optimum dipping times had to be experimentally determined for each of the ion-implanted junction cases represented by the three sequences under study. The optimum conditions were found to be different for the three sequences, with the $p^+/n/n^+$ cells of sequence III requiring the least amount of dipping (30 s) and sequences II cells the longest (150 s).

While HF dipping appears to be a panacea, there are a number of serious problems associated with its use. First, it becomes an extra required process step, adding cost to the manufacturing sequence. It is a process requiring the use of acid with the attendant safety and waste-removal problems. Also, at

this time, the mechanism by which the HF solution improves the contact between the screen-printed metal film and the silicon is not known, thereby making control of this process difficult. Furthermore, as will be described below, while the HF dipping improves the fill-factor in all cases, it sometimes leaves the metal-film-silicon interface susceptible to serious degradation causing incompatibility with the next process step of spray-on AR coating.

In preparation for the spray-on AR coating process, cells are batch-dipped, 25 at a time, in a 2% solution of $HF:H_2O$ (60 ml:3000 ml), thoroughly rinsed in bubbling DI water, and dryed. For purposes of comparison, the AM-1 characteristics of all cells are measured before and after AR coating. The spray-on AR coating process described previously [1,2] was used for all results reported here.

From previous data and verification tests, it is expected that application of the AR coating will result in an increase in the short-circuit current and cell efficiency of about 35% with little effect on other cell parameters. These results were obtained on cells with evaporated Ti/Ag metallization or cells with screen-printed thick-film metal but generally not dipped in HF solutions. When ion-implanted cells which require HF dipping are spray-coated, sporadic instabilities and degradation of the cell fill-factor are observed. This effect is illustrated in Fig. 7 which shows that while the short-circuit current is increased by 33%, the fill-factor is substantially reduced resulting in a net decrease in cell efficiency. In addition, some instability is also present in the AR coated case as shown by the two I-V traces in Fig. 7 taken about 15 s apart. The sporadic nature of the degradation in fill-factor within a cell lot is illustrated in Tables 3 and 4 which show the measured cell characteristics for lot 147 (sequence II processing) before and after spray AR coating. Extreme cases in which an entire lot was degraded, and other cases in which no cells were adversely affected by the spray-on AR process have also been observed.

The sensitivity of such cells to evaporated AR coating was tested by a random selection of eight cells from four lots and by evaporating a ZrO_2 coating of nominal 725-Å thickness after screen-printing and HF dipping. The results of this test, given in Table 5 along with selected data from these lots of cells processed in the ordinary way, show that the degradation is not induced by an evaporated AR coating.

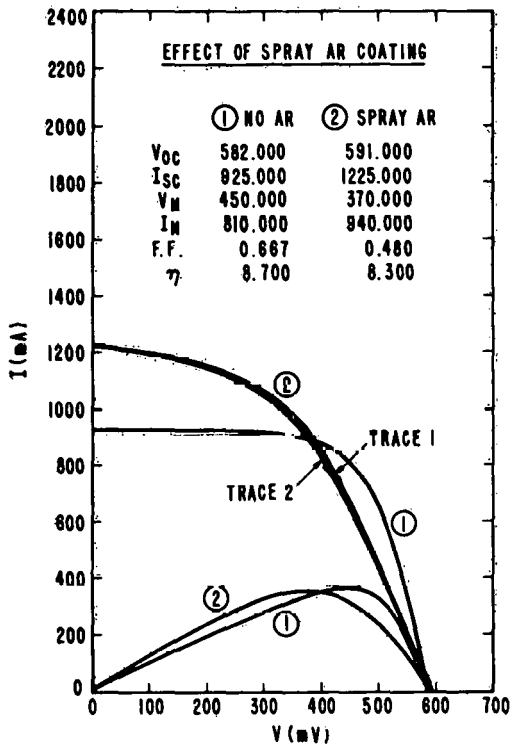

Figure 7. Effect of spray AR coating on performance of ion-implanted cells.

It is also important to note that this effect does not occur with solar cells made with $POCl_3$-diffused junction even when such cells are HF dipped. This is illustrated in Fig. 8.

TABLE 3. MEASURED CELL PARAMETERS PRIOR TO COATING FOR LOT 147

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D2NS147001	.575	979.	9.01	.671	.067	39.41	859.	.441	.090	24.4
D2NS147002	.570	982.	8.16	.611	.476	12.84	786.	.436	.081	24.4
D2NS147003	.579	999.	9.03	.655	.930	20.99	851.	.446	.090	24.6
D2NS147004	.579	1,025.	8.94	.631	.561	23.07	861.	.436	.089	24.5
D2NS147005	.583	1,003.	9.04	.649	.652	17.12	853.	.445	.090	24.7
D2NS147006	.573	1,009.	8.42	.611	.485	40.47	822.	.430	.084	24.9
D2NS147007	.577	1,008.	8.79	.634	.643	57.25	827.	.447	.088	24.9
D2NS147008	.578	1,004.	8.97	.649	.674	53.45	857.	.440	.090	24.9
D2NS147009	.583	1,023.	9.38	.660	.054	20.76	892.	.442	.094	25.0
D2NS147010	.582	1,021.	9.05	.639	.049	82.74	858.	.443	.090	24.9
D2NS147011	.569	1,005.	8.13	.597	.217	29.54	794.	.430	.081	25.1
D2NS147012	.556	993.	6.99	.532	.356	20.93	718.	.409	.070	25.0
D2NS147013	.570	1,000.	8.15	.600	.934	260.00	809.	.423	.081	25.1
D2NS147014	.577	1,017.	8.83	.630	.596	52.83	842.	.440	.088	24.5
D2NS147015	.576	1,013.	8.53	.614	.391	341.40	815.	.440	.085	24.7
D2NS147016	.573	1,012.	8.36	.606	.176	162.10	810.	.434	.084	24.9
D2NS147017	.574	997.	8.19	.601	.291	11.59	818.	.421	.082	24.9
D2NS147018	.569	994.	7.85	.583	.279	459.50	762.	.433	.079	25.1
D2NS147019	.580	1,019.	9.11	.648	.243	9.41	874.	.438	.091	25.0
D2NS147020	.568	1,014.	7.98	.581	.544	13.58	801.	.419	.080	25.0
D2NS147021	.576	1,000.	8.73	.637		1,201.00	846.	.433	.087	25.1
D2NS147022	.575	1,017.	8.95	.643	.210	60.90	868.	.433	.090	25.1
D2NS147023	.575	1,000.	8.79	.642	.709	51.01	832.	.444	.088	25.1
D2NS147024	.579	1,027.	9.05	.640	.569	13.01	855.	.445	.091	25.3
D2NS147025	.580	1,004.	9.00	.650	.458	22.80	855.	.442	.090	25.2

TABLE 4. MEASURED CELL PARAMETERS AFTER SPRAY-ON AR COATING FOR LOT 147

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D2NS147001	.581	1,273.	10.73	.610	.219	34.89	1,105.	.408	.107	25.0
D2NS147002	.579	1,274.	10.28	.586	.137	13.15	1,031.	.419	.103	25.1
D2NS147003	.586	1,301.	10.86	.599	.180	45.67	1,104.	.413	.109	25.2
D2NS147004	.583	1,278.	8.07	.456	.191	2.25	893.	.379	.081	25.4
D2NS147005	.587	1,285.	8.53	.476	.365	15.37	883.	.406	.085	25.2
D2NS147006	.582	1,299.	10.57	.577	.214	6.78	1,091.	.399	.104	25.4
D2NS147007	.585	1,300.	10.77	.596	.981	671.10	1,082.	.418	.108	25.4
D2NS147008	.585	1,288.	9.69	.542	.241	146.90	1,005.	.405	.097	25.4
D2NS147009	.584	1,126.	4.41	.283	.377	.35	572.	.324	.044	25.5
D2NS147010	.587	1,314.	9.60	.524	.500	517.90	1,006.	.401	.096	25.5
D2NS147011	.579	1,303.	10.09	.585	.277	31.36	1,092.	.404	.105	25.5
D2NS147012	.566	1,288.	9.05	.522	.270	29.29	953.	.395	.091	25.4
D2NS147013	.580	1,287.	10.56	.585	.062	9.30	1,057.	.412	.104	25.6
D2NS147014	.583	1,292.	7.94	.444	.281	6.36	872.	.383	.080	25.6
D2NS147015	.583	1,296.	8.30	.446	.276	67.83	850.	.391	.080	25.5
D2NS147016	.582	1,301.	10.26	.571	.015	30.88	1,085.	.397	.103	25.6
D2NS147017	.583	1,266.	10.42	.595	.506	7.67	1,041.	.421	.104	25.6
D2NS147018	.579	1,286.	9.51	.543	.734	58.95	1,037.	.389	.096	25.6
D2NS147019	.585	1,303.	9.24	.511	.503	199.90	966.	.402	.093	25.7
D2NS147020	.574	1,294.	7.30	.414	.622	92.06	842.	.364	.073	25.8
D2NS147021	.583	1,293.	10.59	.596	.166	7.96	1,072.	.419	.107	25.6
D2NS147022	.582	1,289.	8.15	.458	.603	174.60	964.	.355	.082	25.8
D2NS147023	.583	1,286.	8.44	.475	.062	54.80	1,020.	.347	.085	25.7
D2NS147024	.583	1,303.	9.07	.503	.995	9.14	995.	.383	.091	25.8
D2NS147025	.584	1,251.	6.64	.383	.605	21.30	822.	.339	.067	25.8

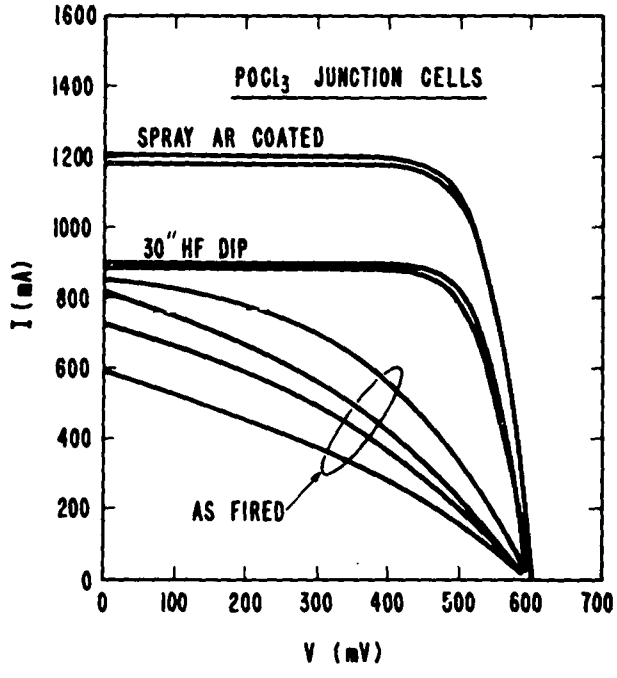

Figure 8. Effect of spray AR coating on performance of $POCl_3$-junction cells.

TABLE 5. COMPARISON OF ZrO_2 EVAPORATED AR WITH SPRAY AR (SCREEN-PRINTED CELLS)

Lot, Cell No.	I_{sc_1} (mA)	I_{sc_2} (mA)	$\Gamma = \frac{J_{sc_2}}{I_{sc_1}}$	η_1 (%)	η_2 (%)	FF_1	FF_2	F_2/F_1	Comment
994, 14	965	1312	1.35	8.16	10.44	0.603	0.559	0.927	Evaporated ZrO_2
939, 1	942	1315	1.39	9.50	13.16	0.716	0.700	0.978	Evaporated ZrO_2
943, 5	995	1375	1.38	9.87	13.45	0.702	0.679	0.966	Evaporated ZrO_2
941 25	990	1333	1.35	9.82	12.86	0.700	0.668	0.954	Evaporated ZrO_2
939, 2	935	1300	1.39	9.58	13.08	0.727	0.703	0.967	Evaporated ZrO_2
944, 13	935	1325	1.42	9.00	12.50	0.703	0.679	0.966	Evaporated ZrO_2
941, 10	1005	1368	1.36	9.73	12.78	0.688	0.653	0.949	Evaporated ZrO_2
943, 6	990	1340	1.35	9.80	13.0	0.700	0.673	0.961	Evaporated ZrO_2
941, 23	972	1318	1.36	9.4	11.9	0.696	0.644	0.925	Spray AR, best in lot
941, 14	984	1286	1.31	9.6	6.5	0.696	0.360	0.517	Spray AR, typical degraded cell
944, 23	992	1308	1.32	10.0	12.3	0.712	0.659	0.926	Spray AR, best in lot
944, 19	959	1162	1.21	9.8	5.9	0.697	0.373	0.535	Spray AR, typical degraded cell
943, 3	992	1342	1.35	9.7	12.8	0.699	0.673	0.963	Spray AR, best in lot
943, 14	991	1325	1.34	9.8	8.0	0.701	0.425	0.606	Spray AR, typical degraded cell

SECTION IV

PROGRESS IN SOLAR-CELL AND PANEL FABRICATION

A. SOLAR-CELL FABRICATION - SEQUENCES I, II, AND III

During this quarter, solar-cell fabrication from solar-grade wafers was completed. This brings the total number of cells fabricated since January 1979 to 1500, with about 500 in each of the three sequence categories. AM-1 illuminated electrical characteristics for all cells have been measured and stored in our data bank. These data have been examined, but because of the compatibility problems described in Section III, it is difficult to make quantitative statistical comparisons of the completed cell performance. However, since all cells were subjected to HF dipping in such a manner as to optimize their performance, comparisons can be made prior to AR coating, and estimates of the completed-cell parameters made on the basis of the known effect of the AR coating in the absence of compatibility problems.

The composite average values of the AM-1 parameters measured prior to AR coating for all cells in sequences I, II, and III are given in Table 6. The estimated values listed with AR coating were obtained by assuming a 31% increase in short-circuit current, a logarithmic increase in open-circuit voltage, i.e., $V_{oc_{AR}} = V_{oc} + 0.026 \ln(1.31)$, and a decrease in fill-factor due to series resistance. It was noted in Section III that for some processed cell lots, no apparent degradation was noted due to the spray-on AR coating process. The measured parameters of the best performing cells from these lots are also listed in Table 6 to indicate peak values obtainable with these processes. In addition, in the course of our work, 100 cells were fabricated with junctions formed by $POCl_3$ diffusion, and the average parameters for these cells are also listed in Table 6 for comparative purposes.

The relative ranking in performance of the cells made by the three manufacturing sequences and by the $POCl_3$ process warrants some comment.

From among the three sequences, clearly the sequence III process yielded the best cells with measured AM-1 efficiencies reaching 13% even though the fill-factors were consistently below 70%. These solar cells are made using n-type solar-grade starting silicon with an initial $POCl_3$ "gettering" diffusion step; after etching they are implanted with boron and phosphorus in such a manner that a $p^+/n/n^+$ structure results. The importance of the $POCl_3$ gettering

TABLE 6. COMPARISON OF AVERAGE SOLAR-CELL PARAMETERS FOR SEQUENCES I, II, AND III

Manufacturing Sequence	Structure	Measured - No AR				Estimated - With AR				Best Measured With AR			
		$\overline{I_{sc}}$ (mA)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$ -	$\bar{\eta}^*$ (%)	$\overline{I_{sc}}$ (mA)	$\overline{V_{oc}}$ (mV)	$\overline{FF}$ -	$\bar{\eta}$ (%)	I_{sc} (mA)	V_{oc} (mV)	FF -	η (%)
I	$n^+/p/p^+$	870	557	0.701	8.1	1140	567	0.673	10.4	1146	571	0.685	10.7
II	$n^+/p/p^+$	970	574	0.675	8.9	1280	584	0.650	11.6	1268	578	0.680	11.9
III	$p^+/n/n^+$	1020	585	0.686	9.7	1336	595	0.660	12.5	1368	597	0.670	13.0
$POCl_3$	$n^-/p/p^+$	867	584	0.755	9.3	{1177	594	0.748	12.7}**		1205	610	0.761

*Cell area = 42 cm^2
**Measured values

step was assessed by omitting that step for several lots, then merging these lots with others for common subsequent processing. The results for one such lot and a typical sequence III lot are given in Tables 7 and 8. The benefit from the gettering shows up as a net increase of 15% in average cell efficiency due mostly to a +9.6% increase in short-circuit current.

That the inclusion of the $POCl_3$ gettering step is cost-effective can be seen in Tables 9 and 10 which show a net savings of \$0.133/W resulting from the increased efficiency.

In the processing of sequence III cells, problems similar to those in sequences I and II were experienced. The ^{11}B implant dose for the junction layer had to be doubled to 4×10^{15} cm^{-2} in order to obtain consistent sheet resistance values of $\sim$50 $\Omega/\square$. Even at this dose level, problems were encountered in obtaining low-resistance screen-printed contacts, and dilute HF rinsing for 30 to 60 s was required to obtain marginally acceptable fill-factors approaching 70%. In addition, instability and degradation of the fill-factors after spray-on AR coating were noted about as frequently as with sequence I and II processing.

The importance of back-surface-field (BSF) effects and gettering can also be seen in a comparison of the performance of sequence I and II solar cells. The major difference is in the processing associated with the doping or contacting of the back surface of the cells. In sequence II, a boron-glass deposition [2] and high-temperature drive-in are used both to diffuse boron into the back of the wafer and to anneal the phosphorus implant in the front-junction layer. We have shown in previous work [3] that the boron-glass, high-temperature anneal performs an effective gettering treatment resulting in an increase in diffusion length or preservation of long diffusion length in the starting silicon. In sequence I, an aluminum alloying process [3] is used to form the p^+ BSF and back contact, and no intentional gettering processes are employed.

A comparison of the performance data for sequence I and II solar cells given in Table 6 shows that the average cell efficiency for sequence II cells is higher than that of the cells produced by sequence I. Furthermore, the lower fill-factor of sequence II cells is more than compensated for by considerably higher short-circuit current and open-circuit voltage, factors which are known to be affected by gettering and BSF effects.

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3. R. V. D'Aiello, Automated Array Assembly, Phase II, Quarterly Report No. 5, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-79/1, March 1979.

TABLE 7. SEQUENCE III CELLS

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TABLE TO CHECK CALCULATOR INPUT PRIOR TO COATING FOR LOT NUMBER 983

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D3NS983001	.576	968.	9.26	.699	.767	285.70	850.	.458	.093	25.7
D3NS983002	.576	962.	9.17	.697	.828	690.30	863.	.447	.092	25.7
D3NS983003	.566	935.	8.72	.695	.872	2,814.00	803.	.453	.087	25.6
D3NS983004	.591	1,042.	9.96	.682	1.885	29.81	888.	.471	.100	25.8
D3NS983005	.583	1,015.	9.62	.685	1.676	127.60	876.	.461	.097	25.9
D3NS983006	.592	1,035.	9.23	.635	1.724	25.35	867.	.447	.093	25.9
D3NS983007	.590	1,040.	10.06	.692	1.464	1,759.00	925.	.457	.101	26.1
D3NS983008	.592	1,055.	10.16	.686	1.593	167.20	919.	.464	.102	26.1
D3NS983009	.591	1,037.	10.06	.692	1.318	22.37	905.	.467	.101	26.1
D3NS983010	.592	1,054.	10.11	.684	1.257	1,550.00	906.	.469	.102	26.1
D3NS983011	.586	1,045.	9.77	.674	.694	174.90	897.	.458	.098	26.2
D3NS983012	.590	1,042.	10.22	.701	1.335	131.20	911.	.471	.103	26.2
D3NS983013	.591	1,042.	10.10	.692	.339	99.65	925.	.459	.101	26.3
D3NS983014	.584	1,044.	9.96	.689	1.079	26.67	905.	.462	.100	26.4
D3NS983015	.567	960.	8.61	.683	.744	813.70	810.	.447	.087	26.4
D3NS983016	.586	1,083.	10.23	.631	.534	1,802.00	918.	.468	.103	26.4
D3NS983017	.577	1,044.	9.76	.684	1.178	895.40	912.	.449	.098	26.3
D3NS983018	.590	1,047.	10.03	.636	.281	1,435.00	907.	.464	.101	26.9
D3NS983019	.586	1,041.	9.97	.690	1.929	607.90	904.	.463	.100	26.4
D3NS983020	.588	1,034.	9.93	.694	.137	176.80	903.	.464	.100	26.4
D3NS983021	.591	1,067.	10.06	.687	2.179	364.70	913.	.463	.101	26.4
D3NS983022	.592	1,049.	9.89	.672	2.322	3,418.00	894.	.465	.099	26.4
D3NS983023	.589	1,054.	10.14	.696	1.697	17.44	919.	.463	.102	26.4

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AVERAGE CALCULATOR INPUT VALUES PRIOR TO COATING FOR LOT NUMBER 983

AVE OPEN CIR VOLT	AVE CELL CURRENT	AVE MAX POWER	AVE FILL FACTOR	AVE SER RESIS	AVE SHUNT RESIS	AVE PMAX CURRENT	AVE PMAX VOLTAGE	AVE EFF	AVE BASE TEMP
.585	1,028.	9.79	.686	1.212	758.03	892.	.466	.098	26.2

TABLE 8. SEQUENCE III CELLS PROCESSED WITHOUT $POCl_3$ GETTERING

PAGE 1

TABLE TO CHECK CALCULATOR INPUT PRIOR TO COATING FOR LOT NUMBER 114

CELL NUM	OPEN CIR VOLT	CELL CURRENT	MAX POWER	FILL FACT	SER RESIS	SHUNT RESIS	PMAX CURRENT	PMAX VOLT	EFF	BASE TEMP
D3NS114001	.571	942.	8.37	.661	1.065	28.22	828.	.424	.085	27.2
D3NS114002	.569	920.	8.50	.688	.372	126.60	804.	.444	.086	27.1
D3NS114003	.570	929.	8.64	.693	.619	99.45	827.	.439	.087	27.2
D3NS114004	.575	939.	7.70	.606	.719	41.24	773.	.418	.078	27.3
D3NS114005	.575	947.	8.31	.648	.481	128.10	832.	.419	.084	27.3
D3NS114006	.572	953.	8.66	.674	.902	142.50	835.	.436	.088	27.4
D3NS114007	.569	936.	8.56	.633	.160	18.99	830.	.433	.086	27.4
D3NS114008	.570	946.	8.76	.689	.513	276.80	831.	.443	.089	27.4
D3NS114009	.576	944.	8.01	.627	.852	150.40	779.	.432	.081	27.6
D3NS114010	.575	938.	8.01	.632	.405	29.02	786.	.428	.081	27.5
D3NS114011	.572	944.	8.69	.684	.212	264.60	820.	.445	.088	27.5
D3NS114012	.570	940.	8.72	.692	.307	451.70	832.	.440	.088	27.6
D3NS114013	.569	937.	8.59	.686	.871	13.70	828.	.436	.087	27.7
D3NS114014	.573	938.	8.14	.645	.032	311.40	783.	.437	.082	27.8
D3NS114015	.572	949.	8.26	.647	.041	1,136.00	842.	.412	.084	27.7
D3NS114016	.568	926.	8.38	.678	1.204	13.60	819.	.430	.085	27.7
D3NS114017	.568	928.	8.47	.682	1.323	302.80	840.	.423	.086	27.8
D3NS114018	.569	943.	8.66	.689	1.754	170.40	819.	.444	.088	27.7
D3NS114019	.572	938.	8.33	.661	.038	58.75	804.	.435	.084	27.7
D3NS114020	.572	932.	8.12	.648	.953	164.30	794.	.429	.082	27.8
D3NS114021	.570	933.	8.64	.691	.281	119.30	831.	.437	.087	27.7
D3NS114022	.569	935.	8.65	.690	.259	695.70	816.	.445	.088	27.6
D3NS114023	.571	940.	8.24	.654	1.113	438.70	806.	.430	.084	27.8
D3NS114024	.572	938.	8.20	.650	.549	28.66	793.	.434	.083	27.8

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AVERAGE CALCULATOR INPUT VALUES PRIOR TO COATING FOR LOT NUMBER 114

AVE OPEN CIR VOLT	AVE CELL CURRENT	AVE MAX POWER	AVE FILL FACTOR	AVE SER RESIS	AVE SHUNT RESIS	AVE PMAX CURRENT	AVE PMAX VOLTAGE	AVE EFF	AVE BASE TEMP
.571	938.	8.40	.667	.626	217.11	815.	.433	.085	27.6

TABLE 9. COST ANALYSIS WITH $POCl_3$ GETTERING STEP, 13% EFFICIENCY CELL

COST ANALYSIS:SEQUENCE #3(B):3" WAFER#13% CELL#30MW#AG FRONT#AG BACK. 10/19/79 16:39:59 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.621 WATTS PER SOLAR CELL AND 7.8 CM (3") DIAMETER WAFER
CELL THICKNESS: 10.0 MILS. CELL ETCH LOSS: 3.0 MILS. CELL KERF LOSS:10.0 MILS.

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	P. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.5%	MEGASONIC CLEANING	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.1	0.007	0.4
2	99.0%	POCL3 DEPOSITION AND DIFFUSION	(B)	0.0	0.003	0.015	0.004	0.003	0.005	0.030	0.0	0.030	2.4	0.023	1.4
3	95.0%	SODIUM HYDROXIDE ETCH:3 MILS	(A)	0.0	0.055	0.001	0.008	0.001	0.001	0.065	0.0	0.066	5.2	0.006	0.4
4	99.5%	MEGASONIC CLEANING #2	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.1	0.007	0.4
5	99.0%	ION IMPLANTATION:B,2.E+15,10 KEV	(B)	0.0	0.062	0.027	0.057	0.090	0.107	0.344	0.0	0.344	27.2	0.750	43.5
6	95.0%	ION IMPLANTATION:P,2.E+15,30 KEV	(B)	0.0	0.061	0.027	0.056	0.088	0.105	0.335	0.0	0.336	26.6	0.733	42.5
7	99.5%	MEGASONIC CLEANING #3	(B)	0.0	0.006	0.003	0.002	0.001	0.001	0.012	0.0	0.012	0.9	0.005	0.3
8	98.0%	900C. DEG. DIFFUSION:1/2 HR.	(B)	0.0	0.011	0.003	0.003	0.002	0.003	0.021	0.0	0.021	1.7	0.013	0.7
9	99.5%	MEGASONIC CLEANING #4	(B)	0.0	0.006	0.003	0.002	0.001	0.001	0.012	0.0	0.012	0.9	0.005	0.3
10	99.0%	POST DIFFUSION INSPECTION:10%	(B)	0.0	0.000	0.000	0.000	0.001	0.001	0.002	0.0	0.002	0.2	0.005	0.3
11	98.0%	THICK AG METAL:33% BACK & DRY	(B)	0.053	0.006	0.005	0.007	0.003	0.003	0.078	0.0	0.078	6.2	0.024	1.4
12	98.0%	THICK AG METAL:9% FRONT & FIRE	(B)	0.025	0.006	0.007	0.008	0.004	0.005	0.055	0.0	0.055	4.3	0.035	2.0
13	99.0%	HF DIP	(B)	0.0	0.002	0.001	0.000	0.000	0.000	0.004	0.0	0.004	0.3	0.003	0.2
14	99.0%	AR COATING:SPRAY-ON	(B)	0.001	0.006	0.000	0.003	0.001	0.002	0.013	0.0	0.013	1.0	0.012	0.7
15	90.0%	TEST	(B)	0.0	0.005	0.000	0.004	0.005	0.006	0.020	0.0	0.020	1.6	0.041	2.4
16	98.0%	REFLOW SOLDER INTERCONNECT 1	(B)	0.002	0.011	0.0	0.004	0.004	0.004	0.026	0.0	0.026	2.0	0.029	1.7
17	99.5%	GLASS/PVB/CELL ARRAY ASSEMBLY 1	(B)	0.168	0.028	0.0	0.005	0.003	0.004	0.208	0.0	0.208	16.5	0.027	1.6
18	100.0%	ARRAY MODULE PACKAGING	(A)	0.006	0.002	0.0	0.000	0.000	0.000	0.009	0.0	0.009	0.7	0.001	0.0
	72.4%	TOTALS		0.256	0.282	0.098	0.169	0.207	0.249	1.261	0.0	1.261	100.0	1.726	100.0
			%	20.33	22.38	7.77	13.37	16.42	19.73	100.00					

FACTORY FIRST COST,$/WATT: 0.24 DEPRECIATION,$/WATT: 0.01 INTEREST,$/WATT: 0.03
LAND COST,$/WATT: 0.0 INTEREST,$/WATT: 0.0

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 30.0 MEGAWATTS.
345 DAYS OF FACTORY PRODUCTION PER YEAR. 8.00 HOURS PER SHIFT. NO. OF SHIFTS PER DAY VARIES BY PROCESS STEP
EQUIPMENT NOT SHARED. FULL ALLOCATION TO PROCESS.

TABLE 10. COST ANALYSIS WITHOUT $POCl_3$ GETTERING STEP, 11.5% EFFICIENCY CELL

COST ANALYSIS:SEQUENCE #3(B):3" WAFER;11.5% CELL;30MW;AG FRONT;AG BACK. 10/19/79 16:39:59 PAGE 1

PROCESS COST OVERVIEW-$/WATT

ASSUMPTIONS: 0.549 WATTS PER SOLAR CELL AND 7.6 CM (3") DIAMETER WAFER
CELL THICKNESS: 10.0 MILS. CELL ETCH LOSS: 3.0 MILS. CELL KERF LOSS:10.0 MILS.

STEP	YIELD	PROCESS		MAT'L.	D. L.	EXP.	O. OH.	INT.	DEPR.	SUBTOT	SALVG.	TOTALS	%	INVEST	%
1	99.5%	MEGASONIC CLEANING	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.0	0.007	0.3
2	95.0%	SODIUM HYDROXIDE ETCH:3 MILS	(A)	0.0	0.061	0.001	0.009	0.001	0.001	0.072	0.0	0.072	5.2	0.007	0.4
3	99.5%	MEGASONIC CLEANING #2	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.0	0.007	0.3
4	99.0%	ION IMPLANTATION:B,2.E+15,10 KEV	(B)	0.0	0.069	0.030	0.063	0.109	0.119	0.382	0.0	0.382	27.4	0.833	43.0
5	99.0%	ION IMPLANTATION:P,2.E+15,30 KEV	(B)	0.0	0.069	0.030	0.063	0.100	0.119	0.382	0.0	0.382	27.4	0.833	43.0
6	99.5%	MEGASONIC CLEANING #3	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.0	0.007	0.3
7	98.0%	900C. DEG. DIFFUSION:1/2 HR.	(B)	0.0	0.011	0.003	0.003	0.002	0.003	0.021	0.0	0.021	1.5	0.013	0.7
8	99.5%	MEGASONIC CLEANING #4	(B)	0.0	0.007	0.003	0.002	0.001	0.001	0.014	0.0	0.014	1.0	0.007	0.3
9	99.0%	POST DIFFUSION INSPECTION:10%	(B)	0.0	0.001	0.000	0.001	0.001	0.001	0.003	0.0	0.003	0.2	0.005	0.3
10	98.0%	THICK AG METAL:33% BACK & DRY	(B)	0.060	0.007	0.006	0.009	0.003	0.004	0.088	0.0	0.088	6.3	0.027	1.4
11	98.0%	THICK AG METAL:9% FRONT & FIRE	(B)	0.028	0.007	0.008	0.009	0.005	0.006	0.063	0.0	0.063	4.5	0.040	2.1
12	99.0%	HF DIP	(B)	0.0	0.003	0.001	0.000	0.000	0.000	0.005	0.0	0.005	0.4	0.003	0.1
13	99.0%	AR COATING:SPRAY-ON	(B)	0.001	0.006	0.000	0.003	0.001	0.002	0.013	0.0	0.013	1.0	0.012	0.6
14	90.0%	TEST	(B)	0.0	0.006	0.000	0.005	0.006	0.007	0.023	0.0	0.023	1.6	0.047	2.4
15	98.0%	REFLOW SOLDER INTERCONNECT 1	(B)	0.002	0.015	0.0	0.005	0.005	0.006	0.033	0.0	0.033	2.4	0.040	2.1
16	99.5%	GLASS/PVB/CELL ARRAY ASSEMBLY 1	(B)	0.191	0.033	0.0	0.006	0.006	0.007	0.242	0.0	0.242	17.4	0.051	2.6
17	100.0%	ARRAY MODULE PACKAGING	(A)	0.007	0.002	0.0	0.000	0.000	0.000	0.010	0.0	0.010	0.7	0.001	0.0
	73.1%	TOTALS		0.290	0.314	0.093	0.185	0.233	0.278	1.394	0.0	1.394	100.0	1.939	100.0
			%	20.80	22.55	6.70	13.30	16.70	19.94	100.00					

FACTORY FIRST COST,$/WATT: 0.26 DEPRECIATION,$/WATT: 0.01 INTEREST,$/WATT: 0.03
LAND COST,$/WATT: 0.0 INTEREST,$/WATT: 0.0

NOTE: (A)=EXISTING TECHNOLOGY; (B)=NEAR FUTURE; (C)=FUTURE ANNUAL PRODUCTION: 30.0 MEGAWATTS.
345 DAYS OF FACTORY PRODUCTION PER YEAR. 8.00 HOURS PER SHIFT. NO. OF SHIFTS PER DAY VARIES BY PROCESS STEP
EQUIPMENT NOT SHARED. FULL ALLOCATION TO PROCESS.

Although the complete assessment of solar cells fabricated with junctions formed from $POCl_3$ diffusion is not part of the present contract objectives, it should be noted that excellent performance characteristics (see Table 6) resulted for the 100 cells made with such junctions. The reason for this, as noted in Section III, is the compatibility of this junction-formation process with the screen-printing and spray-on AR coating process. While a detailed understanding of the mechanisms involved is lacking at present, it remains as a clear experimental observation that the screen-printed thick-film inks form a lower resistance contact and result in higher fill-factors for $POCl_3$ junction layers than for any of the ion-implanted layers of sequences I, II, and III.

B. CELL INTERCONNECT AND PANEL ASSEMBLY

1. Overview

The construction and initial testing of a radiant-heat mass reflow soldering assembly (Fig. 9) was described in Quarterly Report No. 6 [1]. This machine is used to reflow the solder in the formation of the final interconnection between cells, cell strings, and bus bars in an assembled array in which copper tabs have previously been soldered to the solar cells. During this quarter, a complete cell-array layout and assembly process has been demonstrated. This included developing methods for screen-printing solder paste onto the cells, formation and solder-attachment of the tabs, array layout, transfer to the radiant-heat reflow assembly, and reflow soldering to form the complete interconnection of a 15x5 cell array.

2. Interconnect Technology

An approach has been devised to interconnect the solar cells to produce panel arrays. This new process reduces human handling of the cells, connects them economically and uniformly, and prevents solder lumps (which can cause cell breakage during lamination) at the connections.

Screen printing was selected for the application of solder paste front and back of the cell as shown in Fig. 10. There is no orientation of the pattern front to back; therefore, in the screening operation a method was devised to align solder paste application front to back. A lever mechanism was added to the screening subplate with a marking stylus, so that while the front pad is screened, the back is marked in relation to the front solder pad. The screening machine and plate details can be seen in Figs. 11 and 12.

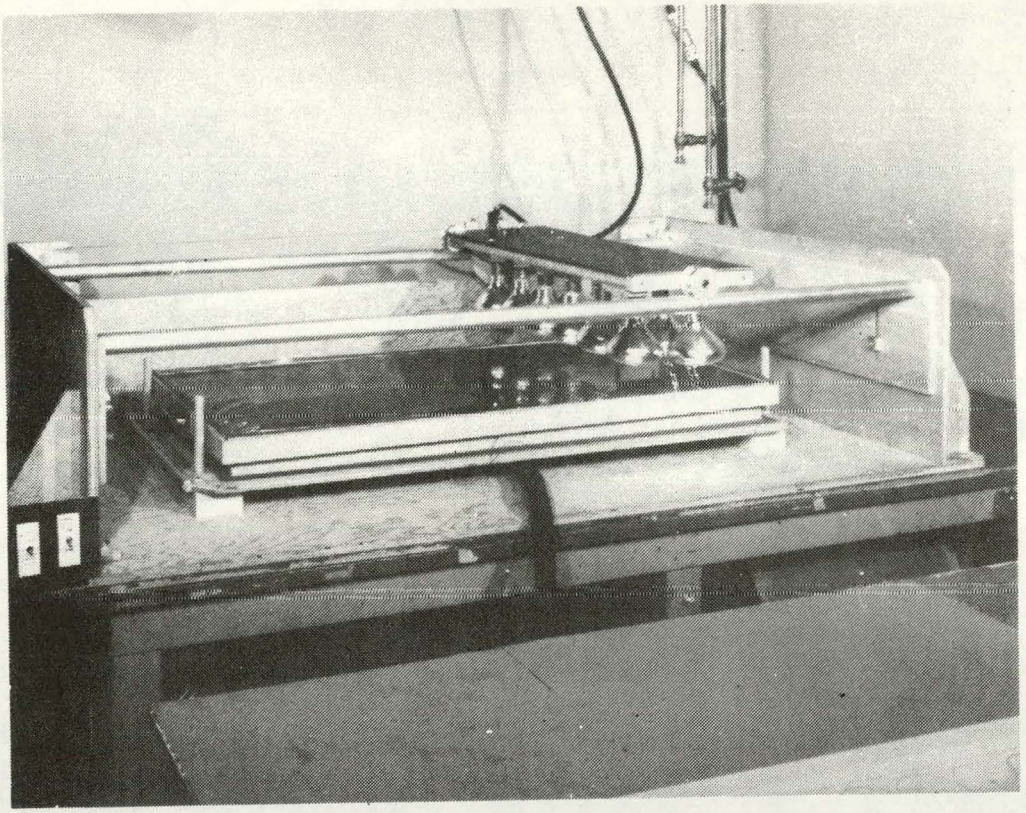

Figure 9. Radiant-heat mass reflow soldering assembly.

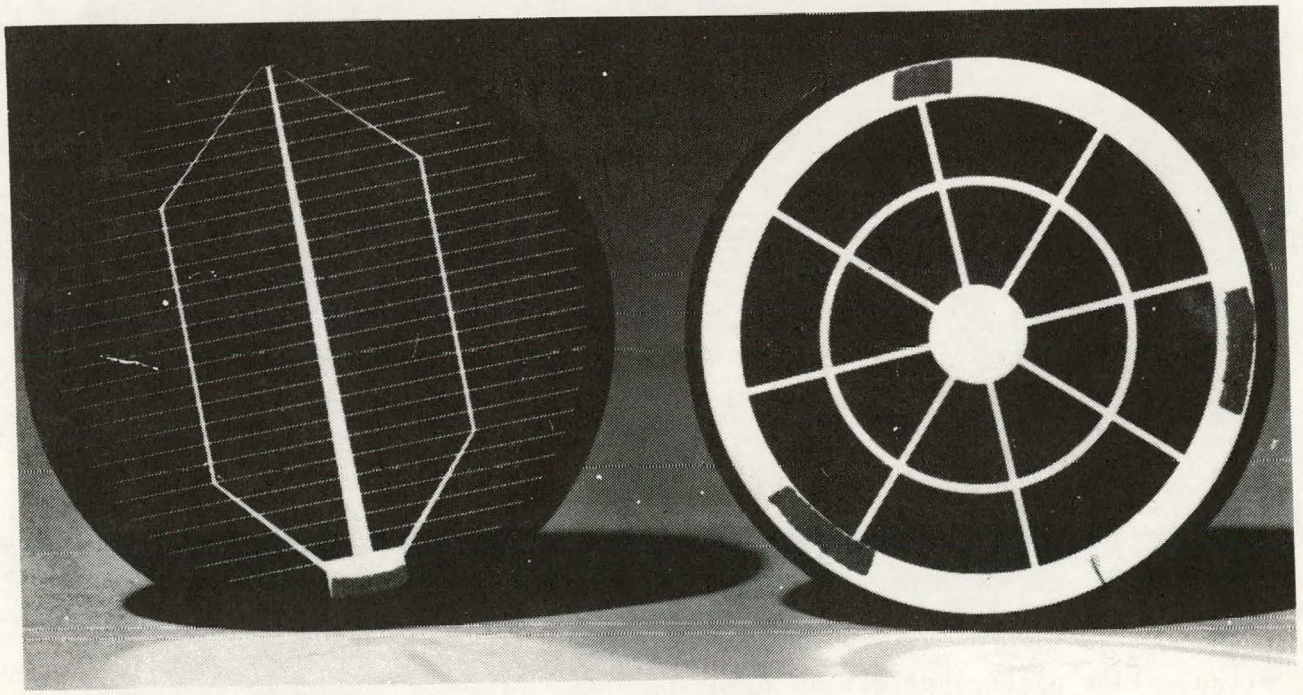

Figure 10. Patterns of front and back of solar cell.

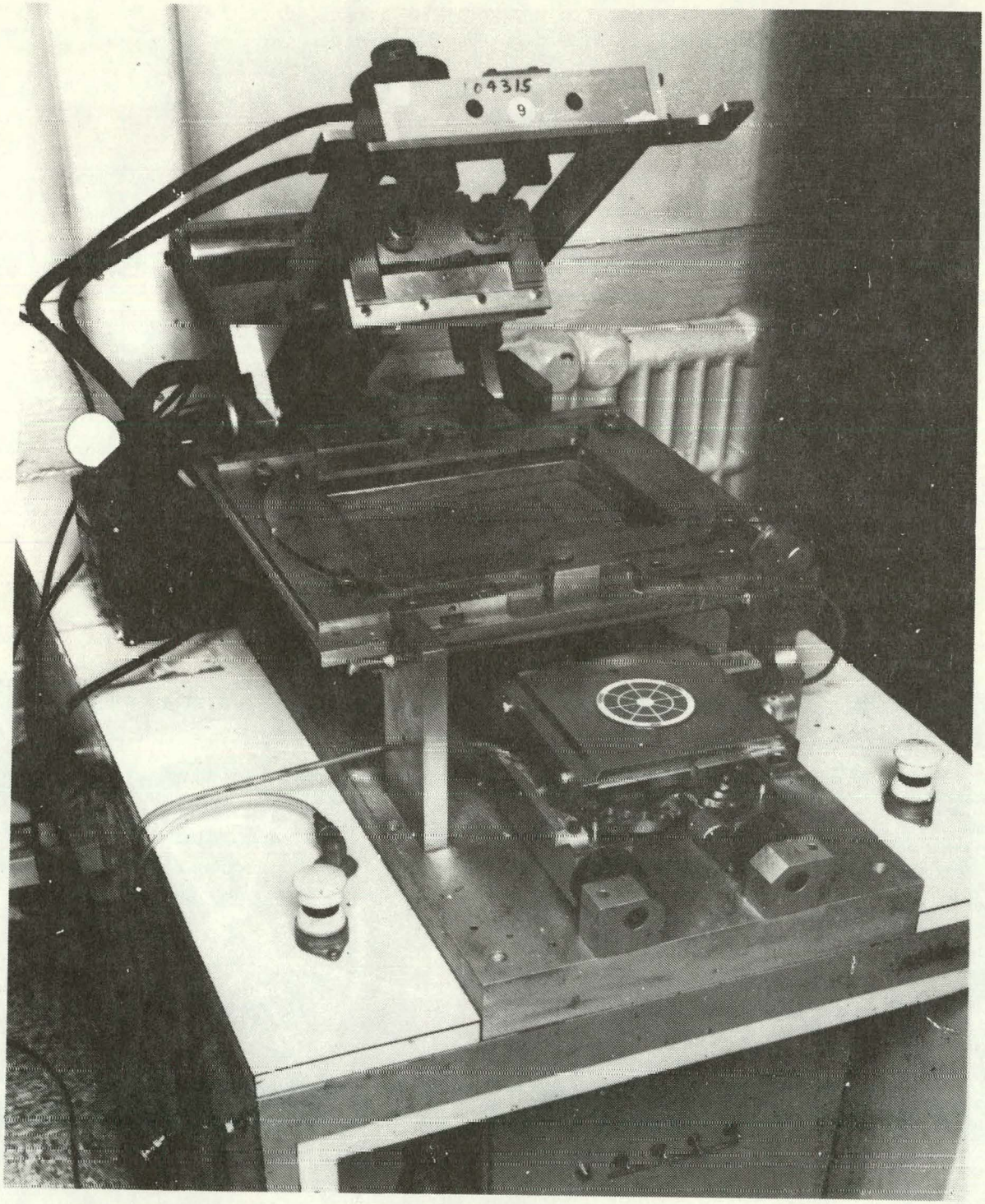

Figure 11. Screening machine and plate details for front of solar cell.

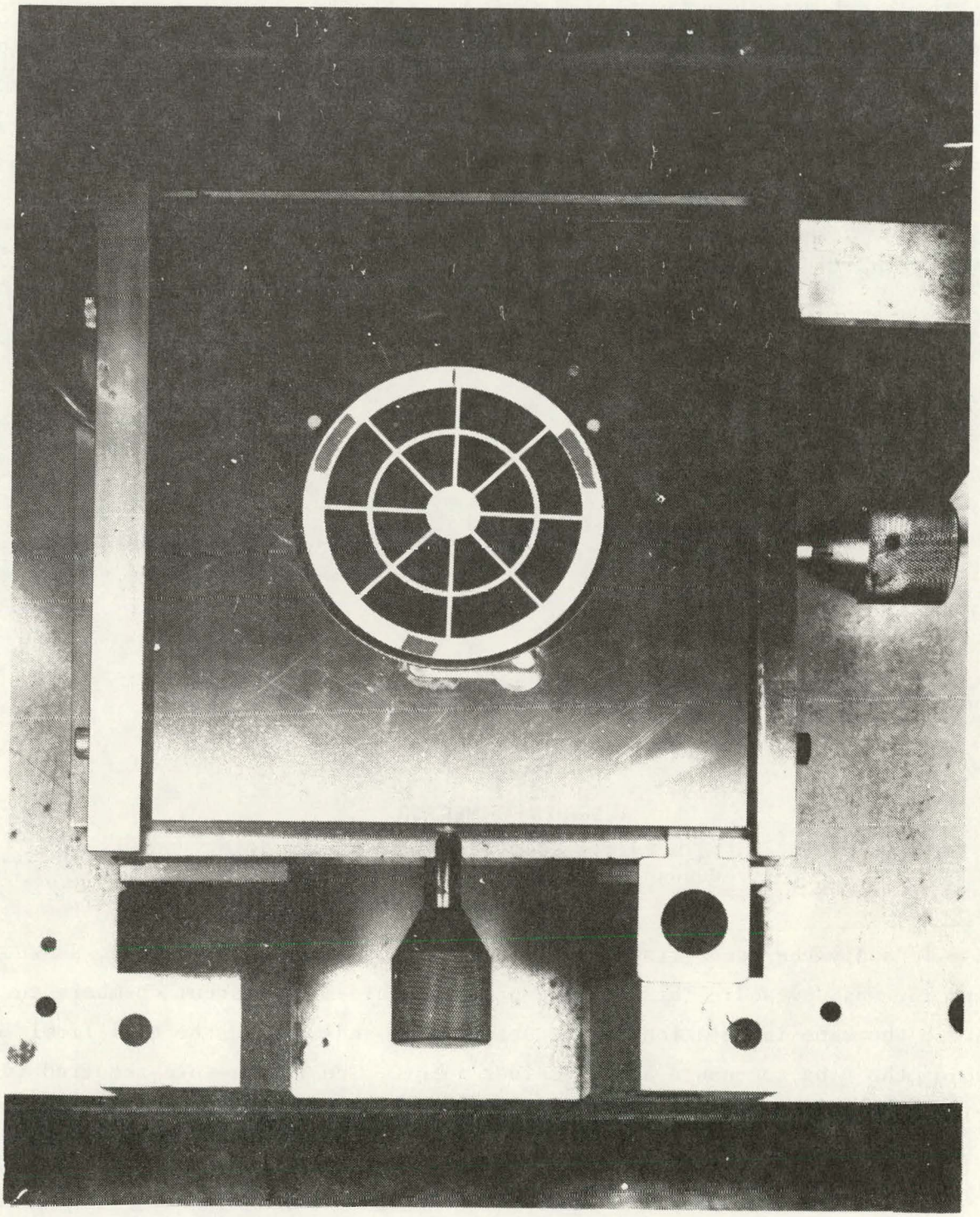

Figure 12. Screening machine and plate details for back of solar cell.

After the screening operation, the cells are ready for attachment of the connecting tabs. The tabs are formed from a reel of pretinned Cu ribbon 0.002 in. thick x 1/8 in. wide purchased from Alpha Metals.* Tools were made to cut and form the tabs. A strain relief is required on the tabs to compensate for the linear expansion difference between glass, cells, and copper conductors, also adding flexibility to comply to the flexing of the panels due to wind and temperature changes. Two types of strain relief geometries used for series interconnect and for redundant-parallel connection are shown in Fig. 13.

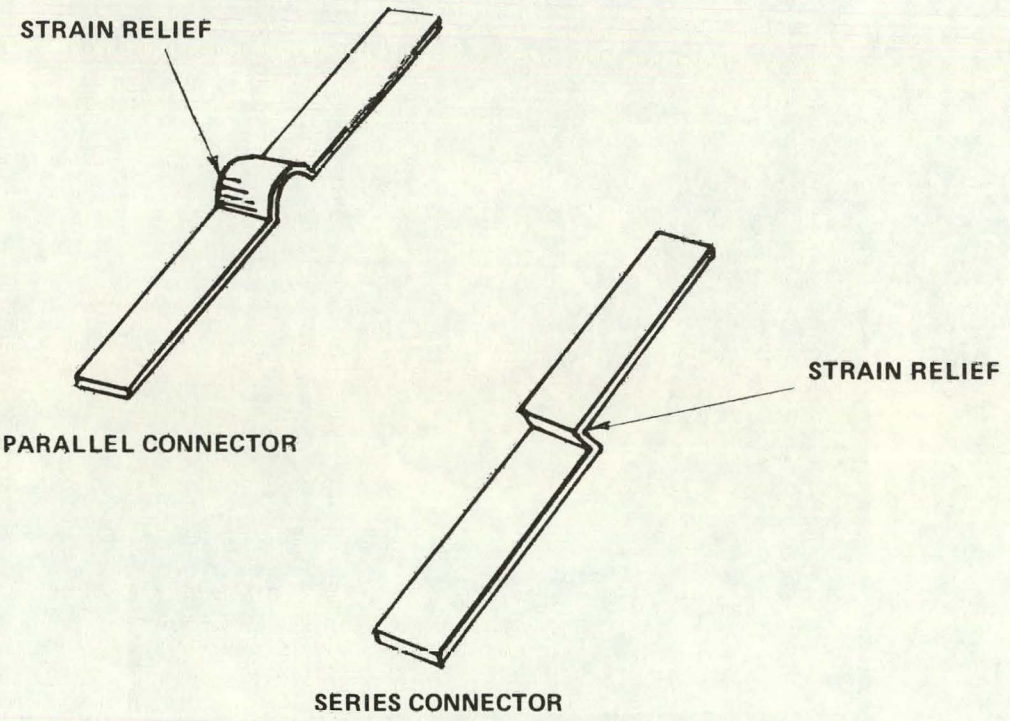

Figure 13. Strain relief geometries for series interconnect and redundant-parallel connections.

To apply the connecting tabs to the cells, a soldering fixture, shown in Fig. 14, was devised. This fixture provides guides and vacuum chambers to locate the tabs in relation to the solder pads and to hold the cell firmly on top of the tabs to ensure a good solder joint. The temperature required to melt the solder, 200°C, is provided by IR lamps for 40 to 50 s. Figure 15 shows a close-up of this fixture.

*Alpha Metals, Inc., Jersey City, NJ.

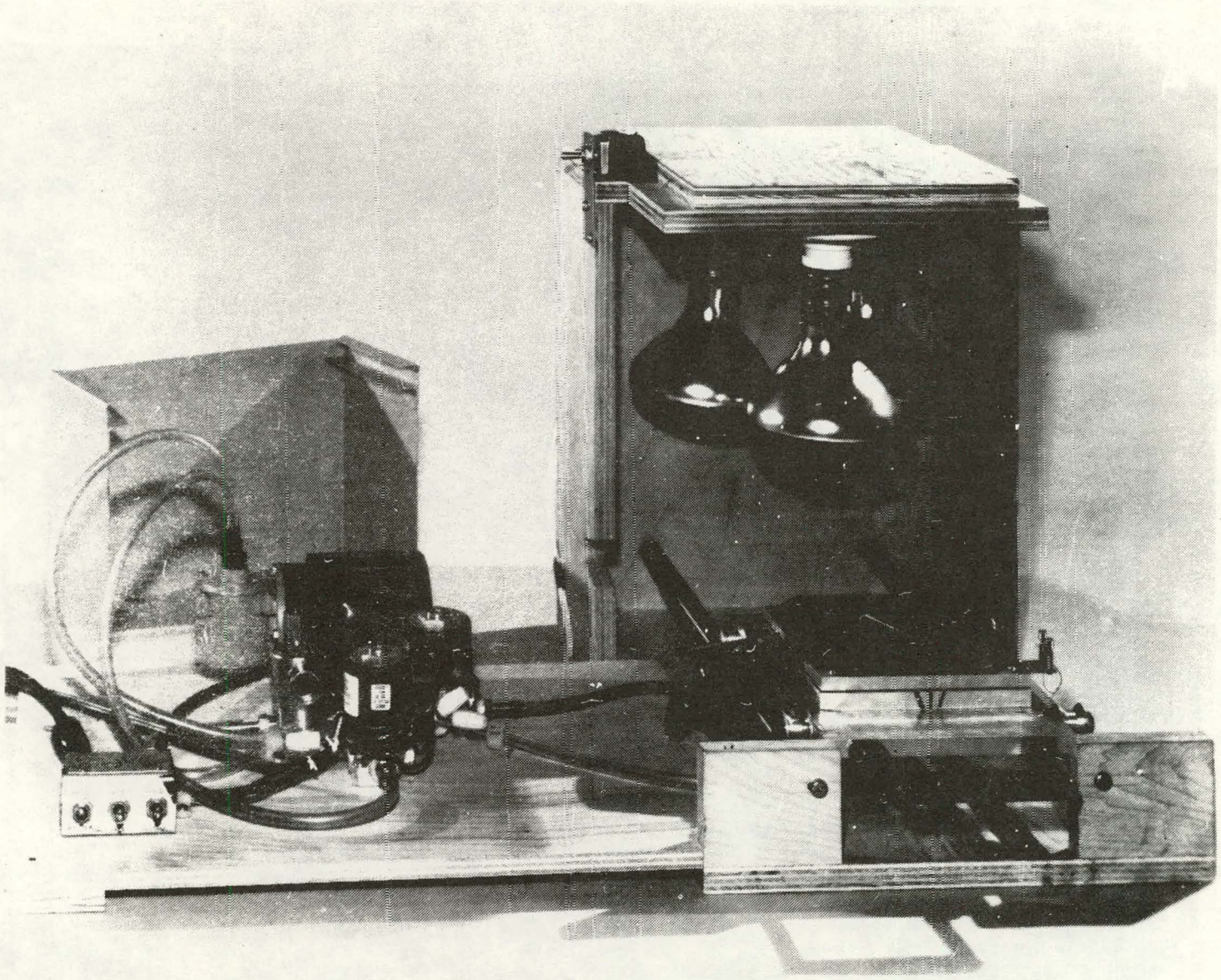

Figure 14. Soldering fixture.

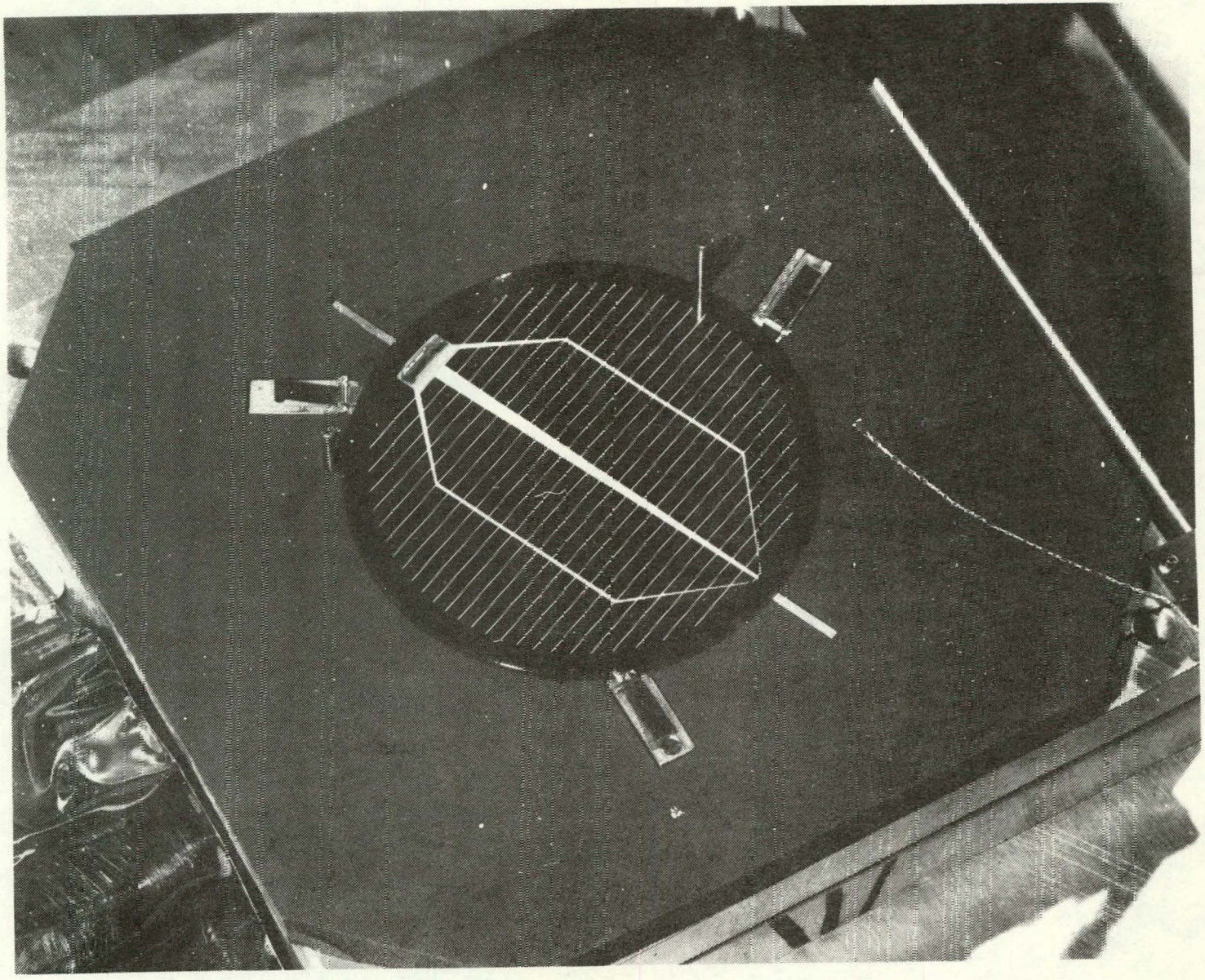

Figure 15. Detailed view of soldering fixture with cell in place.

When enough cells are available to complete a panel array, they are connected together on another IR fixture. At present, the combination arrays are three rows of cells having one tab and two rows of cells with three tabs comprising 12 cells or 15 cells per row. The five rows of 12 cells will give a panel 40 x 14 in., and three combinations of 5 rows of 15 cells, a panel 48 x 40 in.

The tabbed cells are now placed in the proper sequence on a vacuum table which is provided with computer-developed circular perimeter on true center in the desired array configuration. It also provides directional lines to align the tabs in the proper relation to the adjacent cells. This table is shown in Fig. 16. After locating all the cells in the desired array under vacuum, they are transferred to the radiant-soldering vacuum table in Fig. 17. The vacuum is released on the layout table and applied to the radiant-soldering table. The array is now in proper sequence, ready to be connected. The radiant table is provided with kapton cover sheets, held in place with spring tension (see Fig. 17). The kapton cover provides a flattening pressure to the flexible tabs directly on the solder pads with force provided by the vacuum down-pull. When the heat is applied, the kapton expands rapidly so the spring tension relieves the wrinkling effect. The kapton cover not only ensures good junction but also controls the height of the solder joint within 0.001 to 0.002 in. above the cells. After the covers are applied, a bank of IR lamps is passed over the array giving an overall temperature of 200°C at a rate of 1 ft/min. After a complete cycle, about 4 min, the kapton covers are removed. The layout vacuum table in Fig. 16 is placed on top of the array, and the vacuum is removed from the IR table and applied to the layout table which in turn draws up the array to be transferred on the carrier connecting table. See Fig. 18. When the vacuum is cut off, the five rows of connected cells are deposited on the surface. Three 5-row arrays then are connected together in series to create a 48 x 40-in. panel of 225 cells. To ensure a good external output connection, we developed an expanded "W" configuration connecting bus-bar (Fig. 19). This bar, after autoclaving lamination, can be connected to the external cable.

The feasibility of the interconnect process described above was demonstrated in the layout and soldering of several 15x5 arrays. The only problem encountered was in the array reflow, where a flow of excess solder from the pads moved along the tabs filling the stress-relief loops. Considerably less

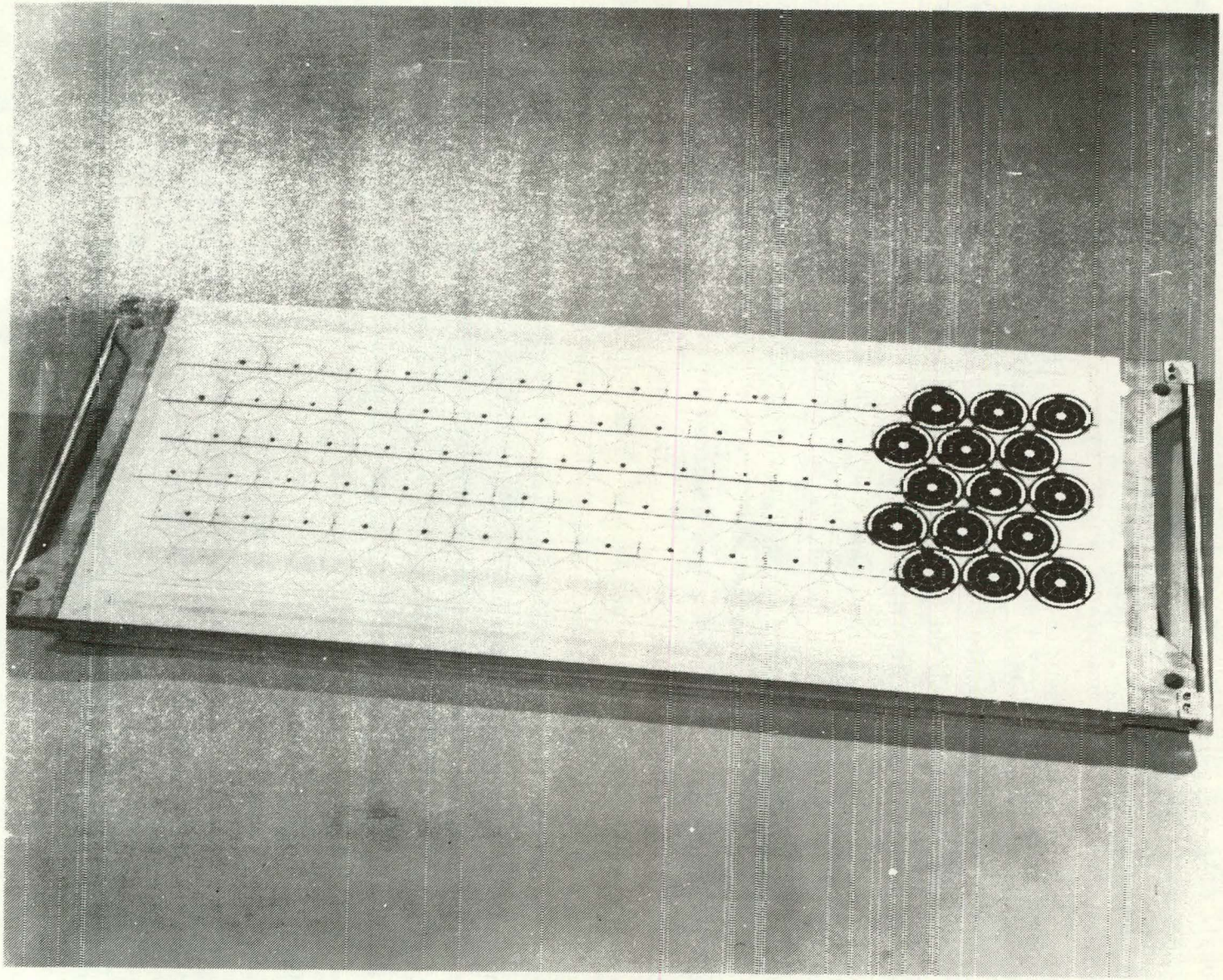

Figure 16. Vacuum table used for cell alignment.

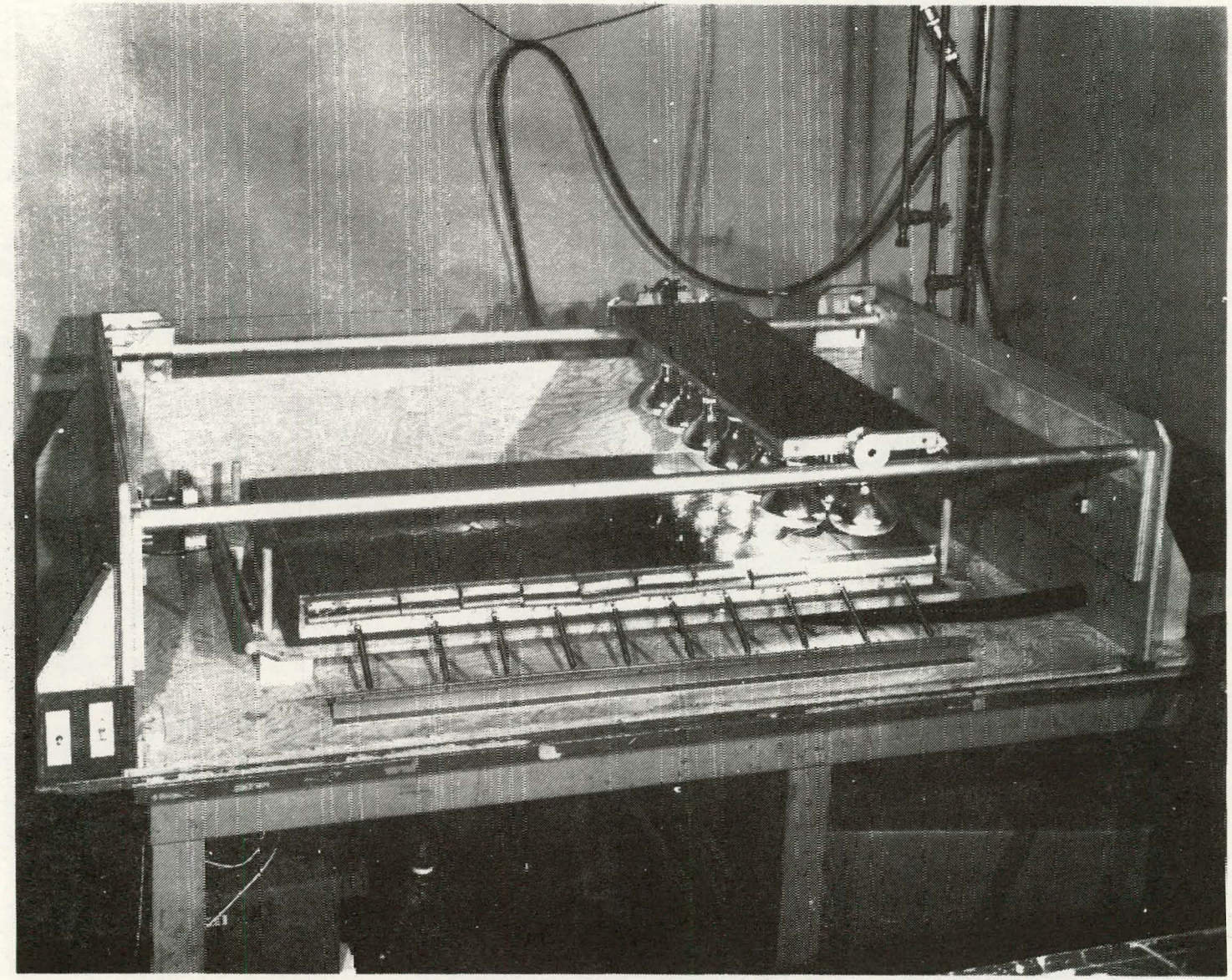

Figure 17. Radiant-soldering vacuum table.

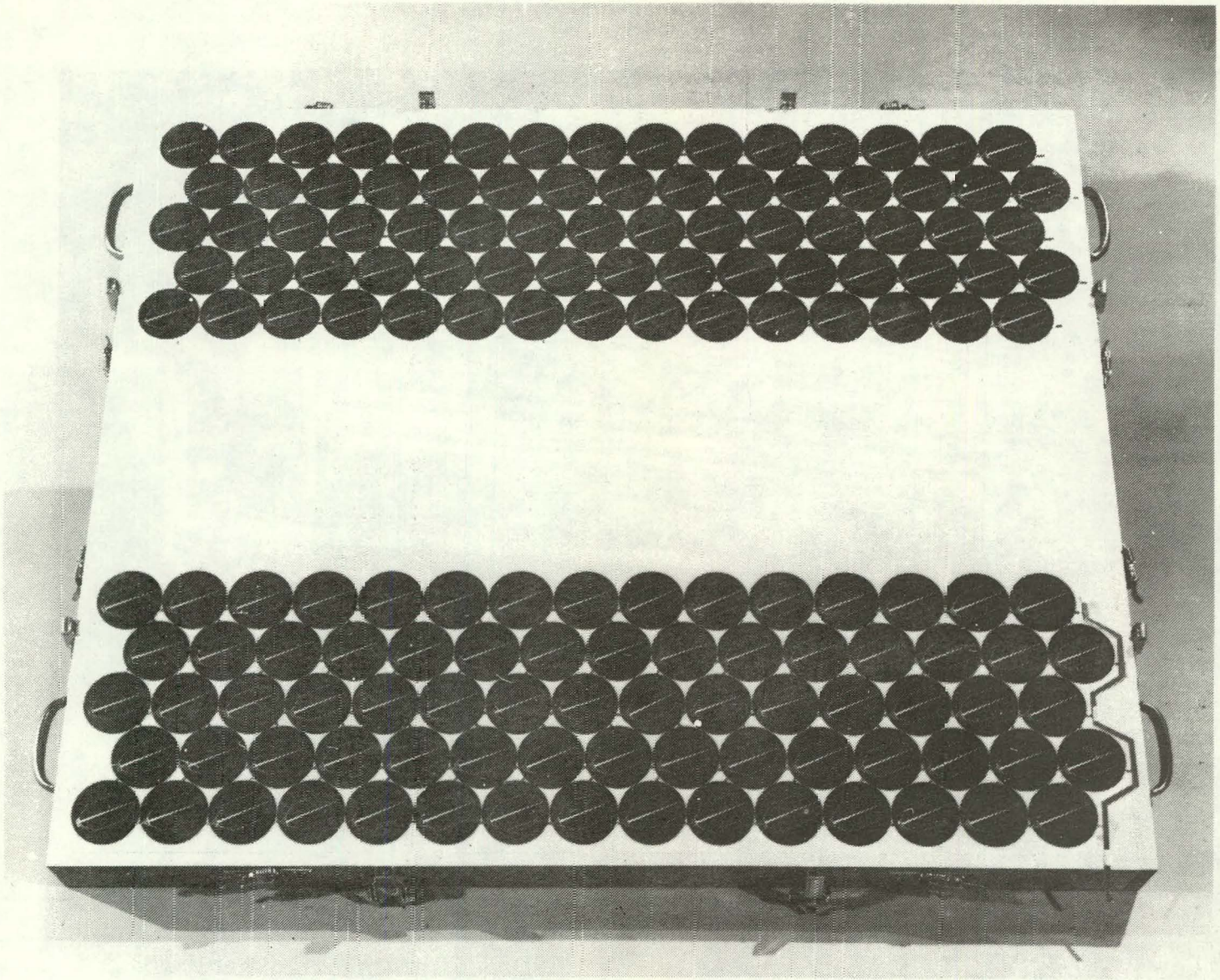

Figure 18. Layout table.

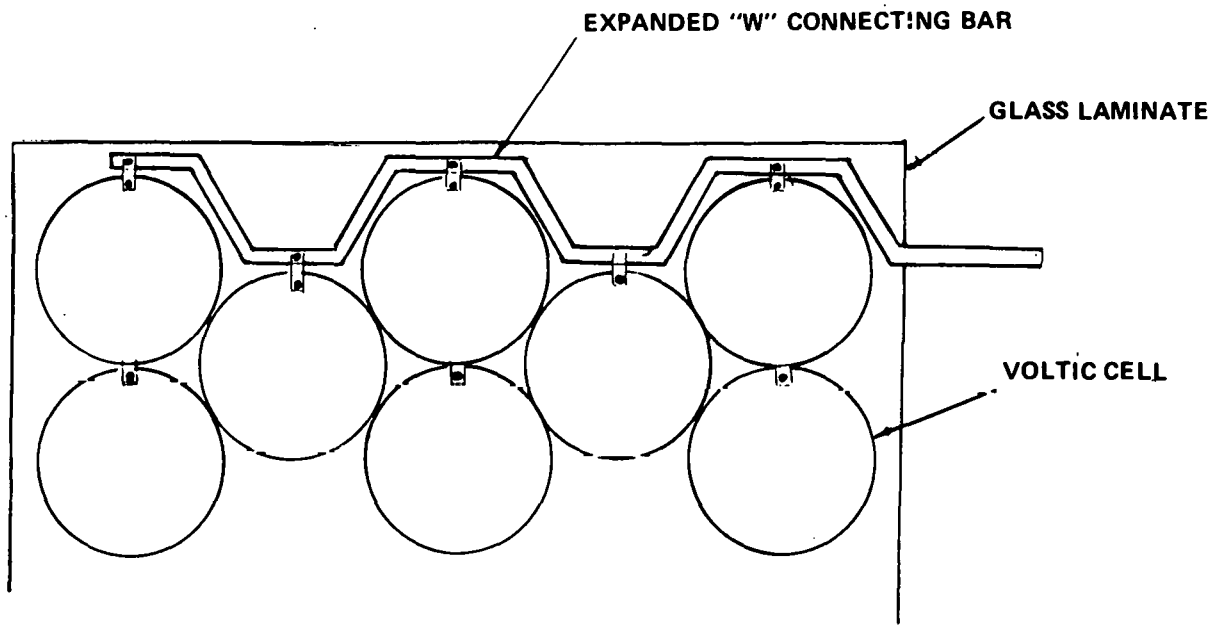

Figure 19. Expanded "W" connecting bar.

solder paste is required on the cells. To accomplish this, a solder paste with smaller particle size was purchased* and a finer mesh screen with a 0.002-in emulsion thickness was ordered.

3. Panel Assembly

Double-glass panel lamination has been continued during this quarter. The cells used in this period were sequence I and III, and ranged in thickness from 0.009 to 0.011 in. Previous cells used averaged 0.015 in. thick. Two panels of 225 cells (48x40 in.) were laminated; in addition, four panels of 60 cells (40x15 in.) were made. In a few cases cell breakage occurred, and the breakage was traced to solder spikes made by hand soldering since the reflow soldering assembly described above was not operational when these panels were assembled.

*Formon No. 8922 solder paste purchased from E. I. DuPont, Electric Material Division, Wilmington, DE.

The full history of these laminated panels can be seen in Table 11 which describes the various methods of lamination and relative problems. These breakages should be eliminated by our new IR connecting fixtures which eliminate solder lumps.

The process used in laminating the panels was described in Quarterly Report No. 5 [3]. As noted in that report, bubbles or air pockets occur at the extreme edges of the panels. This phenomenon also occurred in the latest two-step lamination process. Air is definitely sucked into the PVB layer due to the shrinking of the volume of PVB at cool-down. One small panel was autoclaved in a vacuum bag in a one-step process and no bubbles occurred.

Breaking of the glass occurs at the conductive strap junction because it is difficult to control the height joint during hand soldering. Precautions were taken to file pockets so that the total 0.015 in. of the thickness of one conductor overlaps, but, as mentioned, hand soldering is uncontrollable. The new developed expanded "W" connecting strap will avoid this problem.

4. Frame Technology

During this reporting period, we have continued to use the same framing method described in Quarterly Report No. 6. A section of framing is shown in Fig. 20. An improvement was added to eliminate breakage of laminated panels due to the contact of raw metal to glass. A gasket was introduced between the glass laminate and the aluminum structural frame. This cushioning gasket will prevent scratches on the laminate glass which often initiates minute fractures that will propagate under physical forces. This gasket also provides room for expansion and contraction of the panel. One piece of extruded structure can be developed to retain the panel with a top edge that can be rolled over the panel, as discussed in previous reports. It is imperative that the gasket be used to protect the glass and take up the overspringing of the metallic rollover portions.

TABLE 11. PANEL LAMINATION SUMMARY

Panel No.	Array Size	Cell Type	EVAC Dur. (Min) T=amb	Peak Temp. (°F)	Dwell Time (min)	One-Step Process Press (psi)	One-Step Process Autoclave Cycle (psi)	Two-Step Process Press	Two-Step Process Cool Down w/VAC	Two-Step Process Cool Down w/Press	Result
012479	5x13	Ruf-cut Wafers	15	280	15			No	x		Bubbles at edge
012979	5x13	Ruf-cut Wafers	5	268	15			No	x		Incomplete flow/edge bubbles
021079	15x18	Ruf-cut Wafers	15	285	30			No	x		Edge bubbles/crack cells
022479	15x18	OCLI*	30	270	30			No	x		Panel badly broken
030379	15x18	RCA Dem.	15	280	20			No	x		Bubbles at edge
04279A/B	15x18	OCLI	35	310	20						Perfect
071679	13x5	OCLI	5	175	30			15 psi	x	x	Several small edge bubbles
071779	13x5	OCLI	5	275	30			15 psi			More edge bubbles
073179	5x12	RCA-I	10	275	45			15 psi	x	x	Air trapped in pores of Al metallization
081479	5x12	RCA-III	10	275	45			15 psi	x	x	Glass cracked over high spot on power lead
081579	5x12	RCA-III	5	275	45			5 15	x	x	Small bubbles along bus bar
090179	15x15	RCA-III	15	275	30	15					Edge scallop
091579	15x15	RCA-III	15	275	30			15	x	x	Edge bubbles
092179	12x5	RCA-III	10	275	30			14	x	x	Cell fractures due to solder lumps

*Optical Coating Labs, Inc., Santa Clara, CA.

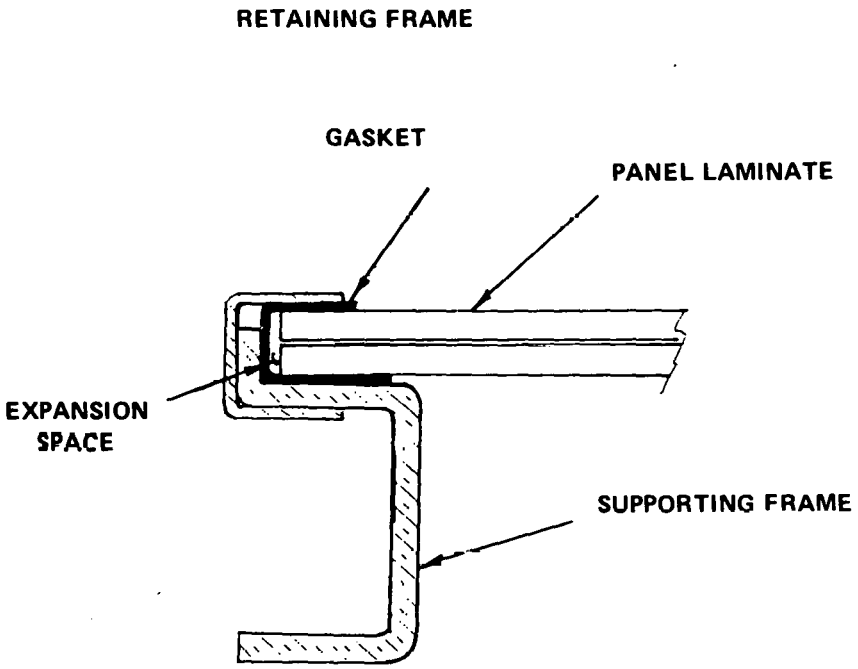

Figure 20. Frame configuration.

SECTION V

CONCLUSIONS

During this quarter, process studies with three manufacturing sequences have been completed with the fabrication and testing of 1500 solar cells made from solar-grade silicon starting wafers. From the data and experience accumulated the following major conclusions concerning materials and processes can be made:

(1) Ion-implantation parameters and annealing techniques which were previously optimized to yield high-efficiency solar cells with quality Czochralski starting wafers cannot be directly applied to the solar-grade wafers used in this study. The changes in the implant parameters required for compatibility with the solar-grade wafers will result in a higher cost for the ion-implantation process.

(2) Even when the implant and annealing parameters are modified to yield apparently satisfactory conditions, compatibility problems were experienced with the screen-printed contacts and the spray-on AR coating process. This manifests itself in the form of excess series resistance after the application and firing of the thick-film contact. This resistance can be reduced to acceptable levels by dilute HF acid rinsing, but the metal-silicon interface remains sensitive to the application of the spray-on AR coating, thus drastically lowering the yield of completed cells.

(3) The compatibility problems described in (2) above were <u>not</u> experienced in the fabrication of cells with junctions formed from a $POCl_3$ gaseous diffusion source. Because of this, the best overall performance was achieved with such cells.

Several additional conclusions concerning the technical details drawn from this work are listed below:

- Of the three manufacturing sequences studied, sequence III, $p^+/n/n^+$ cells exhibited the best cell characteristics with a 13% peak AM-1 efficiency.
- The addition or inclusion of a gettering step in the processing is cost-effective because it can result in an efficiency increase high enough to more than offset the cost of the gettering step.

- Sequence I processing was found least effective. The aluminum p^+ back-surface process did not result in a measurable increase in cell V_{oc} or I_{sc}.

SECTION VI

PLANS FOR THE NEXT QUARTER

The plans for the next quarter include:

(1) Evaluation of 15 meters of dendritic web silicon received from Westinghouse with the elements of sequence I processing.

(2) Continued development of the interconnect and reflow solder technology for panel assembly.

(3) Panel assembly as above and lamination of six double-glass panels (0.36x1.0 m).

(4) Continued examination of process compatibility problems with special attention to the case of junctions formed by $POCl_3$ gaseous diffusion.

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2. R. V. D'Aiello, Automated Array Assembly, Phase II, Interim Report, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-79/1, January 1979.
3. R. V. D'Aiello, Automated Array Assembly, Phase II, Quarterly Report No. 5, prepared under Contract No. 954868 for Jet Propulsion Laboratory, DOE/JPL-954868-79/2, March 1979.

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