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HIGH PERFORMANCE MICROSYSTEM PACKAGING: A Perspective

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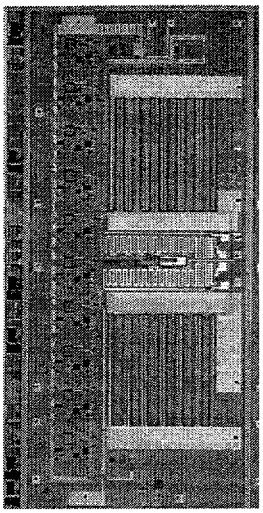
Abstract: The second silicon revolution will be based on intelligent, integrated microsystems where multiple technologies (such as analog, digital, memory, sensor, micro-electro-mechanical, and communication devices) are integrated onto a single chip or within a multichip module. A necessary element for such systems is cost-effective, high-performance packaging. This paper examines many of the issues associated with the packaging of integrated microsystems, with an emphasis on the areas of packaging design, manufacturability, and reliability.

INTRODUCTION

The world is now entering the "second silicon revolution," in which a multitude of functions will ultimately be integrated onto a single piece of silicon creating *intelligent, integrated microsystems*. During the "first silicon revolution," from the 1950's through to the present day, discrete devices gave way to integrated circuits of increasing complexity, with increasing functionality, and improved reliability, yet at ever decreasing costs. The "second revolution" will see the integration of analog and digital logic/memory with micro-electro-mechanical systems (MEMS), physical, chemical, and radiation sensors, and optoelectronic/RF (wireless) communications technology. The result will be multichip modules, and eventually monolithic silicon structures, likely integrated directly with devices based on compound semiconductors (e.g., GaAs), that have the capability to *sense, think, act and communicate*. This will enable the realization of a new generation of integrated circuits that know where they are and what is happening around them.

By definition, the intelligent, integrated microsystem will be a combination of any subset of the functions described above. An example of its simplest form is shown in Figure 1. This is an intelligent sensor, which measures an analog parameter, such as the concentration of an impurity gas, and which converts the analog signal to a digital, network addressable output. This simple microsystem senses and thinks, with communication being through traditional electrical connections.

DISCLAIMER



Integrated microsystems can be fabricated in either one of two ways – monolithic or multichip. All functions can be integrated onto a single chip of silicon, as was done with the integrated hydrogen sensor shown in Figure 1. As more functions are combined, complexity and cost issues may drive some products to monolithic integration, while others may drive towards multichip module (MCM) architectures. Initial production costs, as well as costs of ownership (such as costs for next level system integration or field replacement of defective units) will often be the critical consideration in monolithic versus MCM integration. MCM architectures will likely be most prevalent initially, but the use of monolithic structures will grow as design and manufacturing technology improves.

Figure 1 Close up of integrated hydrogen sensor chip, an example of a monolithic integrated microsystem

A multitude of applications, commercial as well as defense, will propel the development of this technology. For example, the key to cost-effective active automotive braking systems will be intelligent, integrated microsystems. In this case, the microsystem senses the dynamics of the skid, uses the sensed yaw as input to an on-board computer model and then selectively and independently brakes each wheel. While the automotive market will be a major driver of the technology, it will be only a small slice of this growing market, as shown in Figure 2. In fact, by 2000, intelligent, micro-electro-mechanical systems alone will represent a $14B (US) market.

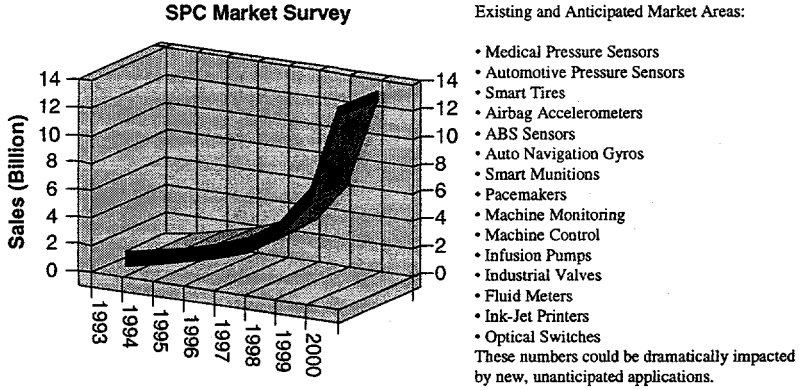


Figure 2 Market projection for Intelligent Micro-Electro-Mechanical Systems sales and market areas

Ultimately, the intelligent, integrated microsystem must itself be integrated into the larger system. Packaging of the microsystem will be required for system insertion. The challenges of packaging microsystems include all of those associated with the packaging of integrated circuits, plus many others. The focus of this paper will be to examine some of the packaging issues now emerging with integrated microsystem technology.

EXAMPLE CHALLENGE

To illustrate the context of many of the issues associated with packaging an integrated microsystem, a MicroNavigator (μN) prototype will be used. The μN is a highly integrated navigation system consisting of three main functional parts – a GPS (Global Positioning System) SAASM (Selective Availability, Anti-Spoofing Module) receiver with full PPS (Precise Positioning Service) capability, an IMU (Inertial Measurement Unit) made using MEMS sensors, and a navigation computer.

Such a system knows its location anywhere on the surface of the earth with high precision. The GPS receiver allows absolute location determination with frequent updates. Between updates the μN can determine its location and orientation by using readings from a 3-axis accelerometer and a 3-axis gyroscope in the IMU. A μN system can have a wide variety of uses, ranging from the tracking of transportation vehicles to precision guidance for advanced weaponry. A subset of its functionality would meet the needs of the active automotive braking system described earlier.

A simplified block diagram of the μN is shown in Figure 3. The μN includes digital and analog devices (CMOS and bipolar), MEMS devices, RF circuitry, and an array of passive components. Thus it meets the definition of an intelligent, integrated microsystem.

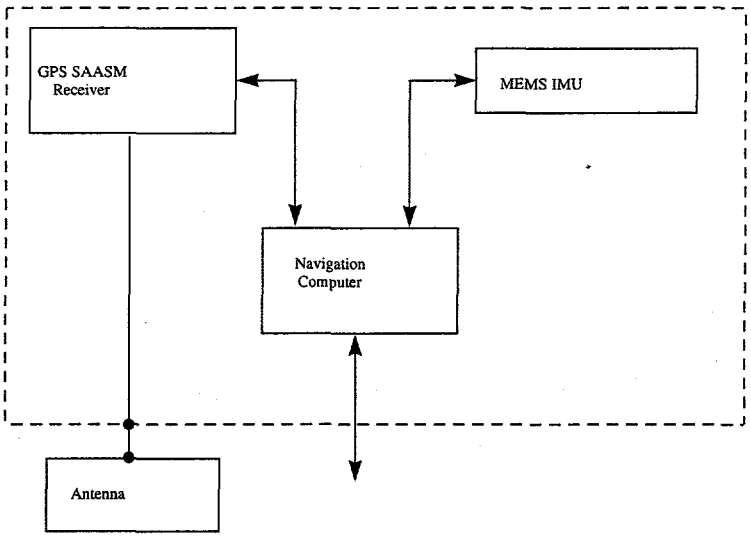


Figure 3 Block diagram of MicroNavigator microsystem

Issues associated with the packaging of integrated microsystems fall into three primary areas – design, manufacturability, and reliability. Design considerations include computer tools for simulation, partitioning, layout optimization, and testability. Manufacturability issues include use of existing infrastructure, standards, assembly approaches, reworkability, materials compatibility, and test approaches. Reliability concerns include tribology, higher power densities, new failure modes, and new material interfaces. In many instances the packaging knowledge and infrastructure in these areas do not currently exist to meet all the requirements. The concerns, shortcomings, and status in these areas will be discussed in more detail in the following sections.

ISSUES

Design

There are a wide variety of issues which must be considered in a full microsystem package design. Although not an exhaustive list, Table 1 enumerates many of these for a general microsystem. Selected items particularly relevant to the μN are discussed in more detail below.

Table 1 Packaging Design Issues for Microsystems

- **Computer Aided Design Tools**
  - ⇒ Space Analysis (physical size considerations and trade-offs)
  - ⇒ Partitioning (optimization of functional and physically part groupings)
  - ⇒ Technology Trade-offs
  - ⇒ Functional Simulation
  - ⇒ Subsystem Simulation (performance, noise, crosstalk, power/ground bounce, ...)
  - ⇒ Substrate Layout/Routability
  - ⇒ Testability Analysis
  - ⇒ Thermal Analysis
  - ⇒ Mechanical Analysis
  - ⇒ Linkages Between Tools
- **Interactions Between Dissimilar Components**
  - ⇒ Electromagnetic Interference (EMI)
  - ⇒ Thermal
  - ⇒ Mechanical
- **Testability**
  - ⇒ Boundary Scan implementation and application (IEEE standard)
  - ⇒ Internal Test Nodes
  - ⇒ Built-in Self-Test
- **Special Concerns for MEMS Devices**
  - ⇒ Packaging Environment
  - ⇒ Mechanical Isolation
  - ⇒ Thermal Isolation
- **Special Concerns for Photonics Devices**
  - ⇒ Waveguide Matching
  - ⇒ Optical Windows
  - ⇒ Precision Alignment
- **Special Concerns for Sensor Devices**
  - ⇒ Communication with Environment to be Sensed
  - ⇒ Mechanical Protection
  - ⇒ Contamination Control
- **Multidisciplinary Packaging Expertise**

Since microsystems require the integration of multiple technologies, the development of multidisciplinary packaging expertise is required. No longer will it be sufficient for the package or assembly "expert" to be focused in a single or a few areas (such as high frequency digital CMOS), since the interactions between various elements of the system cannot be as easily decoupled as in historical system approaches. For example, in the μN possible interferences exist between the RF receiver (which contains very high gain amplifier elements) and the switching noise from the digital signal processing devices. The thermal load from the high power devices can also cause detrimental effects on the MEMS sensors, which are temperature sensitive.

Considerations of such interactions can be assisted by the use of computer tools. Ideally one would desire a fully integrated suite of simulation tools that would allow full electrical simulation at the system level, including packaging parasitics and cross-talk. Integrated with this would be the ability to simulate thermal and mechanical properties from the same database. In addition to the usual design tools one considers for individual ICs or traditional packaging approaches, for an integrated microsystem one would also desire the ability to perform partitioning and packaging system-level trade-offs. Such an integrated design system would include the elements illustrated in Figure 4.

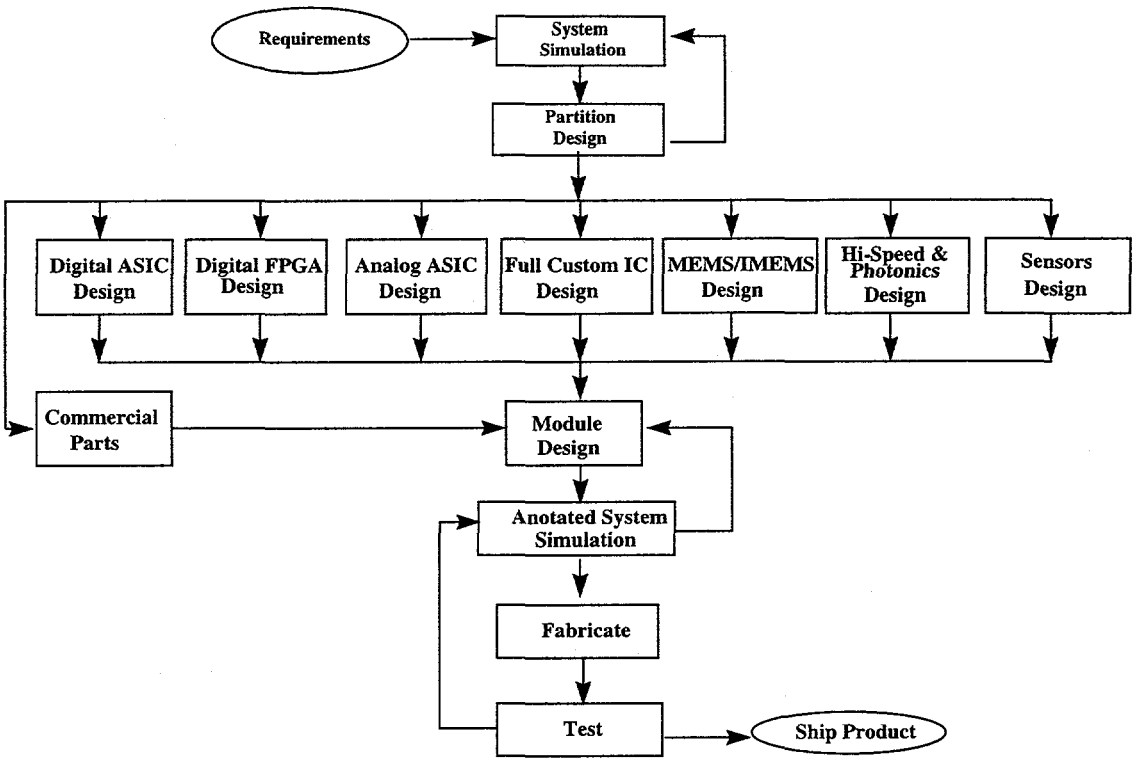


Figure 4 Overview of design flow for integrated microsystem design

Unfortunately, there is no such complete design system available today. Various manufacturers have different parts of the system, but in many cases interfaces between the design tools from different manufacturers are cumbersome at best.

Another important factor which must be taken into account early in the design cycle is testability. An efficient means both to test individual parts of the system for functionality and to isolate defective components for rework or repair is essential for cost-effective assembly and product delivery.

The layout of the μN shown in Figure 5 illustrates how some of these considerations can affect a design. The RF front end is self-contained on a single board which allows its testing as a separate module. It also permits complete EMI shielding of this analog circuitry; the back plane of the board is a full ground plane, and the front surface is enclosed by a metal can. The SAASM KDP and processor module is a separate MCM, which again allows complete functional testing of this block. The main processor board contains the MEMS inertial sensors, the navigation computer, and various discrete components. The MEMS devices are packaged in separate hermetic packages, one containing the 3-axis accelerometer, the other containing the 3-axis gyroscope. They must be in separate hermetic packages since for proper operation the accelerometer requires a controlled dry environment at near atmospheric pressure, whereas the gyroscope requires a vacuum environment. In addition, both of these devices are sensitive to temperature variations, so each hermetic MEMS package contains temperature sensors and heaters to measure and control the temperature.

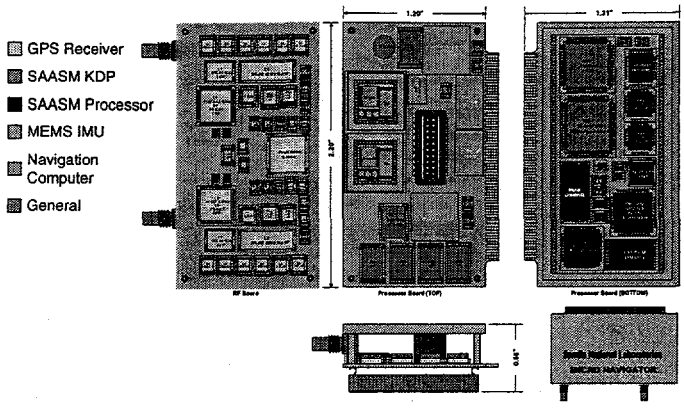


Figure 5 Layout of MicroNavigator modules with component placements

The four primary die associated with the navigation computer (microprocessor, SRAM, EEPROM, and output interface) are area array devices (either flip chip or mBGA). This allows straightforward testing as individual die (so they can be considered Known Good Die), again simplifying the testing of the module as a whole.

Part of the design process must include an analysis of the interconnection density required to connect the various components on substrates versus that available in various substrate technologies. Considerations of this lead to the use of standard printed wiring board technologies for the RF front end and the navigation computer board, and an MCM-D substrate for the SAASM module.

Manufacturing

Reducing cost while increasing functional capability is a prime driver for integrated microsystems. To effectively achieve this goal all aspects of the process for realizing a microsystem must be manufacturable. A global list of many of the issues associated with manufacturing microsystems is given in Table 2. Several selected items particularly relevant to the μN are discussed in more detail below.

Table 2 Packaging Manufacturability Issues for Microsystems

- **Utilization of Existing Infrastructure**
- **Standards**
  - ⇒ I/O pitch
  - ⇒ MEMS Operating Voltage
  - ⇒ Communication Frequencies/Protocols
- **Materials Compatibility**
- **Special Concerns for MEMs**
  - ⇒ Die Separation
  - ⇒ Die Attach
  - ⇒ Package Sealing
  - ⇒ Process Temperature Limitations
  - ⇒ Package-Induced Stress
- **Reworkability**
- **Special Concerns for Photonics Devices**
  - ⇒ Fiber Alignment
  - ⇒ Window Sealing
  - ⇒ Contamination
- **Special Concerns for Sensor Devices**
  - ⇒ Die Attach
  - ⇒ Package Permeability
  - ⇒ Contamination Control
- **Testability**
  - ⇒ Known Good Die
  - ⇒ Fault Isolation
  - ⇒ Internal Test Nodes
  - ⇒ Built-in Self-Test
- **Common Assembly Format on Submodules**

A primary concern in the design process must be ensuring that the microsystem is manufacturable, which in turn translates into cost-effective assembly and test. In order to minimize costs, it is necessary to utilize the existing infrastructure to the maximum extent possible. For example, if one can use standard wirebond or surface mount technologies, one then has access to a widely installed base of equipment, manufacturers, and production experience. Flip-chip approaches, although becoming more widespread, still do not have the widespread acceptance for high I/O parts that these older technologies possess. A promising compromise is the trend towards chip scale packages, which can provide the density advantages of flip chip but enable simpler testing and use of standard surface mount assembly techniques.

Another item needed to simplify manufacture is the implementation of standards for the newer technologies (such as chip scale packages). By having standardized I/O or array pitches, process development and implementation is greatly simplified, as is the ability to swap parts from different manufacturers into a given substrate design. Since microsystem packaging will take place at the system level in many companies, a level at which proprietary concerns become tantamount, it may be necessary to have the CEOs of such companies formally request that the packaging standards committees and consortia develop the appropriate standards.

An example in the μN where currently standard packaging processes cannot be used is for the MEMS devices. Since there are freely moving mechanical structures on the surface of the die, special precautions must be taken during the process of separating the die on a wafer to minimize particulate formation. These devices are also especially sensitive to stress in the die, so die attach processes which minimize stress both during and after mounting must be used. The need to package some devices in a vacuum environment (and maintain that vacuum over long periods) is another non-standard process. One way in which these issues may be addressed in the future is by the trend towards a "blurring" of the line between wafer fabrication and device packaging; in a number of cases, packaging is being pushed into the fabrication facility and is, in effect, becoming a back-end fab process.

In the μN there are several separately assembled modules. To simplify the assembly process, on a given module the parts are made in similar formats. For example, on the navigation computer board, the IC die are solder attached to the board with area array connections in a chip-scale package format (such as the mBGA). This allows all parts on this board to be assembled as surface mount devices.

Material compatibility between different technologies must also be considered during the manufacturing flow. For example, the MEMS devices may have anti-stiction coatings applied to enhance performance but which may have temperature sensitivities which may preclude the use of some materials systems requiring high temperatures in other parts of the assembly process.

During the design phase, testability considerations must play an important role to ensure manufacturability. For a product as complex as many microsystems may be, fault isolation to identify bad parts, assembly defects, etc. is critical as is a viable rework process. Decisions must be made for the cost trade-offs associated with obtaining Known Good Die versus a lesser level of testing at the individual die level and the accompanying increased risk of failure after assembly. Another trade-off is that of including internal test nodes to increase observability of faults and improve identification of faulty components. Still another option is use of devices containing boundary scan circuitry, which allow direct test access to I/O pins on die internal to a module. For many applications, a built-in self-test approach can provide significant advantages. This can be implemented either through custom ASIC designs (particularly if they are already part of the microsystem design) or through programmable logic. In the μN the main interface chip is an FPGA, which allows for some self test features to be programmed into this device.

Reliability

Since relatively few microsystems have been designed and manufactured, field data on reliability is sparse. For example, no MicroNavigators are aging in the field today. However, a variety of considerations for reliability can be enumerated, as given in Table 3. Rather than discuss issues of particular interest to the μN, in this section we will discuss more broadly microsystem reliability.

Table 3 Packaging Reliability Considerations for Microsystems

- **Special Concerns for MEMS Devices**
  - ⇒ Tribology on the μm Scale
  - ⇒ Contamination
  - ⇒ Particles
  - ⇒ Cleaning
  - ⇒ Outgassing
  - ⇒ Surface Aging
  - ⇒ Stiction
  - ⇒ Mechanical Fatigue
- **Special Concerns for Photonic Devices**
  - ⇒ Outgassing
  - ⇒ Contamination
  - ⇒ Cleaning
  - ⇒ Power Cycling
- **Special Concerns for Sensors**
  - ⇒ Contamination
  - ⇒ Calibration Drift
  - ⇒ Environmental Interactions
  - ⇒ Reversibility
- **Microsystem Interactions**
  - ⇒ Interactive Aging Mechanisms
  - ⇒ Thermal Response
  - ⇒ Mechanical/Electrical Modulation
  - ⇒ Package Interfaces
- **Assessment Approaches**
  - ⇒ Test Chip Family
  - ⇒ Smart Packaging
  - ⇒ Built-in Monitoring

The integrated nature of the microsystem suggests that some testing of reliability will have to be on the system level, and not the component or subsystem level. However, once an aging mechanism is identified within a system, life extension development may be better performed on test structures focused on the mechanism in question rather than full-up microsystems.

The existence of moving micro-parts introduces tribology and contamination concerns. For example, a small spec of silicon dust remaining after wafer sawing could easily perform like the proverbial "monkey wrench" in macro-gears. Reliable implementation of moving parts within the microsystem require: (1) new particle-free chip singulation processes, (2) cleaning and heating steps that leave surfaces of moving parts in the "correct" frictional state to minimize wear rate and avoid sticking, (3) ultraclean assembly to avoid particulate contamination, and (4) sealing steps with atmosphere control. Questions that need to be answered in order to ensure proper functionality in the long term include the following: Does the slow outgassing of die attach material change the tribology of the moving parts? Given a controlled sealing atmosphere, what rate of aging of surfaces takes place? As the atmosphere in sealed parts equilibrates with the ambient, at what point is performance degraded?

Previous important questions in packaging have been answered by extensive use of test structures or test chips that exhibit a response to the package or package environment which is enhanced over that of ordinary product ICs. For example, Sandia ATC2.5 chips are sensitive to corrosion and thermal flux; they can be used to measure degradation rates and to compare packaging designs. Similarly Sandia ATC4.0 and 4.1 can measure mechanical stress exerted on the chip by the package in both wirebonded and flip chip formats. To evaluate reliability for microsystem packaging, a new family of test chips will need to be developed. This test family must have moving parts, RF communications links, and analog and digital noise-sensitive circuits in addition to the chemical, mechanical, and thermal sensors of past test chips. Checking

for material compatibility between such a test microsystem chip and proposed assembly processes and packaging design would be a first start for reliability studies.

Thermal management has consistently surfaced as a challenge with systems running at higher frequency, performing more functions, and occupying less volume. The new thermal challenge may come from the extra power the inherent inefficiencies in RF and photonic circuitry provide with the unknown thermal response of moving parts over their lifetime. It is expected that a standard packaging strategy of trying to create an isothermal system by distributing the heat throughout the system will apply to microsystems. In this case the use of highly conductive thermal substrates such as copper, aluminum, aluminum nitride ceramic, AlSiC cermet, and thin surface microheatpipes is recommended. Having built-in temperature sensors with feedback to system functions may be advantageous in thermal management — e.g., consider the microprocessor that turns off when your computer overheats as a primitive example of self regulation.

Although other degradation paths are possible they have not been confirmed because microsystems are in their infancy. For example, any organic materials used will slowly outgas; subsequent deposits on the moving parts and on optical elements may prove fatal. In addition, the modulating mechanical stresses caused by moving parts may induce unwanted modulation of the transistor properties. Assuming friction and wear-out problems are solved, little is known about mechanical fatigue for structures on the micron scale. Lastly, the many new packaging interfaces of the microsystem must be tested over time under temperature and power cycling.

Everything is not more difficult in microsystem packaging. One advantage inherent in microsystems with multiple technologies is the ease with which sensors, processing, and feedback can be added. "Smart" packaging comes naturally. For companies about to field microsystems for the first time, being able to interrogate systems returned from the field as to their evolving internal environment and symptoms could provide quick product improvement. Built-in logic to switch between redundant paths when degradation is detected could greatly enhance field reliability. Warnings to the user about remaining time for reliable performance could add value to products.

Reliability challenges loom large on the microsystem horizon, but the many technologies that contribute to microsystem realization also promise to quantitatively reveal aging mechanisms and provide a quick, logical path to product improvement.

SUMMARY

Microsystem packaging issues can be categorized as design, manufacturing, or reliability.

Integrated design software to simulate the intermingled environments of RF, analog, digital, sensors, and micro-mechanics will require extensive development and refinement. Thoughtful layout will be needed to ensure testability of individual functions within the microsystems in order to troubleshoot or tune a design and production line. As in any new area, packaging design rules of thumb will emerge and allow new engineers to quickly learn the "logic" of the business.

Manufacturing carries on the theme of quick, definitive testing to allow straightforward yield enhancement on the line. Built-in testing with automatic fault assignment should be the goal of microsystems assembly. If the testing is performed in real time on the manufacturing line, then methods for rework become important in both the MCM and monolithic microsystem.

Packaging reliability concerns have not yet been prioritized given the newness of the field. However, initial system developments indicate a new level of cleanliness and surface friction state must be considered in all assembly processes. Material compatibility and slow degradation would best be determined by defining microsystem test structures which show measurable change with only small degradation.

Cost-effective packaging is a necessary element of the second silicon revolution. The challenges of microsystem packaging have begun to be addressed. The large market for microsystems makes it clear that any challenge will be overcome. The "smart" nature of the microsystem provides a route for packaging improvement; any shortcomings will produce anomalous readings on the system sensors and allow early detection and subsequent redesign. Just as people are quick to alert doctors of ineffective cures, microsystems will immediately alert their designers to improper packaging or system design.

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GLOSSARY OF ACRONYMS

ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
ATC	Assembly Test chip
CEO	Chief Executive Officer
CMOS	Complementary Metal-Oxide-Semiconductor
EEPROM	Electrically Eraseable, Programmable Read-Only Memory
EMI	Electromagnetic Interference
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
IC	Integrated Circuit
IEEE	The Institute of Electrical and Electronics Engineers, Inc.
IMU	Inertial Measurement Unit
I/O	Input/Output
KDP	Key Data Processor
μN	Micro Navigator
mBGA	mini Ball Grid Array
MCM	Multichip Module
MCM-D	Multichip Module Deposited thin film substrate
MEMS	Micro-Electro-Mechanical Systems
PPS	Precise Positioning Service
RF	Radio Frequency
SAASM	Selective Availability, Anti-Spoofing Module
SPIE	Society of Photo-optical Instrumentation Engineers
SRAM	Static Random Access Memory