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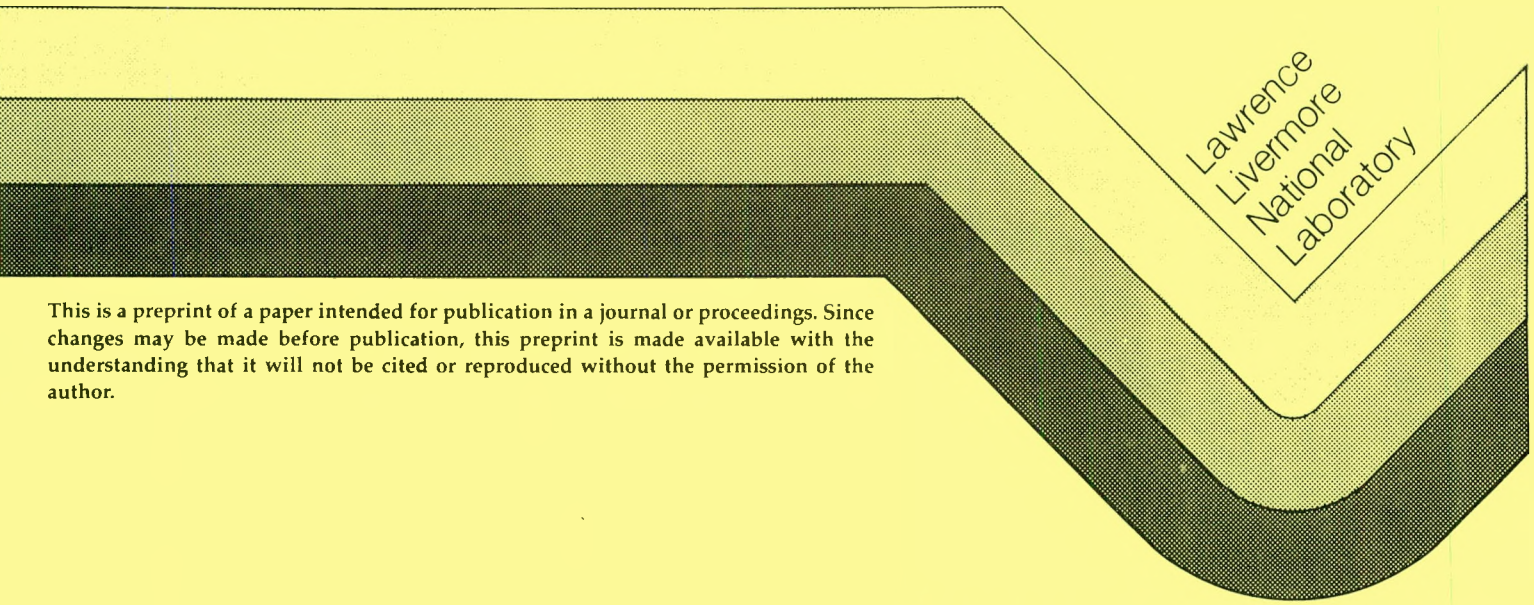

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Abstract

Magnetic compression circuits show the promise of long life for operation at high average powers and high repetition rates. When the Atomic Vapor Laser Isotope Separation (AVLIS) Program at Lawrence Livermore National Laboratory needed new modulators to drive their higher power copper lasers in the Laser Demonstration Facility (LDF), existing technology using thyratron switched capacitor inversion circuits did not meet the goal for long lifetimes at the required power levels. We have demonstrated that magnetic compression circuits can achieve this goal. Improving thyratron lifetime is achieved by increasing the thyratron conduction time, thereby reducing the effect of cathode depletion.

This paper describes a three stage magnetic modulator designed to provide a 60 kV pulse to a copper laser at a 4.5 kHz repetition rate. This modulator operates at 34 kW input power and has exhibited MTBF of ≈1000 hours when using thyratrons and even longer MTBFs with a series stack of SCRs for the main switch.

Within this paper, the electrical and mechanical designs for the magnetic compression circuits are discussed as are the important performance parameters of lifetime and jitter. Ancillary circuits such as the charge circuit and reset circuit are shown.

Introduction

Extensive experience with thyratron driven capacitor inversion circuits for driving moderate power copper lasers (≈10 kW input) convinced us that this type of circuit would not exhibit the lifetime required for the new higher power lasers. The dI/dt, peak amplitudes, and repetition rates of existing modulators caused premature thyratron failure due to cathode depletion and anode erosion; a factor of three increase in power requirements would only increase the problem. An examination of other types of modulator switches, technologies, and circuit topologies did not reveal a simple, inexpensive, or proven alternative. It was determined that the more complex magnetic compression circuits could reduce the electrical stress on the thyratron thereby potentially increasing lifetime; but their use, in turn, raised questions concerning jitter, long term reliability, efficiency, and component lifetimes.

This presentation begins with a listing of the electrical and mechanical constraints placed upon the modulator design. This is followed by selection of a circuit topology chosen to meet the electrical requirements. After a general discussion of magnetic switch design, the paper continues with the specific electrical and mechanical design for the components which comprise the circuit topology. A brief description of ancilliary circuits is followed by performance data. The appendix discusses a general philosophy for magnetic switch design and includes definitions for the terminology used throughout this paper.

Electrical and Mechanical Requirements

As with any engineering project, there exists system requirements, specifications, limitations, and goals that must be satisfied by the product design and performance. The specific modulator electrical requirements are derived from the desired operational parameters for the laser and the main switch. Physical restrictions imposed by the system packaging of the laser, modulator, power supplies, trigger systems, control systems, etc. establish size and weight constraints. The goals for component lifetimes and the package MTBF determine the scope of repair and testing facilities and are cost driven. The major electrical and mechanical parameters are listed in Table 1.

Table 1. Specifications and Requirements.

Design Specifications	Performance Characteristics
Laser Requirements:	>60 kV peak voltage at laser head ≤40 ns voltage risetime (10% - 90%) 5-6 joules/pulse delivered to laser Continuous operation at ≈4.5 kHz.
Other Specifications:	MTBF ≥1000 hours Time jitter ≤±2 ns on output pulse 1 μs minimum thyratron conduction time 20 kV maximum thyratron voltage
Mechanical Specifications:	Modulator enclosure ≈2'x 2'x6' Cooling by immersion in dielectric coolant with internally mounted liquid to liquid heat exchanger

Modulator Topology

The overall gain required for this modulator design is determined by the ratio of the thyratron conduction time (which is also the hold-off time of the first magnetic switch) to the output pulse risetime. These parameters taken from Table 1 give a minimum gain of 25 (1 μs/40 ns). This suggests either three stages of compression each having a gain of approximately three or two stages of compression each with a gain of five. Because core losses scale with the gain squared (see the discussion in the appendix), a modulator designed for two stages with gains of five will have approximately 85% more core losses than the same modulator using compression gains of three, although some of these losses will be offset by the reduction in capacitor and conduction losses associated with one less stage of compression. After consideration of these and other factors, a topology consisting of three stages was selected.

The output voltage design requirement also indicates the need for a transformer. The circuit location of this transformer is sometimes determined by the switch design in that the circuit impedances can lead to physically impractical mechanical structures (windings having less than one turn or an excessively large number of turns). The desire to operate modulator components at the lowest voltage possible and to minimize the core material needed for the transformer places the transformer between the second and third stage. This circuit topology is shown in Fig. 1.

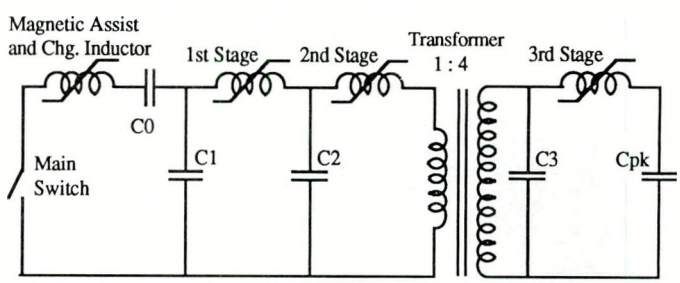

Figure 1. Three stage magnetic compression circuit.

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** Now with Science Research Laboratory, Inc., Somerville, MA.

General Switch Design

The design of a magnetic switch can be divided into two parts; the electrical design and the mechanical design. The electrical design for the circuit shown in Fig. 2 determines the value of the capacitors and the value of the saturated inductor for a specific post-saturation energy transfer time.

For an energy transfer time (τ_{Cn+1}^{chg}), peak operating voltage (V_{Cn}^{pk}), and stored energy (E_{Cn}) the equations are:

$$C_n = 2E_{Cn}/V_{pk}^2 \quad (1)$$

$$\tau_{Cn+1}^{chg} = \pi\sqrt{(L_n^{sat}C_{eq})} \quad (2)$$

Where C_{eq} is the equivalent series value of C_n and C_{n+1} (usually $C_n \approx C_{n+1}$). Once these values are determined, other circuit parameters such as peak and rms currents may also be calculated and used to determine ohmic losses in capacitors and windings.

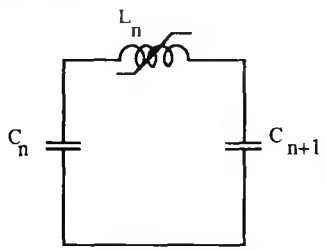

Figure 2. Simplified circuit for single stage.

The mechanical design is much more detailed and requires information on the properties and geometry of the magnetic material and windings in order to achieve the required gain while also satisfying the values determined in the electrical design. The mechanical design must also meet the requirements imposed for cooling and operation at high voltage. This is an iterative process with many variables and is easily implemented in a computer spreadsheet.[1] There are usually numerous possible designs that meet both the electrical and mechanical requirements, so to find a specific solution, some parameters have to be chosen by the designer.

For toroidal core geometries, the equations used in the mechanical design are:[2]

$$Vol_n \approx Gain_n^2 * E_{Cn} * \pi^2 * \mu_r^{sat.} * \mu_o / (4 \cdot * (\Delta B_s * pf)^2) \quad (3)$$

$$L_n^{sat} = \mu_r^{sat} * \mu_o * w_n \cdot * N_n^2 * \ln(OD/ID)/(2\pi) \quad (4)$$

$$\langle V_{Cn} \rangle * \tau_{Ln}^{sat} = N_n * A_n \cdot * \Delta B_s \quad (5)$$

To ensure operational performance, the discharge time of a given stage should be equal to or less than the hold-off time of the next stage with this relationship held for every compression stage in the modulator. Achieving this overlap of saturation and hold-off times of adjacent switches usually requires several iterations of the mechanical design for the entire modulator, but only the last iteration will be presented herein.

First Stage Design. Having specified the peak input charge voltage on C_o to be 20 kV (≈8 joules) and after including losses due to the thyratron inversion circuit, the peak charge voltage on C_1 is approximately 19 kV. With a gain of ≈3, a 1 μs thyratron conduction time , and input energy at 7.2 joules per pulse (determined from previous iterations), the electrical design for the first stage gives the value for C_1 = 40 nF, C_{eq} ≈20 nF, τ_{C2}^{chg} ≈330 ns, and L_1^{sat} ≈550nH.

To begin the mechanical design, a ferrite toroid was chosen with a ΔB_s ≈0.6T (assuming a dc reset current) and the nominal dimensions 101.6 mm ID, 152.4 mm OD, and 12.7 mm thick. The packing factor, 0.9, includes small gaps between individual toroids for cooling and is calculated as the total magnetic cross-section area divided by the total area encompassed by the turns of the winding. Several ferrites have been used which met our needs: CMD 5005 from Ceramic Magnetics, PE-11B from TDK, and C-7D from Stackpole (no longer a producer of ferrites).

The value used for μ_r^{sat} is subject to discussion. Since magnetic materials do not reach saturated permeabilities of unity until the H field is several tens of thousands of ampere-turns per meter, an average value over the entire energy transfer time (determined experimentally to be approximately 1.9-2.0) is used. Substituting these numbers into Eq. (3) gives $Vol_1 \approx 1.3*10\text{-}3\ m^3$. This volume requires a stack of 10 toroidal cores thereby giving a combined area cross-section of $3.23*10^{-3}\ m^2$. From Eq. (5), 5 turns (rounded up from 4.9) are required.

The calculation for saturated inductance requires specific information on the winding geometry. Mechanically, the turns on this switch are constructed of 0.375 inch diameter aluminum rods positioned on and touching the inside and outside diameters of the ferrite toroids. At the ends of the toroidal stack, the rods are fastened with screws to a printed circuit board which has wide (low inductance) traces which connect the outside rods to the appropriate inside rods thereby completing the circuit around the core. Since it is important to enclose the ferrite core as completely as possible to minimize leakage inductance, four parallel sets of turns are used, and to further enclose the core, two rods, electrically in parallel, are used for the outside turns.[3] The printed circuit boards not only complete the electrical connections for the turns in a low profile (i.e., high pf) low inductance manner, they also serve to maintain the proper relative position of the rods. The overall result is a rigid, self-supporting mechanical structure with clearly defined and controlled inductances. A photo of this switch is shown in Fig. 3. With the rods touching the ferrite, this winding geometry has an 101.6 mm ID, 152.4 mm OD, and 140 mm overall length. These values in Eq. (4) gives a saturated inductance of L_1^{sat} = 566 nH. This value meets the requirements of the electrical design to within a few percent.

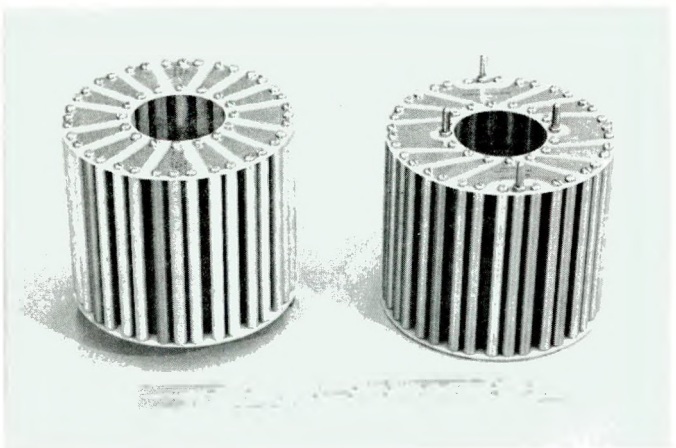

Figure 3. First stage switch.

A discussion of the first stage would not be complete without an examination of the remainder of the circuit. Obviously, the total loop inductance (excluding the switch) must be kept small. This necessitates using low inductance capacitors and compact interconnection circuits (wide parallel plates, etc.). Strontium titanate ceramic capacitors from TDK and Murata Erie satisfy the requirements for low inductance and, in addition, exhibit the required reliability. Fifteen of these 2.7 nF, 30 kV capacitors are mounted between parallel plates to get a total of 40.5 nF to form the C_o and C_1 capacitors.

Second and Third Stage Design. The design for the other stages is basically a repetition of the first stage design with appropriate consideration for losses in earlier stages, different time scales, and circuit parameters modified by reflected impedances due to the transformer. Data for frequency dependent ferrite losses are not readily available from vendors, so empirically developed values are used. The I^2R losses can be determined by measuring or calculating, for the appropriate frequencies, the winding resistance and capacitor equivalent series resistance and multiplying by the rms current as determined from the loop equations. It is important to allocate the losses appropriately. For example, all the first stage core losses will

occur just prior to saturation or when the input voltage on C_1 is at its peak, but the transfer losses (due to winding and capacitor losses) occur after saturation and will reduce the input energy to the second stage. A summary of the input and calculated values for all three stages is presented in Table 3.

Mechanical construction of the second and third stages is different from that of the first stage in that it replaces the printed circuit board with an aluminum plate and replaces the rods on the ID with concentric tubes. This rod and plate style of construction originated in LLNL's Beam Research Program and is particularly useful for high voltage 2 or 3 turn switches.[7] A photograph of the complete modulator is shown in Fig. 4.

Table 3. Input and calculated values for modulator design.

Design Parameter	1st Stage	2nd Stage	3rd Stage
Peak Charge Voltage	19 kV*	18.5 kV	67 kV
Peak Input Energy (joules)	7.22	6.83	5.68***
Input Capacitance	40 nF	40 nF	2.5 nF
Output Capacitance	40 nF	40 nF**	2.0 nF
Calculated Hold-Off Time	992 ns	324 ns	114 ns
Calculated Transfer Time	334 ns	112 ns	31 ns
Calculated Gain	3.05	3.0	3.65****
RMS current at 4.5 kHz	98 A	164 A	60.6 A
Calc. Saturated Inductance	566 nH	63 nH	89 nH
Core Parameters			
ΔB_s	0.6 Tesla	0.6 Tesla	0.6 Tesla
I.D.	101.6 mm	101.6 mm	101.6 mm
O.D.	152.4 mm	152.4 mm	152.4 mm
Height	127 mm	102 mm	127 mm
Volume (m^3)	1.29 E-3	1.03 E-3	1.29 E-3
Winding Parameters			
Number of Turns	5	2	2
I.D.	101.6 mm	101.6 mm	101.6 mm
O.D.	152.4 mm	152.4 mm	152.4 mm
Height	140 mm	108 mm	137 mm
Core Losses			
Core Dissipation (joules/m^3)	200	300	400
Core Loss (joules/pulse)	0.26	0.31	0.52
Transfer Losses			
Winding Loss (joules/pulse)	0.01	0.01	0.002
Capacitor Loss (joules/pulse)	0.08	0.22	0.34

* after inversion circuit losses
** 2.5 nF reflected to transformer primary
*** includes 0.3 joule/pulse loss in the transformer
**** gain is larger due to small value of peaking capacitor

Step-up Transformer. The transformer is configured as an auto transformer with a 1:4 step-up ratio. The core material is 18 cm^3 of unannealed (as cast) Allied 2605 S3A Metglass™ insulated with 0.3 mil Kapton™ plastic film. To keep losses and internal heat dissipation low, the total flux swing is less than 25% of the available voltseconds. The core is reset with a dc reset circuit which is described later. The previously described rod and plate construction is also used for the transformer.

Main Switch. As with most magnetic modulators, a triggered closing switch is needed. The switch requirements are given in Table 4. The initial layout uses a single thyratron for this switch and a magnetic assist is inserted between the thyratron and capacitor C_0 to reduce the anode dissipation. In operation, the thyratron voltage falls upon being triggered, but the current is delayed by the magnetic assist, thereby reducing the turn-on losses. Concurrently, plasma spreads within the thyratron allowing for more effective use of the entire cathode and increases useful operational lifetime. The magnetic assist provides approximately 200 ns of hold-off at full voltage.

The laser presents a very inductive, non-linear load to the modulator. It is not possible to efficiently couple energy into the laser while simultaneously achieving maximum light output. The result of this coupling inefficiency is that substantial energy is reflected from the load towards the modulator input causing the main switch to conduct a second current pulse. The amplitude of the second pulse varies with load parameters, but is approximately one-third of the initial pulse and has essentially the same pulse width. The time interval between the two current pulses is approximately 1 μs at full operating input voltage. The second conduction stores the reflected energy on C_0 where this energy is dissipated before the next charge pulse. The diode clipper circuit placed across C_0 dissipates the energy.

Table 4. Triggered switch requirements.

Jitter	<1 ns
Lifetime	>5000 MTBR
Operating Voltage	20 kV
Recovery Time	< 20 μs
Conduction Time	1 μs
Peak Current (1st Pulse)	≈1.3 kA
Peak Current (2nd Pulse)	≈ .4 kA delayed by ≈ 1 μs from the first current pulse
Average Current	4.8 Amperes

Charge Circuit. The very simple charge circuit for this modulator uses a saturable inductor to resonantly charge C_0. The inductor located between a 6-10 kV regulated dc power supply and the thyratron anode has approximately 70 μs of hold-off time to ensure thyratron recovery. Upon saturation, C_0 is resonantly charged to approximately 1.8 times the dc supply voltage through a series blocking diode in approximately 70 μs. During the charge cycle, the magnetic assist is reset.

Ancillary Circuits

A system requirement on the modulator is for the output pulse jitter to be less than two nanoseconds in order to be able to synchronize the light pulses of many lasers. Jitter may be broadly characterized as having two forms; pulse-to-pulse jitter and long term drift. Long term drift is due to heating of components, aging of switches, etc. and can easily be removed with low level circuitry that adjusts the timing pulse which drives the main switch trigger generator.

Pulse-to-pulse jitter in magnetic modulators has two major causes; differences in the initial voltages on capacitors and variations in ΔB_s on any of the compression stages. There are several methods for controlling or compensating for these problems.

Reset and Bias Circuit. After the discharge pulse, each magnetic core must be returned to precisely the same point on the BH curve prior to the next pulse. In order to maximize ΔB_s and minimize the required magnetic volume, the core should be reset into negative saturation. This modulator uses a dc reset circuit consisting of a current source (a voltage supply isolated with a large inductor) which couples to each of the magnetic cores with a single, noncontacting turn through the cores. The voltage induced across the core by the reset circuit drives the core into negative saturation and, once in saturation, the core is biased at this point by the H field generated by the dc current. All the stages must be held at their bias points for low jitter to be achieved. Ripple current will cause slight variations in ΔB_s but, if necessary, these can be reduced by increasing the current amplitude to bias the cores further into saturation.

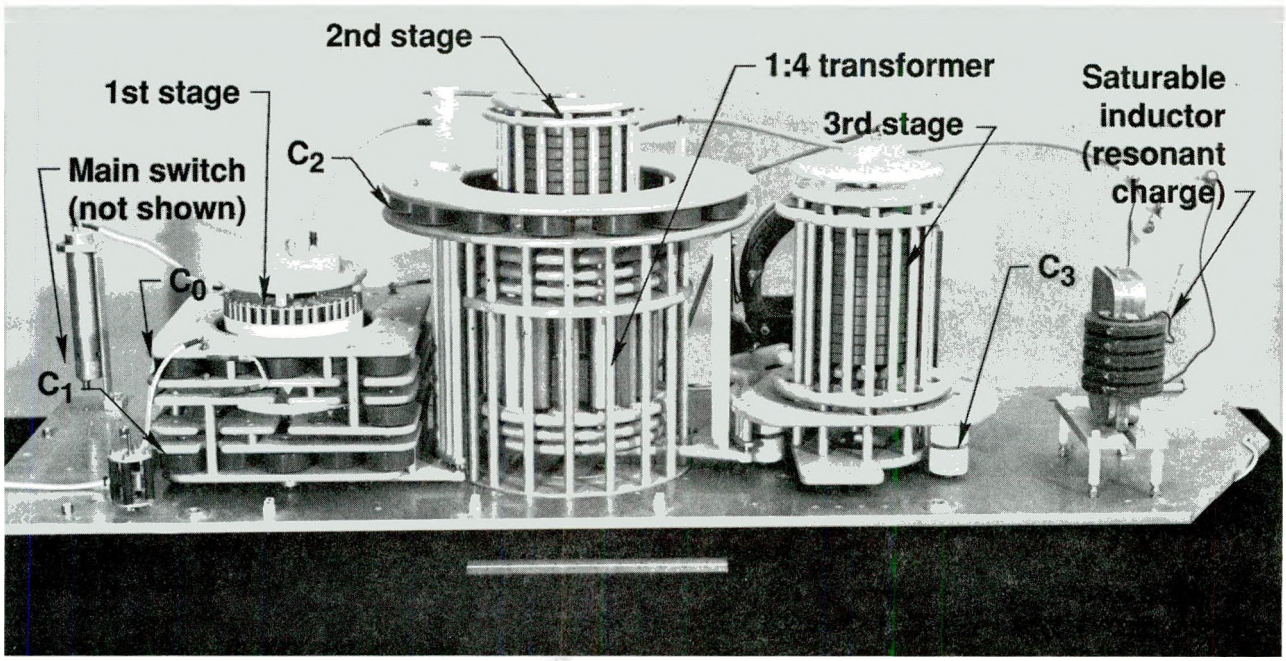

Figure 4. Modulator Assembly

Jitter Compensation Circuit. An additional result of biasing the cores is that all the capacitors, with the exception of C_o, are fully discharged during the interval between pulses and therefore have the same initial condition at the beginning of the next pulse. This is important since it eliminates the effect of voltage variation everywhere except on the input capacitor. Time jitter, Δt, due to variations in peak charge voltage, Δv, on C_o scales as shown in Eq. (6).

$$\Delta t = .5*\Delta v \ *\tau_{prop} \qquad (6)$$

where τ_{prop} is the total propagation delay through the modulator. This design has its minimum propagation delay of 1.44 μs (1 μs + 0.33 μs + 0.11 μs) at full operating voltage. If the input power supply has 1% voltage regulation and the resonant charge has a voltage step-up ratio of ≈1.8, the minimum jitter will be an unacceptable 13 ns (0.01*1.8*.5*1.44 μs). Jitter may be reduced by requiring more precise regulation on the power supply. Since the ultimate objective is to synchronize the output pulses of several modulators, a different approach involves real time adjustment of the pulse-to-pulse timing of the main switch trigger to compensate for voltage variations on C_o. This is achieved by sensing the C_o charge voltage and either advancing the timing of the trigger pulse if the charge voltage is lower than the reference voltage, or delaying the trigger pulse if the charge voltage is higher than the reference voltage. A detailed explanation of the specific circuit used for this modulator is given in a paper by J. V. Hill and D. G. Ball.[5]

Performance Data

Modulator performance is determined from voltage measurements taken at different points. These oscillographs, presented in Fig. 5, verify the calculated values for hold-off and transfer times. Losses also correlate to design with the exception of losses in the inversion circuit which are larger than expected. Overall efficiency, defined as energy delivered to the laser head divided by input energy, is approximately 60%.

The real indeterminates are reliability and lifetime. Collection of this data takes months or even years to compile meaningful lifetime data. Fortunately, one of the objectives of LDF is to accurately determine this information for all the various subsystems and components and, consequently, LDF operates continuously year round. Since operation began in 1985, approximately 45 modulators of this design have accumulated more than 950,000 hours. As component changes have been incorporated, MTBF of the modulator has steadily increased from a few hundred hours to over 2500 hours.

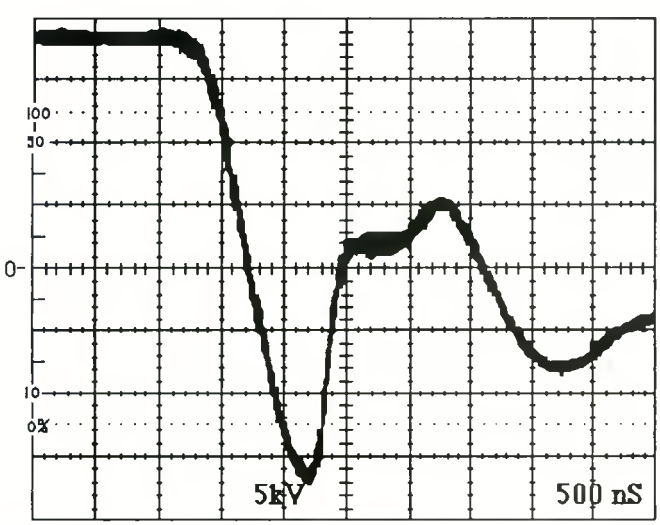

Figure 5a. Voltage on C_o - measured between magnetic assist and C_o.

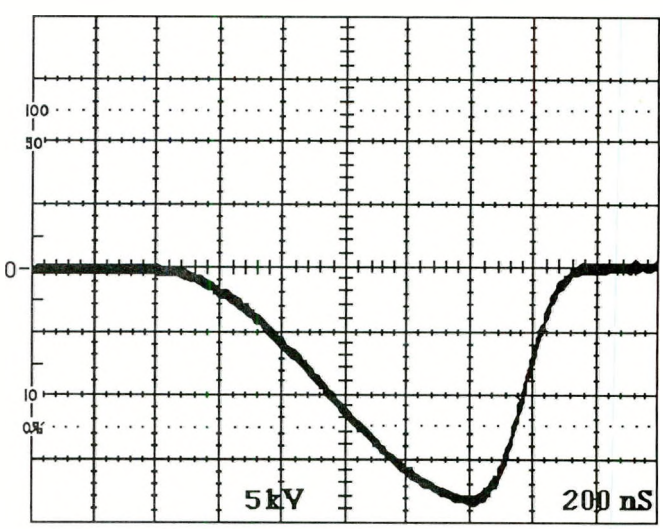

Figure 5b. Voltage on C_1.

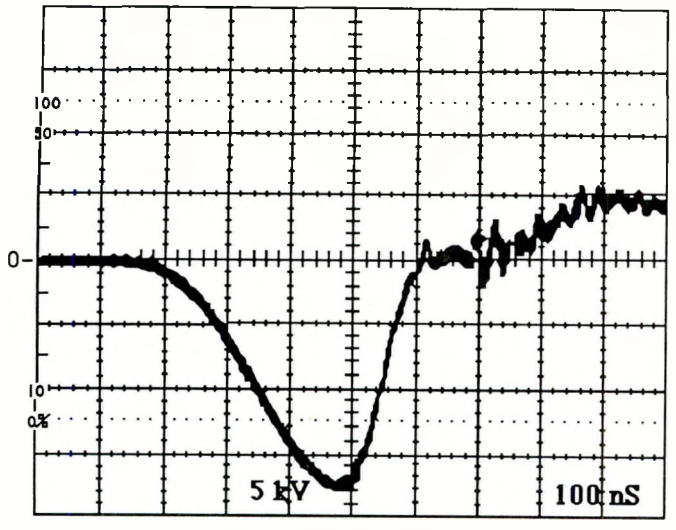

Figure 5c. Voltage on C_2.

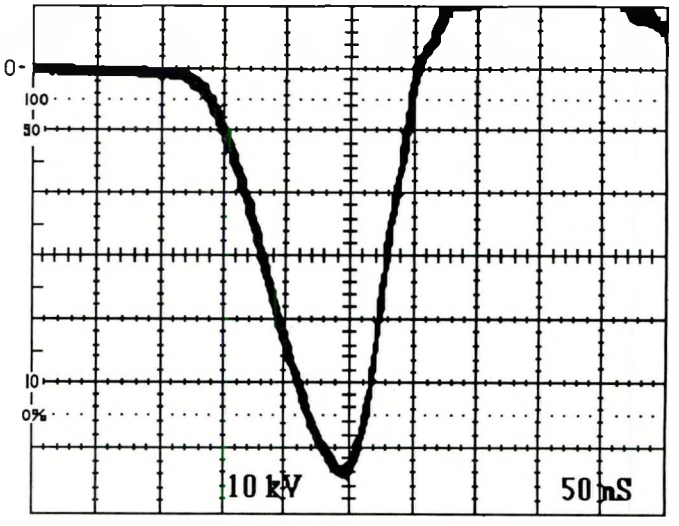

Figure 5d. Voltage on C_3.

Switch Lifetime. The main switch has always been the dominating factor which limits MTBF. Thyratrons from ITT, EG&G, and EEV and the Crossatron from Hughes have been extensively evaluated and with varying results. Although average lifetimes from these devices cover a range of ≈600 to ≈1200 hours, none of them have really met the long term requirements of the AVLIS program. Consequently, in 1987, a development program was begun to design a high voltage silicon controlled rectifier (SCR) stack to serve as a direct drop-in replacement for the thyratrons. With the SCR stack deployment which began in 1989, the MTBF has steadily increased and is now approaching 7000 hours. Details and other parameters concerning this switch are presented in a paper by G. Dreifuerst and B. Merritt.[6]

Other Component Lifetimes. Neither of the magnetic materials has demonstrated any lifetime related failure modes nor has observation revealed any degradation in performance due to mechanical vibration or exposure to the coolant. Many of the other component failures can be attributed to long term exposure to the liquid coolant, and when necessary, these components have been replaced or modified to have better coatings, seals, etc., or removed from within the tank altogether. Long term degradation of solder joints and the aluminum comprising the modulator and tank have also been observed between 10,000 and 20,000 hours.

Conclusions

Magnetic modulator circuits do in fact satisfy the promise of long life at high voltages, high average powers, and high repetition rates, while simultaneously meeting stringent requirements for jitter. In fact, the major limiting factor to long life is the main switch used to initiate pulse compression. The initial goal of extending thyratron lifetimes was achieved although not to the extent of reaching the long term programmatic goals. However, it is apparent that the programmatic goals will be satisfied by the combination of solid-state devices and magnetic compression.

Appendix

Modulator Design. Derivations of the theory of magnetic compression circuit operation and magnetic switch design have been extensively covered in other papers and will not be repeated.[2,7,8] However, certain relationships are important to consider in order to choose a circuit topology, and this requires some definition of the terminology used. Table 1 lists the terms and definitions for the toroidal based design criteria used in this paper.

One fundamental relationship, Eq. (1), defines the minimum required volume of magnetic material as a function of circuit parameters (E_{Cn}), switch parameters (gain and packing factor), and material parameters (ΔB_s and μ_r^{sat}).

$$Vol_n \approx Gain_n^2 * E_{Cn} * \pi^2 * \mu_r^{sat} * \mu_o / (4 * (\Delta B_s * pf)^2) \qquad (1)$$

Eq. (1) shows that core losses, which are directly proportional to the core volume, are a strong function of switch gain. This indicates that multiple switches are usually preferable to a single stage of compression having high gain. Obviously, core losses alone should not be used to determine system design as other loss mechanisms such as resistive losses in conductors and dielectric losses in capacitors are a significant portion of total circuit losses.

The packing factor (pf) also significantly effects core volume meaning that an efficient core design requires careful consideration of the magnetic fields surrounding the magnetic core. This requires that the windings must be tightly coupled to the core regardless of the choice of core material.

Magnetic Material Selection. Experience has shown that reasonable values for gain range between 3 and 10 depending on the choice of magnetic material. Switch designs with a compression gain near the lower limit of this range usually utilize ferrite materials and designs at the upper limits usually utilize metal tapes and, in particular, the amorphous metal tapes. However, gain is only one consideration in selecting a core material. Specific cooling requirements, size and weight limitations, mechanical packaging (particularly at high voltage), and the required efficiency affect the material choice.

The NiZn class of ferrites was chosen for this specific application for several reasons. These ferrites have a dc volume resistivity of 10^6-10^{10} ohm-cm which allows the turns of the windings to be in direct contact with the ferrite thereby maintaining a high packing factor and also simplifying the mechanical packaging. Although the available ΔB is relatively low (0.5-0.75 tesla) and a larger volume of material is required, this also gives more surface area for cooling. Adequately cooling the magnetic core is a serious requirement for long life at 4.5 kHz and submicrosecond saturation times. Together, all these factors gave confidence that development and design time would be short.

The reader should note that there are no fundamental limitations which prevent amorphous materials or other metal tapes from being used in this application, but their use requires stringent attention to packaging and cooling. Schedule constraints did not allow the anticipated development time that solving these problems would have required.

Table 1. Definition of terms.

Term	Definition	Units
Vol_n	minimum magnetic core volume of L_n	m^3
A_n	magnetic cross-sectional area of L_n	$meters^2$
OD	outer diameter of magnetic core (toroid)	meters
ID	inner diameter of magnetic core (toroid)	meters
ΔB_s	useable change in core flux density	tesla
N_n	number of turns on the L_n winding	
w_n	axial length of L_n winding	meters
pf	packing factor - cross-section area of magnetic material divided by total area enclosed by windings	
L_n	the n^{th} stage of magnetic compression	
$L_n sat$	saturated inductance of L_n	henries
$Gain_n$	ratio of charge to discharge time for L_n	
C_n	capacitance at the input of L_n	
E_{Cn}	per pulse energy stored on C_n	joules
$<V_{Cn}>$	average charge voltage on capacitor C_n	volts
$\tau_{Cn} chg$	time required for capacitor C_n to charge to peak voltage	seconds
τ_{Ln} sat	hold-off time - time required to saturate L_n at a given average charge voltage	seconds
τ_{prop}	total propagation delay through the modulator - equal to the sum of the hold-off times of all the stages	seconds
μ_o	free space permeability $= 4\pi * 10^{-7}$	henries/m
μ_r	relative permeability	
$\mu_r sat$	saturated value of relative permeability	
Δt	time jitter	seconds
Δv	pulse-to-pulse variations in peak charge voltage	volts

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