#27
5/8/80

SAND79-1700
Unlimited Release

MASTER

A Microprocessor-Controlled Tester for Evaluation of the Self-Energized Credential System (SECS)

Norman E. Corlis

SF 2900-Q(3-80)

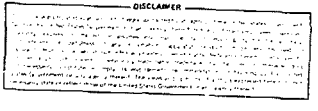
SAND79-1700
Unlimited Release
Printed March 1980

A MICROPROCESSOR-CONTROLLED TESTER FOR EVALUATION OF THE SELF-ENERGIZED CREDENTIAL SYSTEM (SECS)

Norman E. Corlis
TM Advanced Development Division 1584
Sandia Laboratories
Albuquerque, NM 87185

ABSTRACT

The Self-Energized Credential System (SECS) was developed for use in the Plutonium Protection System (PPS) installed at Hanford, Washington. Evaluation and development of the SECS system was enhanced by the use of a microprocessor-controlled portal tester. This tester used infrared (IR) beam sensors to provide information on the direction of travel of the credential wearer and to detect inoperative credentials. A printed record of the portal number, actual code read, time, and direction of the credential passage provided information essential to an assessment of the operability of the SECS.



ACKNOWLEDGMENT

The circuit designs and technical advice provided by David E. Barnes, Harold O. Jeske, and John P. Watterberg, all of Division 1584, contributed greatly to the success of this project.

CONTENTS

ILLUSTRATIONS

A MICROPROCESSOR-CONTROLLED TESTER FOR EVALUATION OF THE SELF-ENERGIZED CREDENTIAL SYSTEM (SECS)

Microprocessor Portal Tester

The Microprocessor Portal Tester (Figure 1) was designed to assist in the evaluation of the electronic Self-Energized Credential System[1] (SECS) that was developed for use in the Plutonium Protection System[2] (PPS) installed at Hanford, WA. The tester is augmented by infrared (IR) beam-breaker sensors which detect a person passing through the portal. Logic within the tester determines the direction of the passage.

In a typical operational sequence, entrance of a person into the portal activates one of the IR sensors. Once within the effective detection area volume of the portal, the personnel-borne credential is activated and its unique code is detected by the portal electronics. This code is then processed by the microprocessor tester, resulting in a listing of the following data:

Correct access code
Actual code read
Portal number
Current time
Direction of credential passage

Two other SECS parameters are also checked by the status logic of the tester. The 110-kHz portal-reference signal is detected to provide an indication of "power up" and the AGC output from the decoder circuit indicates whether the credential transmitted a coded response. The undetected presence of these two parameters is printed out as "NOT UP" and "NO AGC" by the microprocessor.

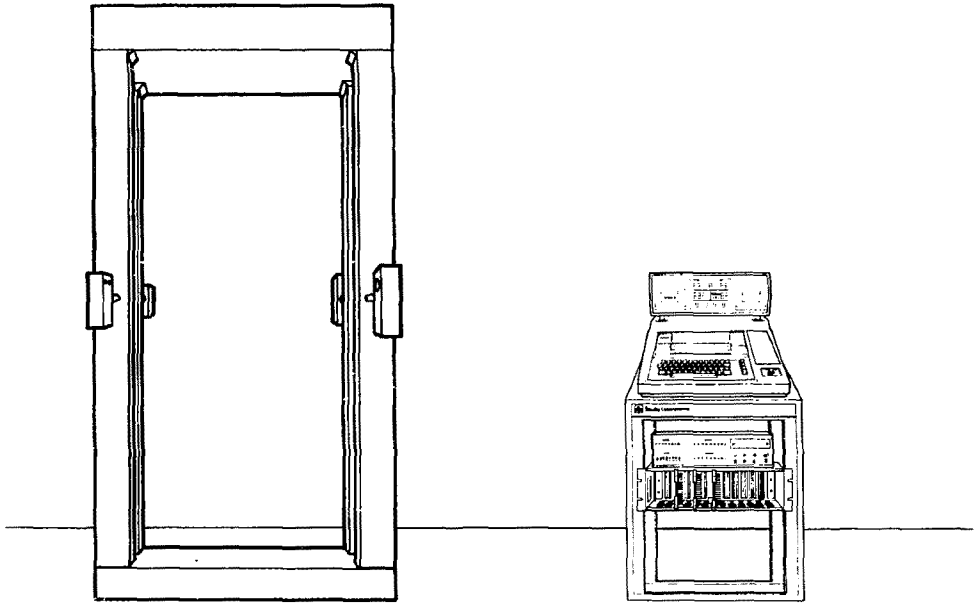


Figure 1. Portal Test Layout

As a result of the above determinations, a thorough monitoring of critical SECS parameters is obtained and a printed record of each passage through the portal is provided. Appendix A contains an example of a typical code printout.

Theory of Operation

The main block elements of the portal system are shown in Figure 2 and are described in greater detail block by block.

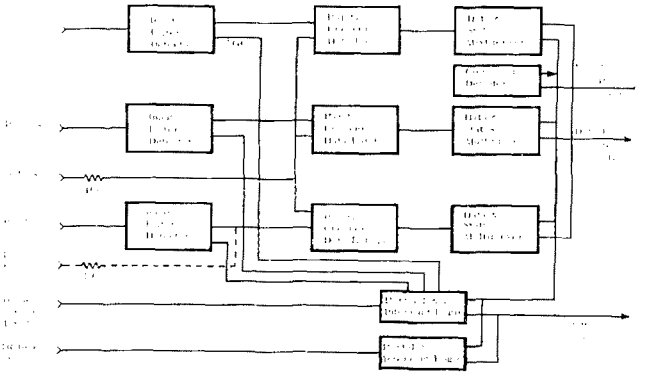


Figure 2. Block Diagram of Portal System

Input Filter and Detector

The input filter and detector (Figure 2) is comprised of two main parts: a passive filter and a peak detector. The passive input filter has a center frequency of 56 kHz with an approximate bandwidth of 2 kHz, followed by an amplifier with a gain of 40 dB. A two-pole filter follows the amplifier for additional selectivity. The code is demodulated by a peak detector controling the threshold of a clipper which is one-half of the input amplitude. From the clipper, a signal is sent to a one-shot (multivibrator) to retime the data. The one-shot is locked out if the input amplitude is below a selected level to preclude false triggering by noise signals at the input. The circuitry diagram is shown in Figure 3.

Code and Parity Discriminator

Once the input signal is filtered and the amplitude variations are removed, the data are fed to the Code and Parity Discriminator (Figure 2). A serial shift register tests the code for the correct parity and two consecutive code words for identical patterns. Two 12-bit parity integrated circuits (IC) (Figure 4) are used to test the code for odd parity and a 16-bit comparator checks two 24-bit code words for identical bit patterns. If both conditions are met, a data latch stores the 16-bit data word and a "data valid" signal is generated. A data valid pulse is generated for each correct frame and resets a six-bit binary clock counter. If a data valid pulse is missing for more than 64 clock periods, the counter resets the data latches. Therefore, the data valid signal must drop out for at least 37 ms before another valid code can be read.

Tester Clock and Control

The clock for the tester is developed by dividing the 110-kHz portal-reference (REF) signal by 64. The divide-by-64 counter (Figure 5) is reset on the positive side of the data signal to align the edges of the clock and data signals. The data valid signal is used to latch the credential code into the data register and to set the host computer interrupt. However, the computer interrupt is not used in this application because the microprocessor polls the input/output (I/O) signals from the IR beam sensors to detect the interruption of the beams.

This technique permits the detection of both a nonoperating credential and a person not wearing a credential. The IR beam logic is locked out after both beams are broken until the microprocessor resets the logic; the data valid signal then drops out and both beams are set to the normal state. This precludes the possibility of reading the credential a second time while it is still in the fringes of the portal's magnetic field.

Three eight-bit ports on the Fairchild F8 microprocessor are used to interface the microprocessor and the portal tester. The status bus on port 0 of the microprocessor receives the nine-bit status word from the tester in two bytes. Port 1 transmits signals from the microprocessor to the tester for status byte control while Port 5 passes the tester's data word in two eight-bit bytes to the microprocessor.

Interrupt Logic - Standard

This circuit (Figure 6) is designed to provide a computer interrupt from the operation of the IR beam sensors. The interruption of the first beam causes the logic to generate signals to turn on a video camera and the portal loop power amplifier, if the system is so configured. As the credential enters the magnetic field of the portal, the credential's internal circuits are activated and its code is read by the receiving circuits and latched in the data register. When the second beam is broken, a computer interrupt is generated. The direction of the person passing through the portal is determined by which beam is broken first. After the computer has read the data register and the direction code, the logic is reset. If the second beam is not broken within 10 s, an internal reset is generated. The system start up procedure for the credential is detailed in Appendix B.

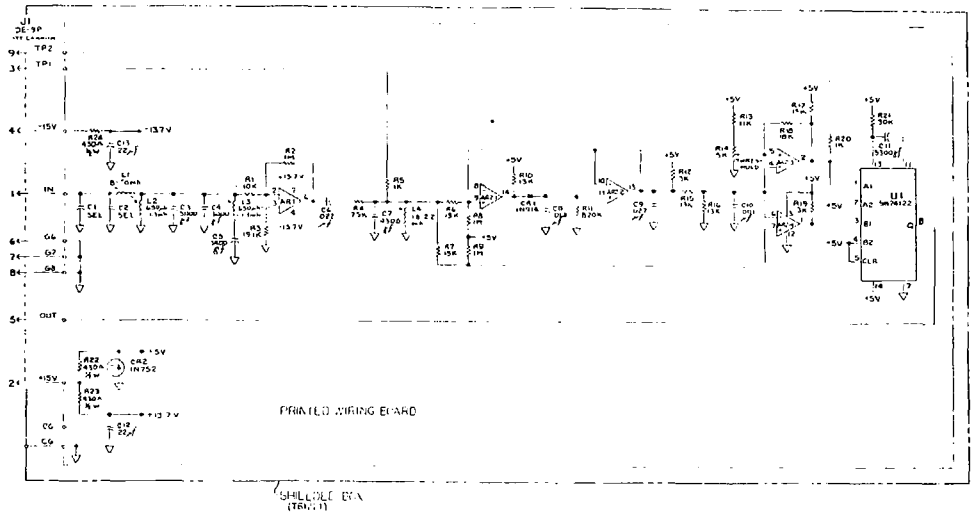


Figure 3. Input Filter and Detector Schematic

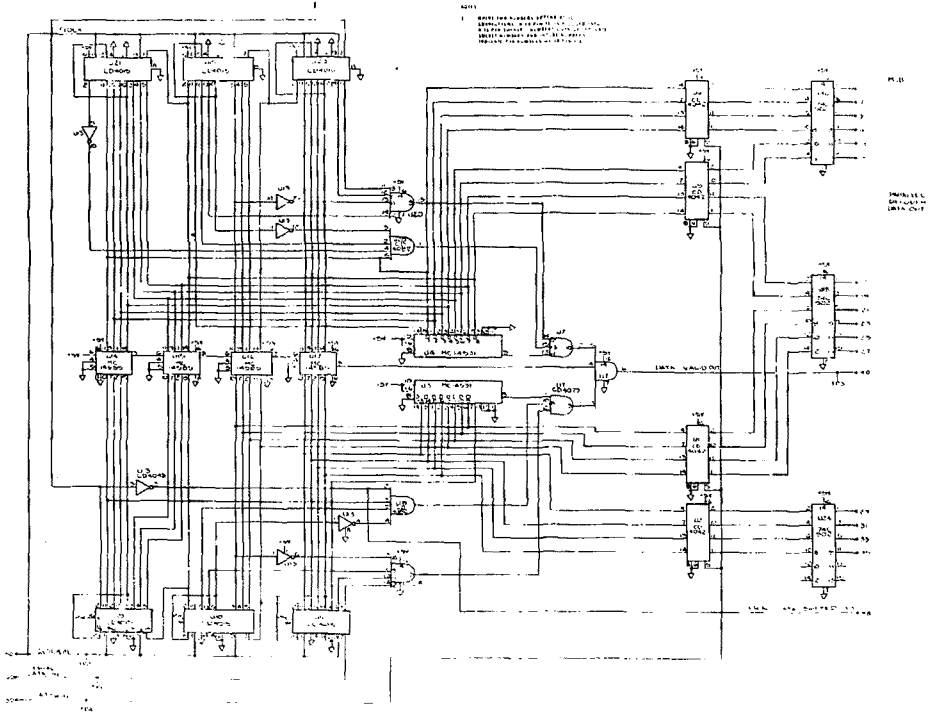


Figure 4. Code Discriminator Schematic

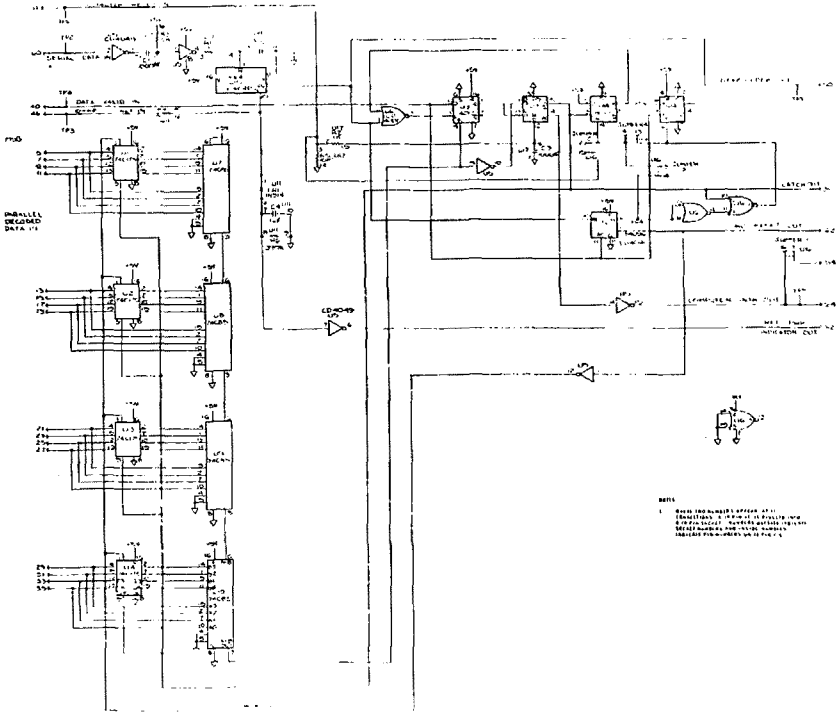


Figure 5. Tester Clock and Control Schematic

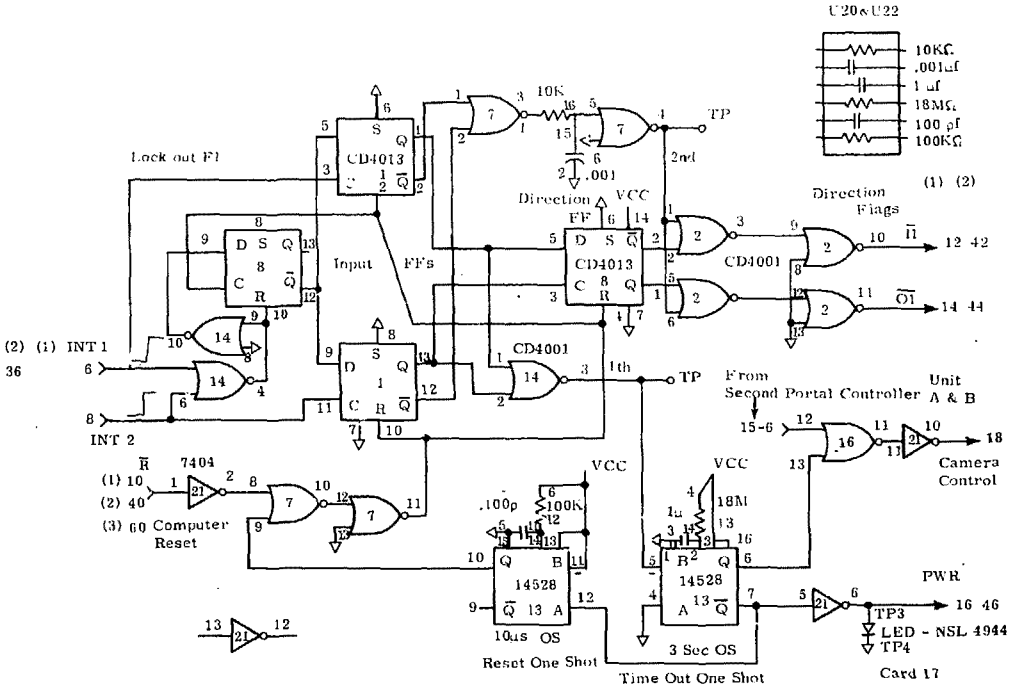


Figure 6. Schematic of Standard Interrupt Logic

Interrupt Logic - Hanford Modification

The first Hanford portal used pressure-sensitive pads to detect a person passing through the portal. These pads produced multiple switch closures as the person walked on the pads. The signals from the pads were filtered by a special IC (MC14490) which produced an output four clock periods after an input signal goes low. A logic circuit was added to prevent multiple computer interrupts from being generated during the passage of one person.

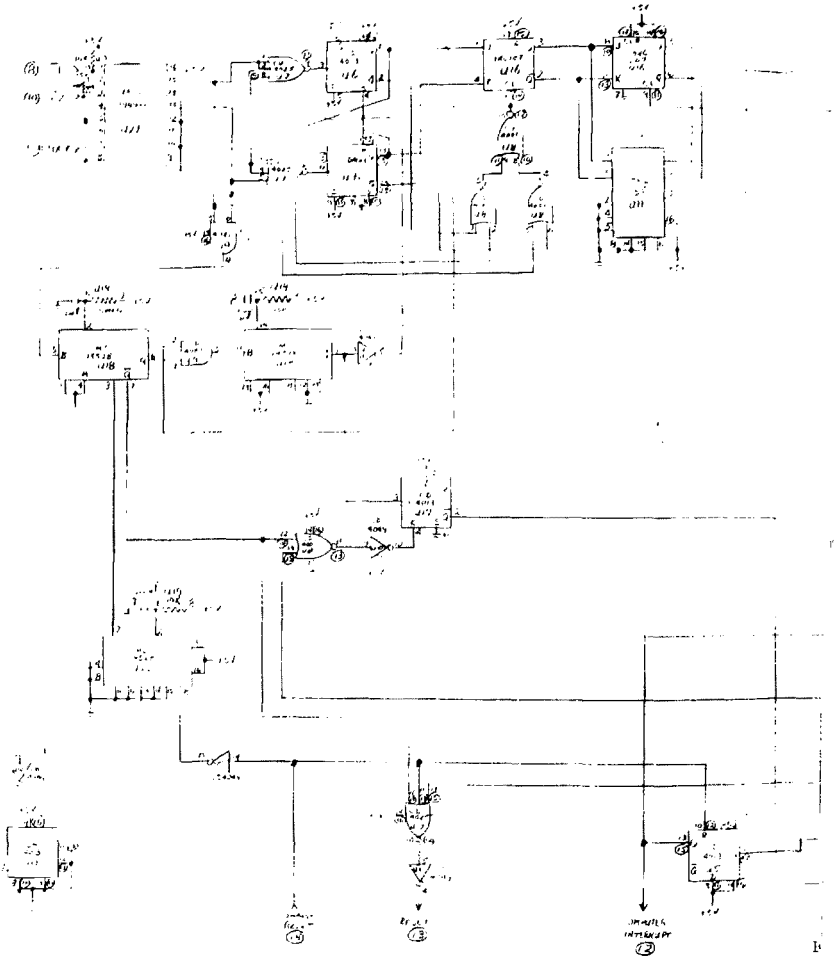
The direction of the person passing through the portal is determined by which switch signal occurs first. When the credential is energized by the portal's magnetic field, the credential's code is read and stored. When the second sensor is activated, an interrupt is generated for the computer which then reads the code, the direction code, and reset the interrupt logic.

System constraints for computer interruption are as follows:

1. Both switches must be activated in less than 10 s
2. The direction of passage must be different or the code must be different from the last stored code
3. The data must be valid.

If only one switch is activated within 10 s, an internal reset is generated.

The complete interrupt logic is shown in Figure 7.



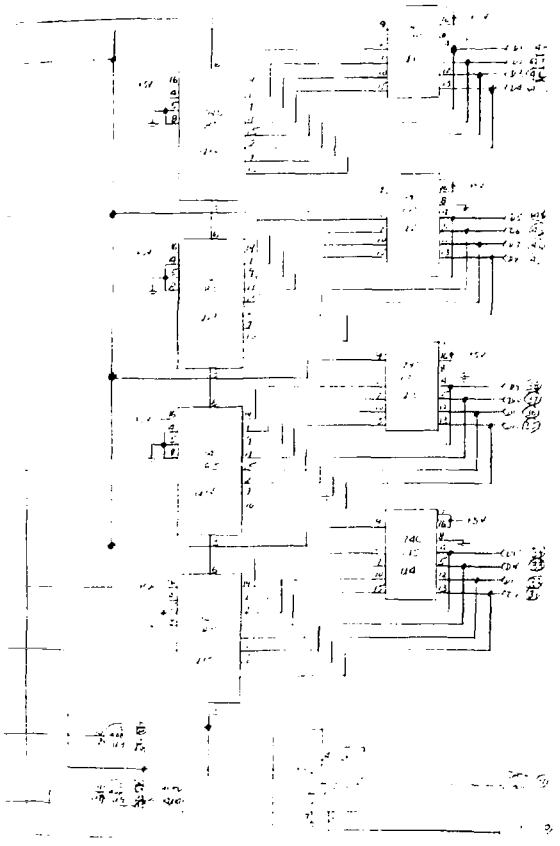


Figure 7. Schematic of Hanford Modification of Interface Logic

Credential Format

The data from the credential are transmitted serially at 1.7-kbits/s in an asynchronous mode. The format has start and stop bits to identify the coded word and a parity bit for error detection. Eight bits of data are included in each 12-bit word, so two 12-bit byte words are transmitted for the full 16-bit code word. The bytes are transmitted continuously as long as the code module is powered. Figure 8 shows the code format, Byte 1.

START	MSB 1	X	X	X	X	X	X	X	Parity	STOP	STOP
Byte 2											
START	0	X	X	X	X	X	X	X	Parity	STOP	STOP

Figure 8. Code Format

The first bit (MSB) in the code word is defined as a "one" while the ninth bit is set to a "zero". Therefore, only 14 bits are variable. This restricts the number of unique code words to approximately 2^{14} minus some ambiguous code words for a net of 16,192 available codes. The time rates are as follows:

Baud rate	1.718 kbps
24-bit word rate	14 ms
Valid code rate	14 ms
First data bit to valid code	18-42 ms
Min time between valid codes	37 ms

Microprocessor

The Fairchild F8 microprocessor was selected for this project. The F8 is a very good "controller" microprocessor with four eight-bit ports and an internal timer which can be used as a clock. There is a cross assembler on the Sandia network operating system (NOS) for software development. However, without an F8 emulator, the machine code must be off-loaded onto a magnetic tape (TI 733 terminal) and then loaded into the microprocessor for each program iteration. Since the F8 has semiconductor memory for RAM, the program has to be loaded after each power loss.

The F8 development board was modified (Figure 9) to adapt it to a 300 baud rate, TI 733 data terminal which has a hard copy printer for output and two magnetic tape machines (Appendix C). The F8 machine code is recorded on magnetic tape and then loaded into the microprocessor for system startup. The development board has a 1-k RAM memory which is more than sufficient for the operating system. The last 26 words in the RAM memory cannot be used for program storage because the board has FAIRBUG monitor routines in a special ROM that uses that portion of the memory and will overwrite those locations.

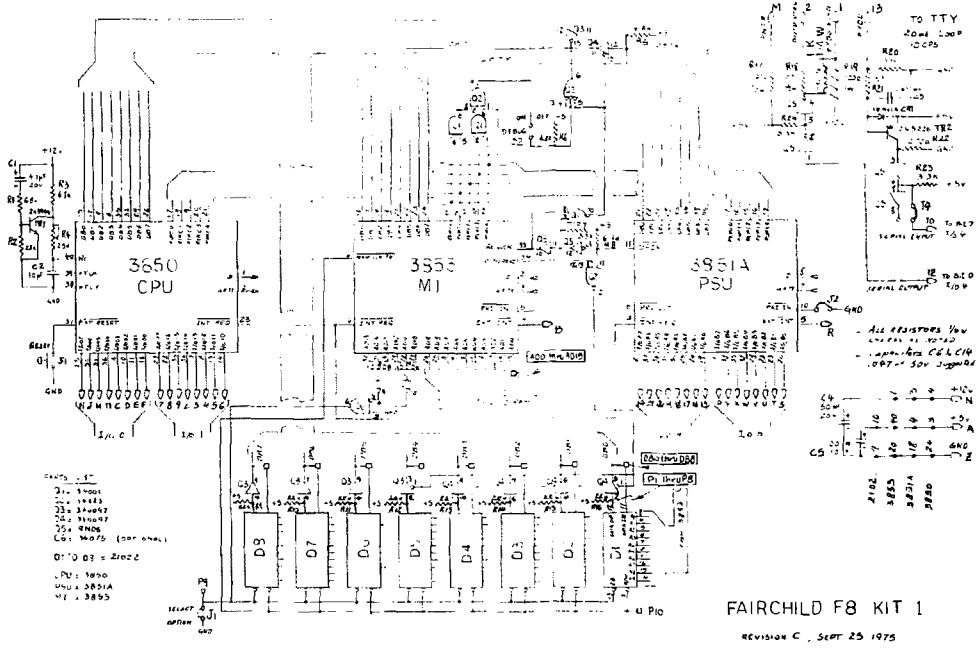


Figure 9. Modified F8 Kit 1 Schematic

IR Beam Sensor Location

The optimum height for the IR sensors was found by experimentation to be approximately 110 cm. This height reduces the possibility of the swinging arms of a person breaking the beam first and too soon. The horizontal distance of each sensor should be 50 cm from the center line of the portal, one pair on each entry/exit. The dimensions permit the credential to be in the primary portion of the magnetic field before the beam is broken and allows the code to be read. The sensors should not be mounted on the portal due to undesirable electromagnetic pickup of the portal field, and shielded-twisted pair cable should be used to connect the sensors to the control chassis. An external support structure must be provided on both sides so that the pairs of sensors can be positioned to face each other. These particular sensors have a conical sensing angle of $\pm 10°$, so the adjustment of the sensors is not critical. There is a LED indicator light in the receiver sensor which may be used for alignment. The LED is normally ON and should go off when the IF beam is interrupted. Appendix D contains schematics of the IR sensor.

References

1. David E. Barnes et al, Self-Energized Credential System, SAND76-0540 (Albuquerque: Sandia Laboratories, December 1976).

2. Thurlow W. H. Caffey and David E. Barnes, The Self-Energized Credential System for the Plutonium Protection System, SAND78-2156 (Albuquerque: Sandia Laboratories, January 1979).

APPENDIX A

Program Software Code

```
        TITLE   'REAL TIME CLOCK'
        ORG H'30'
INTR    IC 4
        BNZ OUT
        LI 250      INC TO SLOW DOWN CLOCK
        LR 4,A
        LIS 1
        AI H'66'
        AIS 8
        LR 8,A      STORE DECS
        CI H'60'    TEST FOR 60
        BC T5
        CLR
OUT     EI
        POP
T5      JMP T10
*
*
*       START ROUTINE
*
INTR    LI H'84'
        LR 0,A      LOAD DELAY CNTER
        LIS 0
        LR 8,A
        DCI H'83D6'   CR/LF
        LIS 5
        LR 4,A
        LIS 0
DEL1    PI H'83E5'    DELAY
        DS 4
        BNZ DEL1
        LIS 13
        LR 4,A
        DCI MSG1
OPT1    PI H'83E5'    PRINT 'INPUT HOURS'
        DS 4
        LM
        LR 1,A
        BNZ OPT1      RET
        DCI H'83AD'
        LR 0,DC       LOAD 0 REG
IN1     PI H'837B'    INPUT HOURS
        DCI HOUR
        ST
        LR QL,A
        PI H'80EB'    ECHO HOURS
        PI H'83D6'    CR/LF
        LIS 5
        LR 4,A
        LIS 0
```

```
DEL2  PI H'83E5'    DELAY
      DS 4
      BNZ DEL2
      LIS 14
      LR 4,A
      DCI MSG2
OPT2  PI H'83E5'
      DS 4
      LM
      LR 1,A
      BNZ OPT2    PRINT 'INPUT MIN'
      DCI H'83AD'
      LR 0,DC
IN2   PI H'837B'    INPUT MIN
      DCI MIN
      ST
      LR QL,A
      PI H'80EB'    ECHO MIN
      PI H'83D6'    CR/LF
      LIS 5
      LR 4,A
      LIS 0
DEL3  PI H'83E5'    DELAY
      DS 4
      BNZ DEL3
      LIS 12
      LR 4,A
      DCI MSG3
OPT3  PI H'83E5'
      DS 4
      LM              PRINT GO TO START
      LR 1,A
      BNZ OPT3
      DCI H'83AD'
      LR 0,DC
IN3   PI H'837B'
      PI H'83D6'      CR/LF
*         START SECOND COUNTER
      LI 253
      LR 4,A          LOAD TIMER
      LI H'7F'        CLEAR TIMER
      OUTS 7
      LIS 3           START TIMER
      OUTS 6
      EI              ENABLE INTERUPTS
      JMP H'110'      JMP TO DAVID ROUTINE
*       MINUTES   COUNTER
```

```
T10   LIS 0
      LR 8,A
      LIS 1
      AI H'66'
      DCI MIN
      AMD
      DCI MIN
      ST
      CI H'60'
      BC T20          JMP TO HOURS CNTER
      CLR
      EI
      POP
*       HOURS COUNTER
T20   LIS 0
      DCI MIN       CLEAR MIN CNTER
      ST
      LI 153        CORRECT .3925 HOUR
      LR 4,A
      LIS 1
      AI H'66'
      DCI HOUR
      AMD
      DCI HOUR
      ST
      CI H'24'
      BNC T30
      CLR
      DCI HOUR
      ST
T30   EI
      POP
*
*
MSG1  DC 6*C'INPUT '
      DC 6*C'HOURS '
MSG2  DC 6*C'INPUT '
      DC 7*C'MINUTE '
MSG3  DC 5*C'GO TO
      DC 6*C' START'
HOUR  EQU H'3E4'
MIN   EQU H'3E5'
      END
```

```
        TITLE SEC3 EVALUATION
        ORG H'110'
        CLR
        DCI CNT1
        ST
        ST
        ST
        ST
        ST
        JMP BEGIN
IDS     DC 2,H'DC0D'
        DC 2,H'DB01'
        DC 2,H'B861'
        DC 2,H'9777'
        DC 2,H'D268'
        DC 2,H'9207'
        DC 2,H'8920'
        DC 2,H'8008'
        DC 2,H'CD11'
        DC 2,H'8108'
        DC 2,H'CE4A'
        DC 2,H'9117'
        DC 2,H'AE01'
        DC 2,H'AB1D'
        DC 2,H'AC1B'
        DC 2,H'AB01'
        DC 2,H'AB02'
        DC 2,H'AB03'
        DC 2,H'AB04'
        DC 2,H'B268'
        DC 2,H'B468'
        DC 2,H'D468'
BEGIN CLR
        EI
        OUTS 0
        OUTS 1
        OUTS 5
WAIT    INS 0       LOOK FOR DOOR ACTIVATION
        BZ WAIT
        DI
        NI H'40'    CHECK B6 FOR 1 (ACTIVATION TOTAL OUT)
        BZ CTD
        JMP CNTD
CTD     INS 0
        NI H'03'    CHECK FOR PORTAL 1 ACTIVATION
        BNZ STA1
        INS 0
        NI H'0C'     CHECK FOR PORTAL 2 ACTIVATION
        BNZ STA2
        INS 0
        NI H'30'  CHECK FOR PORTAL 3 ACTIVATION
        BNZ STA3
        BR BEGIN
```

```
STA1   DCI IO      STORE IN OR OUT DATA
       ST
       LIS 1
       ST          PORTAL 1 STORED
       LI H'11'
       ST          STAT CONTAINS RESET ON B4 AND PORTAL ADDRESS
       BR CNT
STA2   IR 1
       DR 1
       DCI IO      STORE IN OR OUT DATA
       ST
       LIS 2
       ST          STORE PORTAL 2
       LI H'23'
       ST          STORE RESET ON B5 AND STORE PORTAL ADDRESS
       BR CNT
STA3   IR 4
       DCI IO      STORE IN OR OUT DATA
       ST
       LIS 3
       ST          STORE PORTAL 3
       LI H'45'
       ST          STORE RESET ON B6 AND PORTAL ADDRESS
CNT    NI 7       BLANKS RESET BITS
       OUTS 1      ADDRESS PORTAL BEING ACTIVATED
       INS 0
       NI 04
       BNZ ER1     CHECK FOR FIELD POWER
       PI RES
       JMP ERR1
ER1    INS 0
       NI 08       CHECK FOR AGC
       BNZ ER2
       PI RES
       JMP ERR2
ER2    INS 0
       NI H'10'      CHECK FOR DATA VALID
       BNZ ER3
       PI RES
       JMP ERR3
```

```
ER3   LI H'18'
      LR 7,A      SET R7 TO NUMBER OF STORED I.D.'S
      INS 5
      LR 8,A       LOAD FIRST BYTE OF ID
      DCI ID1
      ST
      DCI STAT
      LM
      NI 07
      INC
      OUTS 1
      INS 5
      LR 5,A      LOAD SECOND BYTE OF ID
      DCI ID2
      ST
      PI PES
      DCI IDI     SET DC TO BEGINNING OF STORED ID ARRAY
CK    LR A,2
      CM          COMPARE FIRST BYTE ID WITH STORED ID
      BZ CK2
      CM
      DS 7
      BNZ CK
      PI PES
      JMP ERR4
CK2   LR A,3
      CM
      BNZ VAD     COMPARE SECOND BYTE ID WITH STORED ID
      JMP VAID
VAD   DS 7
      BNZ CK
      PI PES
      JMP ERR4
CNTO  PI H'83D6'
      PI H'83D6' ROUTINE OUTPUTS NUMBER OF TRANSACTIONS AND
      PI DEL
      LIS 7       BREAKDOWN OF TYPES OF TRANSACTIONS
      LR 8,A
      DCI MSG2
      PI TYPE
      DCI CNT1
      PI H'80E9'
      PI H'83D6'
      PI DEL
      LIS 7
      LR 8,A
      DCI MSG3
      PI TYPE
      DCI CNT2
      PI H'80E9'
      PI H'83D6'
      PI DEL
      LIS 6
```

```
        LR 3,A
        DCI MSG5
        PI TYPE
        DCI CNT3
        PI H'80E9'
        PI H'83D6'
        PI DEL
        LIS 3
        LR 3,A
        DCI MSG4
        PI TYPE
        DCI CNT4
        PI H'80E9'
        PI H'83D6'
        PI DEL
        LIS 4
        LR 3,A
        DCI MSG5
        PI TYPE
        DCI CNT5
        PI H'80E9'
        PI H'83D6'
        PI DEL
        JMP OPT
ERR1    PI H'83D6'
        PI DEL
        LIS 7           OUTPUTS MESSAGE OF FIELD FAILURE
        LR 3,A
        DCI MSG6
        PI TYPE
        DCI CNT1
        LM
        INC
        DCI CNT1
        ST
        JMP OPD
ERR2    PI H'83D6'      OUTPUTS MESSAGE OF NO AGC
        PI DEL
        LIS 7
        LR 3,A
        DCI MSG7
        PI TYPE
        DCI CNT2
        LM
        INC
        DCI CNT2
        ST
        JMP OPD
```

```
ERR3  PI H'83D6'      OUTPUTS MESSAGE OF NO VALID ID
      PI DEL
      LIS 6
      LR 3,A
      DCI MSG8
      PI TYPE
      DCI CNT3
      LM
      INC
      DCI CNT3
      ST
      JMP OPD
ERR4  PI H'83D6'      OUTPUTS MESSAGE OF UNAUTHORIZED ID
      PI DEL
      LIS 4
      LR 3,A
      DCI MSG9
      PI TYPE
      DCI CNT4
      LM
      INC
      DCI CNT4
      ST
      DCI ID1
      PI H'80E9'
      DCI ID2
      PI H'80E9'
      JMP OPD
VAID  PI H'83D6'      OUTPUTS MESSAGE OF AUTHORIZED ID
      LIS 7
      LR 1,A
      PI H'83E5'      RING BELL
      PI DEL
      LIS 4
      LR 3,A
      DCI MSGA
      PI TYPE
      DCI CNT5
      LM
      INC
      DCI CNT5
      ST
      DCI ID1
      PI H'80E9'
      DCI ID2
      PI H'80E9'
      BR OPD
RES   DCI STAT
      LM
      NI H'70'
      OUTS 1          RESET LATCH
      CLR
      OUTS 1
      POP
```

```
OPD   DCI MSG8       OUTPUTS PORTAL NUMBER,TIME OF DAY,
      LIS 8          AND WHETHER IN OR OUT
      LR 3,A
      PI TYPE
      DCI DOOR
      PI H'80E9'
      DCI MSG0
      LIS 1
      LR 3,A
      PI TYPE
OPT   DCI SEC
      LR A,8
      CI
      DCI HOUR
      PI H'80E9'
      LIS 1
      DCI MSGH
      LR 3,A
      PI TYPE
      DCI MIN
      PI H'80E9'
      LIS 1
      DCI MSGH
      LR 3,A
      PI TYPE
      DCI SEC
      PI H'80E9'
      DCI IO
      LIS 1
      CM
      BNZ CM2
      DCI MSGD
      LIS 3
      LR 3,A
      PI TYPE
N     JMP BEGIN
CM2   DCI ID
      LIS 2
      CM
      BNZ CM3
      DCI MSGE
      LIS 4
      LR 3,A
      PI TYPE
      JMP BEGIN
CM3   DCI MSGF
      LIS 9
      LR 3,A
      PI TYPE
      JMP BEGIN
```

```
TYPE  LR K,P
      LR A,KU
      LR 7,A
      LR A,KL
      LR 5,A
TY    LM                    TYPES OUTPUT MESSAGE
      LR 1,A
      PI H'83E5'
      DS 3
      BNZ TY
      LR A,7
      LR KU,A
      LR A,5
      LR KL,A
      LR P,K
      POP
DEL   LR K,P          DELAY 5 CHARS
      LIS 5
      LR 6,A
      LIS 0
      LR 1,A
CDD   PI H'83E5'
      DS 6
      BNZ CDD
      PK
MSG2  DC 7*C'NOT UP='
MSG3  DC 7*C'NO AGC='
MSG4  DC 3*C'NO='
MSG5  DC 4*C'YES='
MSG6  DC 7*C'NOT UP-'     '
MSG7  DC 7*C'NO AGC-'
MSG8  DC 6*C'INVAL-'
MSG9  DC 4*C'NO--'
MSGA  DC 4*C'YES-'
MSGB  DC 2*C'-P'
MSGC  DC 1*C' '
MSGD  DC 3*C' IN'
MSGE  DC 4*C' OUT'
MSGF  DC 8*C' NOT COMP'
MSG6  DC 6*C'INVAL='
MSGH  DC 1*C':'
IO    EQU H'3E1'
DOOR  EQU H'3E2'
CNTT  EQU H'3DA'
CNT1  EQU H'3DB'
CNT2  EQU H'3DC'
CNT3  EQU H'3DD'
CNT4  EQU H'3DE'
CNT5  EQU H'3DF'
STAT  EQU H'3E3'
ID1   EQU H'3D8'
ID2   EQU H'3D9'
HOUR  EQU H'3E4'
MIN   EQU H'3E5'
SEC   EQU H'3E6'
      END
```

APPENDIX B

System Start-Up Procedure for the Credential Reader

APPENDIX B

System Start-Up Procedure for the Credential Reader

NOTES

(1) All bit switches on the front panel of the microprocessor (μP) must be in either the MID or HI Z position.

(2) The REF IN BNC is common to all three decoders.

(3) Two interrupt modules (P1 and P2 on card 17) are wired for positive going signals from the IR beam sensors. The third module (P3 on card 19) requires negative going signals.

Loading Procedure from Magnetic Tape in the T1733:

Insert tape

Rewind - load forward

Reset μP

Key in "L" and "RET"

μP will load first program

Reset μP

Key in "L" and "RET"

The second program will be loaded

Rewind tape

Key in "G35" for the start of the routine

Figure B-1 is a copy of an operating system hard copy record. The μP will respond with "Input hours". Two numeral characters, including leading zeros, must be keyed in and no "RET" is required. The μP will print the numeral characters and then "Input minutes". Two characters must be keyed in and the μP will print the characters and then "Go to Start". Keying in any two characters will start the internal clock and set the interrupt enables. When an interrupt from the beam sensors is detected, the μP will print:

YES or NO for an authorized code
The actual code read - four hexadecimal characters
The number of the portal - P01, P02, P03
The current time - hours, minutes, seconds
The direction of passage - IN or OUT

The time clock in the system is a count-down software divider from a RC oscillator, so it will not be very accurate.

The RC oscillator on the μP PC board should be adjusted with the variable resistor on the board to 2 MHz ±40 kHz; use Pin 1 on IC3850 as the test point.

The system may be reset and restarted by pushing the reset button on the microprocessor's PC board and typing "GO" which starts the preset menu.

Pushing bit "6 UP" PORT 0 on the front panel of the microprocessor causes a printout of the total of the five system conditions:

NOT UP, NO AGC, INVAL, NO, YES, and the current time. Restarting the program resets the five accumulators.

```
?G35
INPUT HOURS  14
INPUT MINUTE 10
GO TO START


NO--FF6A-P03 14:12:34 OUT
NO--FF6A-P03 14:15:45 IN
YES-AB1D-P03 14:19:42 OUT
NO--FF70-P03 14:21:31 IN
NO--FF75-P03 14:34:29 OUT
YES-AB1D-P03 14:43:33 IN
YES-DCOD-P03 14:56:11 IN
YES-DCOD-P03 15:14:57 IN
YES-AB1D-P03 15:16:53 OUT
NO--FF6A-P03 15:32:64 OUT
NO--FF70-P03 15:46:58 OUT
YES-DCOD-P03 16:28:53 IN
YES-AB1D-P03 16:33:25 IN

NOT UP = 00
NO AGC = 00
INVAL = 00
NO = 06
YES = 07
16:34:04 IN
```

Figure B-1. Record Print Out

APPENDIX C

F8 Kit Modification

APPENDIX C

F8 Kit Modification

The Fairchild F8 kit used is an F8 Design Evaluation Kit Number One without a case or power supply. The bare PC board and three power supplies are mounted on a metal chassis with a front panel for switches and LED indicators. One 5 V/1 A and two 12 V/175 mA power supplies are used for the system. The teletype interface circuitry was modified to adapt it to an RS 232 configured I/O. The "0", "1", and "5" ports are cabled to the main control chassis. Port "4" is connected to the data terminal. The kit board has 1 K of RAM, most of which is used by the software program. Since the kit has a preprogrammed FAIRBUG ROM which uses some of the memory addresses for its program, these addresses must not be used by the user's program. The internal timer uses address H '21' for its vectored interrupt; addresses H '3E6' to H '3FF' and scratch pad registers H '3C' to H '3F' are used by the "save routine" of the FAIRBUG monitor program. The user's program must be written around these addresses. Figures C-1 through C-5 show various facets of the kit.

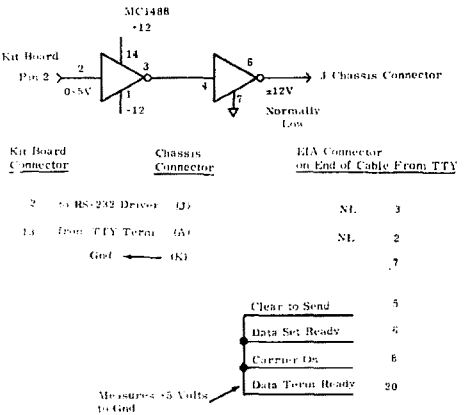


Figure C-1. RS232 Driver

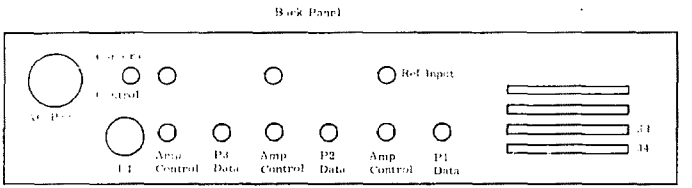


Figure C-2. Back Panel Layout

			Function	
P - 0 Status	Pin	Bit	Byte 1	Byte 2
	F	0	I 1	X
	E	1	O 1	X
	D	2	I 2	Pwr Up
	C	3	O 2	Agc
	H	4	I 3	Data Valid
	K	5	O 3	X
	J	6		X
	H MSB	7	X	X

			Function
P - 1	6	0 - 3 Lines	0 Nop
	5	1 - Decoded to:	1 1 Byte 1
	4	2 -	2 1 Byte 2
	3	3	3 2 Byte 1
	L	4 Reset 1	4 2 Byte 2
	9	5 Reset 2	5 3 Byte 1
	8	6 Reset 3	6 3 Byte 2
	7	7 Bell	7

			Function
P - 4 TTY	15	0	To TTY RS 232
	16	1	X
	17	2	X
	18	3	X
	19	4	X
	20	5	X
	21	6	X
	14 MSB	7	From TTY RS 232

			Function
P - 5 Parallel IN	S	0	Data
	T	1	
	U	2	
	V	3	
	W	4	
	X	5	
	Y	6	
	P MSB	7	

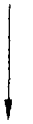


Figure C-3. F8 Port Pinouts

	Pin		Card 17	Pin
	2	Positive		6
	4	Inputs		8
Portal 1				
	6	gnd		
	8	gnd		
	10	gnd		
	12	gnd		
	36	Positive		35
Portal 2	38	Inputs		33
			Card 19	Hanford Modification
	18	Negative		8
Portal 3	20	Inputs		10
	22	gnd		
	24	+5 volts		

Figure C-4. J3 Interrupt Sensor Inputs

Pin	Card 5	Card 9	Card 13	
2	31	31	31	MSB Data Bus
4	32	32	32	
6	33	33	33	
8	34	34	34	
10	35	35	35	
12	36	36	36	
14	37	37	37	
16	38	38	38	
18				
20				
22				Bell
24	5	5	5	Control Lines
26	7	7	7	Control Lines
28	9	9	9	Control Lines
30	19			Reset
32		19		Reset
34			19	Reset
36	61	61	61	I1
38	62	62	62	O1
40	63	63	63	I2
42	64	64	64	O2
44	65	65	65	I3
46	66	66	66	O3
48	67	67	67	
50	68	68	68	

All odd pins are gnd.

Figure C-5. J4 Microprocessor Interface

APPENDIX D

IR Sensor Schematics

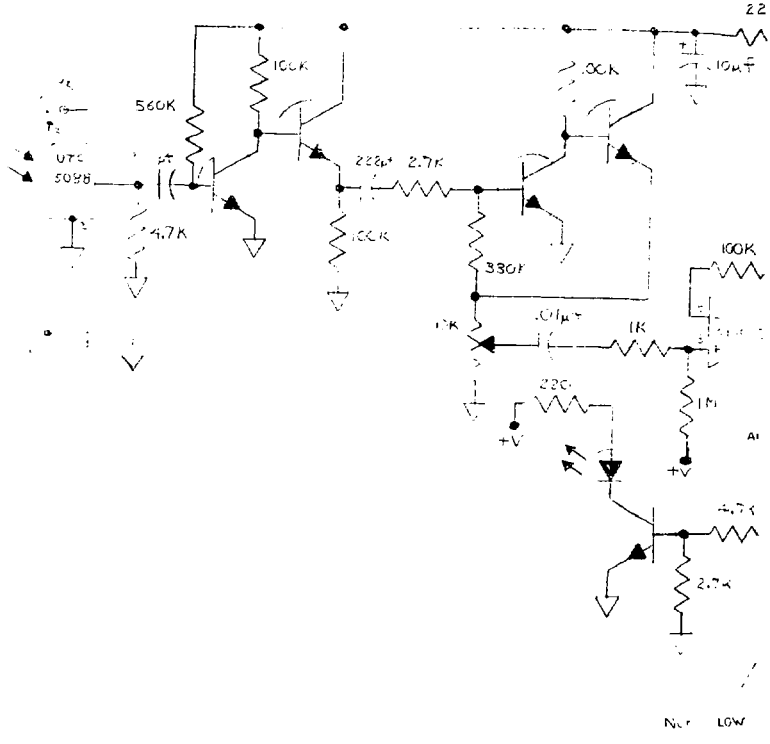
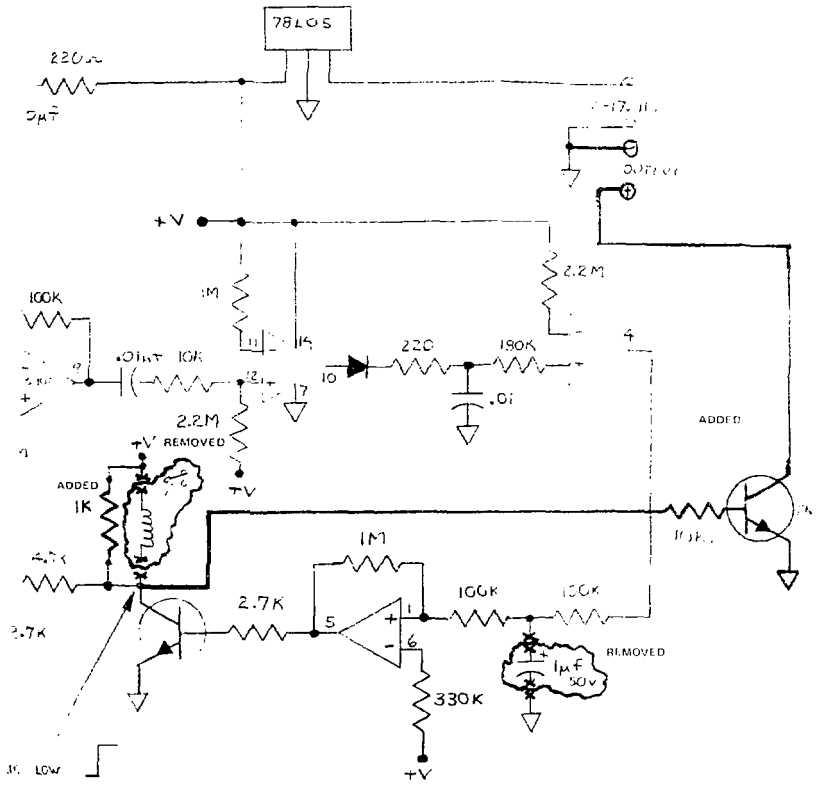


Figure D-1. Colorado Electro-Opti



ro-Optics IA-151 Photoelectric Receiver

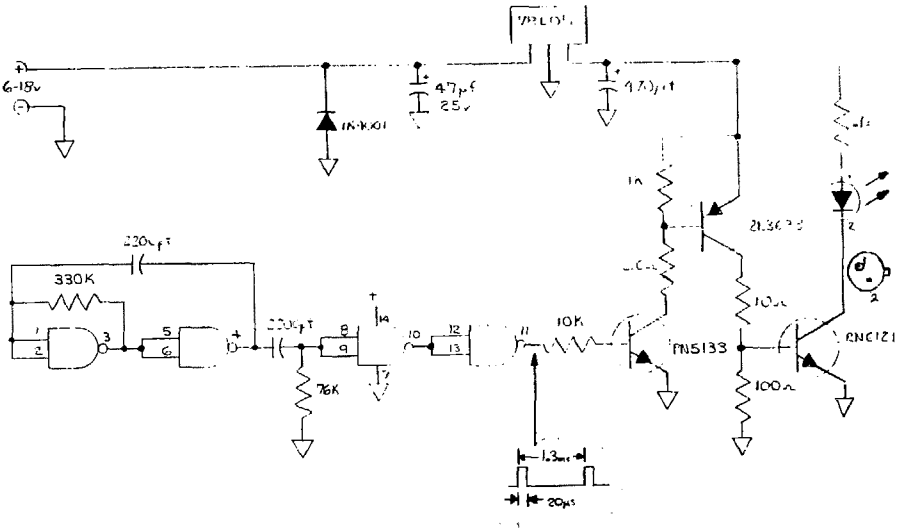


Figure D-3. XMTR 1A-76 Photoelectric System Colorado Electro Optics

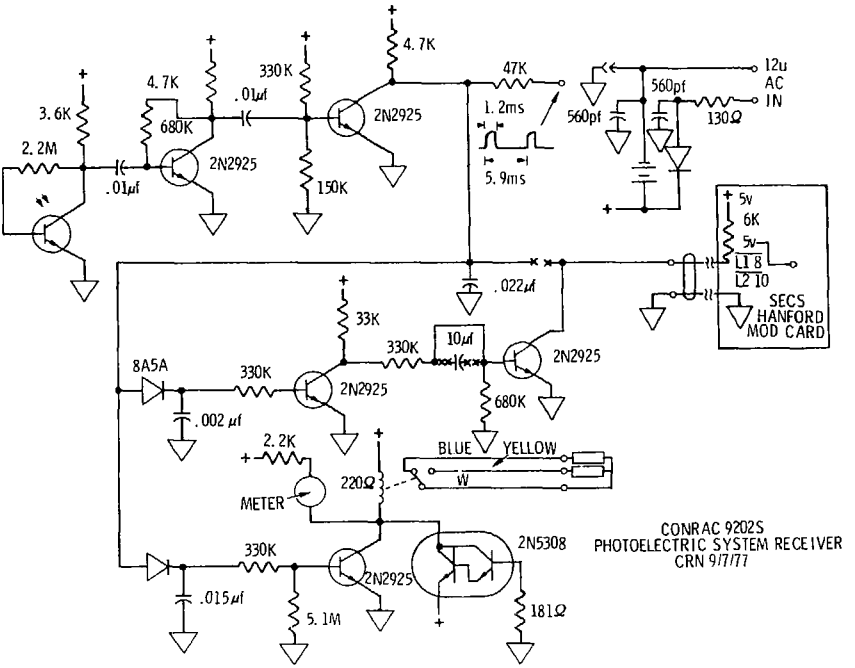


Figure D-4. CONRAC 9202S Photoelectric System Receiver

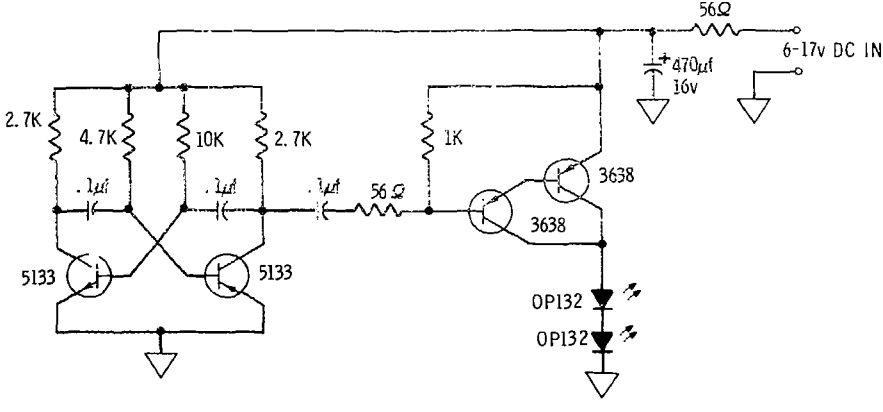


Figure D-5. Colorado Electro-Optics 1A-151 XMITTR

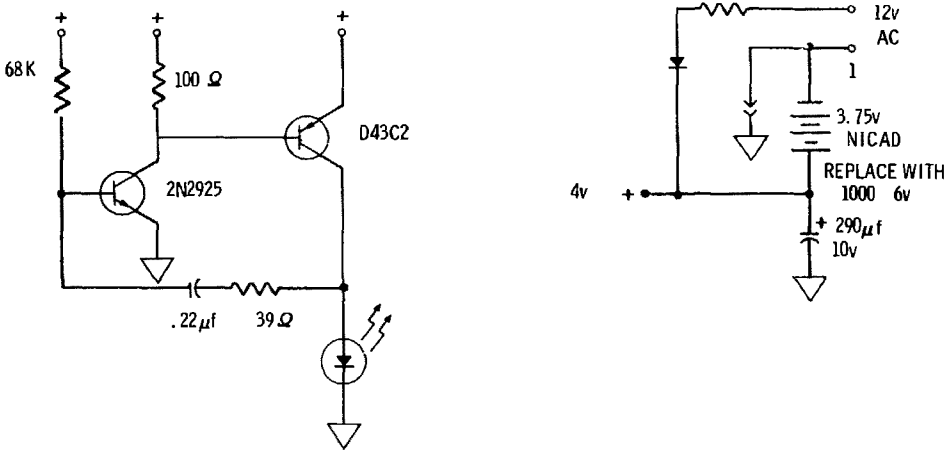


Figure D-6. CONRAC 9202S Photoelectric System Transmitter
(Arrowhead 1900-3R/MC)