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SILICON-ON CERAMIC PROCESS

Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet Task of the Low-Cost Solar Array Project

Quarterly Report No. 14, January 1—March 31, 1980

By
A. B. Whitehead
J. D. Zook
B. L. Grung
K. McHenry
S. B. Schuldt
P. W. Chapman

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Honeywell Corporate Material Sciences Center
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Solar Energy

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Honeywell Corporate Material Sciences Center
10701 Lyndale Ave. South
Bloomington, Minnesota 55420

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SUMMARY

The objective of this research is to investigate the technical feasibility of producing solar-cell-quality sheet silicon which could meet the DOE cost goals. The Honeywell approach is to coat one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt. Results and accomplishments which occurred during the quarter can be summarized as follows:

- Seventy substrates were produced in the production dip coater doped at 5 x $10^{16}cm^{-3}$ boron and delivered to JPL.
- Attempts to use high-purity graphite substrates to monitor the purity of the melt were not successful because of poor crystalline structure on carbon substrates.
- Thermal stress problems in the experimental dip coater were successfully eliminated by adding an afterheater on the coated side of the substrate.
- Large granules of silicon were used in place of bulk silicon to charge the melt, indicating a technique for melt replenishment.
- The new SCIM-II system was completed and put into operation.
- The thermal model of SCIM II was verified at high substrate speeds.
- Forty-six SOC cells were fabricated and tested during the quarter.
- Cell fabrication using ion implantation and thermal annealing was started. A low annealing temperature resulted in a low fill factor and low efficiency. This process is not yet optimized.
- Grain boundary recombination significantly reduces the diffusion length, L_n, in SOC material.
- Measurements of diffusion length show that L_n is a strong function of boron doping, decreasing as $N_A^{-0.3}$.

- At a given doping, L_n and J_{sc} in aluminum-doped material are significantly lower than in boron-doped material.
- Material processed with the Sandia hydrogen plasma treatment looks very promising. Recombination at grain boundaries is significantly reduced.

INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 11% or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be made to wet only that graphite-coated face and produce uniform, thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous-coating process also being investigated have excellent scale-up potential which offers an outstanding, cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 23 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and the rate at which the substrate is withdrawn from the melt.

The solar-cell potential of this SOC sheet silicon is promising. To date, solar cells with areas from 1 to 10 cm^2 have been fabricated from material with an as-grown surface. Conversion efficiencies, η, of about 10% with anti-reflection (AR) coating have been achieved. Such cells typically have open-circuit voltages, V_{oc}, and short-circuit current densities, J_{sc}, of 0.57 V and 23 mA/cm^2, respectively.

The SOC solar cell is unique in that its total area is limited only by device design considerations. Because it is on an insulating substrate, special consideration must be given to electrical contact to the base region. The preferred method uses slots in the substrate perpendicular to the crystalline growth direction. Electrical contact to the base region is made by metallizing the silicon exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing. The best slotted-cell results to date indicate a 10.1% conversion efficiency (AR-coated) on a 4-cm^2 (total area) cell.

The best experimental coated layers have been produced by dipping the substrate into the melt. However, the dipping process has two limitations if scaled up to a production method: 1) The melt becomes progressively contaminated by the mullite substrate. 2) The coating throughput in terms of area per unit time is limited. For these reasons, an alternative method of applying the silicon is being developed, which is termed SCIM (for Silicon Coating by Inverted Meniscus). The first SCIM-coating facility has successfully coated 5-cm-wide mullite sheets with uniform silicon layers by passing the sheets, carbonized surface down, over a trough of molten silicon. The current objective of this task is to uniformly coat slotted substrate sheets 5 inches wide. An improved SCIM coater has been designed and built in order to meet the coating throughput goals of the contract.

SHEET SILICON GROWTH

Dip-Coating Production (J.D. Zook and V. Harris)

The purpose of the production dip-coating activity is to reliably produce SOC material for solar-cell fabrication. During this quarter, SOC material was produced and delivered to JPL and subsequently forwarded to Spectrolab for processing into solar cells. Seventy substrates were delivered, doped at $5 \times 10^{16} cm^{-3}$ boron.

The runs made during the last quarter are listed in Table 1. A number of high-purity graphite substrates were dipped at the beginning of some of the runs, for the purpose of using these substrates to monitor the purity of the melt. Unfortunately, the solar-cell performance of these layers was very poor, as discussed below.

A continuing problem in production dip coating is the occasional formation of dendrites in the middle of some substrates. This problem is usually solved by raising the temperature of the melt, which produces thinner layers. Some of the comments in Table 1 indicate variations in soak time. Apparently, longer soak time reduces dendrite formation. A possible explanation is that the longer soak increases the amount of carbon and/or oxygen dissolved in the melt, thus reducing dendrite formation. During the next quarter, we plan to do some experiments to alter the composition of the ambient gas during growth to see if dendrite formation can be avoided.

Experimental Dip Coating (K.D. McHenry, J.D. Zook, and D. Sauve)

During the past quarter, several design modifications were implemented in the experimental dip coater. The major modification was the addition of a carbon afterheater placed on one side of the substrate. Heat is supplied on the coated side of the ceramic substrate, while forced cooling is maintained on the backside of the substrate. In addition, the afterheater is placed at a slightly elevated position compared with the impinging gas in an attempt to reduce the thermal gradient experienced by the substrate. Addition of the afterheater has virtually eliminated thermal shock problems with the substrates.

Table 1. Dip-Coating Production Results

Run No.	Dopant Level (cm^{-3} boron)	Growth Speed (cm/sec)	Number Dipped	Comments
230	5×10^{16}	0.06	14	Electrical conduction experiment.
231	4.6×10^{16}	0.06	12	High Yield.
232	4.6×10^{16}	0.06	11	Some dendrites.
233	4.6×10^{16}	0.06	10	Substrate no. 10 was "Q" type, still shows warpage.
234	4.6×10^{16}	0.06	11	
235	4.6×10^{16}	0.06	12	Substrates 235-2 and 235-5 broke and fell into the melt.
236	4.6×10^{16}	0.06	12	Substrate 236-5 broke; dendrite problems.
237	4.6×10^{16}	0.06	14	Dendrite problems, rough substrate surfaces.
238	4.6×10^{16}	0.06	12	Changed carbon felt, some dendrite problems.
239	5×10^{16}	0.06	12	
240	5×10^{16}	0.06	12	Some dendrite formation.
241	5×10^{16}	0.06	14	15-sec soak time; fewer dendrites.
242	5×10^{16}	0.06	12	Rough substrate surfaces. Grafelt removed from bottom of support. Not desirable.
243	5×10^{16}	0.06	12	Too fast warmup, crucible sagged.
244	5×10^{16}	0.06	12	
245	5×10^{16}	0.06	12	
246	5×10^{16}	0.06	9	
247	5×10^{16}	0.06	12	First run with narrower substrate holder.
248	5×10^{16}	0.06	9	Some substrates had uneven surfaces.
249	5×10^{16}	0.06	9	New substrate batch, 0.004 in. thicker, some cracked.
250	100×10^{16}	0.06	11	20-sec soaking.
251	5×10^{16}	0.06	14	"O"-type substrates, several cracked.

Note: Runs 247 through 251 had narrower substrate holder; standard holder will be reinstalled on next runs to see if this eliminates cracking condition at holder connection.

A second modification became necessary as a result of a shortage of bulk silicon charges. Several runs were performed using large granules of silicon or silicon "nuggets." Because of packing limitations of these granules, a full charge of silicon could not be put into the SiO_2 crucible prior to heat-up. A quartz tube assembly was inserted in the dip coater in such a way that additional silicon could be fed into the crucible as the original charge started to melt. With this replenishing technique it was then possible to maintain a full charge in the crucible.

The experimental dip coater has been relocated and currently operates from a different power supply. The unit and the new power supply are now set up so that the power is turned on during the early morning hours, thus enabling the dip coater to be ready for operation at the beginning of the normal work day. This procedure will allow for much more efficient use of personnel time and increase the number of substrates dipped per day.

Continuous Coating (J.D. Zook, D. Heaps, H. Burke, R. Hegel, H. Wolner, and E. Masterson)

The continuous-coating process was under intensive development during the quarter, under Honeywell funding. The main effort was the design and construction of a new coating system, which we have designated SCIM II to distinguish it from the first SCIM-coating system. The system is operational, and operation under JPL funding has begun.

The design of the new coater is shown schematically in Fig. 1. There are several key features which are different from the earlier system:

1) The trough-to-substrate distance is more conveniently adjustable during operation. This is important in experimental operation to give the operator additional versatility in controlling meniscus stability. This feature was demonstrated successfully during the first trial run with molten silicon. The trough-crucible assembly could be raised and lowered with the trough filled with molten silicon, without any tendency towards spillage.

2) There are two side heaters which are powered by a separately controlled power supply, to produce transverse temperature uniformity. The initial tests to date indicate that some modifications of these heaters are needed, because the crucible side of the system is considerably hotter than the observer side. This was

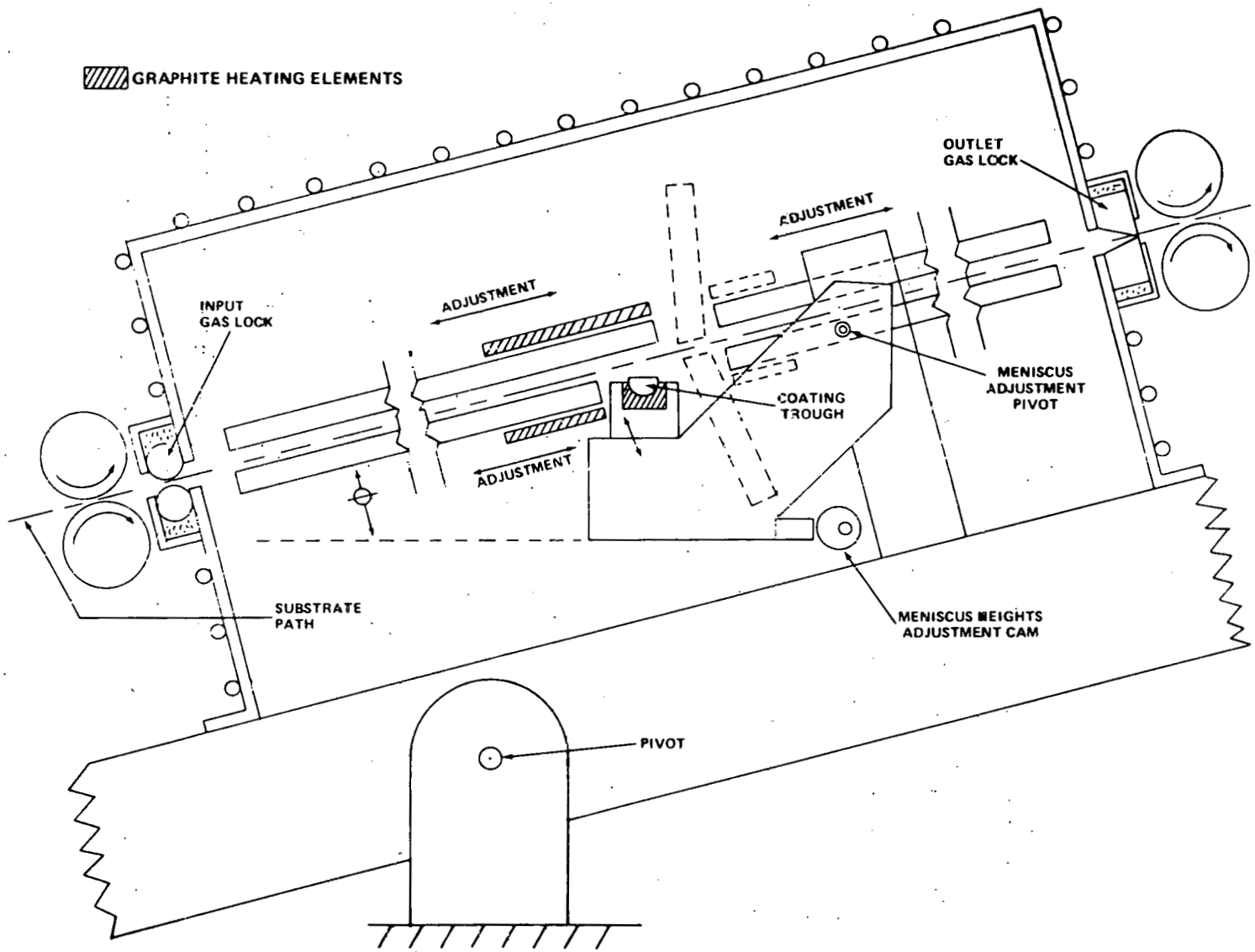


Figure 1. Schematic Illustration of SCIM-II Coater

made particularly evident during the first silicon coating run where the silicon was much thicker on one edge of a 4-inch-wide substrate than it was on the other side. Once needed modifications are made, the use of this separate power supply will greatly simplify the problem of attaining transverse temperature uniformity.

3) The substrate transport uses only cold rollers which are external to the box containing the inert atmosphere needed for growth. This feature means that only 40-inch substrates can be coated, and that the substrates must enter the enclosed system cold, get heated to the melting point of silicon, and then cool back to near room temperature when they emerge from the enclosure. The preheaters were designed to minimize the thermal gradients during heating, as described in Silicon-on-Ceramic Process Quarterly Report No. 13 (P.W. Chapman, et al.), published 15 February 1980. Unfortunately, the design is different for each substrate speed.

The present preheater was designed for a coating speed of 0.25 cm/sec (the JPL contract goal for 1980). Substrates have passed through the system at that speed and higher (up to 0.8 cm/sec) without warping or cracking. At lower speeds (0.1 cm/sec), the substrates buckled, and some of them cracked near the end of the substrate. For coating at lower speeds, a preheater with less thickness will be used to decrease the initial gradient that the substrates see as they enter the enclosed chamber. The thermal modeling calculations used for heater design were described in Quarterly Report No. 13.

Even at the highest speeds, the substrates have cooled to 160^{o}C by the time they come in contact with the rubber rollers at the exit end. Thus, the passive afterheaters are functioning correctly. It should also be noted that even with the buckling and cracking at lower than the design speed, the substrates continued to be transported. Thus, the substrate transport mechanism is successful.

In summary, the SCIM-II system is operational and coating experiments will be conducted under the JPL program. Minor modifications for increased transverse temperature uniformity will be implemented soon. It should also be noted that the automatic temperature controllers have not yet arrived, and some time will be required to install them and assure their proper operation.

CELL FABRICATION AND DEVELOPMENT (B. Grung, T. Heisler, and S. Znameroski)

Cell Performance

During this quarter, we fabricated 46 SOC cells. Our objective was to determine the effects of: (1) heavy doping (2 x $10^{17}/cm^3$) in the base region, (2) melt current in the melt, (3) aluminum doping in the base region, (4) no doping in the melt, and (5) ion-implanted/anneal for the emitter region. These effects are discussed below. The primary characteristics of the cells are given in Tables 2 and 3, where the cells are identified by item numbers. Only three cells (items 1, 4, and 5) have been AR coated so far and the best cell has a conversion efficiency, η, of 8.9% (AM1), for a cell area of 5 cm^2. For the remaining 43 non-AR-coated cells, the highest conversion efficiency was 6.95%.

Heavy Doping Experiment -- Five solar cells (items 1 through 5) were fabricated using SOC material with a boron concentration of 2 x $10^{17}/cm^3$, as compared with the normal concentration of 5 x $10^{16}/cm^3$. The three AR-coated cells have an average open-circuit voltage (V_{oc}) of 0.58 V, an average short-circuit current density (J_{sc}) of 21.4 mA/cm^2, and an average η of 8.6%. The performance of these heavily doped SOC cells is limited primarily by low values of J_{sc}.

Melt Current Experiment -- Eight SOC cells (items 6 through 13) were fabricated to determine the effect of an electric current through the melt during dip coating. It was hoped that this current might reduce melt contamination by influencing the transport of impurities from the substrate into the melt. Based on the results of the eight cells, the electric current does not seem to have an effect on melt contamination.

Aluminum-Doping Experiment -- Eleven SOC cells (items 14 through 24) were fabricated to determine if aluminum doping could produce higher values of J_{sc}, for a given doping concentration. The highest J_{sc} is 14.68 mA/cm^2 (AM1, no AR) for an aluminum-doping concentration of 2.2 x $10^{16}/cm^3$. This value is low compared with an average value of 17 mA/cm^2 for boron-doped samples. Thus, aluminum doping does not produce high values of J_{sc}.

No-Doping Experiment -- Four SOC cells (items 25 through 28) were fabricated to determine the effects of progressive melt contamination on the sheet resistance of the dip-coated SOC material. For the ninth and twelfth substrates

Table 2. Conversion Efficiencies of Recent Slotted-Substrate SOC Cells

Notes:	Item	Cell Number	P-type Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sq cm)	Base Sheet Resistance	Total Area Conversion Efficiencies Before AR (%)	After AR (%)
	1	225 - 3-103	2.0e+017	0.06	0.7	5	5.44	8.54
	2	225 - 4-111	2.0e+017	0.06	0.5	6	4.28	
(1)	3	225 - 5-111	2.0e+017	0.06	0.6	6	3.47	
	4	225 - 6-111	2.0e+017	0.06	0.7	6	5.70	8.30
	5	225 - 6-211	2.0e+017	0.06	0.6	6	6.24	8.91
	6	226 - 3-111	4.7e+016	0.06	0.7	24	6.45	
	7	226 - 3-211	4.7e+016	0.06	0.7	24	6.93	
	8	226 - 8-111	4.7e+016	0.06	0.7	26	5.36	
(2)	9	226 - 8-211	4.7e+016	0.06	0.6	26	3.38	
	10	226 - 9-111	4.7e+016	0.06	0.8	35	6.11	
	11	226 - 9-211	4.7e+016	0.06	0.7	35	5.77	
	12	226 -10-111	4.7e+016	0.06	0.7	34	5.69	
	13	226 -10-211	4.7e+016	0.06	0.6	34	5.84	
	14	227 - 5-111	2.2e+016	0.06	0.8	24	5.73	
	15	227 - 5-211	2.2e+016	0.06	0.6	24	5.57	
	16	227 - 7-111	2.2e+016	0.06	0.7	26	5.43	
	17	227 - 7-211	2.2e+016	0.06	0.7	26	5.40	
(3)	18	227 - 8-111	2.2e+016	0.06	0.9	28	2.51	
	19	227 - 8-211	2.2e+016	0.06	0.8	28	5.62	
	20	227 - 9-111	2.2e+016	0.06	0.8	26	2.12	
	21	227 - 9-211	2.2e+016	0.06	0.8	26	4.75	
	22	227 -11-111	2.2e+016	0.06	0.7	16	5.26	
	23	227 -11-211	2.2e+016	0.06	0.7	16	5.55	
	24	227 -12-111	2.2e+016	0.06	1.1	20	4.86	
	25	228 - 9-111	0.0e+000	0.06	1.6	771	6.06	
(4)	26	228 - 9-211	0.0e+000	0.06	1.7	771	6.00	
	27	228 -12-111	0.0e+000	0.06	1.5	498	4.54	
	28	228 -12-211	0.0e+000	0.06	1.8	498	4.26	
	29	233 - 2-111	4.7e+016	0.06	0.6	0	1.78	
	30	234 - 3-211	4.7e+016	0.06	0.6	0	4.15	
(5)	31	234 - 7-111	4.7e+016	0.06	0.6	0	4.07	
	32	234 - 7-211	4.7e+016	0.06	0.5	0	4.36	
	33	234 - 8-111	4.7e+016	0.06	0.5	0	4.68	
	34	234 - 8-211	4.7e+016	0.06	0.5	0	4.29	
	35	235 - 3-111	4.7e+016	0.06	0.5	13	6.74	
	36	235 - 3-211	4.7e+016	0.06	0.6	13	6.72	
(5)	37	235 - 4-111	4.7e+016	0.06	0.4	0	5.58	
	38	235 - 4-211	4.7e+016	0.06	0.5	0	5.67	
	39	236 -10-111	4.7e+016	0.06	0.6	29	5.45	
(5)	40	237 - 4-111	4.7e+016	0.06	0.8	0	4.30	
	41	237 - 4-211	4.7e+016	0.06	0.8	0	4.27	
	42	237 -10-111	4.7e+016	0.06	0.6	32	4.69	
	43	238 - 8-111	5.0e+016	0.06	0.9	29	6.95	
	44	238 - 8-211	5.0e+016	0.06	0.7	29	5.95	
	45	240 - 3-111	5.0e+016	0.06	0.6	30	6.66	
	46	240 - 3-211	5.0e+016	0.06	0.6	30	6.53	

Notes:
(1) Heavy-doping experiment.
(2) Conduction experiment.
(3) Aluminum-doping experiment.
(4) No-doping experiment.
(5) Ion-implantation experiment.

Table 3. Characteristics of Recent Slotted SOC Cells and Their Corresponding Single-Crystal Control Cells

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)	
1	225 - 3-103-0	142.30	0.575	0.665	14.23	5.44	
1	225 - 3-103-1	217.00	0.584	0.674	21.70	8.54	(AR)
2	225 - 4-111-0	75.30	0.552	0.515	15.06	4.28	
3	225 - 5-111-0	74.90	0.546	0.424	14.98	3.47	
4	225 - 6-111-0	75.30	0.567	0.668	15.06	5.70	
4	225 - 6-111-1	107.30	0.579	0.668	21.46	8.30	(AR)
5	225 - 6-211-0	73.90	0.574	0.736	14.78	6.24	
5	225 - 6-211-1	104.60	0.586	0.727	20.92	8.91	(AR)
6	226 - 3-111-0	80.40	0.551	0.728	16.08	6.45	
7	226 - 3-211-0	83.70	0.554	0.747	16.74	6.93	
8	226 - 8-111-0	81.00	0.547	0.685	16.20	5.36	
9	226 - 8-211-0	79.00	0.521	0.411	15.80	3.38	
10	226 - 9-111-0	80.50	0.553	0.686	16.10	6.11	
11	226 - 9-211-0	81.00	0.548	0.650	16.20	5.77	
12	226 -10-111-0	79.70	0.543	0.657	15.94	5.69	
13	226 -10-211-0	79.30	0.542	0.679	15.86	5.84	
14	227 - 5-111-0	70.60	0.539	0.753	14.12	5.73	
15	227 - 5-211-0	73.40	0.533	0.712	14.68	5.57	
16	227 - 7-111-0	69.30	0.537	0.730	13.86	5.43	
17	227 - 7-211-0	68.00	0.537	0.739	13.60	5.40	
18	227 - 8-111-0	66.50	0.471	0.401	13.30	2.51	
19	227 - 8-211-0	71.00	0.535	0.740	14.20	5.62	
20	227 - 9-111-0	65.60	0.451	0.358	13.12	2.12	
21	227 - 9-211-0	64.50	0.527	0.699	12.90	4.75	
22	227 -11-111-0	65.30	0.531	0.758	13.06	5.26	
23	227 -11-211-0	68.30	0.533	0.763	13.66	5.55	

continued next page

Table 3. Characteristics of Recent Slotted SOC Cells and Their Corresponding Single-Crystal Control Cells (Continued)

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)
24	227 -12-111-0	67.30	0.521	0.692	13.46	4.86
25	228 - 9-111-0	94.10	0.479	0.672	18.82	6.06
26	228 - 9-211-0	95.00	0.483	0.654	19.00	6.00
27	228 -12-111-0	89.40	0.464	0.547	17.88	4.54
28	228 -12-211-0	77.60	0.478	0.574	15.52	4.26
29	233 - 2-111-0	63.20	0.410	0.343	12.64	1.78
30	234 - 3-211-0	66.00	0.492	0.639	13.20	4.15
31	234 - 7-111-0	64.10	0.488	0.650	12.82	4.07
32	234 - 7-211-0	61.10	0.491	0.726	12.22	4.36
33	234 - 8-111-0	63.90	0.499	0.734	12.78	4.68
34	234 - 8-211-0	63.40	0.495	0.683	12.68	4.29
35	235 - 3-111-0	79.30	0.560	0.759	15.86	6.74
36	235 - 3-211-0	79.50	0.558	0.757	15.90	6.72
37	235 - 4-111-0	70.90	0.532	0.740	14.18	5.58
38	235 - 4-211-0	70.60	0.532	0.758	14.12	5.67
39	236 -10-111-0	80.80	0.541	0.623	16.16	5.45
40	237 - 4-111-0	66.00	0.485	0.672	13.20	4.30
41	237 - 4-211-0	68.50	0.480	0.650	13.70	4.27
42	237 -10-111-0	78.30	0.536	0.557	15.66	4.69
43	238 - 8-111-0	82.60	0.556	0.757	16.52	6.95
44	238 - 8-211-0	82.10	0.546	0.664	16.42	5.95
45	240 - 3-111-0	81.70	0.552	0.738	16.34	6.66
46	240 - 3-211-0	79.40	0.550	0.748	15.88	6.53
(Single-Crystal)						
47	R38 - 0-111-0	104.60	0.578	0.765	20.92	9.25
47	R38 - 0-111-1	146.60	0.587	0.730	29.26	12.54 (AR)

continued next page

Table 3. Characteristics of Recent Slotted SOC Cells and Their Corresponding Single-Crystal Control Cells (Concluded)

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area Jsc (mA/sqcm)	Eff. (%)
48	R38 - 0-211-0	104.10	0.580	0.764	20.82	9.23
48	R38 - 0-211-1	146.10	0.587	0.751	29.22	12.88 (AR)
49	R39 - 0-111-0	94.70	0.560	0.750	18.94	7.95
50	R39 - 0-211-0	96.10	0.560	0.750	19.22	8.07
51	R40 - 0-111-0	89.90	0.562	0.760	17.98	7.68
52	R41 - 0-111-0	101.00	0.578	0.717	20.20	8.37
53	R41 - 0-211-0	101.30	0.578	0.731	20.26	8.56
54	R43 - 0-111-0	100.90	0.572	0.757	20.18	8.74
55	R43 - 0-211-0	103.10	0.567	0.666	20.62	7.79
56	R44 - 0-111-0	102.40	0.574	0.752	20.48	8.84
56	R44 - 0-211-0	102.80	0.575	0.766	20.56	9.06

dipped in run no. 228, the sheet resistance was 770 and 500 Ω/□, respectively. Cells fabricated using these SOC substrates had efficiencies in the range from 4.3 to 6.1% (AM1, no AR). This indicates that the mullite progressively contaminates the melt with a p-type dopant, shown to be aluminum in earlier experiments. Such contamination is a basic problem for the dip-coating technique. A similar problem should not exist for the SCIM-coating technique, since the mullite will not be in direct contact with the silicon melt.

Ion-Implant Experiment -- Eight SOC cells (items 20 through 34, and 37 and 38) were fabricated using ion implantation and thermal anneal to form the n^+ emitter region. Arsenic was used as the dopant. For one set of cells, the annealing temperature conditions were 600°C for 30 minutes in flowing nitrogen. The sheet resistance was ∿ 35 Ω/□, which is typical for our phosphine-diffused cells. The resulting cell efficiencies were low, primarily because of low fill factors, as shown in Fig. 2. For a second set of cells, the annealing temperature was 850C for 60 minutes, which are the

SLOTTED SOC CELL

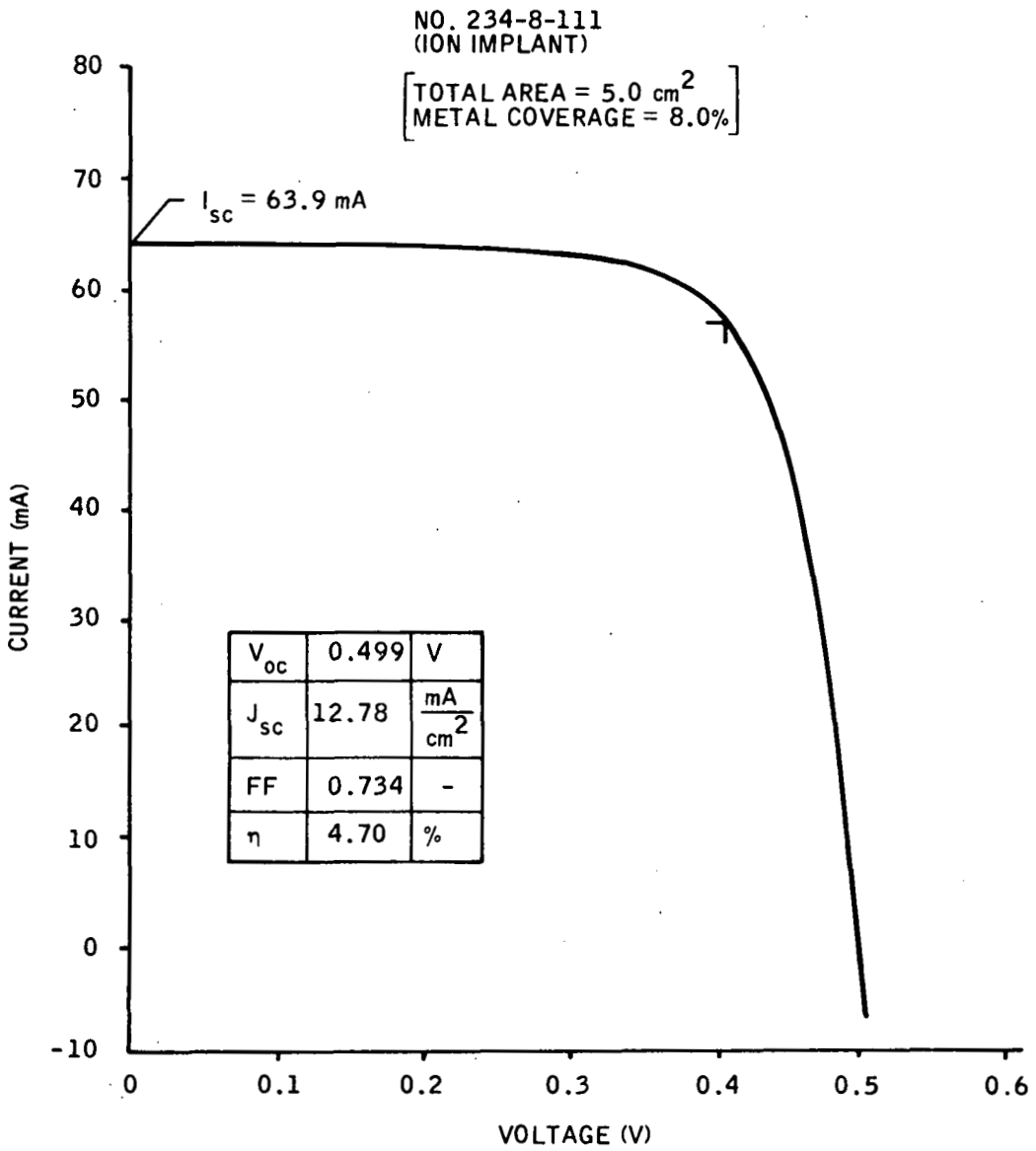


Figure 2. Current-Voltage Characteristics of an Ion-Implanted SOC Cell Thermally Annealed at 600°C for 30 Minutes

same conditions used for our phosphine diffusion. The emitter sheet resistance was ∿ 32 Ω/□, which is essentially the same as that obtained at the lower temperature. However, the efficiency values were much higher. Figure 3 shows one cell annealed at 850C along with a control cell fabricated using the standard phosphine diffusion. The efficiency of the ion-implant/anneal cell is 5.6%, as compared with the 6.7% efficiency of the diffused cell. Clearly, more work needs to be done to determine the proper annealing conditions.

Empirical Expressions

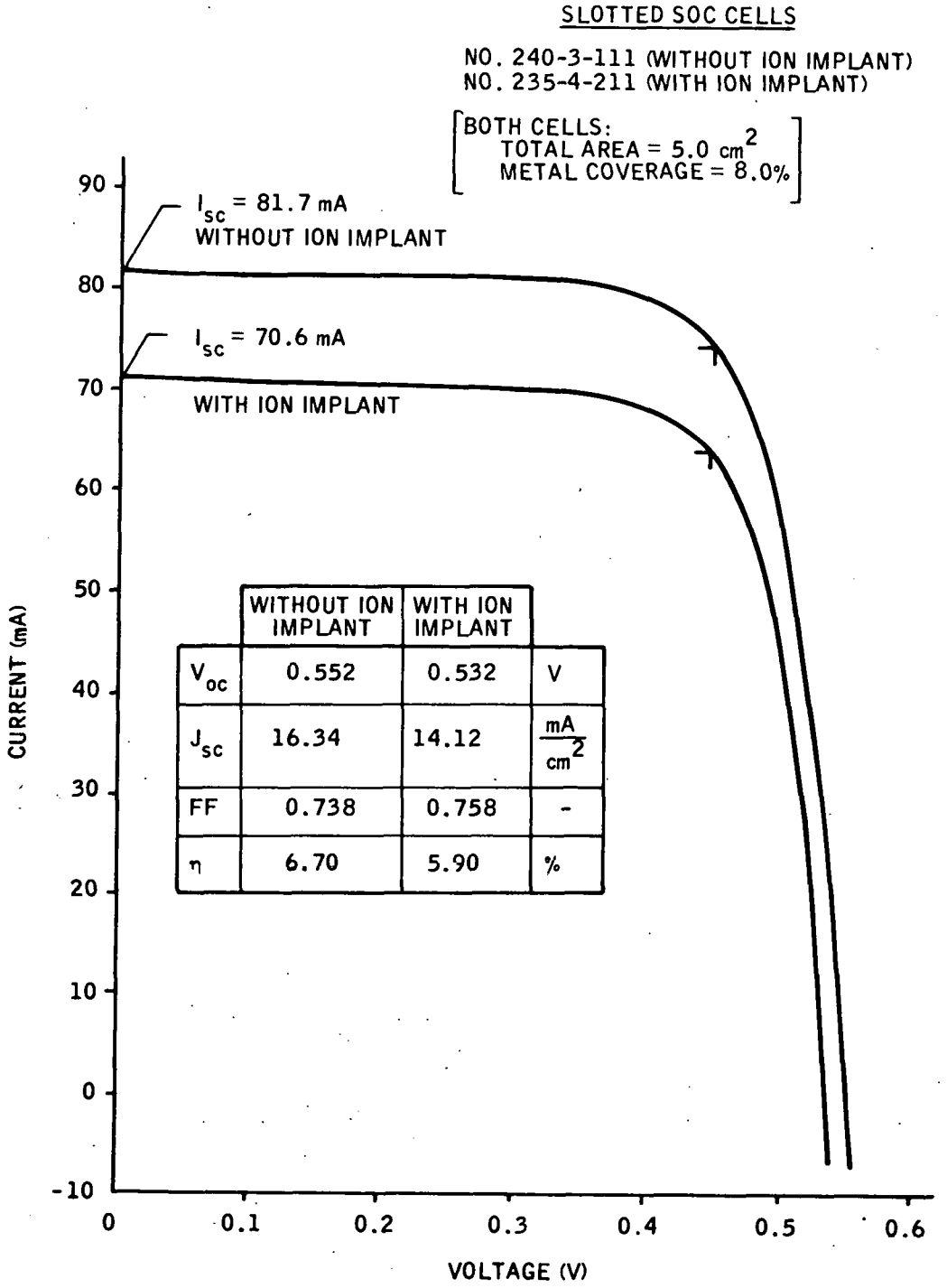
In Fig. 23 of Silicon-on-Ceramic Process No. 4, published 31 October 1979, experimental results were given showing cell performance as a function of the base doping concentration. These results have been updated and the new results are shown in Fig. 4, which represents a total of 136 completed SOC cells. The primary characteristics of all cells are listed in Silicon-on-Ceramic Process Monthly Report No. 36. The cells are divided into 10 groups, where each group corresponds to a given base doping concentration (N_B). In Fig. 4, the experimental results are indicated by the vertical lines. The solid curves can be calculated as follows. First, linear regression is used to determine an empirical relationship between J_{sc} and N_B. The result is

$$J_{sc} = 1.48 \log \left(\frac{9.7 \times 10^{31}}{N_B} \right) \qquad (1)$$

where J_{sc} is in units of mA/cm^2 and N_B is in units of cm^{-3}. Second, linear regression is used to determine an empirical relationship between J_{01} and N_B. For the data given in Table 4 of Monthly Report No. 34, the result is

$$J_{01} = \frac{9.6}{N_B^{0.54}} \qquad (2)$$

where J_{01} is in units of mA/cm^2. Third, the theoretical expression for the specific series resistance, R_sA, as given in Quarterly Report No. 12 published 31 July 1979, is used, with an empirical constant of 1.75 added to approximate the measured results. The resulting expression is



	WITHOUT ION IMPLANT	WITH ION IMPLANT	
V_{oc}	0.552	0.532	V
J_{sc}	16.34	14.12	$\frac{mA}{cm^2}$
FF	0.738	0.758	-
η	6.70	5.90	%

Figure 3. Current-Voltage Characteristics of an Ion-Implanted SOC Cell and a Diffused SOC Cell. The ion-implant cell was thermally annealed at 850°C for 30 minutes.

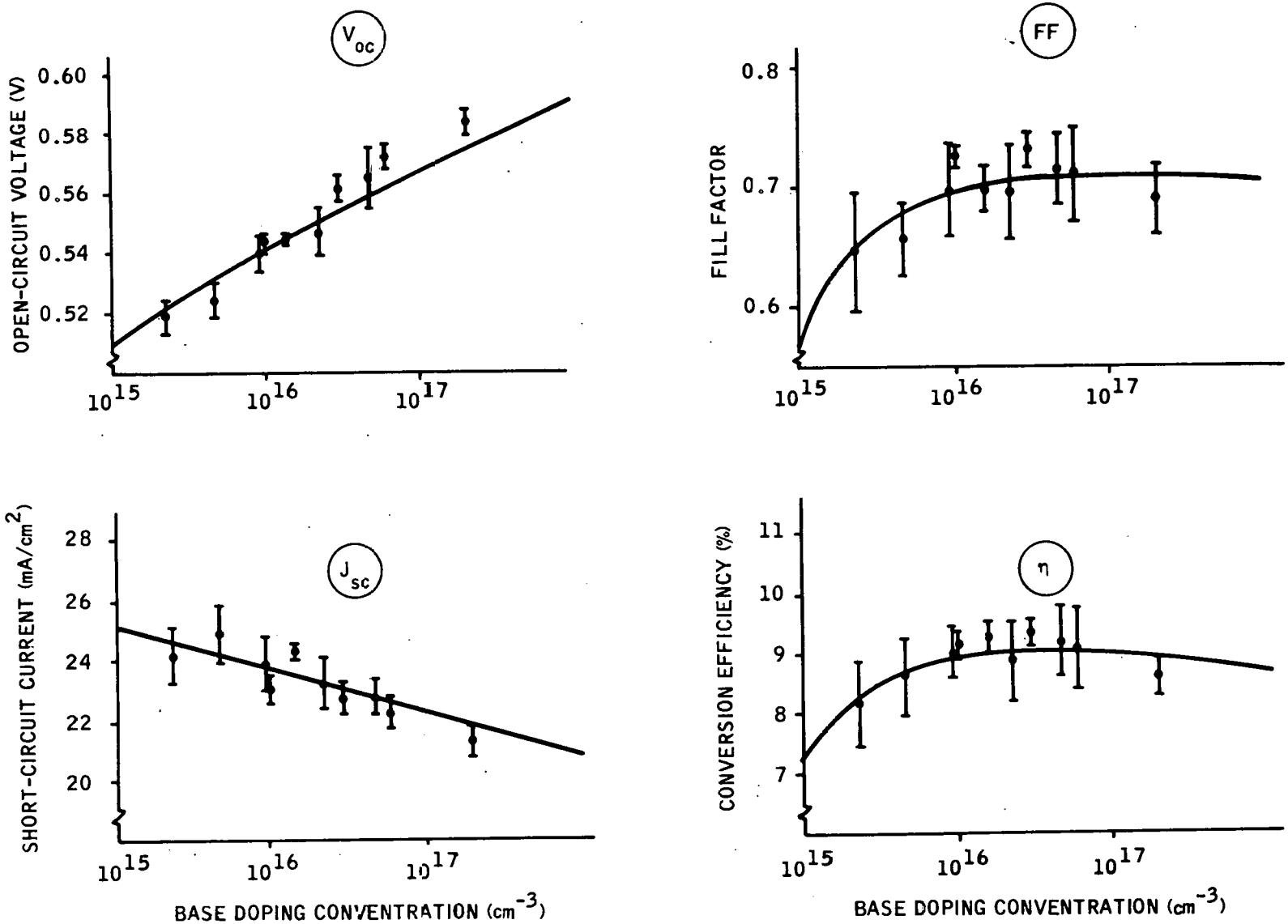


Figure 4. Cell Performance as a Function of Base Doping Concentration, for the 1979 Baseline Cells. Vertical lines are in the experiment results. Solid curves are the calculated results.

$$R_sA = 2.25 + \frac{3.35 \times 10^{15}}{N_B} \quad (3)$$

where R_sA is in units of ohm-cm^2. For Eq. (3), a growth velocity of 0.06 cm/sec is assumed. Finally, the current density is assumed to be given by

$$J = J_{01}\left[\exp \frac{q(V - JR_sA)}{kT} - 1\right] + J_{02}\left[\exp \frac{q(V - JR_sA)}{nkT} - 1\right] + \left(\frac{V - JR_sA}{R_{sh}}\right) - J_{sc} \quad (4)$$

where J_{02} is 10^{-4} mA/cm^2 and n is 2. Equations (1) through (4) give the empirical curves of Fig. 3. Clearly, the empirical curves approximate the experimental result.

The effects of changing some of the parameters in Eqs. (1) through (3) are shown in Figs. 5 through 8. Figure 5 shows the effects of replacing J_{01} and $J_{01} \pm s$, where s is the standard deviation of J_{01} as determined by the linear regression of the J_{01} data. Decreasing J_{01} by s increases V_{oc} by $\sim$ 0.005 V and increases η by $\sim$ 0.1%, for $N_B = 2 \times 10^{16}$/cm^3. The parameter J_{01} has negligible effect on fill factor and J_{sc}. Figure 6 shows the effects of replacing R_sA with $R_sA \pm 1.75$. For $R_sA - 1.75$, the specific series resistance is equal to the theoretical value predicted by Eq. (7) of Quarterly Report No. 12. For this theoretical limit, the fill factor is 0.77 and is 9.8%, for $N_B = 2 \times 10^{16}$/cm^3. The specific series resistance has little effect on V_{oc} and J_{sc}, as expected. Figure 7 shows the effects of replacing J_{sc} with $J_{sc} \pm s$, where s is the standard deviation of J_{sc} as determined by the linear regression of the J_{sc} data. Increasing J_{sc} by s increases slightly the fill factor and increases approximately by about 0.2%, for $N_B = 2 \times 10^{16}$/cm^3. Figure 8 shows the combined effects of decreasing J_{01} by its standard deviation, decreasing R_sA by 1.75, and increasing J_{sc} by its standard deviation. For these three changes, the maximum conversion efficiency, η, is calculated to be 10.3%, for $N_B = 2 \times 10^{16}$/cm^3.

MATERIAL EVALUATION (J.D. Zook, R. Hegel, and C. Wensman)

The emphasis in the material evaluation effort continues to be the measurement of minority-carrier diffusion lengths, L_n, and evaluation of grain boundary recombination. We have measured diffusion lengths over a range of

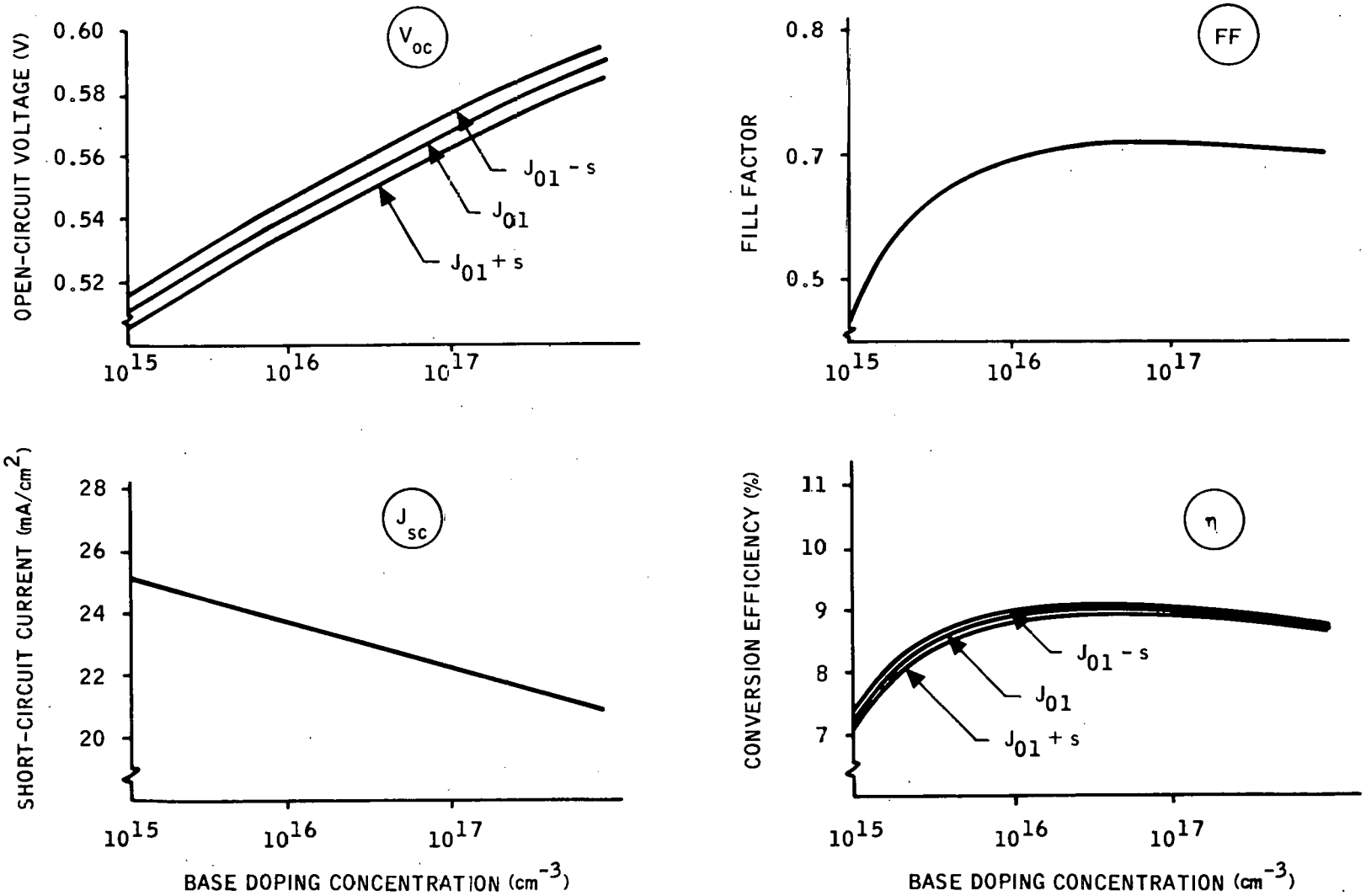


Figure 5. Effects of Changes in the Values of the Parameter J_{01}

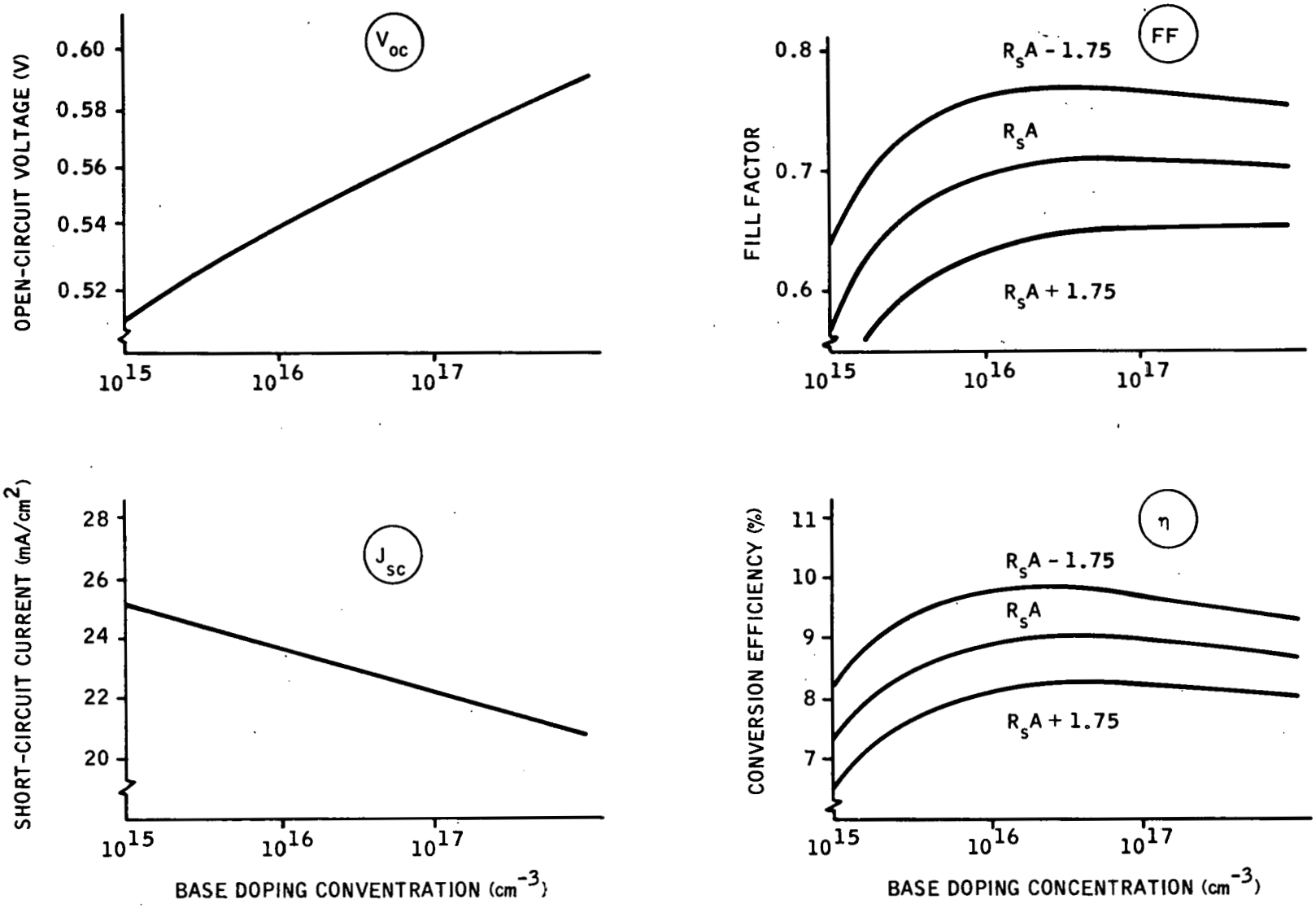


Figure 6. Effects of Changes in the Specific Series Resistance

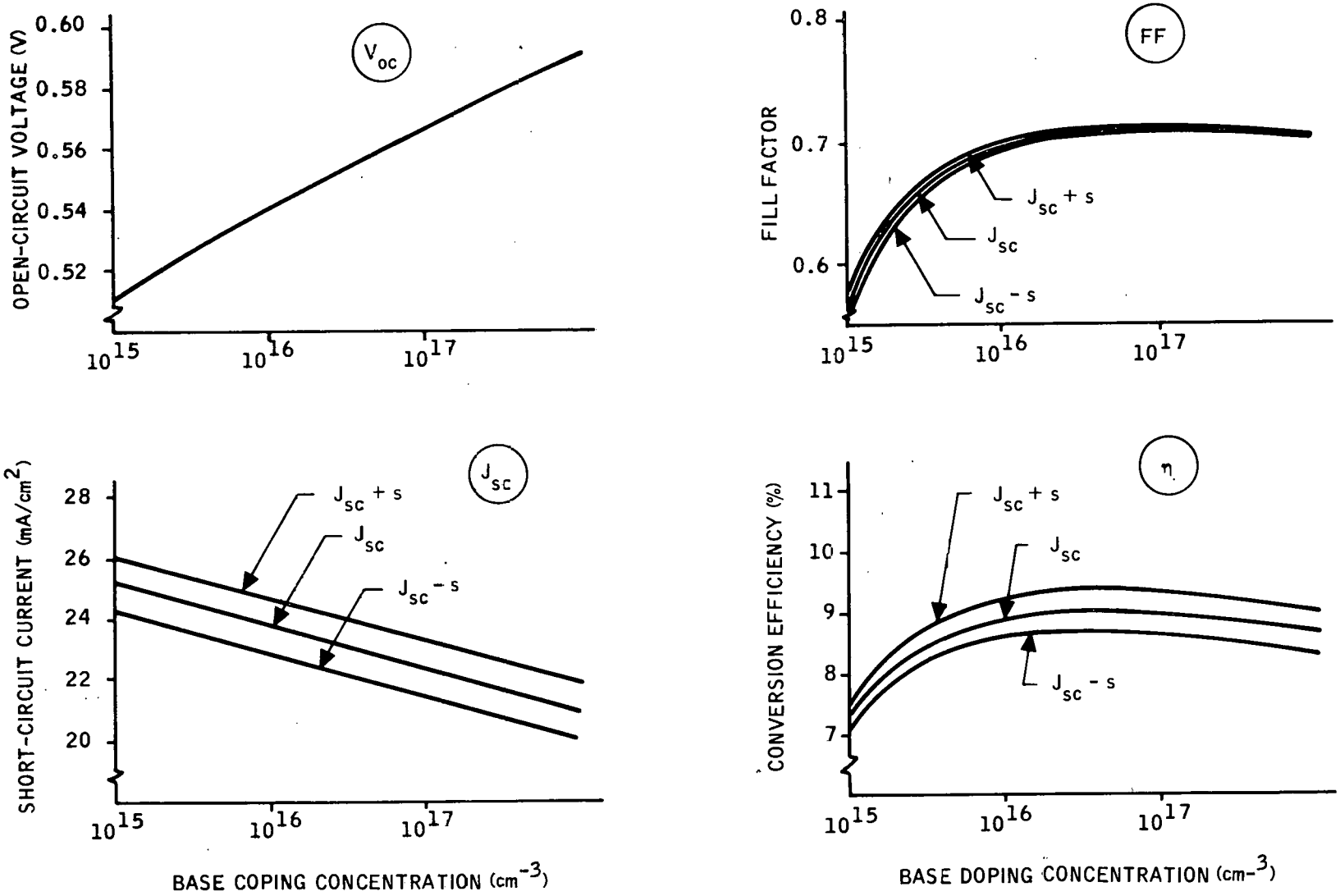


Figure 7. Effects of Changes in Short-Circuit Current Density

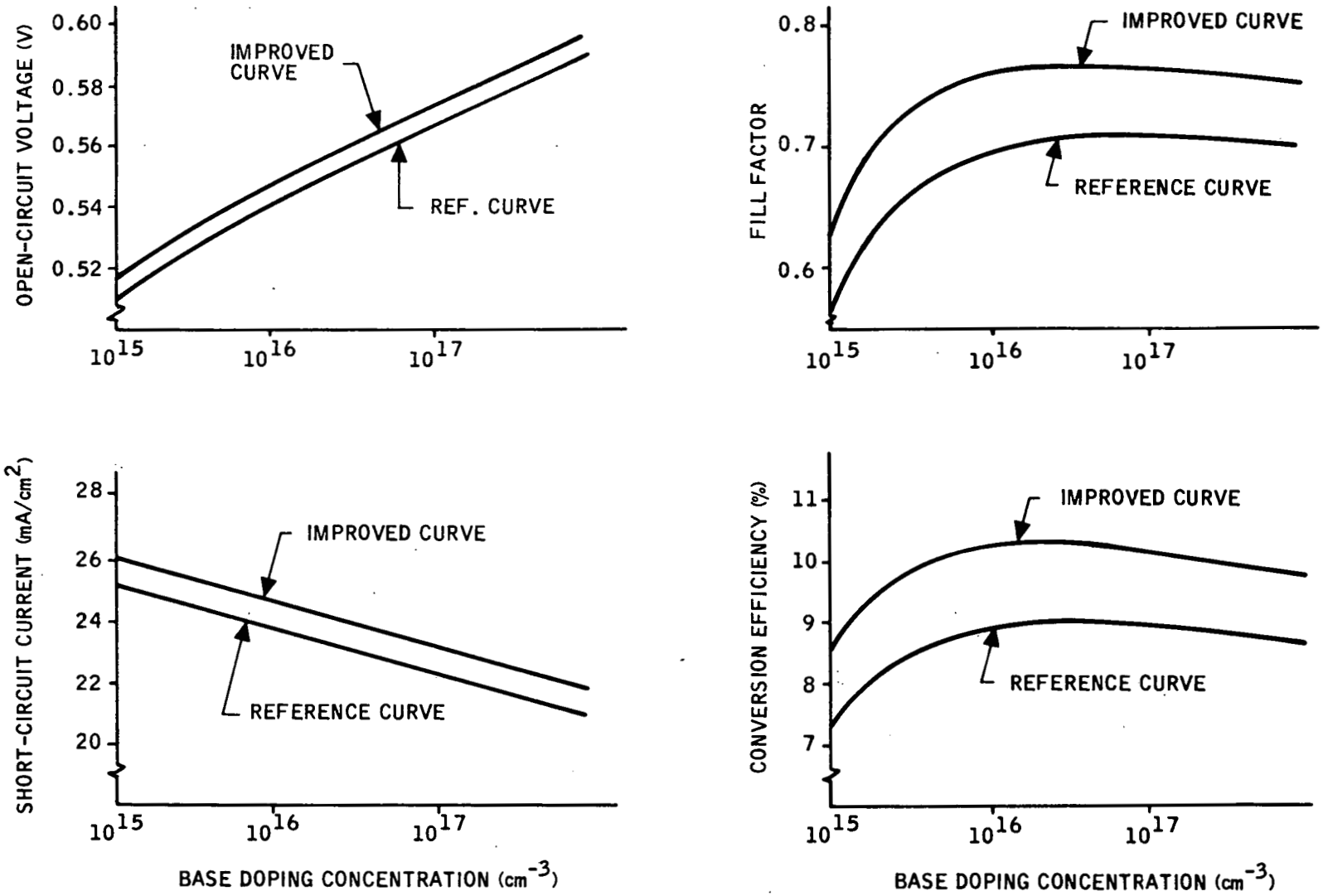


Figure 8. Effects of Simultaneous Improvements in J_{01}, R_sA, and J_{sc}

substrate dopings from 10^{15} boron/cm^3 to 2 x 10^{17} boron/cm^3 and find that L_n decreases rapidly as the doping increases. We also have verified that hydrogen passivation does improve the grain boundary performance.

A summary of our recent measurements is shown in Fig. 9 as a function of doping. The three lines represent approximate fits for the diffusion length within grains, average diffusion lengths, and diffusion lengths at grain boundaries, respectively. In spite of the large scatter in the data, there is a clear tendency for the diffusion length to decrease with doping. The reason for this decrease is not clear, since the boron itself does not produce recombination centers. However, single-crystal silicon does show behavior that is consistent with the behavior within a grain. The solid line is an average diffusion length for Czochralski cells taken from the literature.[1]

The decrease with doping is not understood. A possible explanation for the decrease is Auger recombination,[2] but this mechanism would only become significant at higher doping levels. An alternative explanation is that boron forms complexes with carbon or oxygen, and that these function as recombination centers. If this effect could be prevented, the diffusion length, and therefore the short-circuit current, would be significantly higher at a doping level of 5 x 10^{16}, and the efficiency of SOC cells would be about 10% higher.

The light-beam-induced current (LBIC) measurements of L_n made during the past quarter are summarized in Table 4. This table also includes the measurements of the aluminum-doped samples. The diffusion length is significantly lower in these samples, compared with boron-doped samples at the same doping level. The table also includes data for several edge-fed growth (EFG) diodes that were fabricated at Honeywell using samples supplied by JPL. The processing was identical to that used for our SOC cells and it is clear that the results are comparable. The EFG material contained significant material inhomogeneities, as does SOC material. The strange feature of

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[1] C.R. Fang and J.R. Hauser, 13th IEEE Photovoltaic Specialists Conf. (1978), p. 1318. The original data are from S.I. Soclof and P. Iles, 11th IEEE Photovoltaic Specialists Conf. (1975), p. 56.

[2] J. Dziewior and W. Schmid, Appl. Phys. Letts. 31, 346 (1977).

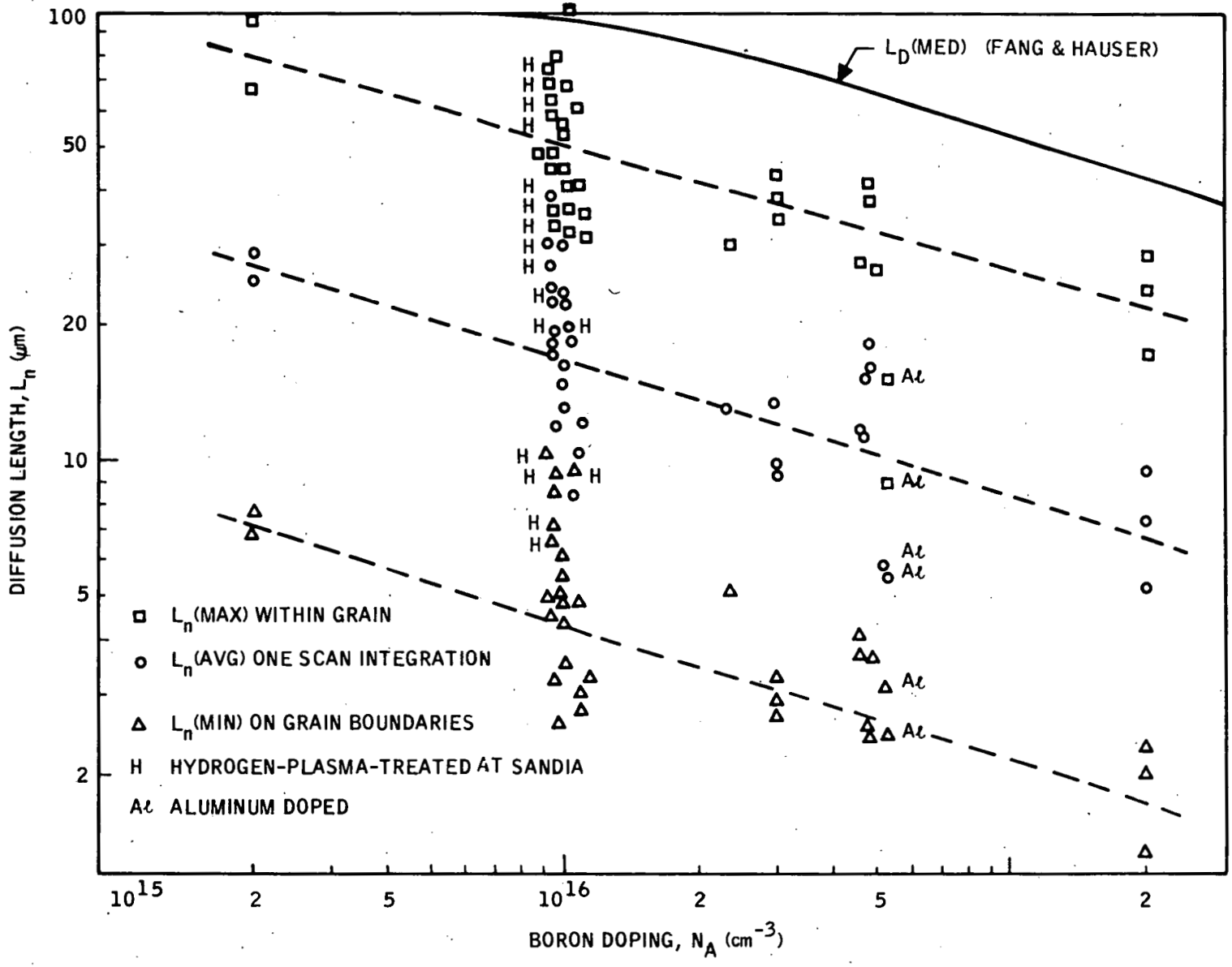

Figure 9. Diffusion Length as a Function of Doping

Table 4. LBIC Measurements of Diffusion Length

Cell No.	Base Doping (cm^{-3})	J_{sc} (mA/cm^2)	$\bar{L}$ (μm)	L_{max} (μm)	L_{min} (μm)	ΔL/L	1 - R	Comments
193-15-1-4	0.9×10^{16}	17.40	19.4	33.3	6.5	0.04	0.758	H-plasma annealed.
217-6-211	3×10^{16}	16.00	9.1	37.4	2.9	0.04	0.770	
217-5-111	3×10^{16}	15.66	13.3	42.4	2.9	0.05	0.738	
202-8-111	1×10^{16}	16.98	18.2	47.6	4.7	0.05	0.741	
225-6-111A	2×10^{17}	21.5	5.2	17.7	2.0	0.04	1.08	AR coated. Cells were shunted; small-area diodes were etched for LBIC.
225-6-111B	---	---	9.9	24.9	2.3	0.04	0.96	
225-6-211D	2×10^{17}	20.4	7.4	29.8	1.3	0.05	0.93	
225-6-111A	2×10^{17}	---	5.4	13.8	2.6	0.07	0.83	Electrolyte technique after etching off junction.
185-1-102	2.3×10^{15}	24.7	26.0	1.07	4.2	0.11	0.98	AR coated.
234-8-111	4.6×10^{16}	12.78	10.9	36.7	3.3	0.06	0.68	Arsenic ion implant.
240-3-211	4.6×10^{16}	15.88	15.3	37.9	2.61	0.06	0.75	
240-3-D7	4.6×10^{16}	15.0	18.1	43.4	3.5	0.06	0.75	
240-3-D5	4.6×10^{16}	16.2	15.9	26.3	2.4	0.06	0.80	
EFG-57-B3	---	14.57	18.5	53.8	2.3	0.07	0.65	(EFG numbers refer to EFG material supplied by JPL.)
EFG-57-B7	---	14.35	22.9	71.2	3.2	0.05	0.64	
EFG-57-B6	---	13.20	13.5	49.7	2.9	0.05	0.69	
EFG-57-A7	---	16.10	27.9	56.1	7.2	0.07	0.66	
EFG-57-A6	---	12.20	8.6	38.8	2.4	0.05	0.71	
EFG-57-A5	---	12.80	8.3	38.9	2.3	0.04	0.68	
EFG-57-A2	---	12.20	6.1	38.4	1.4	0.04	0.68	
235-4-211	4.6×10^{16}	14.12	11.8	36.2	3.1	0.05	0.68	Arsenic ion implant, 860C anneal.
237-4-111	4.6×10^{16}	13.20	12.6	37.5	4.7	0.05	0.68	Arsenic ion implant, 600C anneal.
EFG-58-A5	---	12.80	6.9	20.0	2.2	0.03	0.62	
EFG-58-A6	---	11.20	5.0	12.5	3.6	0.03	0.62	
EFG-58-B6	---	12.6	6.2	22.8	3.2	0.04	0.70	
199-3-111	1×10^{16}	17.26	8.2	40.9	4.80	0.07	0.82	
185-24-202	2.3×10^{15}	16.3	13.0	30.3	5.1	0.04	0.78	Low doping, end of run.
227-11-211	5×10^{16} Al	13.66	5.6	8.9	3.2	0.03	0.90	Aluminum doped.
227-5-111	5×10^{16} Al	14.12	5.8	14.5	2.5	0.03	0.87	
456-2	2×10^{16}	---	5.9	11.7	3.1	0.04	0.96	0.2 cm/sec growth, impure carbon.
465-4	2×10^{16}	---	4.8	8.8	3.1	0.04	1.02	Reused melt.
191-21	1×10^{16}	---	9.1	14.3	5.0	0.10	0.95	
239-1-TB	5.6×10^{16}	13.95	7.7	62.9	1.8	0.04	0.72	Top of sample, poor structure.

Table 4. LBIC Measurements of Diffusion Length (Concluded)

Cell No.	Base Doping (cm^{-3})	J_{sc} (mA/cm^2)	$\bar{L}$ (μm)	L_{max} (μm)	L_{min} (μm)	ΔL/L	1 - R	Comments
EFG-59-B1	---	14.06	10.9	47.1	1.5	0.03	0.58	
EFG-59-B2	---	14.20	13.2	46.7	2.8	0.05	0.56	
EFG-60-A5	---	16.4	25.8	56.3	2.7	0.04	0.61	Best EFG diodes.
EFG-60-A6	---	16.0	23.8	64.2	4.82	0.06	0.66	
210-1-D1	1×10^{16}	---	14.8	46.0	4.4	0.06	0.73	Tungsten diode, before H-plasma anneal.
		19.78	36.9	65.1	9.8	0.06	0.75	Tungsten diode, after H-plasma anneal.
211-1-D1	1×10^{16}	---	17.3	46.3	4.3	0.08	0.74	Tungsten diode, before H-plasma anneal.
		20.44	29.8	67.6	8.5	0.08	0.82	Tungsten diode, after H-plasma anneal.

EFG material was that the LBIC was very low in certain large regions of the material that did not have visible grain boundaries. In contrast, for SOC material, the regions of low L_n always correlate with smaller grain structure.

The H-plasma annealed samples are diodes that were prepared at Honeywell and treated in an H-plasma at Sandia.[3] The substrates were diffused and a back contact was applied. The cells then went to Sandia Laboratories for treatment at various temperatures. They were then returned to Honeywell and the cell fabrication was completed. The results, shown in Table 4 and labeled H in Fig. 9, show that hydrogen passivation at grain boundaries does indeed occur. The diffusion lengths at the grain boundaries are increased considerably.

A second batch of samples was recently returned from Sandia and is still being evaluated. These samples were metallized with a tungsten contact before being sent to Sandia, so that the LBIC data could be taken before and after the hydrogenation treatment. In these samples, the plasma annealing was longer, and the LBIC scans look much improved, within grains, as well as at grain boundaries. The results look very promising, and this effort will be continued.

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[3] C.H. Seagar and D.S. Ginley, Appl. Phys. Letts. 34, 337 (1979); also C.H. Seager, D.S. Ginley, and J.D. Zook, submitted to Appl. Phys. Letts.

ECONOMIC ANALYSIS (S.B. Schuldt)

Cost estimates for SOC panels were recently recalculated in 1980 dollars. Separate calculations were made for our target technology and for progress to date, the main difference being coating speed. Present coating speed is 0.6 mm/sec and target speed is 2.5 mm/sec. The figures in Tables 5 and 6 are the direct costs in the five major Intermediate Pricing Evaluation Guide (IPEG) categories. All the figures are based on an annual production of 5 million square meters of sheet silicon in <u>uncombled modules</u>. EQPT represents 7-year replacement costs of production equipment, including purchase price, installation/removal, and salvage; SQFT is direct production area in square feet; DLAB is direct production labor cost per year; MATS is direct materials cost per year; UTIL is annual cost of electricity used directly in production. It is important to realize that all quantities refer to the annual production quote in <u>assembled modules</u>, and therefore are yielded through cell fabrication and module fabrication process steps.

Table 5. Cost Data for Target Technology. See text for explanation of column headings.

Major Assumptions:

- 5 million m^2 per year production (yielded through solar cell module).
- 83% yield (ceramic panel to module).
- 4-mil polysilicon thickness.
- 2.25 m^2/hr silicon sheet grown each machine.
- $50,800 cost of silicon coating machine.

Task	EQPT	SQFT	DLAB	MATS	UTIL
Carbon coating	66,600	1,440	67,000	1,334,000[a] 23,914,000[b]	24,000
Silicon coating	18,620,840	8,800	1,842,900	1,353,300[c] 2,673,000[d] 19,683,900[e]	428,530
Inspect	1,111,000	5,310	1,867,000	---	12,400
Total	19,798,440	15,550	3,716,600	29,274,300[f] 48,958,200[g]	464,930

[a]carbon, [b]substrates, [c]argon, [d]crucibles, furnaces, insulation
[e]polysilicon, [f]excluding silicon, [g]including silicon.

Table 6. Cost Data for Progress-to-Date Technology. See text for explanation of column headings.

Major Assumptions:

- 0.54 m^2/hr silicon sheet grown each machine.
- Other assumptions as for Target Technology.

Task	EQPT	SQFT	DLAB	MATS	UTIL
Carbon coating	66,600	1,440	67,000	1,334,000[a] 23,914,000[b]	24,000
Silicon coating	77,587,000	36,660	7,680,500	5,637,900[c] 11,136,000[d] 19,683,900[e]	428,530
Inspect	1,111,000	5,310	1,867,000	---	12,400
Total	78,765,000	43,410	9,614,500	42,021,900[f] 61,705,800[g]	464,930

[a]carbon, [b]substrates, [c]argon, [d]crucibles, furnaces, insulation, [e]polysilicon, [f]excluding silicon, [g]including silicon.

Price per square meter is obtained from the IPEG formula

$$PRICE = 0.49\ EQPT + 135.8\ SQFT + 2.1\ DLAB + 1.3\ MATS + 1.3\ UTIL/QUAN$$

The SQFT coefficient is based on 1980 dollars and is therefore 40% larger than the 1975 dollar version. According to this formula, the price, assuming target technology, is \$11.65/m^2 added value and \$16.77/m^2 including hardened silicon costs. Assuming progress-to-date technology, the price would be \$23.99/m^2 added value and \$29.10/m^2 including silicon.

CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

- It was found that dendrite formulation could be lessened by increasing the soak-time. This suggests that a higher carbon and/or oxygen concentration in the melt may be the key to avoiding dendrites.
- Cells with heavy ($2 \times 10^{17}/cm^3$) boron doping exhibited an average conversion efficiency, η, of 8.6%, with a low J_{sc} as the limiting factor.
- In an effort to reduce melt contamination, an electric current was passed through the melt during dip coating. The resulting cells did not show a significant improvement in performance.
- Aluminum doping resulted in lower J_{sc} than boron doping (14.7% versus 17%) for similar doping concentrations.
- The progressive contamination of the melt by the mullite substrate was established. The contamination is a p-type dopant, probably aluminum.
- Empirical expressions were found which relate J_{sc}, J_{01}, R_sA, to N_B. These expressions provide a model which, when optimized, predicts a maximum conversion efficiency of 10.3%, for $N_B = 2 \times 10^{16}/cm^3$.
- Diffusion lengths are found to decrease rapidly as doping increases.
- Hydrogen passivation reduces the grain boundary recombination as shown by the significant increase in diffusion lengths.
- A projection of production costs of modules based on current technology (1/4 target speed for coating) yielded costs that were 1.7 times the target for added value and 2.0 times the target including silicon.

RECOMMENDATIONS

- Set up a system for performing in-house hydrogen plasma processing to passivate grain boundaries.

PROJECTION OF FUTURE ACTIVITIES

With regard to future SOC activities, we plan to:

- Fabricate dip-coated cells to use in efficiency investigation tests by evaluating processing variations.
- Achieve improved uniformity at high speed in the dip coater by improving the thermal profiles and the geometry of the liquid-solid interface.
- Achieve highly uniform temperature gradients in SCIM II.
- Demonstrate uniform coating at 0.06 cm/sec in SCIM II.
- Demonstrate uniform coating on slotted substrates.
- Fabricate cells in which the diffusion is followed by a slow controlled cool.
- Fabricate cells using hydrogen-passivated SOC.
- Use a two-step diffusion for preferential grain-boundary doping.
- Investigate the effect of various atmospheres during growth.
- Continue to evaluate diffusion lengths within grains using LBIC.
- Use finite-difference method to model thermal profiles and processes in SCIM II.

NEW TECHNOLOGY

There were no reportable "new technology" items uncovered during this reporting period.

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 10, 11, and 12, respectively.

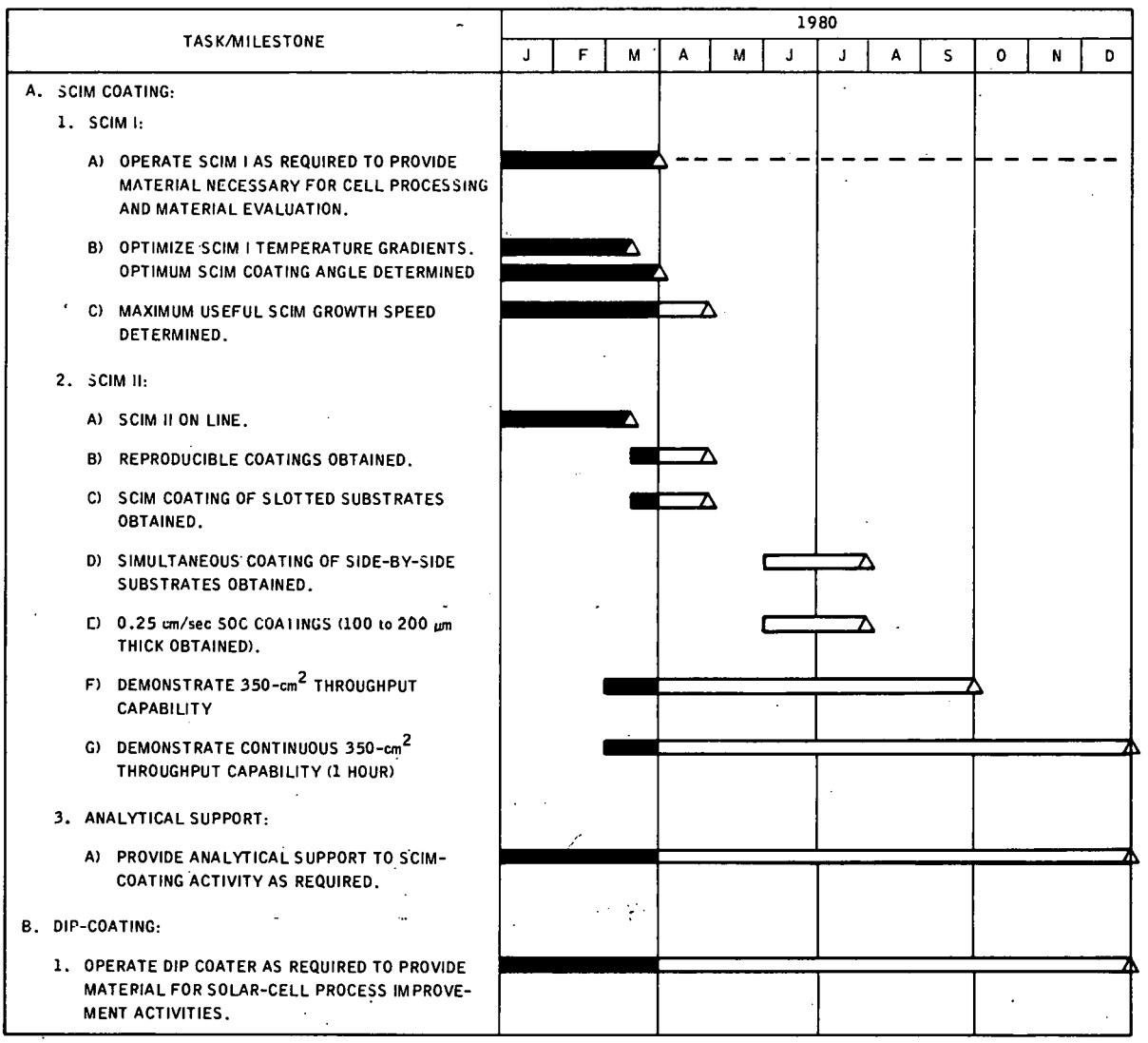

Figure 10. Updated Program Plan

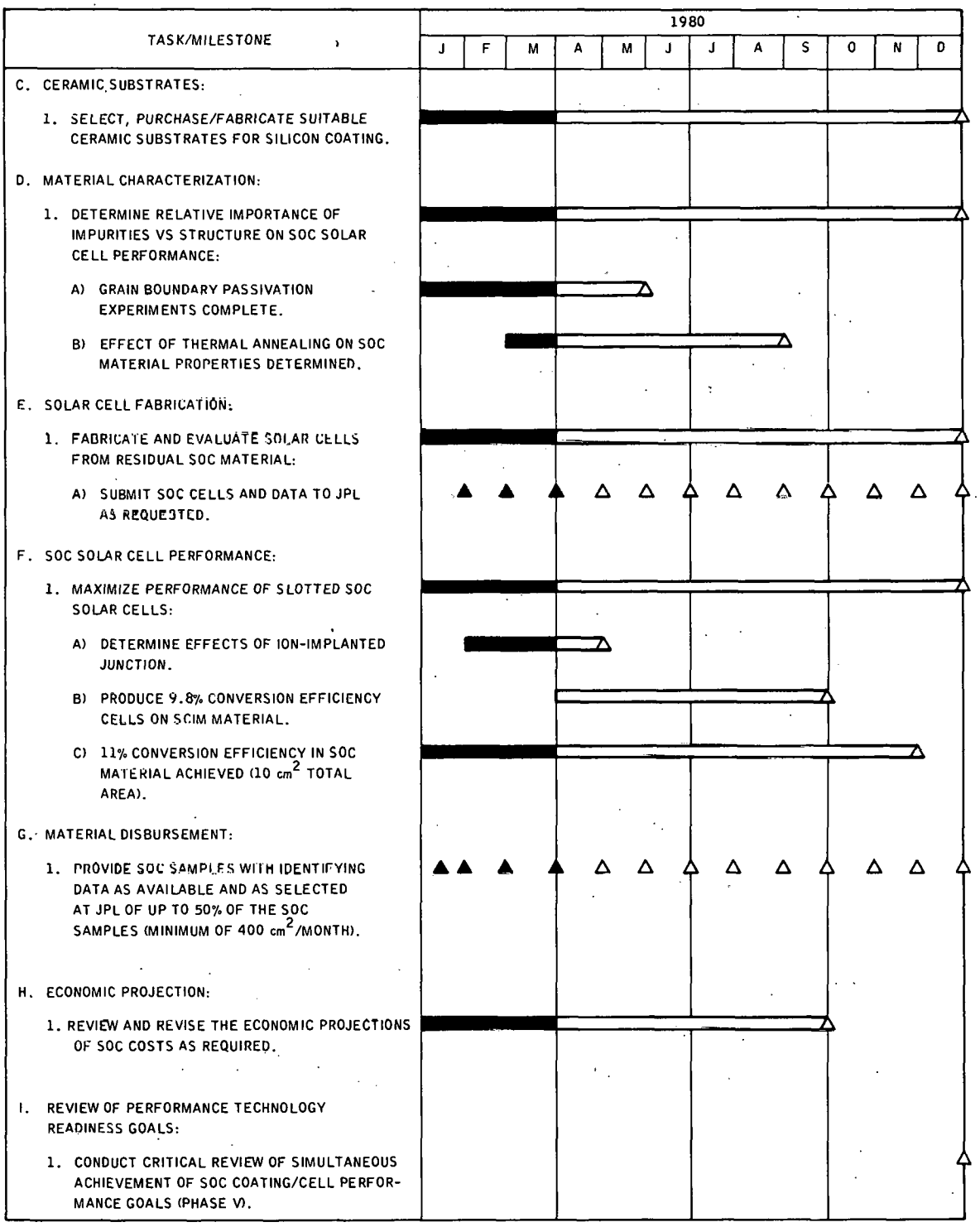

Figure 10. Updated Program Plan (Concluded)

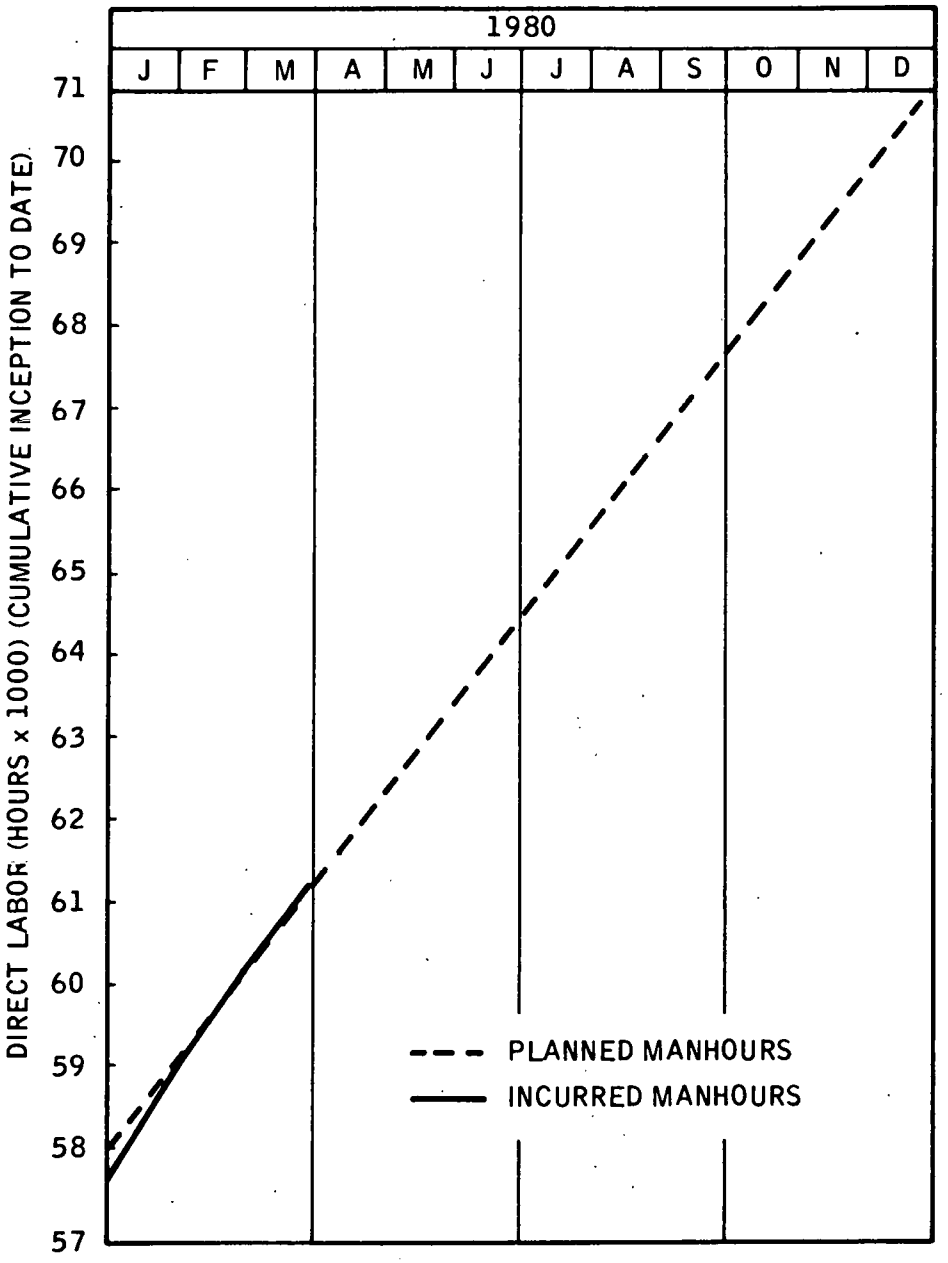

Figure 11. Updated Program Labor Summary

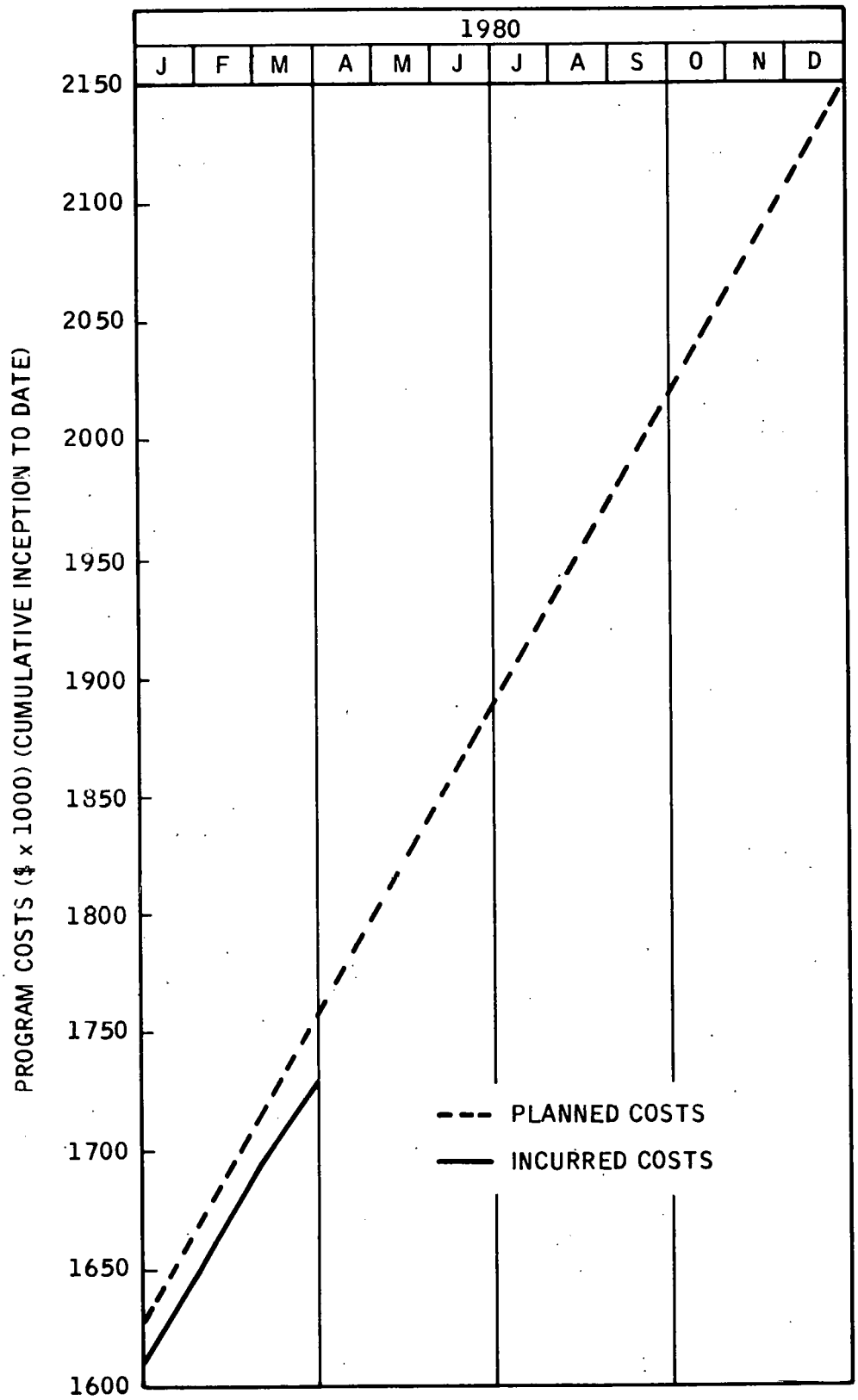

Figure 12. Updated Program Cost Summary

*U.S. GOVERNMENT PRINTING OFFICE:1980 740-145/551