A 500 MHZ PHASE GENERATOR FOR SYNTHETIC APERTURE RADAR WAVEFORM SYNTHESIZERS

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ABSTRACT

A GaAs Phase Generator ASIC has been developed using GigaBit's SC10000 standard cell library which produces the quadratic phase necessary to generate a linear-FM chirp waveform. Fully functional chips have been fabricated using a 3-layer metal, 0.9 μm gate E/D-MESFET process. Measured maximum accumulation rates vary from 450 MHz to 590 MHz. The chip is fully ECL and TTL compatible and is packaged in GigaBit's standard 132-pin ceramic package. The phase generator has been successfully tested in a prototype synthetic aperture radar at Sandia National Laboratories. Sample rates as high as 800 Msamples/sec have been synthesized using two phase generator/sine ROM combinations in parallel driving a TriQuint TQ6112 DAC.

INTRODUCTION

To obtain fine range resolution, synthetic aperture radars (SARs) generate a phase-continuous, frequency variant (pulsed linear-FM "chirp") waveform. Direct digital synthesis of this waveform provides flexibility and accuracy that cannot be achieved by conventional methods [1]. By digitally generating the phase of the chirp, and using this phase to drive a sine ROM and a digital-to-analog converter, various real-time phase and frequency changes can be made to the waveform to achieve greatly enhanced performance of the radar. The high clock rates and large bandwidths required for such waveforms necessitate the use of GaAs circuits.

The phase generator (PG) is designed for use in a real time SAR. The image quality of the SAR requires complete control of the various chirp parameters. The phase and frequency of the chirp must be precisely controllable, with the capability to change the phase offset ($\Delta\phi_T$) at any time during the generation of a pulse. Control of the phase is necessary to compensate for frequency-dependent phase errors in the RF portion of the radar, as well as to allow accurate motion compensation. Knowledge of the current instantaneous frequency of the chirp is necessary for this phase compensation, as well as to use in controlling the amplitude of the analog chirp waveform, which is also frequency dependent. The phase generator provides these capabilities as well as the flexibility to generate chirps with bandwidths up to 720 MHz.

These controllability requirements preclude the use of a phase-locked loop synthesizer, and the power and system requirements make a discrete digital implementation unacceptable. The previous discrete logic implementation of the waveform synthesizer was an ECL 4k RAM bank design. The synthesizer board was 7" x 7", and consumed in excess of 40 W. This design was limited to a maximum pulse length of 20 μsec, and a sample rate of 200 Msamples/sec. These limitations are either eliminated or greatly reduced by using an ASIC implementation consisting of the phase generator chip, a sine look-up table ROM [2], and a high-speed DAC. Figure 1 shows the basic configuration with frequency feed-back.

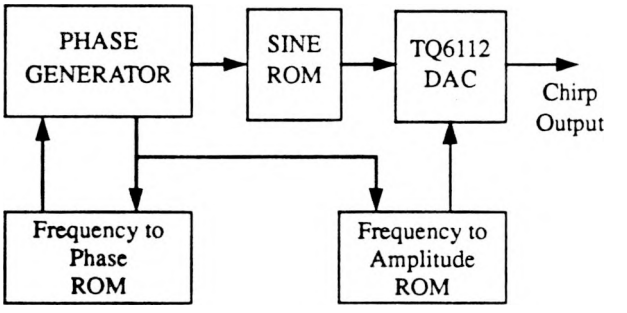

Figure1: Basic DDS configuration with phase and amplitude frequency compensation.

ARCHITECTURE

Figure 2 shows the block diagram of the phase generator. The phase generator produces a quadratic phase according to equation (1).

$$P(T) = (f_0 - 0.5*K)T + 0.5*K*T^2 + \Delta\phi_T \qquad (1)$$

where f_0 = start frequency
K = chirp rate
T = discrete time increment
$\Delta\phi_T$ = phase correction for time T

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This quadratic phase is generated using a double accumulation. The frequency and phase accumulators (FACC & PACC) are 24 bits long with 4-bit pipeline sections, permitting a start frequency resolution of 29.8 Hz and a chirp rate resolution of 14.9 kHz/μs when using an accumulation clock f_s = 500 MHz. The output of the frequency accumulator represents the instantaneous frequency, and feeds the phase accumulator. The 8 msb of FACC (IF) are also output for system nonlinearity compensation, after passing through an equalizer (EQ) to time-align the bits. The output of PACC is the quadratic phase for generating the chirp. The 12 msb of this output are used as address bits (ADDR) to drive the sine ROM. This number of bits was chosen to keep the phase quantization noise power (67 dB down from the signal) well below the theoretical amplitude quantization noise power resulting from the 8-bit DAC (50 dB down) [3].

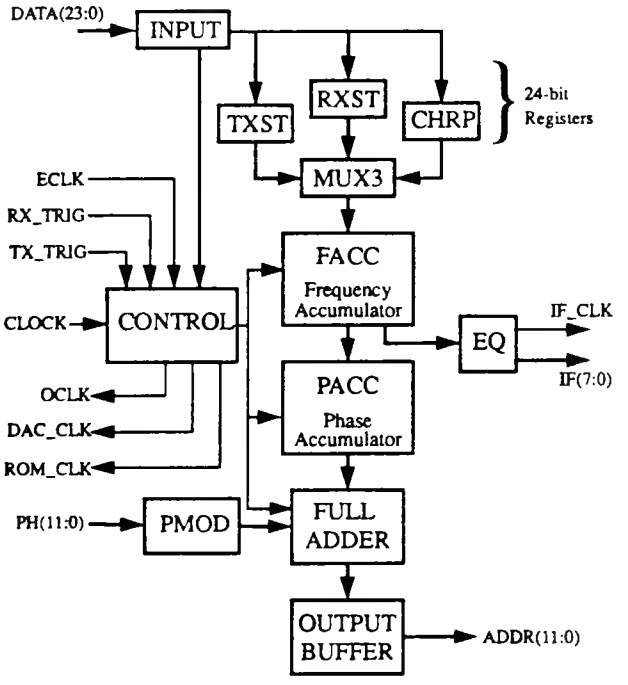


Figure 2: Phase Generator block diagram.

The FULL ADDER block and the PMOD block provide the capability to change the phase of the chirp. The 12-bit external phase value (PH) applied at PMOD is added to the 12 msb of PACC in the FULL ADDER block. The FULL ADDER realigns the phase bits, and the data is converted to ECL levels. PMOD contains data synchronization circuitry which checks the stability of the TTL phase input before clocking it into the FULL ADDER. This prevents glitches in the output phase of the chip due to the misalignment of the PH data.

The control portion of the chip generates the internal accumulator clock and control signals, the external ROM and DAC clocks, and an assortment of external continuous clocks for use throughout the radar system. Accumulation is initiated when either of two trigger signals, TX_TRIG or RX_TRIG, goes high. When the trigger signals are low, the chip is reset. The frequency accumulator gets its start frequency from either RXST or TXST, depending on which trigger is selected. After loading this start frequency into the frequency accumulator, all subsequent accumulations use the chirp rate value stored in CHRP as input. The accumulator clock (ACC_CLK) can either be generated internally or externally (from ECLK). The external option allows multiple phase generator chips to be used in parallel to increase the sample rate at the DAC.

The input clock accepts ECL levels for f_c < 500 MHz, but for f_c up to 1 GHz a clock with greater than 1 V peak to peak swing is required. RX_TRIG and TX_TRIG are both ECL in order to provide the sharp edges necessary for precise timing of the chirp. The PH input bus and the IF output bus are TTL in order to accommodate TTL EPROMs in the phase feedback loop (start phase vs. frequency control). IF is supplied with a clock (IF_CLK) signifying when data is valid. The internal accumulator clock is sent off chip as OCLK, to be used with multiple phase generator configurations. The DAC_CLK and ROM_CLK can be independently delayed through a programmable clock control word, allowing greater flexibility in the board level timing requirements. The DAC_CLK, ROM_CLK, OCLK, and the 12-bit phase output are all 25Ω ECL drivers, allowing each phase generator to drive two ROMs and two DACs. This drive capability together with the accumulator clock synchronization capability allows double side-band (DSB) radar implementations with effective sample

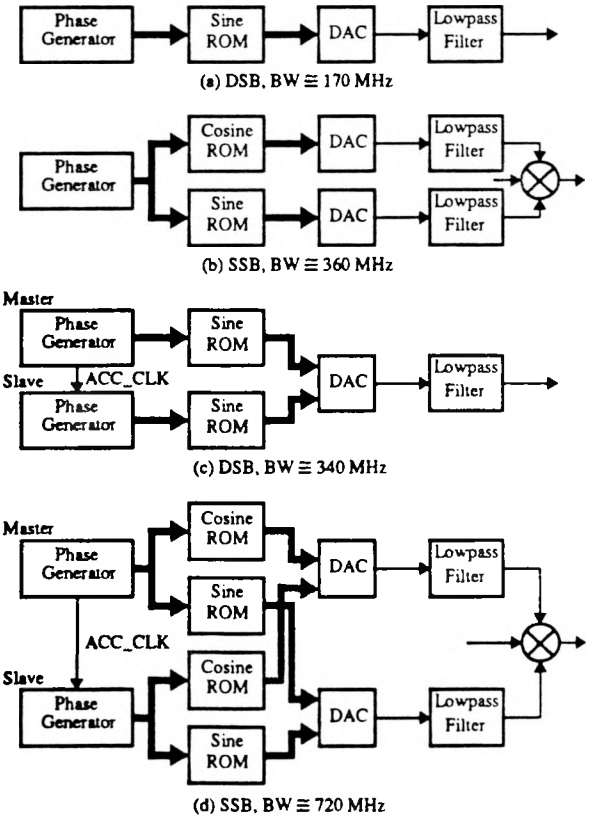


Figure 3: Synthesizer configurations, ACC_CLK = 500 MHz

rates as high as 1 GHz, and single side-band (SSB) implementations with effective sample rates as high as 2 GHz (figure 3).

PROCESS

The phase generator is manufactured using GigaBit Logic's production proven 0.9 µm gate E/D MESFET process [4]. The process uses 4" LEC wafers, gate recessing, Si+ implantation through Si_3N_4 cap, 10X DSW photolithography, dry etching and enhanced lift-off techniques. The process is further improved by using a very thin Si_3N_4 cap, low implantation energy and rapid thermal annealing to obtain a shallow channel, which provides higher K values and transconductance. It also makes available 3 levels of gold interconnect and a MIS capacitor. Two pinch off voltages are available in the process, -0.7 V and +0.1 V for depletion and enhancement FETs respectively. The K value and transconductance of the depletion mode FET (measured at V_{gs} = 0V) are 135 $\mu A/V^2\mu m$ and 160 mS/mm, respectively, while for the enhancement mode FET, they are 185 $\mu A/V^2\mu m$ and 190 mS/mm (measured at V_{gs} = 0.6 V).

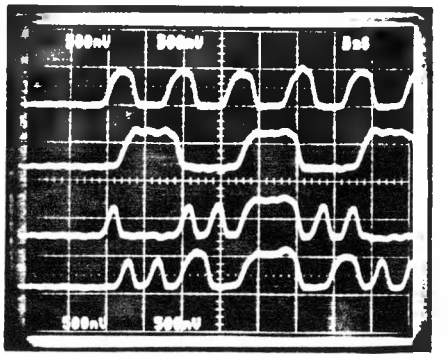
CIRCUIT DESIGN

The logic gates used in the design of the phase generator are low power, high performance standard cells from GigaBit Logic's SC10000 library. The library uses differential source-coupled logic (SCL), similar to differential ECL (also known as Current Mode Logic, CML). Using a novel biasing technique that adjusts tail current by monitoring FET and resistor parameters over process and temperature variations, the cell requires very small voltage swing while maintaining good noise margin [5].

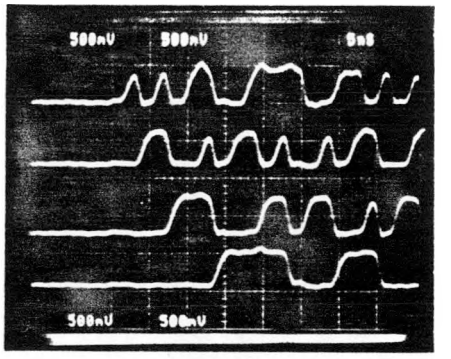
DEVICE RESULTS

Fully functional phase accumulators were obtained and characterized. The DC functionality of the chips were checked on the wafers and packaged parts were tested using a commercial tester operating at 1 MHz. Greater than 95% fault coverage was obtained.

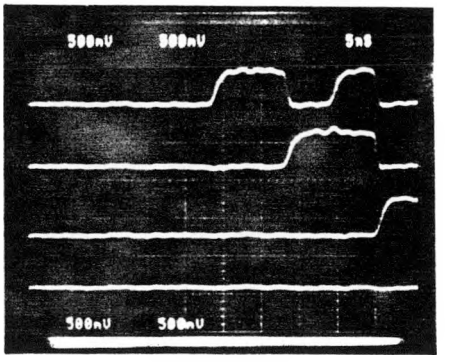
Layout simulations showed the 4-bit accumulator and adder blocks to have a carry ripple time of less than 1.5 ns. High speed operation was verified by programming the part using the commercial tester, then using a high speed signal generator for the clock input. The output address bits were observed and captured on an oscilloscope. The tester provided the RX_TRIG signal to the chip in a loop mode operation and also the trigger signal to the oscilloscope. Figure 4 shows the output waveforms at a clock frequency of 500 MHz for the case where the start frequency is programmed as 5 and the chirp is set to 1. The frequency increments each cycle in the following manner: 5, 6, 7, 8, 9 etc. Therefore, the output phase sequence will be 5, 11, 18, 26, 35, 45, 56 etc. In the photographs, the output of the accumulator is seen along a vertical axis (i.e. the same time) and computed by converting the binary bits A0 through A11 to decimal, with A0 being the lsb. Only 4 outputs could be viewed on the oscilloscope at the same time, and therefore a one-bit overlap (A0 to A3, A3 to A6, A6 to A9) was inserted in the photos to make sure that the oscilloscope trigger point was the same between pictures. Outputs A10 and A11 were low (not shown).



(a) A0 to A3



(b) A3 to A6



(c) A6 to A9

Figure 4: Phase Generator output, RXST=5, CHRP=1.

The die measures 5.1 mm x 5.1 mm (figure 5) and is packaged in GigaBit's standard 132 pin ceramic package. Measured maximum accumulation rates vary from 450 MHz to 590 MHz over a temperature range of 10°C to 70°C. The power dissipation of the chips vary over 4.1 W to 5.0 W (nominal) using standard ECL and TTL supplies.

Figure 5: Phase generator die (5.1 mm x 5.1 mm).

SYSTEM RESULTS

Two phase generators (PGs) were used in a SAR system using the configuration shown in figure 3(c). The PGs were driven by an 800 MHz system clock, which was generated by a surface acoustic wave device. The accumulation clock was programmed to 400 MHz, with the master PG supplying the accumulator clock to both PGs. The master PG supplied an 800 MHz DAC_CLK to the TQ6112 DAC, and the slave provided the SELECT signal to the DAC to multiplex between the 8-bit sine ROM inputs.

The printed wiring board containing the chirp synthesizer is a 12-layer glass-epoxy board occupied mostly by discrete ECL gates, flip-flops, and counters. The synthesizer occupies a total space of approximately 22 in^2, which includes the two phase generators, two sine ROMs, two PROMs, the TQ6112 DAC, an HADC77200 DAC (part of the amplitude control loop), and various capacitors and inductors for controlling power plane noise. The DACs were contained in a metal isolation can placed on the board to eliminate external EM interference. Board layout induced power plane noise limited the out-of-band energy in the output chirp to 35 dB down from the signal band. The theoretical noise floor is 50 dB down (determined from the number of bits driving the DAC). Analysis on the performance of the phase generator showed it to be functioning properly despite the noisy power planes.

APPLICATIONS

The phase generator chip can be used in a number of phase and frequency modulation applications. The 12-bit phase modulation input allows better than 0.1° phase resolution, and the 24-bit accumulator width allows a frequency resolution of 29.8 Hz at f_{acc} = 500 MHz (directly proportional to the accumulator clock frequency f_{acc}). Combining the phase generator with the sine ROM [2] allows synthesis of double and single sideband signals (CW or chirp), as well as various PSK and FSK modulated signals. Its flexibility also allows various SAR modulation techniques which help eliminate range ambiguity problems.

CONCLUSION

The digital phase generator ASIC has been successfully designed and fabricated using GigaBit Logic's SC10000 library. Maximum clock frequencies of 590 MHz have been demonstrated over a temperature range of 10°C to 70°C. The nominal power dissipation of the chips vary from 4.1 W to 5.0 W.

The phase generator chip has performed well as part of a chirp synthesizer in a synthetic aperture radar system using a parallel configuration together with 2 custom sine ROMs and a TriQuint TQ6112 DAC. The synthesizer used a sample rate of 800 MHz. The resulting chirp power spectrum had rejection levels greater than 35 dB. The size and controllability of the chip enabled the SAR to fully meet the system specifications using only a fraction of the board space which would have been required with discrete device implementation.

ACKNOWLEDGEMENT

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