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PHASE I OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE LOW COST SILICON SOLAR ARRAY PROJECT

Motorola Report No. 2258/4

Annual Technical Report

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ANNUAL TECHNICAL REPORT

FEBRUARY, 1977

JPL CONTRACT NO. 954363

BY

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1.0 SUMMARY

This annual report is a critical review and compilation of work performed to analyze, both technically and economically, the state of technology readiness for the automated production of solar cells and modules. The long-term objective solar module characteristics include a selling price of less than $.50/peak watt and a mean-time-before-failure (MTBF) of 20 years in any terrestrial environment. While efficiency is important to attaining the cost goal, it is a most significant factor in array economics; accordingly, this program has stressed high efficiency, with a suggested cell goal of 15%.

The analysis emphasized technical evaluation of individual process steps first, and then concentrated upon process sequences for making solar cells and modules. Further analysis was performed to yield a detailed cost study of individual process steps; this was applied to the cost analysis of potential process sequences. Potentially economical process sequences formed from process steps deemed to have high technical merit were then identified. Potentially promising technologies needing further development to achieve satisfactory maturity were then identified. It is the conclusion of this study that, while specific areas of technology need advanced development and the source of silicon needs definition, no fundamentally new technology needs to be developed to permit manufacture of solar cells which will meet the 1985 LSSA Program cost goals.

2.0 INTRODUCTION

Phase I of the Automated Array Assembly Task, LSSA Program, is concerned with a comprehensive assessment of the improvements in existing technology that will be needed to develop, within a period of no more than 10 years, an industrial capability for low cost, mass production of very durable, efficient silicon solar photovoltaic modules and arrays.

This program was organized to incorporate solar cell design, process adaptation, process sequencing optimization, technology assessment, solar cell fabrication, interconnection and encapsulation, and cost analysis in an interrelated way such that the final choices for particular process sequences would be realistic and have a high probability for success. Out of the study would also come the identification of areas of technology that could contribute significantly to the long term objectives dependent upon the successful conclusion of additional, specific R&D effort.

There have been interactions and heavy inderdependence upon other Tasks of the LSSA Program, especially upon the tasks responsible for development of a process to supply silicon sheet for solar cell fabrication, and encapsulation of solar cell panels. This interdependence has required, in some instances, assumptions about future results in order to permit progression toward meaningful conclusions in the time frame of this program.

3.0 TECHNICAL DISCUSSION

3.1 DESIGN IMPROVEMENTS

In order to effectively evaluate processes and process sequences, it was first necessary to establish minimum, or baseline, design considerations for the solar cell and its constituent elements. It has been Motorola's contention throughout this contract that it is necessary to develop a solar cell design model (or design models) which effectively characterize the highest efficiency silicon solar cell capable of being produced utilizing current or anticipated semiconductor processing techniques, subject to the major constraint that the estimated cost in dollars per watt of the final assembled and installed array of silicon solar cells be minimized. Any process sequence, thus, must be based on a solar cell design model which reflects current state-of-the-art practices as well as additional concepts not currently incorporated in solar cells but envisioned as likely to contribute to future solar cell improvement. The following sections first treat basic design considerations, and then discuss specific solar cell design features.

3.1.1 BASELINE DESIGN MODEL CONSIDERATIONS

A solar cell can be considered as a co-operative group of individual elements, including an antireflection coating, the front surface, a junction region, a substrate, a back surface, and front and back metallizations. Each element can be characterized with a list of desirable properties.

3.1.1.1 ANTIREFLECTION COATING

Desirable features of an antireflection coating on a solar cell include those which:

(i) optimize the transmission of incident photons into the silicon material;

(ii) promote the lowest concentration of surface-state recombination centers at the coating-silicon interface;

(iii) aid in establishing an electric field within the silicon (near the surface) which retards minority carrier flow toward the front surface and recombination at the front surface; and

(iv) passivate and isolate the P-N junction perimeter.

3.1.1.2 FRONT SURFACE

The silicon solar cell should possess a silicon front surface condition which:

(i) minimizes surface defects and maximizes minority carrier lifetime near the silicon surface;

(ii) minimizes surface recombination velocities;

(iii) maximizes the absorption of incident photons by the silicon, complementing the antireflection coating;

(iv) refracts the incident light to optically enhance the possible photon path lengths through the silicon substrate;

(v) promotes the adhesion of metal ohmic contacts.

The surface may be that of an as-grown sheet of silicon, or it may be polished or etched. When the orientation allows, as discussed Section 3.1.2, texture etching can provide a highly controllable, cost-effective way of obtaining most of the properties listed above while accruing additional benefits for solar cell design. A model for a textured front surface is discussed in further detail in Section 3.1.2 of this report.

3.1.1.3 JUNCTION REGION

A study performed on this contract, and included in Section 3.1.3, has concluded that Schottky barrier cells are less favorable than those utilizing P-N junctions. Accordingly, we consider in our baseline design model only the

silicon P-N junction solar cell, which must have a thin, front surface region with an electrical conductivity opposite that of the substrate (e.g., N type surface region on a P type substrate) which:

(i) forms a metallurgical P-N junction;

(ii) is amenable to formation of an ohmic contact without significant degradation of solar cell performance;

(iii) has a low surface recombination velocity, or is designed to effectively minimize surface recombination effects (e.g., has a large built-in drift field);

(iv) has sufficiently high minority carrier lifetime;

(v) has a sufficiently low value of sheet resistance; and

(vi) maximizes the collection efficiency for short wavelength photons.

Property (vi) implies that the P-N junction depth below the front surface be as shallow as can be allowed, subject to satisfying the other five requirements. Traditionally, only junction depths of about 0.5 micron or less have been used, and the best (violet-type) cells have junction depths closer to 0.1 micron. This requirement makes attainment of property (v) more difficult.

3.1.1.4 SUBSTRATE

The solar cell must have a silicon substrate which:

(i) has high minority carrier lifetime for a maximum photo-current generation;

(ii) has a sufficiently high impurity doping level to obtain high open circuit voltage and low electrical resistance;

(iii) is optically thick enough to efficiently absorb an appreciable fraction of incident long wavelength photons but is mechanically

thin enough to conserve silicon; and

(iv) has a low minority carrier recombination velocity at the back surface, or is designed to have a large drift field to effectively minimize back surface recombination effects.

Minority carrier lifetime is of extreme importance to efficient silicon solar cell performance; however, lifetime values practically obtainable may eventually be dictated by economical silicon purification processes. Under more immediate control, and of particular interest insofar as a design model is concerned, is the optical thickness of the silicon substrate. The optical thickness may be enhanced (for a given mechanical thickness) by forcing absorption paths to be other than perpendicular to the cell plane (or P-N junction), and additionally through multiple internal reflections.

3.1.1.5 BACK SURFACE

The solar cell should have a silicon back surface condition which:

(i) minimizes surface defects and maximizes minority carrier lifetime near the silicon surface;

(ii) minimizes surface recombination velocity; and

(iii) reflects unabsorbed incident radiation which passes through the substrate and reaches the back surface.

By reflecting photons reaching the back surface, the optical thickness of the substrate can be at least twice as great as the physical thickness. Moreover, unusable infrared wavelength photons can be re-radiated from the front of the solar cell rather than absorbed at (or near) the back surface.

3.1.1.6 METALLIZATIONS

The solar cell must have metallization contacts to both front and back surfaces which:

(i) provide ohmic electrical contact to the opposite sides of the P-N junction;

(ii) allow reliable, low-loss interconnection with other solar cells and with external circuits;

(iii) minimize solar cell internal series resistance;

(iv) cover (and therefore shadow) a minimum of the cell front surface area; and

(v) allow optical reflection from as large a fraction as possible of the back surface area; and

(vi) are corrosion resistant.

3.1.2 TEXTURED SURFACE

A textured surface, consisting of a uniform distribution of minute pyramids as shown schematically in Figure 3-1, causes light reflected from the first impingement on the solar cell surface to strike the solar cell at least a second time (assuming initial normal incidence). This second impingement increases the amount of light absorbed in the solar cell, improving cell efficiency by reducing the total amount of light reflected from the cell. Incoming, reflected, and refracted ray traces of light normally incident to the overall solar cell, Figure 3-2, show the multiple reflection features of this surface topography.

Another major effect of front surface texturing is that, since light is refracted into the silicon at an angle to the normal of the overall solar cell plane, more light is absorbed within a given thickness of silicon than would occur with normally incident sunlight on a smooth-surfaced solar cell. This

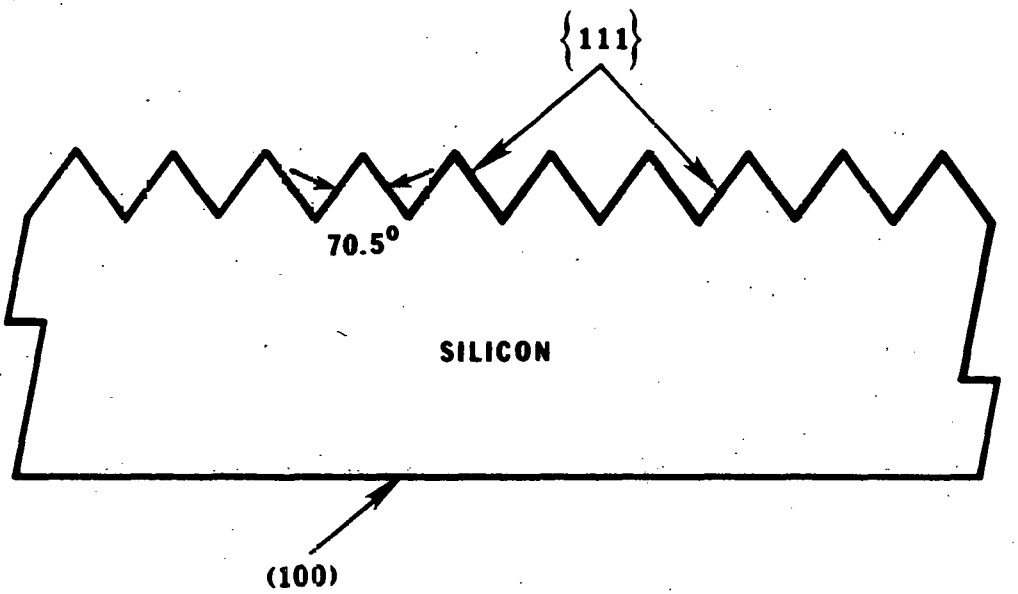

FIGURE 3-1: Cross-sectional diagram of silicon (100) wafer showing geometry of textured surface having {111} faceted pyramids.

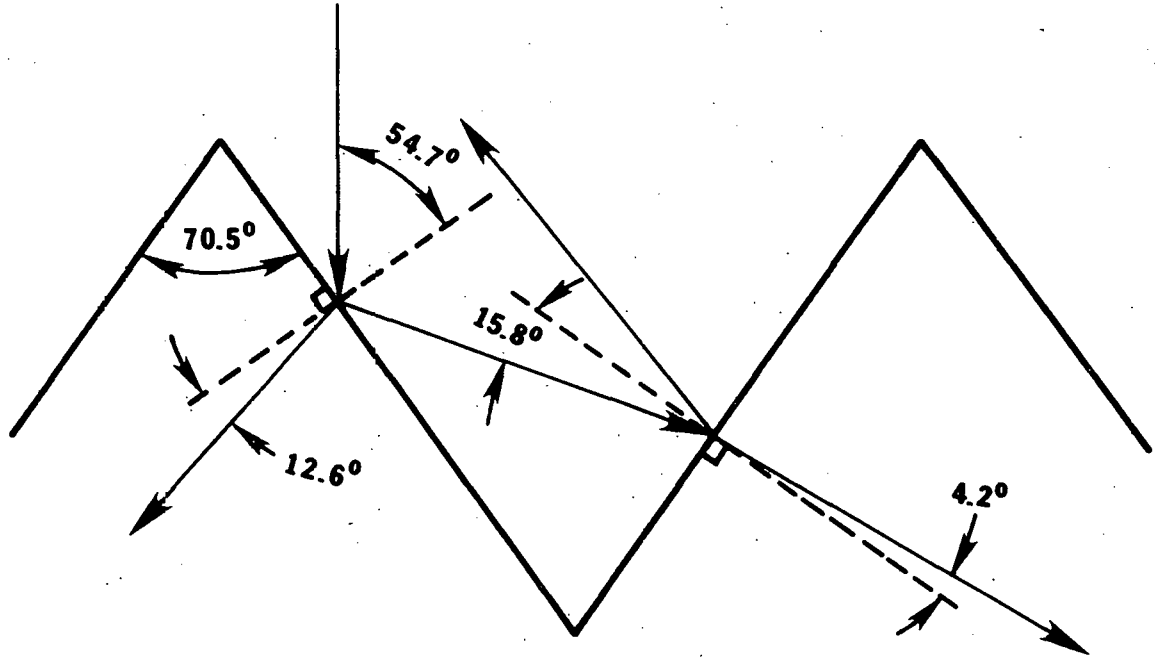

FIGURE 3-2: Diagram of reflected and refracted ray traces and angular relations for light normally incident to the substrate (100) plane of a textured surface solar cell.

property can be separated into its effects in two regions: a microscopic region involving the volumes immediately adjacent to the p-n junction, and a more macroscopic region involving the bulk of the silicon below the junction.

In the microscopic region near the junction, it is first assumed that the surface relief of the pyramidal structures is large (averaging greater than 10μ) compared to the p-n junction depth (less than 0.5μ). Light normally incident to a textured surface solar cell strikes the surface facets at an angle near 55°. Figure 3-3 diagrammatically demonstrates the refracted paths of a normal incidence light beam on a smooth surface cell and also in an analogous fashion on a textured surface facet. The optical path length of the refracted beam within the region of the junction is greater than the normal path length by a factor of $\frac{1}{\cos\phi}$ in the case of the textured surface. This increased path length has an effect equivalent to increasing the absorption coefficient of light in the silicon by the same factor (over the smooth cell normal incidence beam). Thus, within the region near the junction, more light is absorbed, creating more carriers, and increasing cell efficiency for very shallow junctions. Assuming that the index of refraction of silicon is 3.75, the angle ϕ is approximately 12.6° and $\frac{1}{\cos\phi}$ is approximately 1.025. While this near surface (microscopic) phenomenon is effective throughout the solar spectrum, it is most significant in the short wavelength end of the solar spectrum where the silicon absorption coefficient is greatest. The phenomenon is, thus, expected to enhance somewhat the blue response of the solar cell.

A larger effect is seen in the macroscopic region within the bulk of the cell below the microscopic junction region. Light incident normal to the plane of the overall cell is refracted by the textured surface through an angle of 12.6° from the normal to the facet. (Figure 3.2). This is equivalent to an angle of 42.2° from the normal of the overall cell, i.e., ϕ=42.2°, Figure 3-3, so that the path length through the bulk is increased

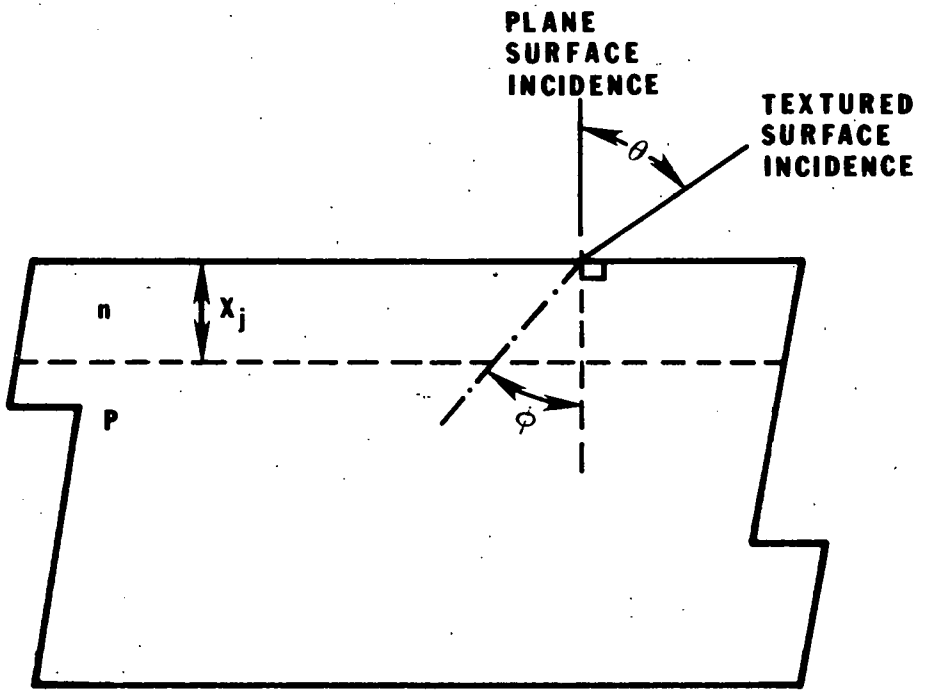

FIGURE 3-3: Representation of increased absorption path length of textured surface light ray trace compared to trace normal to a plane surface.

by a factor of $\frac{1}{\cos 42.2^\circ}$, equal to 1.35. This is the equivalent of increasing the path length through the bulk by 35%, making each three units of solar cell thickness look like four units of thickness. Restated, the number of carriers created in an optical path length of four thickness units is generated within three mechanical thickness units of the front surface and the p-n junction. This makes the cell far more responsive to the longer wavelengths of incident sunlight, which have smaller absorption coefficients in silicon than the short wavelengths.

A further effect of the angle of travel of the refracted beam through the bulk occurs at the back surface of the cell. If the back surface of th cell is not textured and is a plane, all light refracted through the front textured surface can be shown to strike the back surface of the cell at an angle exceeding a critical angle, resulting in total reflection from the back surface toward the front surface. (The condition for total internal reflection

$$n_{Si} \sin \varepsilon = n_{ext}$$

yields angles of about 15.5° for air and near 24° for most plastics and SiO_2.) Total internal reflection occurs when the angle ϕ exceeds the angle ε, Figure 3-4. The angle ϕ for normal incidence on the textured front surface is 42.2°, thus satisfying the condition for total internal reflection. Non-normal incidence will produce different values for the angle ϕ, but the angle ϕ will always satisfy total internal reflection conditions.

Total internal reflection from the back surface can be advantageously utilized in one of two ways. First, the internally reflected beam will be further absorbed on its second pass through the material, again creating more carriers and increasing cell efficiency. Alternately, a thinner cell (conserving silicon) could be made to display the same efficiency as a thicker standard cell. The magnitude of the effect of the second pass absorption will be, of

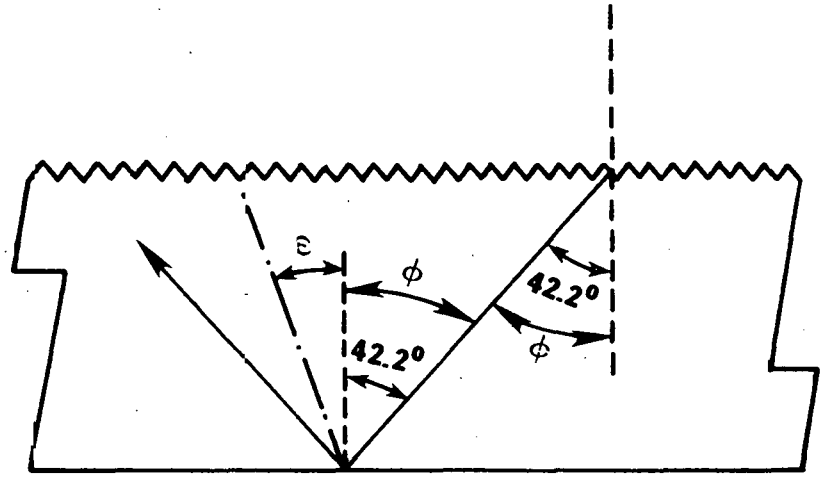

FIGURE 3-4: Path of beam refracted from textured surface illustrating total internal reflection from back surface if the brewster angle $\varepsilon < 42.2°$.

course, a function of the total cell thickness and the minority carrier lifetime of the cell substrate.

More subtle advantages also occur with a textured surface. The textured surface, formed by etching, leaves a surface which is relatively free of work damage. A plane surface, on the other hand is often achieved by polishing, leaving a finite degree of work damage in the crystal surface layer. Such damage is known to adversely affect both carrier lifetimes and surface recombination velocity; it can propagate during high temperature processing, aggravating the damage. This additional advantage of textured surface etching will not apply to solar cells fabricated from silicon ribbon (if it is directly grown to have smooth, damage-free surfaces), or from chem-etched wafers.

For any unit area in the plane of the substrate, the (100) plane, the corresponding area of the textured surface described above will be a factor of $\sqrt{3}$ times larger. When ohmic metal contacts are applied, this increased surface area will serve to reduce the magnitude of the contact resistance. Furthermore, the textured surface itself can promote better metal adhesion to the silicon surface.

Finally, the mechanism causing reduced reflection of incident light discussed at the outset of this section will also lessen the requirements on antireflection coatings chosen for the solar cell surface. For example, the differences in total reflection obtained when using a perfectly matched antireflection coating and when using a somewhat less than perfect one will be much less pronounced, perhaps allowing coatings to be chosen for increased cost-effectiveness and convenience of processing.

3.1.3 SCHOTTKY BARRIER SOLAR CELLS

Silicon solar cells can be broadly classified as either Schottky barrier solar cells or P-N junction solar cells. Either, in theory, could meet the goals of the LSSA Project. In order to obtain the LSSA Project goal of silicon solar cell modules which operate with at least 10% efficiency, it is necessary that the individual cells operate at greater than 10% efficiency. This is required since module optical transmission losses, thermal resistance, cell packing density, and space utilization will lower the overall efficiency.

A survey of the recent literature on Schottky-type cells has been performed, and a list of references in chronological order appears at the end of this section. No reference has been found which reports large area silicon Schottky-type solar cells which exhibit greater than a 9.5% efficiency.[9] (Schottky-type cells with 15% efficiency have been reported on GaAs.[15]) Recent professional society conferences have given no indication that a breakthrough in the present state-of-the-art of silicon Schottky cell technology is imminent, although studies are continuing. In fact, although theoretical computations have been mentioned in the literature claiming that the upper limit on conversion efficiency is slightly better for the Schottky barrier cell than for a P-N junction cell,[7] the state of the technology is quite the opposite.

Metal-semiconductor solar cells reported to date exhibit inherently low output voltages. This effect is a consequence of high diode "saturation" (dark) currents and low metal-semiconductor barrier heights. Thus, the possible high photo-generation current densities theoretically available with Schottky cells are offset by low output voltages.

Metal-oxide-semiconductor solar cells[5,12] have been fabricated, exhibiting open circuit voltages as high as 0.52 volts.[18] In such cells, current flow

requires tunneling through the interfacial layer. The best such cells have shown only an 8% conversion efficiency,[8,16] indicating reduced current collection efficiency (through the interfacial layer) compared to the metal-semiconductor cells.

No experimental results have been shown to give credence to the possibility of obtaining increased Schottky cell voltages while maintaining high currents. On the other hand, the high generation current possibilities ascribed to such cells can be approached by P-N junction cells. In fact, high generation current densities along with high open circuit voltages have been reported for P-N junction solar cell structures fabricated incorporating violet-cell and textured surface techniques.

It is often stated (or implied) that Schottky cells are easily fabricated, giving an inherent processing simplicity (and cost) advantage over junction cells. This is a major misconception. Schottky cells require precise control of metal depositions in the thickness ranges of less than 100A in order to optimize trade-offs between conductivity and reflectance. Such control is difficult by evaporation, and more controllable sputtering techniques have resulted in lower open circuit voltages, presumably due to penetration of sputtered atoms through the interfacial layer into the silicon.[19] Yield, efficiency, and cost problems can be expected to continually plague this fabrication step. Schottky-type solar cells require the same highly conductive metal collection grid and anti-reflection coating deposition as do P-N junction cells. Rather than being simpler, the fabrication complexity for a good silicon Schottky solar cell would be about the same that of a good silicon P-N junction solar cell. It is Motorola's conclusion that the technological uncertainties that must be resolved in order to demonstrate the (slight) theoretical advantages of the silicon Schottky solar cell are much too great to permit considering it as a serious contender at this time.

3.1.3.1 SCHOTTKY BARRIER SOLAR CELL BIBLIOGRAPHY

1. S.S. Li, F.A. Lindholm, and C.T. Wang, "Quantum Yield of Metal-Semiconductor Photodiodes", J. Appl. Phys., 43, 4123, (1972).
2. W.A. Anderson and A.E. Delahoy, "Schottky Barrier Diodes for Solar Energy Conversion", Proc. IEEE, 60, 1457 - 1458, (1972).
3. E.J. Charlson, A.B. Shah, and J. C. Lien, "A New Silicon Schottky Photovoltaic Energy Converter", IEEE Electron Devices Meeting, (1972).
4. R. J. Stirn and Y.C.M. Yeh, "Solar and Laser Energy Conversion with Schottky Barrier Solar Cells", IEEE Photovoltaic Specialists Converence, 10, 15, (1973).
5. M.A. Green, F.D. King, and J. Schewchren, "Minority Carrier MIS Tunnel Diodes and Their Application to Electron and Photo-Voltaic Energy Conversion- I. Theory", Solid State Elec., 17, 551 - 561, (1974).
6. J. Schewchun, M.A. Green, and F.D. King "Minority Carrier MIS Tunnel Diodes and Their Application to Electron - and Photo-Voltaic Energy Conversion - II Experiment", Solid State Elec., 17, 563 - 572, (1974).
7. D.L. Fulfrey and R.F. McQuat, "Schottky Barrier Solar-Cell Calculations", Appl. Phys. Lett., 24 (4), 167 - 169, (1974).
8. W. A. Anderson, A.E. Delahoy, and R.A. Melano, "An 8% Efficient Layered Schottky-Barrier Solar Cell", J. Appl. Phys., 45 (9), 3913 - 3915, (1974).
9. W.A. Anderson, R. A. Milano, "I-V Characteristics for Silicon Schottky Solar Cells", Proc. IEEE, 63, (1), 206 - 208, (1975).
10. S.J. Fonash, "The Role of the Interfacial Layer in Metal-Semiconductor Solar Cells", J. Appl. Phys., 46 (3), 1286 - 1989, (1975).
11. R.F. McQuat and D.L. Pulfrey, "Analysis of Silicon Schottky Barrier Solar Cells", IEEE Photovoltaic Specialists Conf., 11, 371 - 375, (1975).
12. S.J. Fonash, "Metal-Thin Film Insulator-Semiconductor Solar Cells", IEEE Photovoltaic Specialists Conf., 11, 376 - 380, (1975).

13. Y.C.M. Yeh and R.J. Stirn, "Improved Schottky Barrier Solar Cells", IEEE Photovoltaic Specialists Conf., 11, 391 - 397, (1975).

14. R. J. Stirn and Y.C.M. Yeh, "The AMOS Cell-An Improved Metal-Semiconductor Solar Cell", IEEE Photovoltaic Specialists Conf., 11, 437 - 438, (1975).

15. R.J. Stirn and Y.C.M. Yeh, "A 15% Efficient Antireflection-Coated Metal-Oxide-Semiconductor Solar Cell", Appl. Phys. Lett., 27, (2), 95 - 98, (1975).

16. E.J. Charlson and J.C. Lien, "An Al p-Silicon MOS Photovoltaic Cell", J. Appl. Phys., 46, (9), 3982 - 3987, (1975).

17. S. Shevenock, S. Fonash, and J. Geneczko, "Studies of MIS Type Solar Cells Fabricated on Silicon", IEEE Electron Devices Meeting, 211 - 212, (1975).

18. M. Peckerar, H.C. Lin, and R.L. Kocher, "Open Circuit Voltage of MIS Schottky Diode Solar Cells", IEEE Electron Devices Meeting, 213 - 216, (1975).

19. W.A. Anderson, S.M. Vernon, A.E. Delahoy, K.K. Ng, P. Mathe, and T. Poon, "Variables Which Influence Silicon Schottky Solar Cell Performance", IEEE Electron Devices Meeting, 217 - 219, (1975).

20. W.A. Anderson, "Silicon Schottky Photovoltaic Diodes for Solar Energy Conversion", Quarterly Progress Report, NSF/RANN/SE/AER73-03197/PR/75/3, PB-246-154, (1975).

3.1.4 FRONT SURFACE METALLIZATION

Metal coverage and series resistance tradeoffs are major limiting design considerations on the shape and maximum useful size of solar cells, and the concomitant material process for producing silicon sheet. A critical evaluation of existing metallization geometries has revealed that efficiency may suffer if these designs are extended to large area ribbon or sheet cells. Accordingly, improved contact metallization designs were investigated. Designs which show

the greatest promise over existing designs for improved cell performance have multiple contacts; hence the interconnect and packaging systems should consider the possible need for multiple-contacts-per-wafer. Also, efficient design seems to favor long, narrow rectangular ribbons rather than large area square or round sheet solar cells.

In particular, the front surface metal pattern of a silicon solar cell will influence the performance of both solar cells and modules because of three requirements: 1) the pattern must provide area for an interface point (or points) for electrical connection to other cells; 2) the pattern must provide sufficient area for efficient (low resistance) flow of current, since the metal pattern itself (as well as the cell below) will have an internal series resistance; and 3) the pattern should shadow the least possible area to maximize current generation. Some preliminary conclusions regarding constraints on metal pattern design and on solar cell size can be drawn quickly by considering interactions of these three requirements.

Assume that a silicon solar cell is available with any desired surface area or shape but is constrained to have a fixed, minimum value of surface sheet resistance above the P-N junction. Series resistance of the cell will then depend on the thickness of metal used for a particular front ohmic contact pattern and the resistivity of that metal. If the metal pattern coverage is limited to a reasonable percentage of the front surface area (say, 5 to 10%) and a particular metal system and thickness are adopted (defining sheet resistance), then series resistance depends on pattern topology. The metal "current collection" fingers on the cell surface may contribute appreciably to series resistance. For a single contact region solar cell, as the cell surface area becomes larger (and the metal current-conducting paths become longer) a point will be reached where series resistance has increased beyond an acceptable value. In effect, the permissible surface area of the solar cell has been limited.

This is not true if more than one external electrical contact can be made to the cell. In this case, only one lateral dimension of the solar cell surface needs to be limited. For example, a solar cell fabricated on a rectangular ribbon substrate may be infinitely long if electrical contacts are made along its edges at small intervals, but there must be a practical limit on the width of the cell if acceptably low internal voltage loss (i.e., series resistance) is to be maintained. Calculations have shown that as ribbon widths surpass 10cm, loss of efficiency increases so rapidly that such cells are no longer cost effective. The same principle holds for circular solar cells. Constrained to a fixed area of front surface metal, a circular cell may require multiple contact points around the perimeter to maintain a low series resistance. A larger diameter cell would require more contacts than a smaller diameter cell; and in the limit, as cell diameter becomes still larger, overall cell efficiency must suffer.

The net effect of using multiple electrical contacts at the perimeter of a solar cell is to shift some of the burden of summing the photo-current generated by the active surface of the cell away from the metal pattern on the cell surface to external electrical busses. When such a solar cell is assembled in an array of cells, an additional benefit accrued is increased reliability achieved through partial redundancy of the multiple cell contacts.

3.1.5 BACK SURFACE METALLIZATION

The physical configuration of the back surface of a solar cell will influence its optical properties. It is important from a design standpoint to know, as a function of wavelength, the degree of light absorption, reflection, and transmission at the cell back surface, since these factors will influence cell efficiency as a function of thickness (multiple light pass from reflection) and heating effects (absorption at the back surface).

Another variable affecting optical performance at the back surface is the configuration of the front surface. If the front surface is texture-

etched and the back surface is non-absorbing, for example, total internal reflection from the back surface should always occur.

Experiments have been performed to measure, as a function of wavelength, the reflection of light from the back surface of a silicon wafer with various front surface and back surface configurations. The purpose of these experiments was to determine if any cell performance advantages can exist with a patterned back metal. Samples with both polished (or isotropically etch-polished) and texture-etched front surfaces were utilized for each back surface configuration.

Test wafers were prepared from 0.8 - 1.2Ωcm p-type silicon wafers. The starting wafers were isotropically etched on one side and polished on the other. Some of the test wafers utilized the polished side as the back surface, and others used the etched side as the back surface. The front surfaces of all test wafers were prepared such that one-half of the wafer was texture-etched. The entire front surface of each test wafer was then coated with 700A of silicon nitride to serve as an antireflection coating.

Half of the back surface of each test water was similarly coated with 700A of silicon nitride while the other half was covered with a thick metal film. The back was configured in such a way as to divide the entire test wafer into four classes of front/back surface condition combinations:

1. textured front/dielectric back;
2. textured front/metal back;
3. smooth front/dielectric back;
4. smooth front/metal back.

Integrated sphere reflection tests were then performed. Data were taken over wavelengths from 0.35μm to 2.0um to determine the reflectance characteristics of the interface at the test wafer back surface.

In each case where the back surface was covered with metal (which had been sintered) the empirical reflectance curves agreed perfectly with theoretical curves for reflectance from the front surface of the silicon wafers. The smooth front surface reflectance approached a value of 30% at 2.0μm, and the textured front surface reflectance approached a value of 10% at 2.0μm. In both cases where the test wafer back surface was covered with dielectric (and, during the measurements, backed by an extremely efficient absorber) a back surface reflectance effect was observed. For wavelengths below 1.1μm where the silicon wafer absorption is good, reflectance curve shapes are identical for both dielectric-covered and metal-covered back surface wafers. (The wafers utilized in these measurements were sufficiently thick to totally absorb any light in this wavelength range reflected from the back surface.) However, for wavelengths longer than 1.1μm, where silicon becomes transparent, an additional reflectance component was observed for wafers with dielectric coated backs. The smooth front surface test wafer reflectance approached 50% at 2.0μm, and the textured front surface test wafer approached 50% reflectance at 2.0μm. Therefore, in going from a metal backed cell to a dielectric backed cell, the smooth front surface wafer shows a 33% increase in reflectance while the textured front surface wafer shows a 400% increase in reflectance. This large increase in reflectance for textured surface wafers is a result of the total internal reflection condition inherent to textured wafers.

The possibility of patterning the back surface metal in order to utilize reflection of the longer wavelength portions of the solar spectrum back toward the front surface has ramifications other than increased absorption of useful light. For example, infrared wavelengths longer than 1.2 micrometers can be reflected from the back surface and ultimately out of the module, reducing cell and module operating temperature and increasing module efficiency. Additionally, a cost trade-off occurs between the additional cost of patterning the back

surface metal, the cost savings of decreased metal consumption, and the effective cost reduction brought about through increased cell efficiency.

3.1.6 METALLIZATION TEST PATTERN

As discussed in the two previous sections, a major factor in determining solar cell performance is the metallization pattern. The metallization must efficiently collect current while shadowing the minimum active area. In achieving optimum designs, thus, it is necessary to determine allowable contact metallization line widths, both from an achieveable fabrication feasibility standpoint and from a series resistance standpoint.

The limitations of metal contact pattern linewidths will vary with the surface flatness of the silicon. Accordingly, two types of surfaces were studied: polished and textured etched. These two types of surfaces represent extremes in surface microscopic smoothness. Both, however, are on macroscopically plane surfaces and will not necessarily present the effects of surface warp or ripple possible from sheet or ribbon growth. The effects of these latter parameters must be evaluated when sufficient representative ribbon samples become available.

A test pattern photoresist mask, Figure 3.5, was designed with linewidths ranging from 0.0003 inch to 0.0500 inch. Dielectrics (or metals) can be patterned on the desired surfaces by standard photolithographic techniques.

The evaluation technique, on both polished and textured test wafers, included the formation on the surface of a dielectric, either silicon dioxide or silicon nitride, and patterning the dielectric with the test pattern. The patterns were visually inspected and evaluated. The patterned wafers were then electroless nickel plated and solder coated. Optical inspections indicated minimum linewidth limitations due to photoresist procedures, and

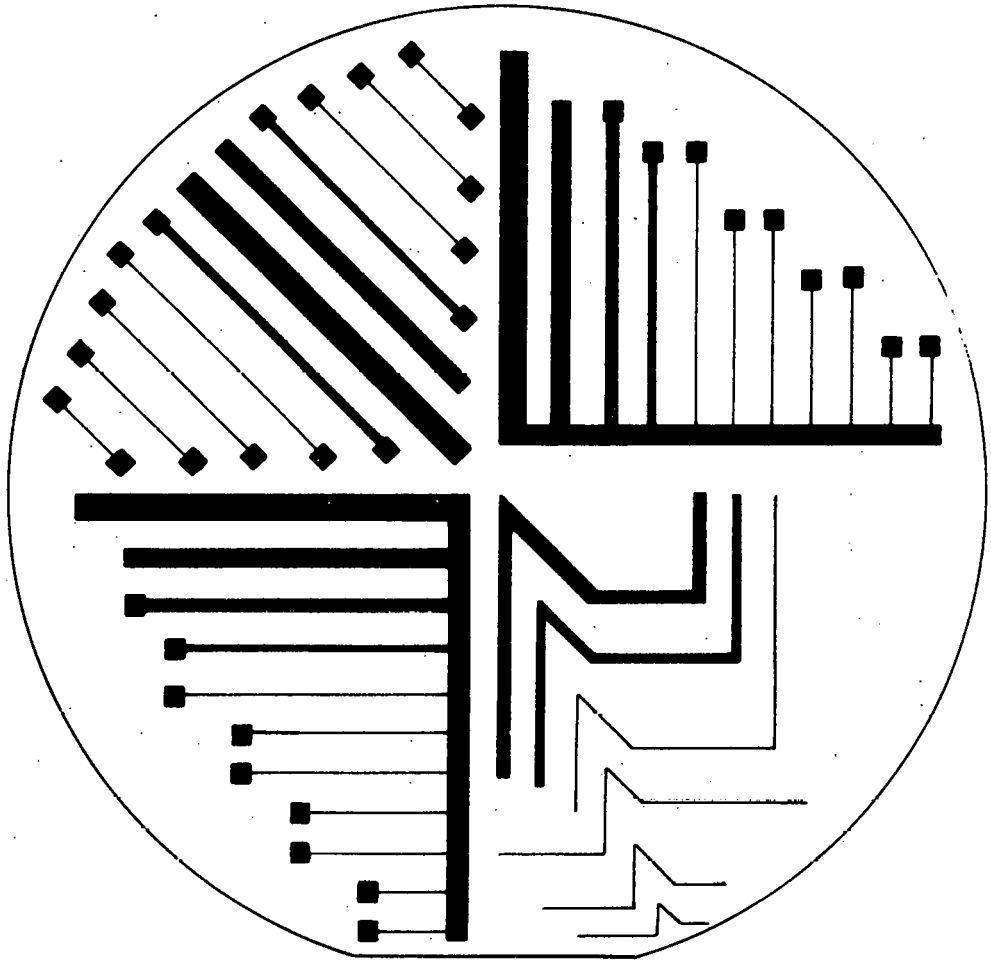

FIGURE 3-5: Metallization and solder test pattern. The pattern contains linewidths ranging from 0.0003 inch to 0.0500 inch. Pattern is designed such that lines are withdrawn from solder coating at horizontal, vertical, and angular directions. In addition, the pattern contains included angles of 45°, 90°, and 135°.

electrical continuity measurements determined line resistance after soldering. Sheet resistance versus metal linewidth was tabulated for both textured and polished surfaces to determine the relative ohmic properties of a small number of wide lines versus a large number of narrow lines for solar cell current-collecting patterns.

Results to date indicated that there is no problem in obtaining the smallest (0.0003 inch) line width on polished wafer surfaces using our standard photolithographic techniques and equipment. To the contrary, textured surfaces present a special problem. In order to maintain the integrity of the dielectric covering the peaks of the textured surface pyramids in areas where no preohmic pattern is to appear, a much more viscous photoresist must be used, as discussed in a later section. Application of this viscous resist produces a much thicker layer in the "troughs" of the textured surface. and this, in combination with the optical properties of the textured surface itself, seems to set a practical lower limit on preohmic line width resolution. Patterns were formed by contact printing from the mask. Inspection has shown that line widths smaller than 0.001 inch have not been clearly and consistently opened. Textured surface pyramids may have base widths on the order of 10 microns; therefore linewidths of 0.0005 inch (12.7 microns) may encompass only a single pyramid. Pyramid heights on the order of 10 microns prevent true contact printing. Thus, light scattering among the pyramids contributes to an inherent limit of line width resolution. Exposing with more collimated light source, such as is used with projection or proximity printing, should help to minimize these effects.

Wafers used for photolithographic studies, as well as a comparable set of polished test wafers, were plated with nickel and solder-dipped to obtain maximum metal build-up for a given line width. These lines were then measured for sheet conductance/resistance.

Experiments have been performed with textured surface wafers coated with silicon dioxide and prepared using standard viscosity (44 cp) photoresist to allow formation of soldered metal lines with widths between 0.0003 inch and 0.0500 inch. For line widths less than or equal to 20 mils, soldered line sheet resistance ρ(in Ω/sq.) is given by

$$\log \rho = -1.09 - 0.75 \log W,$$

where W is the line width in mils. This means ρ is proportional to $W^{-3/4}$. (If the solder bead build-up were hemicylindrical, then ρ would be proportional to W^{-1}.) For line widths greater than 20 mils the capillary effect of fine lines tends to become suppressed and the sheet resistance tends to become independent of line width, indicating a constant thickness at the larger widths.

The relation between sheet resistance and line width (given above) for lines less than 20 mils wide implies that, for a given area of metal line coverage, one wide contact finger will introduce more series resistance than two contact fingers distributed over the same active cell area, but each finger being half as wide. Thus, for soldered contact systems of equal total area, many narrow fingers are more efficient than fewer wide fingers, as long as the thinnest lines are at least 0.001 inch wide to preserve physical and electrical continuity.

3.2 PROCESS ADAPTATION

A major portion of the contractual effort involved a technical assessment of potential process steps for manufacturing silicon solar cells. First, a matrix of possible processing steps was assembled. Second, a group of evaluation criteria was defined to allow a technical evaluation of the usefulness of each individual process step when examined as an isolated step for manufacturing solar cells. Most of the individual process steps were then evaluated, either directly in the laboratory or through indirect methods such as literature

surveys, vendor contacts, and detailed discussions with process engineers in the Motorola manufacturing and research areas (for both discrete and integrated circuit products). This technical evaluation process resulted in the categorization of these individual process steps to reflect both technical readiness and an estimation of future technical utility. This section identifies the various process steps, their evaluation, and their technical categorization.

3.2.1 EVALUATION CRITERIA

Evaluation criteria were established to consider both the individual process step itself and also effects on properties of a solar cell resulting from its incorporation in the cell manufacturing sequence. Among the evaluation criteria were:

- Cost
  - Labor
  - Material
  - Capital
  - Expense Items
- Performance
- Controllability
- Amenability to automation
- State of readiness
- Reliability considerations
- Amenability to future sheet (ribbon) geometries.

Whenever applicable, each of these criteria was applied to both the process itself and to properties of the resulting solar cell. A poor rating in either case would result in an overall unsatisfactory rating. Performance of surface lapping silicon, for example, is judged favorably as an isolated process step,

but lapped silicon is rated poorly as a starting surface when considering its effects on solar cell performance. It must be understood that process steps do not stand on their merits as individuals, but on their ability to contribute synergistically to a process sequence. Each step must, then, be evaluated first, by itself, and second, as a member of a process sequence.

In this technical evaluation phase, cost criteria were applied in only a qualitative manner, reflecting only estimated and relative costs of competing processes. A detailed process step cost study was subsequently performed, and is reported in a later section.

The only other criterion which may not be self-explanatory is that involving sheet geometries. This requires an evaluation of a process step's suitability for application to a sheet which may have an irregular shape and also may be non-planar in nature. The sheet may, for example, be a ribbon which varies in edge shape, has surface ripples, and is warped. Some processes are relatively insensitive to these factors, while others become virtually useless. As-grown sheet is considered as having more severe geometrical problems than large area sliced sheets, which may also be utilized and must be considered as potential long-range substrates.

3.2.2 TECHNOLOGY ASSESSMENT CATEGORIES

A set of initial technology assessment categories was established at the beginning of the program. During the course of detailed process step evaluation, the set of categories was modified to reflect more accurately the requirements for evaluation of projected usefulness. The updated categories were as follows:

Category 1: Processes which are judged unlikely to be utilized in any recommended process sequence.

Cateogry 2: Processes which appear to require a major technological advancement to ensure usefulness. Technology in these areas

must be continually monitored to assess future applicability.

Cateogry 3: Processes which appear potentially promising, but which have required evaluations or equipment not available during the time-frame of this contract. Additional efforts should be expended on these processes.

Category 4: Proven processes which have a high chance of successful incorporation into future process sequences.

3.2.3 STARTING CONDITION OF SILICON SURFACE

The starting condition of the silicon surface plays a critical role in subsequent processing steps and in cell efficiency.

3.2.3.1 SAWED SURFACE (CATEGORY 1)

It is unlikely that silicon will be utilized in the as-cut condition. Although this form of silicon is the cheapest available today, near-surface damage (and possible contamination from the saw blade and coolant) can badly degrade the crystal properties upon subsequent processing. Heating of the sawed surface can result in polyganization or recrystallization, converting the area in which the p-n junction is to be formed into a polycrystalline region. Heating may also propagate surface damage far into the bulk, resulting in a heavily dislocated, low lifetime material. All of these factors can degrade efficiency in a severe, uncontrolled manner.

One possible exception to this conclusion exists, however. Severe surface damage may be utilized to getter undesirable impurities from the bulk silicon below. High temperature annealing of a sawed surface may produce this desirable result. Subsequent to annealing, an undamaged silicon surface could be revealed by etching the sawed surface, hopefully removing both the

damage and the impurities. There is at this time insufficient information available to draw conclusions; additional studies should be undertaken.

3.2.3.2 SAWED AND ETCHED SURFACE (CATEGORY 4)

This is the best candidate broadly available today. Etching is utilized to remove the sawing damage and contamination. Etching wafers can leave surfaces that contain only gradual undulations of a magnitude so small that no pattern having linewidths of interest to solar cell production should experience any masking difficulties because of surface non-planarity. Thus, apart from the future realization of direct sheet growth, this combination produces the cheapest material suitable for solar cells and has indeed been used to manufacture solar cells. Sawing kerf loss, and material removed by etching, are major drawbacks, however, to this being the most economical approach for long range utilizaton.

3.2.3.3 LAPPED AND/OR POLISHED SURFACE (CATEGORY 1)

Lapping produces a matte appearing surface on a silicon wafer. It will be a flat surface, and, if done carefully, both sides of a wafer can be made plane and parallel by lapping them both. Lapping doesn't necessarily produce a surface having less damage than careful sawing, but a sawed surface will not be as flat as a lapped surface. This process is slow, batch orientated, and labor intensive, and hence is too expensive for ultimate solar cell use.

Polishing is a process like lapping, in which successively finer grit media are used to end up with a mirror-flat scratch-free surface. This degree of smoothness is necessary in order to obtain, by photographic means, the very fine line geometries utilized on many semiconductor devices and integrated circuits. However, solar cell geometries are about an order of magnitude coarser, so polished surfaces are not required for solar cell processing even

where patterning is done photographically. Furthermore, polished surfaces typically contain more mechanical crystal damage than etched surfaces, making them potentially less satisfactory for solar cell use.

Both lapping and polishing are too costly for incorporation into a process sequence to make inexpensive solar cells.

3.2.3.4 CLEAVED SURFACE (CATEGORY 2)

Direct cleaving of silicon wafers or sheets from crystals would eliminate kerf losses, and could possibly produce smooth surfaces directly. To date, however, no process has been developed for cleaving wafers from a boule with anything approaching a satisfactory yield. If a major breakthrough in this area could be realized, it would be very cost competitive. No work appears to be currently underway in this area, however.

3.2.3.5 AS-GROWN SHEET SURFACE (CATEGORY 2)

This is the responsibility of several contractors in the LSSA Program Task II. Breakthroughs in technology are still required to make as-grown sheet practical in the large scale necessary. However, judging by the progress made to date, and the potentialities of the process, it must be assumed that the probability of success is high. The various processes being studied all have the possibility of providing as-grown surfaces suitable for efficient solar cell processing.

The geometrical variations in silicon sheet, however, can greatly influence the usefulness of some solar cell processing, fabrication, and encapsulation choices. It must be made clear that two separate philosophies may be pursued. The first simply states that the large area sheet must conform to certain geometrical limits in order to allow solar cell processing and encapsulation to be performed by essentially conventional silicon wafer processing methods.

The second, the converse of the first, states that whatever the shape that results from the sheet growth method, it will be used, forcing solar cell processing and encapsulation to conform to the delivered geometry.

The most likely ultimate choice, of course, will be a compromise between the two extreme philosophies in order to achieve cost effectiveness. The compromise may, however, provide non-planar, rough surfaced sheets as compared to today's surface texture and flatness standards for wafers. Accordingly, later processes which are recommended under this Task IV study must have the flexibility of handling such future material, or must be clearly labeled as applicable only to optimum surfaces.

3.2.3.6 TEXTURE-ETCHED SURFACE (CATEGORY 4)

Texture-etching has been shown to be a repeatable and uniform process on (100) oriented silicon surfaces. Texture-etching can be performed on any of the previously discussed silicon surface conditions. Costs of texture-etching are equal to, or less than, those for other techniques for silicon etching, producing silicon costs only marginally above those of present sawed and etched wafers. For this additional cost, a surface with distinct optical advantages (and attendant efficiency increases) is produced. The textured surface is dramatically different in nature from polished or etched surfaces now used widely in the semiconductor industry. This requires certain modifications of other steps in a process sequence utilizing textured surfaces. These modifications are easily achieved.

The main caveat which must be kept in mind is that texture-etched surfaces currently require (100) oriented surfaces. If future sheet processes cannot produce (100) surfaces, texture-etching development must be attempted for other silicon orientations. If, in the future, a choice must be made between two

sheet growth processes of otherwise similar properties, the advantage will lie with the sheet process which can be texture-etched.

3.2.4 IN-PROCESS SURFACE CLEANING OR ETCHING

Any solar cell manufacturing process will require cleaning steps at some stages. Further, most manufacturing sequences will require etching steps.

3.2.4.1 WET CHEMICAL CLEANING OR ETCHING (CATEGORY 4)

Processes in this category are widely utilized in the semiconductor industry with a high degree of success. Several major concerns exist at this time, however. First, it is possible to have unwanted contamination from wet chemicals. For any given process sequence and for each different manufacturing area, control limits will have to be defined for possible contaminants. At this time, no difficulties are seen in this area. Second, the use of wet chemicals limits the level of future cost reductions to the cost of those chemicals consumed, a serious limit if large quantities of chemicals are required. (This must include D.I. water which is consumed in rinsing after wet chemistry steps.) A third consideration is the disposal of waste chemicals. This can contribute additional materials and facilities costs to the utilization of wet chemistry. Nevertheless, because of its current strong position in the semiconductor industry, wet chemistry must still be considered a major possiblity for future use.

3.2.4.2 PLASMA CLEANING OR ETCHING (CATEGORY 4)

This is a dry process incorporating an RF field to excite a plasma. The energetic plasma is then used to remove material from the surface, either

through bombardment by inert energetic plasma ions, or by reactive ions liberated from molecules injected into the plasma. Based on their increasing acceptance by the semiconductor industry, plasma etching and cleaning steps have a high likelihood of supplanting at least some of the more traditional wet chemistry process steps.

A silicon nitride film for example, may be patterned utilizing a plasma etching process with excellent results. The plasma etching process, when compared to the wet chemistry process for etching, is less complicated and less time consuming. After application, alignment, and development of a photoresist film, etching of the exposed dielectric requires the following steps for the plasma and wet chemistry processes:

PLASMA	WET CHEMISTRY
Load in etch carrier	Load in etch carrier
Etch in plasma	Etch in solution
Remove photoresist	Rinse in D.I. H_2O
	Dry
	Remove photoresist

Not only is the plasma step simpler, it consumes only a small amount of material (etching gas) as compared to consumed acid and D.I. water for wet chemistry etching.

Plasma removal of photoresist ("ashing") has a similar appeal for process simplicity and consumed materials. Photoresist materials have notoriously contained metallic contaminants which, if left on the wafer surface and heated in subsequent process steps, could migrate into the silicon and degrade minority carrier lifetime. It is possible that photoresist removal by plasma techniques alone could leave such metallic impurities on the wafer surface. Evaluation of this aspect of plasma processing for solar cell fabrication, where high lifetime must be maintained, must be performed at a future date.

3.2.4.3 VACUUM BAKING AND REVERSE SPUTTERING (CATEGORY1)

While results are reportedly adequate, the comparative capital costs are prohibitive for further consideration.

3.2.4.4 TEXTURE-ETCHING (CATEGORY 4)

Rather than texture-etching as a pre-processing step, it can be incorporated within a process sequence. The previous discussion is applicable here.

3.2.4.5 CLEANING BY SCRUBBING (CATEGORY 4)

A technique relatively new to the semiconductor industry is cleaning of silicon wafers by the mechanical scrubbing of their surfaces with brushes. Until recently, such scrubbing was avoided to eliminate possible mechanical damage to the silicon surface. Studies have shown, however, that removal of tightly adhering (and otherwise difficult to remove) dirt particles can be achieved through scrubbing without silicon damage. The removal of these particulates is seen to improve process control, device quality and performance, and overall process yield.

Mechanical scrubbing, however, may not be possible on warped or rippled surfaces such as may be forthcoming from future large area sheet production, or on textured surfaces which may house impurities in valleys too tiny to be effectively reached by brush bristles. Manufacturers have recently indicated, however, that cleaning equivalent to mechanical scrubbing may be accomplished hydraulically with a pressurized spray of water.

Numerous vendors now have automatic and semi-automatic scrubbing equipment of both types available. Yield increases of several semiconductor lines within Motorola (precise data is considered proprietary) indicate that scrubbing is technically advantageous.

3.2.4.6 GAS STREAM DRYING (CATEGORY 4)

Wet chemistry steps reqire a subsequent drying operation. Drying by exposure to a (hot) gas flow has been one of the standards in the industry. It is forgiving of shape and is the prime contender for sheet geometries.

3.2.4.7 GRAVITY (CENTRIFUGE) DRYING (CATEGORY 4)

For round wafers, centrifuge or "spin" drying has become another of the semiconductor industry standards. In that industry, wafers are thicker and smaller than those likely to be utilized for future solar cells. This technique may require special adaptation for very large area, thin solar ce l substrates such as long ribbons.

3.2.5 LIFETIME ENHANCEMENT AND PRESERVATION (CATEGORY 3)

Solar cell processing may require minority carrier lifetime improvement of the starting material, and must incorporate special precautions (and possibly specific techniques) to preserve lifetime during processing. Such processes fall into four general categories of lifetime enhancement: Complexing and removal of impurities, temperature-time profiling, leaching, and precipitation of impurities on damage sites or defects.

A literature survey on gettering of impurities in silicon has been performed; initial observations are that a variety of gettering processes has been investigated, and that the technology of impurity gettering is complex and far from developed to its full potential. In short, these processes all fall precisely within the definition of Category 3. Future efforts must be directed toward this area. A brief review of gettering is given here, followed by a bibliography of gettering references.

3.2.5.1 LITERATURE SURVEY OF GETTERING

In original investigations[1] into the removal of metallic impurities from silicon, the basic approach was to grow (or deposit) some type of oxide layer onto the surface of the silicon. The basic idea was that at high temperatures, the metallic impurities would diffuse to the surface and become trapped in the oxide layer. Various oxides, including phosphorus -, boron -, vanadium -, and lead - silicon oxides, were used. It was found that phosphorus glass did the best job.

Since then, studies[3,10,13] have shown that the metallic impurities are not gettered into the phosphorus glass, but instead aregettered to the heavily doped silicon under the glass. Apparently, the mechanism is one of increased solubility of metallic impurities in the phosphorus-doped silicon. Removal of impurities from the silicon, thus, requires removal of not only the oxide layer, but also the surface layer of silicon itself.

Normally, in bipolar processing, phosphorus gettering is used to transport metallic impurities away from active device areas to an unused portion of the wafer (i.e., the isolation diffusion or the back of the wafer). In MOS processing, a phosphorus glass is deposited on top of the passivation oxide to getter sodium impurities from the gate oxide[11]; this glass, however, appears to do little gettering of metallic impurities from the bulk of the silicon.

It has also been shown that a preoxidation gettering of the backside of the wafer will reduce the generation of oxide-induced stacking faults[14] (OISF). It is believed that OISF act to precipitate metallic impurities and thus degrade device characteristics. It is also believed that OISF are sites of enhanced phosphorus diffusion, and thus cause emitter-collector piping defects in bipolar devices.

It has been found that the use of various chlorine compounds during oxidation will getter both metallic impurities from the bulk silicon [4,7,8] and sodium impurities from the oxides that are grown[5,6,9,12] Chlorine gettering can be used only during oxidation because it could otherwise cause extreme etching and pitting of the silicon[4]. Chlorine gas has been used with some success, but it may cause etching of the silicon. Hydrogen chloride has been the most successful gettering compound.

The chlorine gettering mechanism is believed to be diffusion of metallic impurities to the surface, followed by formation at the surface of volatile metallic chlorides which are then carried away by the gas flow. The gettering effect improves with increasing temperature (especially above 1000°C) and increasing amounts of HCl. The limit to the amount of HCl used occurs when significant etching of the silicon begins, or condensation of hydrochloric acid droplets takes place in the cooler portions of the furnace tube. The optimum mixture of HCl is about 5 - 10% HCl by volume in dry O_2.

It has also been discovered that the use of HCl will clean the furance tube of metallic impurities, and thus reduce contamination from that source to virtually nil[6]. The process used is 10% HCl in dry oxygen at 1150°C for 6 hours.

It should be noted that the use of HCl with steam instead of dry O_2 will still getter Na and the oxides thus grown, but will not as effectively getter the metallic impurities from the bulk. It is believed that the accelerated oxidation of metallic impurities in steam inhibits the formation of volatile metal chlorides.

It is well known that various types of crystallographic defects in silicon will tend to precipitate metallic impurities. This principle has been used to getter impurities by deliberately introducing defects in the back of the wafer, using them to trap metallic impurities migrating from the active device

regions. It should be emphasized that this method does not remove metallic impurities from the wafer, but merely moves them around. Methods of introducing defects include mechanical abrasion and ion implantation of Ar, O, P, Si, As, or B. As was suggested earlier, sawing damage may also be an appropriate starting point.

Boron diffusions have been used to getter metallic impurities from silicon, but are not as effective as phosphorus[3]. The mechanism is apparently the formation of metal precipitates, rather than any increased solubility of pairing.

Some gettering action has also been observed with the use of Si_3N_4 layer[18]. Gettering can also be achieved through the appropriate use of controlled heating and cooling rates, and the temperature range of controlled heating and cooling. These cycles apparently function through a precipitation process, removing impurities from electrically active sites.

Since solar cell efficiency is extremely dependent upon lifetime, gettering cycles to improve or preserve lifetime seem appropriate for future incorporation into solar cell process sequences. The exact choice (or choices) will require further experimental work, however.

3.1.5.2 GETTERING BIBLIOGRAPHY

1. A. Goetzberger and W. Schockley "Metal Precipitates in Silicon P-N Junctions," J. APPL. PHYS., 31 (10), 1821 - 1824, (1960).

2. S.W. Ing Jr., R.E. Morrison, L.L. Alt, and R.W. Aldrich, "Gettering of Metallic Impurities from Planar Silicon Diodes," J. ELECTROCHEMICAL SOC. 110 (6), 533 - 537, (1963).

3. J.S. Adamic Jr. and J.E. McNamara, "A Study of the Removal of Gold from Silicon Using Phosphorus and Boron Glass Gettering," ECS Meeting, (1964).

4. P.H. Robinson and F.P. Heiman, "Use of HCl Gettering in Silicon Device Processing," J. ELECTROCHEMICAL SOC., 118 (1), 141 - 143, (1971).

5. M.C. Chen and J.W. Hile, "Oxide Charge Reduction by Chemical Gettering with Trichloroethylene During Thermal Oxidation of Silicon," J. ELECTROCHEMICAL SOC., 119 (2), 223 - 225, (1972).

6. R.J.Kriegler, Y.C. Cheng, and D.R. Colton, "The Effect of HCl and CL_2 on the Thermal Oxidation of Silicon," J. ELECTROCHEMICAL SOC., 119, (3), 388 - 392, (1972).

7. R.S. Ronen and P.H. Robinson, "Hydrogen Chloride and Chlorine Gettering: An Effective Technique for Improving Performance of Silicon Devices," J. ELECTROCHEMICAL SOC., 120 (11), 1578 - 1581, (1973).

8. D.R. Young and C.M. Osburn, "Minority Carrier Generation Studies in MOS Capacitors on N-Type Silicon," J. ELECTROCHEMICAL SOC., 120 (11), 1578 - 1581, (1973).

9. K. Hirabayashi and J. Iwamura, "Kinetics of Thermal Growth of HCl-O_2 Oxides on Silicon," J. ELECTROCHEMICAL SOC., 120 (11), 1595 - 1601, (1973).

10. R.L. Meek and C.F. Gibbon, "Preliminary Results of an Ion Scattering Study of Phosphosilicate Glass Gettering," J. ELECTROCHEMICAL SOC., 121 (3), 444 - 447, (1974).

11. D.V. McCaughan, R.A. Kushner, and S. Wagner, "Complete Removal of Sodium from Silicon Dioxide Films by Formation of Phosphosilicate Glass," J. ELECTROCHEMICAL SOC., 121 (5), 724 - 725, (1974).

12. C.M. Osburn, "Dielectric Breakdown Properties of SiO_2 Films Grown in Halogen and Hydrogen - Contaminating Environments," J. ELECTROCHEMICAL SOC., 121 (6), 809 - 815, (1974).

13. R.L. Meek, T.E. Seidle, and A.G. Cullis, "Diffusion Gettering of Au and Cu in Silicon," J. ELECTROCHEMICAL SOC., 122, (6), 786 - 796, (1975).

14. G.A. Rozgonyi, P.M. Petroff, and M.H. Read, "Elimination of Oxidation - Induced Stacking Faults by Phosphorus Gettering of Silicon Wafers," J. ELECTROCHEMICAL SOCIETY, 122, (12), 1725 - 1729, (1972).

15. C.N. Berglund, D.R. Colton, and R.J. Kriegler, "Gettering in MOS Systems," ECS Meeting Abstracts, 159 - 162, (1976).

16. T.E. Seidel, "A Description of Gettering Processes," ECS Meeting Abstracts, 163 - 166, (1976).

17. G.A. Rozgonyi, "Dislocations, Stacking Faults, and Native Defect Centers in Silicon Wafers - II Defect Elimination and Device Correlations," ECS Meeting Abstracts, 171 - 173, (1976).

18. P.M. Petroff, G.A. Rozgonyi, and T.T. Sheng, "Elimination of Process - Induced Stacking Faults by Preoxidation Gettering of Si Wafers - II. Si_3N_4 Process," J. ELECTROCHEMICAL SOC., 123 (4), 565 - 570, (1976).

19. G.A. Rozgonyi and R.A. Kushner, "The Elimination of Stacking Faults by Preoxidation Gettering of Silicon Wafers - III. Defect Etch Pit Correlation with p-n Junction Leakage," J. ELECTROCHEMICAL SOC., 123, (4), 570 - 576, (1976).

3.2.6 JUNCTION FORMATION

The most complex and critical steps in solar cell processing involve junction formation. In order to stay within the design requirements of an efficient solar cell, the junction depth must be controlled to be consistently less than 0.5 micrometers, and preferably less than 0.2 micrometers. This places stringent control problems on the techniques utilized for junction formation.

3.2.6.1 EPITAXY (CATEGORY 1)

Motorola has obtained long and continued experience in automated silicon epitaxial growth. Silicon deposition is accomplished in RF-heated, cold-walled chambers by chemical vapor deposition at temperatures near 1100°C. Present and projected state-of-the-art have shown that accurately controlled deposition of silicon at thicknesses of (or below) 0.25 micrometers will be impractical. In this range, thickness is difficult to control. Interdiffusion of impurities is appreciable at these high deposition temperatures, resulting in further control difficulties, and degrading performance. Projected yields and resulting costs make this method unlikely.

The only foreseen possibility is a low temperature plasma-aided or vacuum-aided deposition. At this time, these processes are considered speculative.

3.2.6.2 DIFFUSION (CATEGORY 4)

Diffusion is a generic term utilized to describe thermal motion of impurities employing a broad variety of doping techniques. Diffusion is normally accomplished by deposition of a shallow (source) region of impurity in the silicon, followed by a high temperature redistribution; these items take place either sequentially or simultaneously. All diffusion processes

have the common feature of rather isotropic introduction of a dopant into exposed surfaces, with first order junction depth control being accomplished by time and temperature. Control of surface concentration is commonly obtained by utilizing solid solubility of an impurity in silicon to establish an easily controlled impurity source. Temperature is frequently utilized as the controlling parameter for the level of solid solubility, lower doping levels occurring at lower temperatures. Since diffusion is a high temperature process, unwanted effects contributing to reduced lifetime can occur during the high temperature exposure. For example, fast-diffusing impurities serving as efficient recombination centers in the silicon lattice can be accidentally added; crystal structure deterioration, particularly at near-surface regions (e.g., oxidation-induced stacking faults and their subsequent evolution into more complex defects) can be introduced; and oxygen precipitates of various types can be formed. Hence, choice of a diffusion process sequence must consider the resultant lifetime that can be reproducibly obtained, as well as the formation of the P-N junction itself.

Deposition of diffusion sources by chemical vapor deposition (CVD) or by vapor transport are the most widely utilized techniques in the semiconductor industry. These technologies are fairly mature and have been successfully applied to the fabrication of high efficiency solar cells.

Spin-on application of diffusion sources is also commonly used in areas of the semiconductor industry today as an alternative to the more conventional gaseous carrier methods. Further, spin-on diffusion sources can be utilized as antireflection coatings on solar cells.

Most present uses of spin-on diffusion sources are on round wafers which can be readily spun at high speeds during application. Such spinning processes may not be transferrable to rectangular ribbon or very large sheet geometries, but may require spray-on or roll-on technology to be developed. Other than the

exact application method, however, the remainder of the technology should be directly applicable to future geometries.

Typical spin-on sources consist of a solution of an organic silicate, an alcohol, and a small proportion of an organic compound of the desired dopant element. The liquid is usually filtered, and is in the form of a solution rather than a suspension. It is applied to the wafers using standard photoresist spinners. Subsequent heat treatment forms a doped silicon oxide layer on the surface of the wafers, the organic components of being driven off. [1] This densified layer acts as the dopant source during diffusion.

Spin-on diffusion sources can be formulated for specific dopants and dopant concentrations. [2, 3, 4] In addition, as is the case for gaseous diffusion sources, sheet resistivity and junction depth can be controllably varied by changing the diffusion temperature and time. Dopant surface concentrations have been varied up to solid solubility and have been controlled experimentally by the dopant concentration of the spin-on film. [4]

Wafer-to-wafer dopant uniformity has been shown to be excellent. A lot of 52 wafers, for example, boron diffused from a spin-on source showed a mean standard doping deviation of 3%. [5] Production performance has also been tested on small signal PNP transistors manufactured solely from spin-on sources. Such transistors met all the DC electrical specifications for devices manufactured from conventional gaseous diffusion sources. [6]

Since diffusion occurs from a doped oxide film, diffusion of different dopants and/or concentrations can be performed simultaneously on opposite sides of the wafer without concern for cross-contamination. This feature could allow, for example, P-N junction formation simultaneous with back surface field diffusion.

Textured silicon surfaces, as well as ribbon or other surfaces with irregularities in the macroscopic range, may cause some problems with spin-on diffusion sources. It is possible, for example, that the pyramids of a textured surface

might cause uneven film thickness, being thicker than average in the valleys between pyramids and being correspondingly thinner at the tips of the pyramids.

All of these considerations indicate the need for studies of alternate spin-on diffusion source application methods.

SPIN-ON BIBLIOGRAPHY

A bibliography of spin-on diffusion sources by personnel consulted on this program is listed below:

1. J.N. Smith, S. Thomas, and K. Ritchie, "Auger Electron Spectroscopy Determination of the Oxygen/Silicon Ratio in Spin-On Glass Films". Journal of the Electrochemical Society", 121 (6), (1974).
2. U.S. Patent 3,789,023, "Liquid Diffusion Dopant Source for Semiconductors", Kim Ritchie assigned to Motorola.
3. U.S. Patent 3,832,202, "Liquid Silica Source for Semiconductors", Kim Ritchie assigned to Motorola.
4. K.M. Mar, "Diffusion Characterization of Spin-On Borosilica Films for Application in Wafer Processing", Electrochemical Society Meeting, Washington, D.C., May 2 - 7, (1976).
5. S.P. Sykes and K.M. Mar, "Investigation of the Factors Affecting the Doping Uniformity Using a Spin-On Borosilica Diffusion Source", Electrochemical Society Meeting, Las Vegas, October 17 - 22, (1976).
6. K.M. Mar and R. Foo, "Application of Doped Spin-On Glasses ad Diffusion Sources for Transistor Fabrication", Electrochemical Society Meeting, Toronto, May 11 - 16, (1975).

3.2.6.3 ION IMPLANTATION (CATEGORY 4)

Ion implantation of the dopant, unlike diffusion, is not isotropic, but is unidirectional, with depth dependent upon implantation energy. Ion

implantation can be performed with extremely pure, mass analyzed dopants, avoiding any undesired contamination. Surface concentration can be controlled by ion dose. The main drawback to ion implantation is the high capital cost. Ion implantation may be utilized to form the P-N junction directly, or the implanted layer may serve as a well-controlled source of impurity for a subsequent diffusion step. If a subsequent diffusion is not performed, the implanted dopant must at least be activated by a high temperature anneal. This temperature may be as great as 900°C if resistance furnace heating is used and high doping efficiency is to be maintained.

For solar cell applications, throughput is dependent on ion beam current. Machine technology has progressed to the point of producing sufficiently high dopant ion beam currents to be a serious contender for solar cell processing. Still greater beam currents appear feasible, making ion implantation compatible with the longer range LSSA Project cost goals.

As will be discussed in a later section, efficient solar cells have been fabricated at Motorola utilizing an ion implanted junction, establishing ion implantation as a viable process technique for P-N junction formation.

3.2.6.4 ALLOY (CATEGORY 1)

This original technique for P-N junction formation was largely bypassed by other processes due to its lack of control and its intractability for anything but simple patterning. For solar cell use, the alloying material would have to be removed, exposing the (liquid phase epitaxy) regrown region below. Since the surface region is grown from solution, its impurity profile may not be controlled as desired to produce a drift aiding field. There appears to be no new development on the horizon to create renewed interest in alloying for solar cell P-N junction formation.

3.2.7 CONTACT METALLIZATION

Metallization constitutes the interface between the silicon and the module and because it is a critical interface, often determines both module performance

and module reliability. On one hand, solar cell contact metallization must cover the minimum possible area while achieving minimum resistance. On the other hand, the metallization must provide excellent mechanical adherence to the cell in environments which contain moisture, apply mechanical stress and in some applications, experience high voltage between solar cells and the package. The metallization system is almost always involved in the failure of semiconductor components, and it is expected to be a critical component of solar module reliability.

3.2.7.1 VACUUM DEPOSITION (CATEGORY 1)

Vacuum deposition is the predominent metallization method utilized in the semiconductor industry. For most semiconductor devices and integrated circuits, a metal (or layers of metals) is deposited by evaporation or sputtering onto the entire wafer surface and subsequently patterned into small geometries in a photolithography (photoresist) step. Solar cell metallization, on the other hand, employs a large geometry pattern with (by comparison) coarse lines. Some patterns can be made amenable to evaporation through a mask, thus eliminating the photoresist step. Totally redundant multiple contacts cannot however, be patterned through a metal mask if all metallization lines are to be directly interconnected on the cell surface. (Portions of the masking pattern would be unsupported and would fall out.) Evaporation through a mask and photolithographic removal are both very wasteful of material, typically utilizing no more than 5% of the metal consumed. Further, both processes require further chemical consumption for etching the excess metal, either from the wafer or the evaporation mask. Capital cost of vacuum equipment is higher than that for any other metal deposition technique. Vacuum deposition is not expected to be a viable contender for future solar cell application. (A more detailed discussion of cost information is presented in Section 3.6.)

3.2.7.2 PLATING (CATEGORY 4)

Plated contacts which satisfy all contact metallization criteria have been produced in the Motorola Solar Energy R&D Laboratory. Accordingly, plating is considered to have a high probability for future usage in solar cell contact metallization. Plated contacts are amenable to automation. Costs for materials are moderate, but labor and capital costs are low. Most important, plating is the most forgiving of all metal processes to surface and geometrical irregularities.

3.2.7.3 CHEMICAL VAPOR DEPOSITION (CATEGORY 1)

Chemical vapor deposition of metal contacts employs the decomposition of a metal-bearing gaseous compound, often in the presence of a second gas. Primary candidates are metal-organic compounds (which are generally very expensive) and material waste is appreciable. It is doubtful that cost savings over established vacuum technology can be realized. Metallization by means of chemical vapor deposition should be considered only via an evolution of potentially useful new systems, decreased raw materials costs, and improved material utilization.

3.2.7.4 PRINTING (SILK SCREENING) (CATEGORY 4)

Printed contacts are painted (and simultaneously patterned) directly onto the silicon solar cell surface. Printed contacts for solar cells have considerable appeal due to the possible lower cost of this approach when compared to more conventional methods of contacting silicon, such as metal evaporation or sputtering. The printing process itself is not only fast, but the capital cost of equipment is low. The line widths required for solar cells are close to the limits of resolution for printing, however, and may limit its use to plane surfaces.

Printed contact materials utilize a carrier or binder. Following application, printed contacts must be heat treated ("fired") to promote electrical contact and physical adhesion to the silicon, and to enhance conductivity of the film. The carrier is removed during firing, but it still must be inert with respect to the silicon so that junction quality is preserved.

Adhesion and contact resistance of printed contacts require special attention. Typically, present printed metal systems are either copper or silver based, and have been designed for adherence to ceramic parts rather than silicon surfaces. Since neither copper nor silver forms inherently strong mechanical bonds with silicon, adhesion may be promoted through the incorporation of glass frits into the printing material; these frits sinter to an oxide film on the silicon surface. Incorporation into the printing material of other metals, in addition to frits, is also utilized in an effort to enhance adhesion. The dependence of glasses for adhesion of printed contacts can produce unsatisfactorily high electrical contact resistance due to reduced metal-silicon contact area. Trade-offs occur, thus, between frit quantities, silicon surface preparation, metal combinations, metallization patterns, and contact firing temperatures. It has been observed that low temperature firing of contacts will result in poor contact adherence and poor interconnection reliability, while high temperature firing can generate yield and efficiency losses due to alloying, shorting, or lifetime degradation when applied over very shallow p-n junctions.

Six conductive ink samples were given a preliminary evaluation during this program period. They are formulated and classified as:

1. Silver with frit
2. Silver without frit
3. Silver with 2% palladium with frit

4. Silver with 2% palladium without frit

5. Silver with 2% platinum without frit

6. Copper with frit

In order to evaluate contact resistance and adhesion, these samples were applied to silicon surfaces with both an intentional oxide thickness and a minimum oxide thickness. In the first case, a layer of silicon dioxide was formed in the contact areas to a thickness of approximately 100A. This thickness of SiO_2 is slightly greater than that which would normally form on a silicon wafer which has been stripped and exposed to the ambient for a period of several days. The metal inks were then applied and processed according to the manufacturers' suggested temperature cycles to test their ability to penetrate a native layer of SiO_2. The second case, contact areas were cleared with hydrofluoric acid, rinsed, and dryed immediately prior to conductive ink application. This technique produces the minimum possible oxide thickness under the metal without the use of vacuum techniques; it provides that thickness of SiO_2 seen in most semiconductor industry metallization processes.

In order to reduce the influence of other unwanted variables, all six formulations were applied to individual large area planar diodes on a single silicon wafer. The diodes were approximatley $2.5cm^2$ in area with a contact area approximately $0.2cm^2$. All diodes were N on P, with the P-type substrate common to all diodes. The diodes were fabricated by ion implantation and had textured surfaces. The junction depth under each contact area was greater than that of the surrounding areas, being near 1.2 micrometers. As N-type regions of the diodes were electrically isolated from each other, it was possible to process the wafer as a unit and perform testing on the individual segments without scribing or otherwise interfering with the integrity of the wafer.

Firing temperature cycles utilized were those suggested by the manu-

facture of the silver containing formulations, and below the recommended 600°C to 1000°C firing temperature for the copper formulation. The temperature rise and fall rate was approximately 50 degrees per minute, and the peak temperature was 550 degrees C. The atmosphere was air, and the wafers were allowed to stay at the final temperature for three to five minutes. After firing, the wafer segments were tested for adherence, and electrical parameters were measured to evaluate series and shunt resistances resulting from poor ohmic contact or diode degradation respectively.

Adherence of the inks to the diodes was first observed. As anticipated, the copper formulation showed extremely poor adherence and will have to be treated separately. All five of the silver formulations, however, showed reasonable physical adherence in a "Scotch tape test".

The electrical performance of each ink was then evaluated. None of the inks showed significant penetration through the intentionally formed SiO_2 layer, while all exhibited electrical contact to the HF etched surface. This indicates that storage without an etching step immediately prior to ink application is inadvisable.

With freshly-etched surfaces, the series resistance was frequently high, indicating that either a high contact resistance was present or that the applied layers were too thin to adequately carry the desired current. The former possibility implies the desirability of a more controllable formation and/or a more severe heat treatment. The latter suggests either a thicker layer or a subsequent solder coating. In none of the above experiments was any significant degradation of the diode characteristics due to shorting or lifetime killing observed.

Among the unknowns of printed metallization is the long term reliability of modules operating in the terrestiral environment, and how this depends on processing and formulation variables.

It is a current conclusion that extensive developmental work on printable contact metallization formulations for silicon solar cells is needed. Attendant to this formulation development is the necessity for further process definition and development for solar cell application. A basic understanding of printed contact-silicon interfacial physics should be obtained. Sufficient promise exists for such commitment.

3.2.7.5 LAMINATION (CATEGORY 2)

The attachment of pre-shaped metallization patterns by lamination, such as a tape transfer technique, is also potentially attractive. Further development is necessary before it can be considered viable. Potential problems are similar to those facing printed metallization. No lamination research is being reported at this time.

3.2.7.6 SOLDER COATING (CATEGORY 4)

In many cases, solar cell metallization systems will be composed of a base metal system for electrical and mechanical contact to the silicon surface, and a solder coating which will be thick enough to act as the primary current-carrying metal. Sophistication of processing already exists in the solder coating areas, and little development work is required. However, it is necessary that the surface of the underlying metallization be amenable to controllable solder coating, implying that the soldering cycle may have to be tailored to the metallurgical properties of the contact metallization.

3.2.8 ANTIREFLECTION (AR) COATING

A necessity for achieving maximum efficiency from the solar cell is a high quality antireflection coating system. In some cases, this antireflection coating may be used for P-N junction passivation.

3.2.8.1 VACUUM DEPOSITION (CATEGORY 4)

The same basic comments made for metal vacuum deposition apply here, except that it is seldom required to pattern the AR film since it is generally

applied after metallization (a mechanical mask may be used to prevent AR film deposition on the bonding pad areas). Film thickness control is critical. While suitable technology is now available, other methods appear to be cost preferable. On the other hand, vacuum deposition is the best current method for applying some materials as AR films.

3.2.8.2 CHEMICAL VAPOR DEPOSITION (CATEGORY 4)

Silicon nitride could constitute an excellent choice for the anti-reflection coating on silicon solar cells. In addition to its useful refractive index ($n \cong 2.0$), it is the best silicon P-N junction passivant known to the semiconductor industry. It is extremely stable and inert. Silicon nitride can be deposited by low temperature CVD processes in a "soft" state which permits easy patterning using standard SiO_2 etching processes, and then can be transformed by a modest thermal cycle into its high density state. The CVD process could be much cheaper than a vacuum deposition process, and comparable to (or cheapter than) a spinning process if the deposition reactor capacity can be made large.

Silicon nitride has been deposited at 600°C in a hot wall, quartz lined furnace. The nitride is deposited from the reaction of silane (SiH_4) and ammonia (NH_3) in a nitrogen carrier gas. Deposition cycles of approximately 50 minutes have resulted in silicon nitride layers of 1050A° ± 100A°, this excellent uniformity applying to both variations within a run and variation from run-to-run. As established, the process deposits the nitride on wafers placed horizontally in the furnace; as a result this deposition system is capable of processing only five 3" wafers per run. This low throughput would be unacceptable for long range LSSA Project goals.

As an alternative deposition approach, greatly increased area throughput has been reported by silicon nitride deposition at a reduced (less than 1 atmosphere) pressure. Such a system has been utilized to simultaneously coat

seventy-five 3 inch diameter wafers with silicon nitride films having a thickness uniformity of ±5%.

3.2.8.3 DIRECT GROWTH (SiO_2) (CATEGORY 1)

The index of refraction of SiO_2 is essentially equal to those of all of the proposed encapsulant materials, making purposeful growth of SiO_2 as an AR coating unnecessary. If bare cells are considered, the SiO_2 would be a reasonable AR material. If it forms a better surface material for encapsulant bonding in a package, SiO_2 may be reconsidered; this event is considered unlikely.

3.2.8.4 PLASMA DEPOSITION (CATEGORY 2)

Deposition of antireflection dielectric coatings can be performed by plasma-aided CVD reactions at much lower temperatures than are possible by thermally activated CVD. This area is receiving considerable attention by the semiconductor industry, but it still needs technological advancment prior to extensive consideration for the LSSA Project.

3.2.8.5 SPIN-ON OR SPRAY-ON DEPOSITION (CAGEGORY 3)

Antireflection coating compounds can be applied in the same manner as photoresist, followed by a bake cycle to complete chemical reactions and/or to drive off solvents. Further heat treatment is frequently necessary to densify the film in order to realize optimum optical properties of the material.

Spin-on sources to deposit antireflection coatings of tantalum oxide or titanium oxide have been commercially formulated. As an example, a single application of spin-on can give a TiO_2 film which can be patterned in the as-

deposited condition. Following a 925°C densification, it has a thickness ranging from 800 to 1100A, is resistant to HF etching, and has an index of refraction of approximately 2.0. Application following metallization requires much lower temperature annealing steps. 250°C for 30 minutes can be used to give an AR coating of usagle quality; reliability of such low temperature-fired films needs to be ascertained.

While spin-on antireflection coatings may be useful on round, polished wafers, they will most likely be unsatisfactory for solar cells of rectangular shape or with surface roughness (either ripple, an as-grown surface, or a texture-etched surface). As discussed in Section 3.3.1, photoresist application by spinning on textured surfaces results in non-uniform thicknesses of photoresist over the surface features. It is anticipated that future application of this type of antireflection coating must be by spray-on techniques. At this point in time, it appears that spray-on thickness control and uniformity are not suitable for quality antireflection coating.

3.2.9 ANNEALING

All solar cell manufacturing process sequences require some high temperature annealing.

3.2.9.1 RESISTANCE FURNACE HEATING (CATEGORY 4)

This is the almost universal semiconductor industry tool. As currently utilized, its energy consumption is high. However, in a continuous, automated environment, the energy dissipation per unit area of silicon is capable of appreciable reduction from today's practices. Uniformity and control exist now, even for large area sheets, and the technology is proven.

3.2.9.2 DIRECT RADIANT HEATING:

HIGH TEMPERATURES (CATEGORY 2)

LOW TEMPERATURES (CATEGORY 4)

This technique has had only limited application in semiconductor technology for high temperatures, and has several inherent problems. The life of high intensity radiant sources is short, and output is somewhat variable during that lifetime. Uniformity and efficiency of heating require reflective surfaces for radiant energy manipulation; these can also degrade with use. When employed for high temperature (where radiant energy absorption is good) heating of silicon, direct radiant heating of large areas to a specific temperature is hard to control. Major technological advances are required for high temperature applications.

Low temperature applications, such as for solder reflow or photoresist baking, are well developed and are considered viable at this time.

3.2.9.3 LASER AND ELECTRON-BEAM HEATING (CATEGORY 3)

These emerging technologies show promise of excellent control and good efficiency. Application to semiconductor technology has been, however, limited, and requires further study before conclusions can be drawn. E-beam heating is being explored on another program under LSSA Task IV. Laser heating can be accomplished in any atmosphere, but E-beam heating must be performed in a vacuum.

3.2.9.4 RF HEATING (CATEGORY 1)

RF heating is broadly used in silicon epitaxy to obtain high temperatures in a "cold-wall" (and thus noncontaminating) system. Heating of the silicon for epitaxy is indirect, however, in that a conducting susceptor is first heated by the RF field; this susceptor, in turn, conductively heats the silicon.

This process is energy inefficient. A cold-wall system is not considered necessary for solar cell processing. Silicon wafers could be directly heated by RF energy, but the temperature control has been shown to be poor.

3.2.10 PATTERNING

Metallization, antireflection coatings, and dielectric layers for diffusion masks may require patterning in any given solar cell fabrication process.

3.2.10.1 PHOTOLITHOGRAPHY (CATEGORY 4)

Photolithography can be accomplished by either contact printing (direct mask contact to the silicon) or by projection or proximity (out-of-contact) masking techniques. Both proximity and projection require sophisticated optics, but can give extremely long mask life and well defined patterns on irregular surfaces. Both are far preferable, thus, to contact printing. In any case, mask alignment to the silicon substrate should be primarily mechanical, as opposed to optical, and realignments should be avoided if possible because they tend to be expensive. Exposure will continue to be by ultraviolet or visible light unless some technological breakthrough occurs in either laser, E-beam, or X-ray exposure. Application is expected to be limited to dielectric patterning.

3.2.10.2 SHADOW MASKING:

VACUUM METALLIZATION (CATEGORY 1)

PRINTED METALLIZATION (CATEGORY 4)

ION IMPLANTATION (CATEGORY 4)

This technique is too wasteful of material to be utilized for vacuum metallization of solar cells. On the other hand, planar P-N junctions can be formed by

shadow masking during ion implantation with excellent results and low cost. If planar junctions are utilized with ion implantation, masking will definitely be done by this technique.

Printed contacts are generally applied through a screen which, in effect, is a shadow masking operation. Printing contacts (in a manner analogous to operation of a printing press) would yield direct application in the desired pattern; this technique, however, appears to be receiving no current development.

3.2.11 INTERCONNECTION

Interconnections of solar cells into modules pose some stringent requirements for performance and reliability. The interconnection scheme must not contribute a substantial series resistance, or performance of the module can be seriously degraded. Experience derived from the semiconductor industry would suggest that metallurgical interactions are the most likely failure mechanisms. These can lead to reduced output, for example, as a result of increased series resistance, or interference with the optical path, or, perhaps more commonly, opened connections.

3.2.11.1 SOLDER REFLOW (CATEGORY 4)

The most widely used, and probably the most cost effective, solar cell interconnection scheme utilizes solder reflow. The technology is ready and has proven reliability. Properly applied, it can be used for the simultaneous formation of all interconnects in a module.

3.2.11.2 THERMAL COMPRESSION AND ULTRASONIC LEAD BONDING (CATEGORY 1)

Though widely used in the semiconductor industry, thermal compression bonding is useful mainly on small diameter (less than about 100μm) wires where deformation is accomplished by pressures low compared to the fracture

strength of silicon. Where millimeter sized bonds are required, this process is expected to be too damaging to the substrate to warrant further consideration.

Ultrasonic bonding is a low pressure process which utilizes ultrasonic energy to smear metal surfaces together, thereby establishing intimate contact for a metallurgical bond. It is not area limited, as is thermal compression bonding, but can damage substrates. It is also an unlikely future choice.

3.2.11.3 WELDING (CATEGORY 3)

Welded contacts are potentially as viable as those made by solder reflow. Welding, however, requires higher temperatures than soldering and can result in damage to the solar cell. Welding is used on small space cells, but its application to high current terrestrial cells will require additional innovation. Further detailed study is required before recommendation for future use can be made.

3.2.11.4 FILLED ADHESIVES (CATEGORY 2)

Metallic filled adhesives have had little or no application for bonding wires to solar cell metallizations. Filled adhesives are used in the semiconductor industry for relatively large area bonding (e.g., die attach). These materials have poorer electrical conductivities than metals, and the better ones (e.g., gold filled) are expensive. In a solar panel, where thermally or mechanically induced tensile stresses on the interconnect wires may be expected, the reliability of filled adhesive bonds is questionable. However, this field is continually changing, and should be monitored.

3.2.11.5 CLAMPED CONNECTORS (CATEGORY 1)

A direct clamping to the cell metallization is possible, especially if metal smearing at the contacts can be achieved without damage to the cell

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	COST[1] LABOR	COST[1] MATERIAL	COST[1] CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
1. Starting Material Surface										
a. Sawed	L	H	M	L	H	M	H	H	U	1
b. Sawed and etched	M	H	M	L	M	M	H	H	U	4
c. Lapped	L	H	M	M	M	H	H	H	U	1
d. Polished	M	H	M	H	H	H	H	H	U	1
e. Cleaned	U	U	U	U	L	U	L	U	U	2
f. As grown sheet	U	U	H	U	L	U	L	U	-	2
g. Texture-etched	H	H	H	L	L	L	H	H	H-U	4
2. In Process Cleaning or Etching										
a. Wet Chemical	H	H	H	L	M	M	H	H	H	4
b. Plasma	M-U	H-U	H	L	L	M	M	U	H	4
c. Vacuum Baking	M	H	L	M	L	H	H	H	L	1
d. Reverse Sputtering	H	M	L	M	L	H	M	H	L	1
e. Texture-Etching	H	H	H	L	L	L	H	H	H	4
f. Brushing	H	H	H	L	L	M	H	H	U	4
g. Gas Stream Drying	H	H	H	L	L	L	H	H	H	4
h. Gravity (centrifuge) Drying	H	H	M	L	L	M	H	H	L	4

H = High

M = Moderate

L = Low

U = Unknown or Insufficient data to make evaluation

Blank - Not meaningful evaluation

[1] Qualitative or preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	COST[1] LABOR	MATERIAL	CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
3. Lifetime Enhancement & Preservation										
a. Complexing and Removal	M	M	M	M	M	M	M	J	U	3
b. Temperature - time profiling	M-U	H	H	L	L	H	H	U	U	3
c. Leaching	M-U	M	H	L	L	M	M	U	U	3
d. Precipitation (damage sites)	M-U	M	M	L	L	M	M	U	U	3
4. Junction Formation										
a. Epitaxy	M	L	M	M	M	H	M	M	M	1
b. Diffusion	M	H	M	M	M	M	H	H	H	4
c. Ion Implantation	H	H	H	M	L	H	M	H	H	4
d. Alloy	L	L	M	M	M	H	L	M	M	1

H = High

M = Moderate

L = Low

U = Unknown or insufficient data to make evaluation

Blank - Not meaninfgul evaluation

Qualitative or preliminary evaluatio

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	COST[1] LABOR	COST[1] MATERIAL	COST[1] CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
5. Metallization										
a. Vacuum	H	M	M	M	M	H	H	H	M	1
b. Plating	H	H	H	L	M	L	M	H	H	4
c. Chemical Vapor Deposition	L	M	M	M	H	M	L	U	M	1
d. Printed	M	H	H	L	M	M	L	U	M	4
e. Lamination	U	U	H	L	M	M	L	U	M	2
f. Solder Coating	H	H	H	L	L	M	H	H	H	4

H = High

M = Moderate

L = Low

U = Unknown or insufficient data to make evaluation

Blank - not meaningful evaluation

[1]Qualitative or preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	COST [1] LABOR	COST [1] MATERIAL	COST [1] CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
6. Antireflection Coating										
a. Vacuum Deposition	H	H	M	M	M	H	H	M	M	4
b. Chemical Vapor Deposition	H	H	M	L	M	M	H	H	H	4
c. Direct Growth (S_iO_2)	L	H	H	L	L	M	H	H	H	1
d. Plasma Deposition	U	M	M	M	M	H	L	U	M	2
e. Spin-on or Spray-on Deposition	M	M	H	M	M	M	M	U	M	3

H = High

M = Moderate

L = Low

U = Unknown or Insufficient data to make evaluation

Blank - Not meaningful evaluation

[1] Qualitative or preliminary evaluatio

TABLE I: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	COST: LABOR	COST: MATERIAL	COST: CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
7. Annealing Sources										
a. Resistance Furnace	H	H	H	L	L	M	H	H	H	4
b. Radiant	M	M	H	L	H	M	M	M	M	2/4
c. Laser	U	H	H	L	L	H	L	U	H	3
d. Electron Beam	U	H	M	M	L	H	L	U	U	3
e. RF	M	M	M	L	L	H	M	M	M	I
8. Patterning		—								
a. Photolithography	H	H	H	M	M	H	H	H	H	4
b. Metal Shadow Masking	M	M	M	M	H	M	H	H	M	I
c. Ion Implantation Shadow Masking	H	H	H	L	L	L	H	H	M	4

H = High

M = Medium

L = Low

U = Unknown or Insufficient Data to make evaluation

Blank - Not meaningful evaluation

I Qualitative or preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

PROCESS	PERFORMANCE	CONTROLLABILITY	AMENABILITY TO AUTOMATION	COST[1] LABOR	COST[1] MATERIAL	COST[1] CAPITAL	STATE OF READINESS	RELIABILITY CONSIDERATIONS	SHEET GEOMETRIES	CATEGORY
9. Interconnection										
a. Solder reflow	H	H	H	L	L	M	H	H	H	4
b. Thermal Compression Bonding	M	H	M	M	L	M	H	M	L	1
c. Ultrasonic	M	M	M	M	L	M	H	M	L	1
d. Welding	H	M	M	M	L	M	H	H	M	3
e. Filled Adhesives	M	H	H	L	H	M	L	U	M	2
f. Clamped Connections	M	M	L	M	M	M	L	U	L	1

H = High

M = Moderate

L = Low

U = Unknown or insufficient data to make evaluation

Blank = Not meaningful evaluation

[1]Qualitative or preliminary evaluation

TABLE 1: PROCESS EVALUATION MATRIX (CONTINUED)

itself and pressure can be maintained in the package. Without such smearing, moisture ingression to the contacts would increase resistance and reduce module reliability. Tooling would be expected to be complex to provide smearing without fracturing cells, with little assurance of control or reliability. This process is deemed unlikely to succeed for solar cells.

3.2.12 CATEGORY 4 PROCESSES

The processes which at this time appear to have a very high probability of incorporation into a future production process are tabulated here as a separate group of category 4 items.

1. Starting Condition
   a. Sawed and Etched Surfaces
   b. Texture-Etched Surfaces
2. In-Process Surface Cleaning or Etching
   a. Wet Chemical
   b. Plasma
   c. Texture-Etching
   d. Scrubbing
   e. Gas Stream Drying
   f. Gravity (Centrifuge) Drying
3. Junction Formation
   a. Ion Implantation
   b. Diffusion
4. Metallization
   a. Plating
   b. Printing
   c. Solder Coating

5. Antireflection Coating
    a. Vacuum Deposition
    b. Chemical Vapor Deposition
6. Annealing
    a. Resistance Furnace Heating
    b. Low Temperature Radiant Heating
7. Patterning
    a. Proximity Photolithography
    b. Projection Photolithography
    c. Ion Implantation Shadow Masking
8. Interconnection
    a. Solder Reflow

3.3 PROCESS SEQUENCING OPTIMIZATION AND SOLAR CELL FABRICATION

Solar cell fabrication is accomplished by performing a number of individual process steps in a process sequence. While isolated individual process steps may appear satisfactory when assessed alone, experience in the semiconductor industry has shown that most process steps require modification and trade-offs when incorporated into an optimum process sequence. Such modifications may necessarily be drastic, making an otherwise seemingly desirable individual process step undesirable when utilized in the sequence. This study portion of the program was undertaken to identify and optimize overall process sequences.

3.3.1 TEXTURED SURFACE-PHOTORESIST INTERACTIONS

As an example of process step interactions, a process sequencing study investigated photoresist coverage of textured surfaces. The study identified

an undesirable effect, resulting in corrective modifications to the photoresist procedure.

A process interaction between photolithography of dielectrics on textured surfaces and plating of metal contacts was observed. The dielectric is deposited on the textured surface to act both as an antireflection coating and as a plating mask. Following dielectric deposition, the dielectric is patterned photolithographically to define the metal contact pattern; and the metal contacts are plated into the pattern openings. (The retained areas of dielectric serve as a plating mask.) Failure of the dielectric as a plating mask can be observed in a scanning electron microscope (SEM) photomicrograph (5000X), Figure 3-6. Here, metal has plated onto unintentionally exposed silicon peaks of the textured surface.

In our laboratory, normal photoresist procedure for polished wafers utilizes thin, 44 cp (0.044 $N \cdot S/m^2$) photoresist and spin speeds of 5000 rpm. This procedure was applied initially to patterning silicon nitride dielectric layers deposited on textured surfaces, and resulted in exposure of silicon peaks and their subsequent plating with metal. Following identification of this phenomenon as a photoresist problem, the photoresist technique has been modified. Complete photoresist protection appears to be achieved by increasing photoresist viscosity to 240 cp (0.24 $N \cdot S/m^2$) and reducing spin speeds to 3000 rpm.

3.3.2 PROCESS SEQUENCE SELECTION

Process sequences were selected utilizing the process steps placed in Category 4. The process sequences are amenable to either P-on-N or N-on-P cells. (For the sake of conciseness and convenience of presentation, the processes outlined will result in N-on-P type cells.) The process sequences

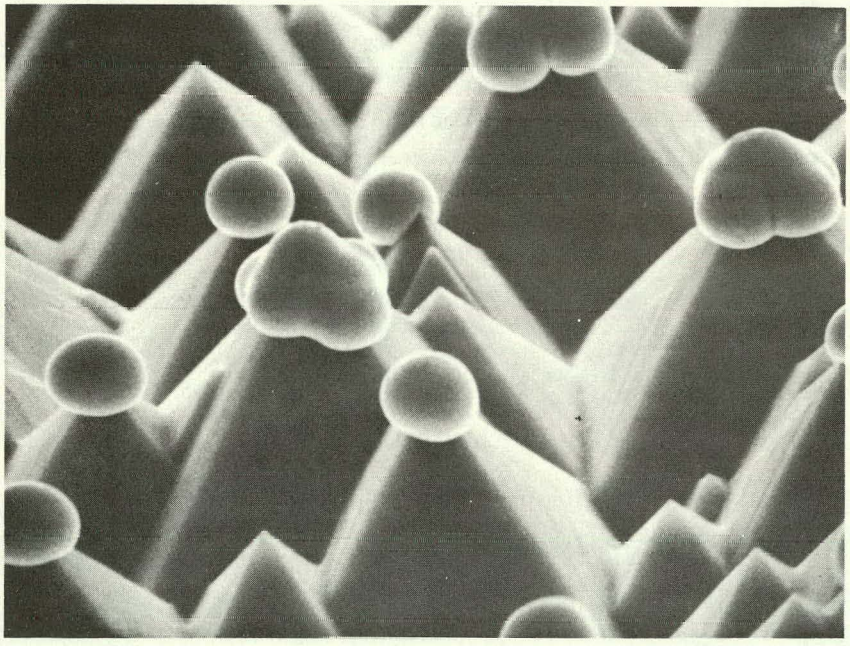

FIGURE 3-6: SEM Photomicrograph of electroless nickel plated surfaces of unprotected pyramid peaks, 5000X, 60° tilt.

are also chosen from process steps tolerant of any silicon substrate geometry and to varying degrees of surface waviness, warp, etc.

3.3.2.1 ION IMPLANTATION/DIFFUSION PROCESS SEQUENCE

A process sequence utilizing ion implantation to form the P-N junction and diffusion to form the back surface field is listed below:

1. Perform P+ diffusion over entire wafer, simultaneously growing layer of SiO_2. This forms the back surface field.
2. Apply resist to one side, remove SiO_2 on opposite side, remove resist.
3. Texture etch exposed silicon surface.
4. Deposit silicon nitride (CVD) over wafer surfaces.
5. Pattern metal grid into silicon nitride on textured surface using photolithographic techniques, simultaneously cleaning dielectric from back surface.
6. Ion implant front (textured) surface with N-type dopant to form N-P junction. Ions are mechanically masked from wafer edge to form planar junction.
7. Anneal wafers to activate implanted ions. P-N junction in metal grid openings is deeper than beneath nitride.
8. Plate and sinter metallization, front and back.
9. Solder coat.

3.3.2.2 DIFFUSION PROCESS SEQUENCES

Two process sequences utilizing diffusion for both P-N junction and back-surface field formation are identified below:

DIFFUSION PROCESS SEQUENCE 1

1. Perform Blanket P+ Diffusion, Oxide Growth
2. Apply Photoresist, Protect Back, Etch Planar Junction Pattern in Oxide.
3. Texture Etch Exposed Front Area.
4. Diffuse Planar Junction
5. Remove Diffusion Oxide, Deposit Silicon Nitride
6. Photoresist Metallization Pattern, Protect Back
7. Metal Contact Diffusion
8. Strip Back, Clear Contact Areas
9. Plate and Sinter Metallization, Front and Back
10. Solder Coat

DIFFUSION PROCESS SEQUENCE II

1. Perform Blanket P+ Diffusion, Oxide Growth
2. Apply Photoresist, Protect Back, Etch Planar Junction Pattern in Oxide
3. Texture Etch Exposed Front Areas
4. Diffuse Planar Junction
5. Remove Diffusion Oxide, Deposition Silicon Nitride
6. Photoresist Metallization Pattern
7. Plate and Sinter Metallization, Front and Back
8. Solder Coat

The primary difference between the two diffusion process sequences is that the first provides a deep P-N junction beneath front metal contacts while the second sequence does not.

3.3.3 SOLAR CELL FABRICATION

Solar cells have been fabricated in our laboratory utilizing both ion implantation and diffusion process sequences for P-N junction formation. These cells were then evaluated and compared. Evaluation was based upon short circuit current, open circuit voltage, maximum power point, and process yield.

Ion implanted cells have been evaluated under AM0 spectrum, $100mW/cm^2$ illumination. A three inch diameter cell with a planar implanted junction in a textured surface exhibited a maximum power point near 565mW. The planar junction area, including metallization area, is approximately $43cm^2$, while the wafer area is near $45cm^2$. This indicates an AM0 conversion efficiency of approximately 13.1% based upon junction area and 12.6% based upon total wafer area. These efficiency figures would, of course, be higher if considered under AM1 illumination, and indicate that ion implantation is a viable process technique for high efficiency solar cells.

Diffused-junction cells have been similarly evaluated, but under tungsten illumination calibrated to yield the same test as those obtained on ion implantation is a viable process technique for high efficiency solar cells.

In all solar cell fabrication tests, P-N junction depth was near 0.5 micrometer, deeper than optimum for maximum short wavelength response and overall cell efficiency. For shallower junctions, however, it was found that yields were higher for diffusion and ion implantation process sequences which had deeper junction areas under the contact metallization regions than for diffusion process sequences lacking that teature.

3.4 INTERCONNECTION AND ENCAPSULATION

In order to establish working systems of useful size, individual solar cells must be interconnected in some manner, and then encapsulated. Interconnection and encapsulation both play a major role in establishing (and enhancing) module reliability.

There is a trade-off between solar cell durability in harsh environments, and encapsulation requirements to protect the cell from these environments. This trade-off must be considered in terms of a minimum twenty year service life for the encapsulated cell.

The cost effectiveness of any particular encapsulation structure is heavily dependent upon the expected life (MTBF, or mean time before failure) of a totally unprotected cell as compared to the expected life of that cell within the encapsulation structure. It is presently felt by Motorola that single sided encapsulation structures, such as mounting on a glass cover, or using an epoxy-fiberboard substrate plus a silicone adhesive and covering for the cells, are insufficient to protect cell structures for long term terrestrial service. Until the MTBF of unencapsulated cells can be projected to 20 years, Motorola feels both front and back covers should be incorporated into the encapsulation system to meet the reliability goals of the LSSA Project.

It is anticipated that the most common failure modes for solar cell modules will be one of two types:

1. Failure of a solar cell interconnect within the package, as a result of strains due to thermal stresses or mechanical motion, or as a result of chemical or electrochemical corrosion.

2. Localized interference of the optical path, by delamination or physical coverage, i.e., by a leaf, localized debris, or wildlife.

3.4.1 INTERCONNECTION

The above failure modes are most severe for single contact, series interconnected cells, suggesting future use of both redundant cell contacts and parallel-oriented cell interconnections. In aiming towards an MTBF of 20 years, it must be expected that some interconnect failures will occur in a large array. In a series-connected panel, failure of an interconnect internal to the package (open circuit to either side of a solar cell) will cause entire module failure (open circuit). The use of redundant contacts to each solar cell will greatly reduce the magnitude of the effect of a single contact failure on the module performance. Instead of an open circuit, the output current will be reduced by some nominal factor (e.g., 5%, but dependent upon detailed cell design) if a single front surface contact opens.

Shadowing by relatively small objects is perhaps the most objectionable failure mode of the series-connected solar cell panel. Although intermittent, shadowing by leaves, debris, or wildlife on the external surface of a module will cause failure; almost total open circuit if an entire cell is shadowed, and reduced current output if the cell is only partially shadowed.

These types of failures may be alleviated by incorporating redundancy within a module through the use of a parallel or series-parallel cell interconnection schemes. Some schemes increase module (and system) reliability while insuring at least equivalent total system performance.

Any interconnection (and encapsulation) design, thus, should permit incorporation of some degree of parallel interconnections.

3.4.2 MODULE MATERIALS AND ENCAPSULATION

Materials must be chosen for solar cell modules, both for interconnection and for encapsulation, on the basis of functional compatability, long term reliability, and cost. The emphasis, while shared between these criteria, cannot compromise long term reliability. Accordingly, a set of encapsulant and interconnect materials was chosen for study on this program, with emphasis on proven histories of stability in terrestrial environments. Interconnection of cells is accomplished by solder reflow. The encapsulant system consists of a front glass cover, a stainless steel back plate, silicone potting, and a stainless steel bezel to act both as a structural member and as a sealing surface for formed-in-place gasketing. This structure has been shown to resist moisture ingression during stress testing as discussed in Section 3.4.4. The structure has good thermal dissipation and should offer long service life. Solar cell encapsulation has been successfully performed utilizing this system.

3.4.3 PROTECTIVE COATINGS FOR METAL ENCAPSULANT PARTS

A metal back plate may be utilized in encapsulating solar cells. It must be corrosion-resistant to achieve the twenty year life expectancy of the module. Both aluminum and stainless steel are possible materials, with stainless steel having the more suitable thermal expansion properties. Aluminum is particularly susceptible to corrosion in environments containing certain pollutants (e.g., salt, some industrial waste gases).

In order to reduce the overall cost of encapsulating solar cells, it would be desirable to utilize a material cheaper than stainless steel. Use of cold rolled steel would result in a savings of 5X (i.e., stainless steel = 60¢/ft^2 -- cold rolled = 12¢/ft^2). These prices reflect the cost of sheets 15 - 18 mils thick. It appears that cold rolled can be used if properly protected from the environment. A material, Rilsan Nylon 11, has been used

for approximately 25 years to coat items such as gas cylinders, underground piping, ship parts and outdoor furniture. It apparently has excellent wear properties for these and other applications. Application of the material is achieved by electrostatic spraying or fluid bed dipping followed by a heat treatment to fuse the powder. Electrostatic spraying can provide layers of approximately 3 mils while fluid bed applications have a minimum thickness of 8 - 10 mils. Material cost of 2¼¢/mil/ft^2 results in 7¢/ft^2 for the electrostatic process and 18¢ - 25¢ for the fluid bed process. Application costs range from 2 to 5 times material cost. Hence, electrostatic spraying of nylon on cold rolled steel could reduce costs and give acceptable long term reliability. Furthermore, numerous colors can be applied, thereby improving reflecting and radiating qualities of the package.

3.4.4 MOISTURE INGRESSION

Semiconductor industry experience on reliability and failure modes indicates that the solar cell metallization and interconnect system can be expected to be perhaps the region most vulnerable to failure resulting from package moisture ingression. Absolute exclusion of moisture from a solar cell module for a period of twenty years would require hermetic seals, and hence would place severe economic strains on the encapsulation system. A far preferable solution would be a moisture resistant cell metallization and interconnect system.

Some current solar cell metallization systems, such as titanium-silver, have already shown reliability problems in moist ambients and would require special protection techniques to achieve a twenty year minimum service life. This is not unexpected from the experience in the semiconductor industry. Design choices for future solar cells should be based on metallization system

reliability in moist ambients, and the final choice may be dictated primarily by this criterion.

It is not just moisture, but the combination of moisture and contaminants in the environment surrounding the metallization and contacts, and the effects of applied or generated electric fields and contact potentials, that must be considered. Even gold, which is considered to be quite inert, has been shown to exhibit severe degradation via electrochemical attack in plastic-encapsulated silicon integrated circuits, and also in hermetic packages that were sealed with some moisture inside.

A stress testing method for measuring moisture ingression into potential encapsulation and materials configurations has been investigated. The technique involves impregnation of color-indicating-dessicant materials into mock-ups of module designs. In a preliminary test, a color indicating dessicant was impregnated into a silicone potting compound in dummy modules with a glass cover and a stainless steel backplate. The modules were then boiled in water for times up to two weeks, periodically inspecting the dessicant. An approximate value for both interfacial and bulk moisture ingression can be obtained merely by visual inspection. This technique is one of those being utilized to evaluate encapsulation designs and materials.

3.5 COST ANALYSIS

Analysis of the costs of performing both individual process steps and process sequences was performed. This analysis was based upon today's technology projected to large volume production, and has been performed in a format conforming to the information chart utilized by JPL for summary of Task IV data. This format identifies the following items:

Material

Expense

Labor

Overhead

Interest

Depreciation

Capital Equipment

Facilities

The three primary assumptions made in this cost analysis are:

1. The factory produces only one product and sells that product to less than ten customers at a rate of 500 peak megawatts/year.
2. The costs reflect today's technology in terms of the level of automation, throughput, maturity of process, etc.
3. Overhead charges can be defined for a new, dedicated factory and need not be patterned after any existing factory.

In order to perform a detailed cost analysis, a methodology was first developed with general inputs and assumptions being defined. It must be cautioned at this time that Motorola's methodology may differ from methodologies used by the other Task IV contractors performing a similar study. This means, thus, that differences in assumptions and cost inputs by each contractor will result in different cost allocations per category. The most meaningful comparison between various contractor's cost analyses must be made on the Total Cost basis. Further, costs were developed on an individual process step basis, but meaningful cost analysis for solar cell manufacturing can only be made for a total process sequence. Each process step cost must, then, be placed in a viable process sequence, and adjusted for the total process sequence yield

following that step in order to have a true significance in manufacturing cost analysis. In order to allow this adjustment to be made, individual processing step costs are being calculated on a 100% yield basis, with a probable process yield percentage being estimated for use in subsequent process sequence yield calculations.

3.5.1 GENERAL AND SPECIFIC COST ASSUMPTIONS

The following pages present in tabular form the assumptions and inputs utilized for the processing cost analysis.

Electrical power consumption has been allocated between the overhead account and the expense account. In calculating the overhead allocation, the base level of building services for lighting and HVAC (heating, ventilating, and air conditioning) was assumed and allocated on the basis of floor space. For the expense allocation, identifiable electrical consumption for each process (including equipment power and HVAC for power dissipation, exhaust and make-up air, and body heat contributed by personnel) was utilized.

In addition to chemicals, electricity, D.I. water, and waste treatment, some process steps have significant consumption of expendable items. Where possible, items such as quartz, brushes, pump oil, holders and carriers, masks, screens, and adhesives have been identified and included in the expense column.

GENERAL INPUTS & ASSUMPTIONS

1. Factory produces only one product and supplies less than ten customers
2. Annual production level = 500,000,000 peak watts
3. Total work days/year = 240; (260-20, vacation, holiday etc.)
4. One work day = 3 shifts = 22.5 work hours; (24-1.5 lunch)
5. First shift, second shift, third shift - 8, 8, 6.5 hrs. respectively
6. Second and third shift premium = 10%
7. Balanced line operation for all three shifts resulting in an effective labor rate of 1.064 times the first shift rate.
8. First Shift Rate = $4.00/hour
9. Silicon starting material cost = $0
10. Starting material sheets = 3 inch (7.6cm) Dia. Silicon wafers; Area = $45cm^2$.
11. One module = 48 starting material sheets
12. Efficiency/cell - 15% (average)
13. Output power/cell = 0.667 peak watts (average/cell)
14. Output power/module = 30 peak watts (average/module)
15. Individual process step cost estimates are based on 100% processing step yields. (Actual process step cost is achieved by multiplying the true process step yields for the overall process sequence)
16. Electricity cost = 2.5¢/KWH
17. Burden and fringes = 40% of labor
18. Interest rate = 9%/year
19. Depreciation on equipment = SL 7 years
20. Depreciation on building = SL 40 years
21. Support electrical consumption = $1.36/$ft^2$/year (Includes lighting at 4 watts/ft^2; HVAC at 40% duty cycle of 10 watts/ft^2 and yearly run rate of 6800 hours or 100% work week plus 10% weekend factor).
22. Other utilities (water) = $0.06/$ft^2$/year (In part, dependent on total number of employees but assumes a density of people per ft^2 consistent with automated production level of Assumption 2.)
23. Miscellaneous building services =$0.45/$ft^2$/year (estimated)

DEFINITION OF ACCOUNTS

1. Materials

Items which are incorporated into the final cell which can be identified in their original form, e.g., (silicon, solder, steel, glass, etc.)

2. Expense Items

Items that are consumed in the manufacturing operations that do not appear (in their original form) in the final cell e.g., (acids, solvents, gases, dopants).

3. Labor

Actual direct labor costs increased by burden and fringes (40%) (Examples of burden and fringe accounts are shown in attachments).

4. Overhead

All other costs not identified as material, expense, labor, interest, or depreciation (examples shown in attachment).

5. Interest

Fee paid on investment debt, (9% of capital: Equipment + Facilities).

6. Depreciation

Straight line 7 year depreciation on equipment (14.3% of capital), 40 year depreciation on facilities (2.5% of facilities).

7. Totals

Sum of materials, expense items, labor, overhead, interest, and depreciation.

8. Process Yield

Estimated thru-put yield; net good units/input units. (Process sequence yield product of process step yields.)

BURDEN ACCOUNTS

(EXAMPLES)

1. Utility Operators
2. Employee instruction time
3. Set-up time
4. Clean-up time
5. Coffee breaks and rest room time
6. Material handling and transfer
7. Data compilation and transfer

EMPLOYEE FRINGES

(EXAMPLES)

1. Vacation
2. Holiday
3. Retirement Fund
4. Insurances
5. Cafeteria
6. F.I.C.A.
7. Unemployment Taxes
8. Credit Union
9. Employee Sales
10. Recreation Activities

ASSUMPTIONS FOR
BUILDING & MANUFACTURING

1. Factory floor space will be 70% production, 30% support (offices, warehouses, cafeterias, etc.)
2. Construction cost for production space is $80/sq. ft.
3. Construction cost for support space is $30/sq. ft.
4. Construction cost for factory is $65/sq. ft.
5. One factory sq. ft. = 1.43 machine sq. ft.
6. Interest Rate = 9%/year.
7. Depreciation Costs = $\frac{1}{40}$ / year
8. Taxes & Insurance = 5%/year
9. Summary & Cost Identification
   - Average Factory Space -
   a. Depreciation = $(\frac{1}{40})$ (65) = $1.62/sq. ft./year
   b. Interest = (9%) (65) = $5.85/sq. ft./year
   c. Taxes & Ins. = (5%) (65) = $3.25/sq. ft./year

OVERHEAD ACCOUNTS
SPECIFIC ASSUMPTIONS

1. Committed Costs: Floor space charges, taxes and insurance, at 5% of construction cost.

2. Direct Factory Overhead: Payroll for supervisors and foreman; expense items not covered previously such as telephone, office supplies, protective clothing, filters, plant supplies, electronic parts, carrier supplies, equipment maintenance, etc.

   2.1 Pay Rates:
   Supervisor = $12,000/year + 25% Fringes
   Foreman = $16,000/year + 25% Fringes
   Maintenance Tech = $11,500/year + 25% Fringes

   2.2 Labor Ratio: S:F:MT:Operator = 3:1:6:100

   ....This results in an effective rate of 15.0% of direct labor on a three shift basis factoring in premiums.

   2.3 Other Expense: 3% of Direct Labor

3. Indirect Factory Overhead:

   3.1 Pay Rates:
   Production Control = $14,000/Yr + 25% Fringes
   Ind. Engineer = $17,000/Yr + 25% Fringes
   Cust. Service = $16,000/Yr + 25% Fringes
   Inventory/Audit = $12,000/Yr + 25% Fringes

   3.2 Labor Ratio:
   PC:IE:CS:IA:OPERATOR = 12:3:1:4:1000

   ...This results in an effective rate of 3.8% of Direct Labor on a three shift basis factoring in premiums.

4. Material Support: Chemical mixing and preparation, purchasing, inventory control, material control, warehouse.

   4.1 Pay Rates:
   Chem. Mix = $8,300/Yr + 25% Fringes
   Purchasing = $16,000/Yr + 25% Fringes
   Inv./Mat'l Control = $14,000/Yr + 25% Fringes
   Warehouse = $12,000/Yr + 25% Fringes

   4.2 Labor Ratio:
   CM:P:IM:W:OPERATOR = 3:2:8:12:1000

   ...This results in an effective rate of 3.7% of direct labor on a three shift basis factoring in premiums.

5. Building Services: Janitorial, security, plant engineering, maintenance, electricity and other utilities at rate for support floor space (background).

   5.1 Support electrical consumption = $\$1.36/ft^2$/year (includes lighting at 4 watts/ft^2; HVAC at 40% duty cycle of 10 watts/ft^2 and yearly run rate of 6800 hours or 100% work week plus 10% weekend factor).

   5.2 Other utilities (water) = $\$0.06/ft^2$/year level of 500,000 peak watts per year.)

   5.3 Miscellaneous building services = $\$0.45/ft^2$/year (estimated)

6. Quality Assurance: QA and AC at 1.5% of direct labor (includes equipment calibration but not process control)

7. Sustaining Engineering:

   7.1 Pay Rates: Technician = $11,500/year + 25% fringes
   Engineer = $17,000/year + 25% fringes

   7.2 Labor Ratio:

   T:E:OPERATOR = 15:15:1000

   ...This results in an effective rate of 5.4% of direct labor on a three shift basis factoring in premiums.

8. R&D Engineering: Assumed constant at $10,000,000/year and constant 10 step process sequence. Therefore, $1,000,000 will be arbitrarily allocated to each process step. For example, the R&D costs would be equivalent to a 4% of gross sales for the factory at $0.50/watt.

9. Major Factory Revisions: Equipment and facilities construction, machine shop, etc. Assumed at zero net cost. Any designed and implemented changes must be offset by an equivalent cost savings.

EXPENSE COSTS

ACIDS

HF	$ 2.90/Gal.
Acetic	$ 3.95/Gal.
Nitric	$ 2.45/Gal.
HCl	$ 2.97/Gal.
Sulfuric	$ 2.45/Gal.
NH_4:HF	$ 2.97/Gal.
Waste Treatment	$ 0.0020/Gal. X DIH_2O consumption

SOLVENTS

Ethylene Glycol	$19.20/Gal.
Iso Alcohol	$ 1.05/Gal.
Acetone	$ 1.15/Gal.
Butyl Acetate	$ 2.60/Gal.
VMP	$ 0.75/Gal.
Resist 44cps	$55.19/Gal.
DIH_2O	$ 0.0031/Gal.
J100	$ 7.25/Gal.

GASES

Nitrogen	$ 0.0033/CF
Helium	$ 0.044/CF
Argon	$ 0.1172/CF
Oxygen	$ 0.002/CF
BCl_3	$ 3.4091/CF
PH_3	$28.0702/CF
Hydrogen	$ 0.044/CF
H_2SiCl_2	$ 8.6331/CF
NH_3	$ 1.0619/CF

The following table shows the specific assumptions made with respect to capital equipment, floorspace, power, and labor for each processing step.

EQUIPMENT DEFINITION
SPECIFIC ASSUMPTIONS

PROCESS STEP	ITEM	COST (K$)	AREA (FT^2)	CAPACITY (WPH)	POWER (KW)	EXHAUST (CFM)	DIH_2O (GPM)	N_2 (l/M)	STAFF (OPI)	MACHINE UTILITY
1. Brushing	Scrubber (HP) Hood for scrubber	14.825 1.435	45	250	.12 .24	80	.2		.33	.88
2. Plasma (Dielectric etch)	Plasma (etchings)	65.0	36	200	5.0	20			.165	.88
3. Standard Solutions	6' Acid Hood 6' Solvent Hood	4.5 3.8	45 45	800 800	1.1 1.1	1800 1800	1.5		.5	92
4. Centrifuge Drying	Rinser-Dryer	2.5	30	600	1.0		1.6	23.2	.25	.88
5. Silicon Etching (one side)	6' Hood Barrel-etch	5	45	200	.5	900	2		.5	.92
6. Silicon Etching (two sides)	6' Hood Barrel-etch	5	45	200	.5	900	2		.5	.92
7. Texture Etch	6' Hood Texture etch	4.5	45	200	1.1	1800			.5	.92
8. Edge Grinding	Edge Grinder	16.1	45	125	1.1	80			.33	.88
9. Photo-resist (Apply-Expose-Develop).	Coater-Oven Developer-Oven Alignment Tool	18.120 15.005 30.718	80 45	250 250 200	2.4 2.4 1.2	120 120			3.96	.88
10. Photo-Resist (Remove)	6' Acid Hood 6' J100 Hood	4.5 4.5	45 45	400 400	1.1 1.1	1800 1800	1.5		.5	.92

EQUIPMENT DEFINITION
SPECIFIC ASSUMPTIONS

PROCESS STEP	ITEM	COST (K$)	AREA (FT^2)	CAPACITY (WPH)	POWER (KW)	EXHAUST (CFM)	DIH_2O (GPM)	N_2 (l/M)	STAFF (OPI)	MACHINE UTILITY
11. Plasma (P.R. Remove)	Plasma (ashing)	1.0	18	100	1.5				.165	.88
12. Dielectric Etch (Wet)	6' Acid Hood	4.5	45	400	1.1	1800	1.5		.5	.92
13. Etch Stop (Apply)	Coater-Oven	33.39	80	500	4.8	120			.33	.88
14. Spin-On Diffn.	Coater-Oven (Spin)	33.39	80	500	4.8	120			.33	.88
15. Spray-On Diffn.	Coater-Oven (Spray)	33.39	80	500	4.8	120			.33	.88
16. Drive-In (Diffusion)	(Diffusion-Drive In) Diffusion FCE	67.0	275	1000	140	125		24	1	.88
17. Silicon Source (Solid)	(Solid Source) Diffusion FCE	67.0	275	500	140	125		24	2	.88
18. Gas Deposition and Diffusion	(Gas Dep. + Diff'n) Diffusion FCE	67.0	275	1000	140	125		24	1	.88
19. Doped Oxide (CVD) Diff'n	(CVD) Diffusion FCE	67.0	275	1000	140	125		24	1	.88
20. Ion Implant	I^2 - 2mA	300.00	400	80	20	200			.5	.75
21. Ion Implant (Advanced)	I^2 - .1A	500.	400	2500	50	200			.5	.75

EQUIPMENT DEFINITION
SPECIFIC ASSUMPTIONS

PROCESS STEP	ITEM	COST (K$)	AREA (FT^2)	CAPACITY (WPH)	POWER (KW)	EXHAUST (CFM)	DIH_2O (GPM)	N_2 (l/M)	STAFF (OPI)	MACHINE UTILITY
22. Vacuum Metallization Cu, Al	(box coater) E-Beam Evap.	112	225	160	12	20	6		.5	.88
23. Thick Film Ag Front	Screen Printer	37.55	40	2000	1					.75
	Annealing FCE	20	64	2000	8	125		15	1	
24. Thick Film Ag Back	Screen Printer	37.55	40	2000	1				1	.75
	Annealing FCE	20	64	2000	8	125		15		
25. Electroless Plating	Electroless Plate									.90
	(1) 6' Hood	4.5	45	7200	1.1	1800	0		1	
	(2) 6' Hoods	9	90	7200	2.2	3600	3		1	
	(2) 6' Hoods	9	90	7200	2.2	3600	0		1	
	(2) 6' Hoods	9	90	7200	2.2	3600	3		1	
	(12) Rinser-Dryer	30	360	7200	12	0	19.2		3	
	(2) 8-pack FCE	134	550	7200	280	250	0	48	2	
	(2) 6' Hoods	9	90	7200	2.2	3600	0		2	
	(2) 6' Hoods	9	90	7200	2.2	3600	3		1	
	(12) Rinser-Dryers	30	360	7200	12	0	19.2		3	
	TOTAL	244	1765	7200	316.1	20050	47.4	48	15	.90
26. Electrolytic Plating	Electroplate	244	1765	7200	316.1	20050	47.4	48	15	.90
27. Solder Coating	Flux Dip Hood Pre-Heat Oven Solder Pot	20	60	7500	5	200			1	.88
	Aqueous Cleaner or Solvent Hood Rinser-Dryer	30	60	7500	2	200	3			

EQUIPMENT DEFINITION SPECIFIC ASSUMPTIONS

PROCESS STEP	ITEM	COST (K$)	AREA (FT^2)	CAPACITY (WPH)	POWER (KW)	EXHAUST (CFM)	DIH_2O (GPM)	N_2 (l/M)	STAFF (OPI)	MACHINE UTILITY
28. Silicon Nitride (CVD) AR	(CVD) Diffusion FCE	67	275	1000	140	125			1	.88
29. Oxide Growth AR	Diffusion FCE	67	275	2000	140	125		(O_2) 24	1	.88
30. Spin-On AR	Coater-Oven (Spin)	33.39	80	500	4.8	120			.33	.88
31. Evaporate AR	(box coater) E-Beam Evap.	112	225	160	12	20	6		.5	.88
32. Add Solder	Flux Applicator Wave-Solder Conveyor	20	60	7500	5	200	3		.5	.88
33. Reflow Solder	Cell Align Belt Furnace Conveyor	70	150	3000	10	200		20	1	.88
34. Conductive Adhesives	Screen Printer	37.55	40	2000	1					
	Annealing FCE	20	64	2000	8	125		15	1	.75
				Panels						
35. Glass Superstrate	Alignment Fixture	12	24	720	.5				2	.88
	(12) Silicone Mix-Dispense	35	432	720	12	600				
	(24) Vacuum Chamber	283	1728	720	36	1200				
	(36) Oven	283	6480	720	360					
	TOTAL	624	8664	720	408.5	1800			2	.88

EQUIPMENT DEFINITION
SPECIFIC ASSUMPTIONS

PROCESS STEP	ITEM	COST (K$)	AREA (FT^2)	CAPACITY (WPH)	POWER (KW)	EXHAUST (CFM)	DIH_2O (GPM)	N_2 (1/M)	STAFF (OPI)	MACHINE UTILITY
36. Glass with Substrate	Same as 35 + (2) Riviter	624	8664	720	408.5	1800			2	.88
		6	48		1.0					
	TOTAL	630	8712	720	409.5	1800			2	.88
37. Electrical Test (Cells)	Solar Simulator Electronic Load Data Acquisition Cell Stage	30	45	1200	2				1	.88
38. Electrical Test (Modules)	Solar Simulator Electronic Load Data Acquisition Panel Stage	95	250	720	4.5				1	.88

3.5.2 PROCESS STEP COSTS

Results of the costing study of each process step are presented in the next tables.

COST SUMMARY
TODAY'S TECHNOLOGY
($/WATT)

PROCESS STEP	MATERIALS	EXPENSE ITEMS	LABOR	OVERHEAD	INTEREST	DEPRECIATION	TOTAL	PROCESS YIELD %	CAPITAL EQUIPMENT	FACILITIES
1. Brushing	0.0	.0073	.0134	.0066	.0023	.0031	.0327	99.5	.0205	.0053
2. Plasma (Dielectric Etch)	0.0	.0031	.0084	.0050	.0064	.0096	.0425	99.8	.0663	.0053
3. Standard Solutions	0.0	.0041	.0061	.0042	.0006	.0005	.0155	99.8	.0031	.0032
4. Centrifuge Drying	0.0	.0014	.0042	.0035	.0003	.0002	.0096	99.8	.0013	.0015
5. Silicon Etching (one side)	0.0	.0124	.0243	.0102	.0012	.0012	.0493	99.5	.0076	.0063
6. Silicon Etching (two sides)	0.0	.0161	.0243	.0102	.0012	.0012	.0530	99.5	.0076	.0063
7. Texture Etch	0.0	.0097	.0243	.0102	.0012	.0011	.0465	99.6	.0068	.0063
8. Edge Grinding	0.0	.0209	.0269	.0113	.0046	.0061	.0698	?	.0407	.0106
9. Photo-Resist (Apply-Expose-Dev.)	0.0	.0107	.0403	.0159	.0073	.0097	.0839	99.4	.0648	.0160
10. Photo-Resist (Remove)	0.0	.0213	.0061	.0042	.0006	.0006	.0328	99.7	.0034	.0032
11. Plasma (P.R. Remove)	0.0	.0009	.0084	.0049	.0004	.0003	.0149	99.9	.0016	.0026
12. Dielectric Etch (Wet)	0.0	.0044	.0081	.0047	.0004	.0004	.0180	99.6	.0023	.0021
13. Etch Stop (Apply)	0.0	.0091	.0067	.0044	.0023	.0031	.0256	99.8	.0211	.0047
14. Spin-On	0.0	.0154	.0067	.0044	.0023	.0031	.0319	--	.0211	.0047

COST SUMMARY
TODAY'S TECHNOLOGY
($/WATT)

PROCESS STEP	MATERIALS	EXPENSE ITEMS	LABOR	OVERHEAD	INTEREST	DEPRECIATION	TOTAL	PROCESS YIELD %	CAPITAL EQUIPMENT	FACILITIES
15. Spray-On	0.0	.0152	.0034	.0032	.0011	.0014	.0243	--	.0095	.0023
16. Drive-In (Diffusion)	0.0	.0099	.0102	.0057	.0026	.0032	.0316	99.5	.0212	.0081
17. Silicon Source (Solid)	0.0	.0173	.0407	.0161	.0053	.0065	.0859	98.0	.0423	.0162
18. Gas Depositon and Diffusion	0.0	.0174	.0102	.0057	.0026	.0032	.0391	99.0	.0212	.0081
19. Doped Oxide (CVD)	0.0	.0174	.0102	.0057	.0026	.0032	.0391	99.0	.0212	.0081
20. Ion Implant	0.0	.0097	.0746	.0357	.1406	.2029	.4635	98.0	1.390	.1723
21. Ion Implant (Advanced)	0.0	.0014	.0022	.0030	.0067	.0101	.0234	99.5	.0695	.0052
22. Vacuum Metallization Cu, Al	.0024	.0490	.0318	.0146	.0236	.0326	.1540	99.0	.2211	.0413
23. Thick Film Ag Front	.0457	.0040	.0060	.0040	.0011	.0016	.0624	99.8	.0107	.0018
24. Thick Film Ag Back	.1988	.0040	.0060	.0040	.0011	.0016	.2155	99.8	.0107	.0018
25. Electroless Plating	.0305	.0256	.0145	.0089	.0011	.0012	.0818	99.6	.0073	.0049
26. Electrolytic Plating	.0305	.0256	.0145	.0089	.0011	.0012	.0818	99.6	.0073	.0049
27. Solder Coating	.0223	.0002	.0014	.0025	.0002	.0003	.0269	99.8	.0021	.0005
28. Silicon Nitride (CVD)	0.0	.0098	.0102	.0057	.0026	.0032	.0315	99.8	.0212	.0081
29. Oxide Growth	0.0	.0049	.0051	.0039	.0013	.0016	.0168	99.8	.0106	.0040

COST SUMMARY
TODAY'S TECHNOLOGY
($/WATT)

PROCESS STEP	MATERIALS	EXPENSE ITEMS	LABOR	OVERHEAD	INTEREST	DEPRECIATION	TOTAL	PROCESS YIELD %	CAPITAL EQUIPMENT	FACILITIES
30. Spin-On	0.0	.0079	.0067	.0044	0023	.0031	.0244	97.0	.0211	.0047
31. Evaporate	.0019	.0022	.0318	.0146	.0236	.0326	.1067	99.0	.2211	.0413
32. Add Solder	.0014	.0001	.0007	.0022	.0001	.0001	.0046	99.8	.0008	.0002
33. Reflow Solder	0.0	.0001	.0170	.0032	.0008	.0011	.0222	99.8	.0074	.0015
34. Conductive Adhesives	.0045	.0002	.0060	.0040	.0011	.0016	.0174	99.5	.0107	.0018
35. Glass Superstrate	.1817	.0004	.0006	.0027	.0012	.0010	.1876	99.4	.0057	.0074
36. Glass with Substrate	.3448	.0004	.0006	.0027	.0013	.0011	.3509	99.0	.0063	.0081
37. Electrical Test (cells)	0.0	.0001	.0085	.0048	.0008	.0012	.0154	99.8	.0079	.0011
38. Electrical Test (modules)	0.0	.0000	.0003	.0021	.0001	.0001	.0026	99.8	.0010	.0002

3.6 PROCESS SEQUENCE CHOICE

Once the costs for each process step and a projected processing yield for that step have been formulated, the cost and yield of specific process sequences can be determined. Based upon both technical and cost data, future process sequences will contain the following steps:

1. Brushing (or pressure scrubbing)
2. Centrifuge drying
3. Texture etching (orientation permitting)
4. Ion implantation
5. Antireflection coating
6. Either printed or plated metallization
7. Solder reflow interconnection
8. Glass covered encapsulation (with metallization reliability determining backing requirement)

The choice between printed metallization or plated metallization has dramatic influence on the process choices for the processing sequence. The printed metallization demands that the antireflection coating be placed on the cell after metallization to avoid a costly realignment. Conversely, the plated metal requires a patterned mask, preferably the antireflection coating, for alignment. This patterned plating mask will most likely require a photoresist sequence. Based upon consumed materials and technology arguments, such a photoresist sequence could well utilize plasma process steps for both etching and photoresist removal. Thus, the single choice between plated and printed metallization demands different process step development as well as process sequence development.

Specific examples of process sequences and cost data are presented in the following tables.

DATA AS READ FROM FILE PLATED METAL TEXTURED BOTH SIDES EXCLUDING PACKAGING

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.7	1.3	.7	.2	.3	3.3	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.5	99.8
3	14	TEXTURIZE NA-OH	.0	1.0	2.4	1.0	.1	.1	4.6	99.6
4	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
5	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.1	99.8
6	15	PR APPLY	.0	1.1	4.0	1.6	.7	1.0	8.4	99.5
7	72	DIELEC ETCH(WET)	.0	.4	.8	.5	.0	.0	1.8	99.6
8	16	PR REMOVE	.0	2.1	.6	.4	.1	.1	3.3	99.7
9	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.3	99.5
10	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.3	99.5
11	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
12	40	ELECTROLESS PLTN	3.0	2.6	1.4	.9	.1	.1	8.2	99.6
13	43	SOLDER COATING	2.2	.0	.1	.2	.0	.0	2.7	99.8
14	60	ELEC. TEST CELLS	.0	.0	.8	.5	.1	.1	1.5	99.8

DATA AFTER FACTORING BY YIELDS

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.8	1.4	.7	.2	.3	3.4	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.6	99.8
3	14	TEXTURIZE NA-OH	.0	1.0	2.5	1.1	.1	.1	4.9	99.6
4	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
5	45	SILICON NITRIDE	.0	1.0	1.1	.6	.3	.3	3.3	99.8
6	15	PR APPLY	.0	1.1	4.2	1.6	.8	1.0	8.7	99.5
7	72	DIELEC ETCH(WET)	.0	.5	.8	.5	.0	.0	1.9	99.6
8	16	PR REMOVE	.0	2.2	.6	.4	.1	.1	3.4	99.7
9	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.4	99.5
10	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.4	99.5
11	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
12	40	ELECTROLESS PLTN	3.1	2.6	1.5	.9	.1	.1	8.2	99.6
13	43	SOLDER COATING	2.2	.0	.1	.3	.0	.0	2.7	99.8
14	60	ELEC. TEST CELLS	.0	.0	.9	.5	.1	.1	1.5	99.8
		TOTALS	5.3	11.0	15.7	8.5	3.4	4.6	48.6	95.1
		%	10.9	22.7	32.2	17.6	7.1	9.5	100.0	

DATA AS READ FROM FILE PRINTED METAL TEXTURED BOTH SIDES EXCLUDING PACKAGING

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.7	1.3	.7	.2	.3	3.3	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.5	99.8
3	14	TEXTURIZE NA-OH	.0	1.0	2.4	1.0	.1	.1	4.6	99.6
4	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
5	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.3	99.5
6	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.3	99.5
7	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
8	36	THICK FILM AG FR	4.6	.4	.6	.4	.1	.2	6.2	99.3
9	37	THICK FILM AG BA	19.9	.4	.6	.4	.1	.2	21.5	99.8
10	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.1	99.8
11	43	SOLDER COATING	2.2	.0	.1	.2	.0	.0	2.7	99.8
12	60	ELEC. TEST CELLS	.0	.0	.8	.5	.1	.1	1.5	99.8

DATA AFTER FACTORING BY YIELDS

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.8	1.4	.7	.2	.3	3.4	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.6	99.8
3	14	TEXTURIZE NA-OH	.0	1.0	2.5	1.1	.1	.1	4.8	99.6
4	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
5	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.4	99.5
6	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.4	99.5
7	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
8	36	THICK FILM AG FR	4.6	.4	.6	.4	.1	.2	6.3	99.3
9	37	THICK FILM AG BA	20.0	.4	.6	.4	.1	.2	21.7	99.8
10	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.2	99.8
11	43	SOLDER COATING	2.2	.0	.1	.3	.0	.0	2.7	99.8
12	60	ELEC. TEST CELLS	.0	.0	.9	.5	.1	.1	1.5	99.8
		TOTALS	26.9	5.4	9.7	5.8	2.7	3.7	54.2	96.3
		%	49.6	10.0	17.0	10.8	4.9	6.8	100.0	

DATA AS READ FROM FILE INTERCONNECT & PACKAGING

PRO #	DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1 50	ADD SOLDER	.1	.0	.1	.2	.0	.0	.5	99.8
2 51	REFLOW SOLDER	.0	.0	1.7	.3	.1	.1	2.2	99.8
3 57	GLASS WITH SUBST	34.5	.0	.1	.3	.1	.1	35.1	99.0
4 61	ELEC TEST MODULE	.0	.0	.0	.2	.0	.0	.3	99.8

DATA AFTER FACTORING BY YIELDS

PRO #	DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1 50	ADD SOLDER	.1	.0	.1	.2	.0	.0	.5	99.8
2 51	REFLOW SOLDER	.0	.0	1.7	.3	.1	.1	2.3	99.8
3 57	GLASS WITH SUBST	34.9	.0	.1	.3	.1	.1	35.5	99.0
4 61	ELEC TEST MODULE	.0	.0	.0	.2	.0	.0	.3	99.8
	TOTALS	35.0	.1	1.9	1.0	.2	.2	38.5	96.4
	%	91.0	.2	4.9	2.7	.6	.6	100.0	

DATA AS READ FROM FILE PRINTED METAL TEXTURED ONE SIDE INCLUDING PACKAGING

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.7	1.3	.7	.2	.3	3.3	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.5	99.8
3	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
4	23	GAS DEP. & DIFF.	.0	1.7	1.0	.6	.3	.3	3.9	99.0
5	73	ETCH STOP APPLY	.0	.9	.7	.4	.2	.3	2.6	99.8
6	72	DIELEC ETCH(WET)	.0	.4	.8	.5	.0	.0	1.8	99.6
7	14	TEXTURIZE NA-OH	.0	1.0	2.4	1.0	.1	.1	4.6	99.6
8	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
9	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.3	99.5
10	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
11	36	THICK FILM AG FR	4.6	.4	.6	.4	.1	.2	6.2	99.8
12	37	THICK FILM AG BA	19.9	.4	.6	.4	.1	.2	21.5	99.8
13	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.1	99.8
14	43	SOLDER COATING	2.2	.0	.1	.2	.0	.0	2.7	99.8
15	60	ELEC. TEST CELLS	.0	.0	.8	.5	.1	.1	1.5	99.3
16	50	ADD SOLDER	.1	.0	.1	.2	.0	.0	.5	99.8
17	51	REFLOW SOLDER	.0	.0	1.7	.3	.1	.1	2.2	99.3
18	57	GLASS WITH SUBST	34.5	.0	.1	.3	.1	.1	35.1	99.0
19	61	ELEC TEST MODULE	.0	.0	.0	.2	.0	.0	.3	99.8

DATA AFTER FACTORING BY YIELDS

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.8	1.4	.7	.2	.3	3.5	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.6	99.8
3	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
4	23	GAS DEP. & DIFF.	.0	1.8	1.1	.8	.3	.3	4.1	99.0
5	73	ETCH STOP APPLY	.0	1.0	.7	.5	.2	.3	2.7	99.8
6	72	DIELEC ETCH(WET)	.0	.5	.8	.5	.0	.0	1.9	99.6
7	14	TEXTURIZE NA-OH	.0	1.0	2.5	1.1	.1	.1	4.8	99.6
8	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
9	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.4	99.5
10	20	DRIVE-IN DIFFUSN	.0	1.0	1.1	.6	.3	.3	3.3	99.5
11	36	THICK FILM AG FR	4.7	.4	.6	.4	.1	.2	6.4	99.8
12	37	THICK FILM AG BA	20.4	.4	.6	.4	.1	.2	22.1	99.8
13	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.2	99.8
14	43	SOLDER COATING	2.3	.0	.1	.3	.0	.0	2.7	99.8
15	60	ELEC. TEST CELLS	.0	.0	.9	.5	.1	.1	1.6	99.8
16	50	ADD SOLDER	.1	.0	.1	.2	.0	.0	.5	99.8
17	51	REFLOW SOLDER	.0	.0	1.7	.3	.1	.1	2.3	99.3
18	57	GLASS WITH SUBST	34.9	.0	.1	.3	.1	.1	35.5	99.0
19	61	ELEC TEST MODULE	.0	.0	.0	.2	.0	.0	.3	99.8
		TOTALS	62.4	8.9	14.6	8.6	2.8	3.7	100.9	98.5
		%	61.8	8.8	14.4	8.5	2.8	3.6	100.0	

DATA AS READ FROM FILE PLATED METAL TEXTURED BOTH SIDES WITH PLASMA INCLUDING PACKAGING

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	71	PLASMA PR REMOVE	.0	.1	.8	.5	.0	.0	1.5	99.9
2	1	BRUSHING	.0	.7	1.3	.7	.2	.3	3.3	99.5
3	14	TEXTURIZE NA-OH	.0	1.0	2.4	1.0	.1	.1	4.6	99.6
4	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
5	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.1	99.8
6	15	PR APPLY	.0	1.1	4.0	1.6	.7	1.0	8.4	99.5
7	2	PLASMA	.0	1.3	.8	.5	.6	1.0	4.2	99.8
8	71	PLASMA PR REMOVE	.0	.1	.8	.5	.0	.0	1.5	99.9
9	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.6	99.5
10	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.3	99.5
11	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
12	40	ELECTROLESS PLTN	3.0	2.6	1.4	.9	.1	.1	8.2	99.6
13	43	SOLDER COATING	2.2	.0	.1	.2	.0	.0	2.7	99.8
14	60	ELEC. TEST CELLS	.0	.0	.8	.5	.1	.1	1.5	99.8
15	50	ADD SOLDER	.1	.0	.1	.2	.0	.0	.5	99.8
16	51	REFLOW SOLDER	.0	.0	1.7	.3	.1	.1	2.2	99.8
17	57	GLASS WITH SUBST	34.5	.0	.1	.3	.1	.1	35.1	99.0
18	61	ELEC TEST MODULE	.0	.0	.0	.2	.0	.0	.3	99.8

DATA AFTER FACTORING BY YIELDS

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	71	PLASMA PR REMOVE	.0	.1	.9	.5	.0	.0	1.6	99.9
2	1	BRUSHING	.0	.8	1.4	.7	.2	.3	3.5	99.5
3	14	TEXTURIZE NA-OH	.0	1.0	2.6	1.1	.1	.1	4.9	99.6
4	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
5	45	SILICON NITRIDE	.0	1.0	1.1	.6	.3	.3	3.3	99.8
6	15	PR APPLY	.0	1.1	4.2	1.7	.8	1.0	8.8	99.5
7	2	PLASMA	.0	1.4	.9	.5	.7	1.0	4.4	99.8
8	71	PLASMA PR REMOVE	.0	.1	.9	.5	.0	.0	1.6	99.9
9	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.1	2.4	99.5
10	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.4	99.5
11	20	DRIVE-IN DIFFUSN	.0	1.0	1.1	.6	.3	.3	3.3	99.5
12	40	ELECTROLESS PLTN	3.1	2.6	1.5	.9	.1	.1	8.4	99.6
13	43	SOLDER COATING	2.3	.0	.1	.3	.0	.0	2.7	99.8
14	60	ELEC. TEST CELLS	.0	.0	.9	.5	.1	.1	1.6	99.8
15	50	ADD SOLDER	.1	.0	.1	.2	.0	.0	.5	99.8
16	51	REFLOW SOLDER	.0	.0	1.7	.3	.1	.1	2.3	99.8
17	57	GLASS WITH SUBST	34.9	.0	.1	.3	.1	.1	35.5	99.0
18	61	ELEC TEST MODULE	.0	.0	.0	.2	.0	.0	.3	99.8
		TOTALS	40.4	9.7	18.3	9.9	4.3	5.8	88.4	94.1
		%	45.8	11.0	20.7	11.2	4.9	6.6	100.0	

DATA AS READ FROM FILE PRINTED METAL TEXTURED ONE SIDE EXCLUDING PACKAGING

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.7	1.3	.7	.2	.3	3.3	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.5	99.8
3	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
4	23	GAS DEP. & DIFF.	.0	1.7	1.0	.6	.3	.3	3.9	99.0
5	73	ETCH STOP APPLY	.0	.9	.7	.4	.2	.3	2.6	99.8
6	72	DIELEC ETCH(WET)	.0	.4	.8	.5	.0	.0	1.8	99.6
7	14	TEXTURIZE NA-OH	.0	1.0	2.4	1.0	.1	.1	4.6	99.6
8	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
9	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.3	99.5
10	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
11	36	THICK FILM AG FR	4.6	.4	.6	.4	.1	.2	6.2	99.8
12	37	THICK FILM AG BA	19.9	.4	.6	.4	.1	.2	21.5	99.8
13	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.1	99.8
14	43	SOLDER COATING	2.2	.0	.1	.2	.0	.0	2.7	99.8
15	60	ELEC. TEST CELLS	.0	.0	.8	.5	.1	.1	1.5	99.8

DATA AFTER FACTORING BY YIELDS

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.8	1.4	.7	.2	.3	3.4	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.6	99.8
3	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
4	23	GAS DEP. & DIFF.	.0	1.8	1.1	.6	.3	.3	4.1	99.0
5	73	ETCH STOP APPLY	.0	.9	.7	.5	.2	.3	2.6	99.8
6	72	DIELEC ETCH(WET)	.0	.5	.8	.5	.0	.0	1.9	99.6
7	14	TEXTURIZE NA-OH	.0	1.0	2.5	1.0	.1	.1	4.8	99.6
8	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
9	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.4	99.5
10	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
11	36	THICK FILM AG FR	4.6	.4	.6	.4	.1	.2	6.3	99.8
12	37	THICK FILM AG BA	20.0	.4	.6	.4	.1	.2	21.7	99.8
13	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.2	99.8
14	43	SOLDER COATING	2.2	.0	.1	.3	.0	.0	2.7	99.8
15	60	ELEC. TEST CELLS	.0	.0	.9	.5	.1	.1	1.5	99.8
		TOTALS	26.9	8.7	12.5	7.4	2.6	3.4	61.4	95.0
		%	43.8	14.1	20.3	12.1	4.2	5.5	100.0	

DATA AS READ FROM FILE PLATED METAL TEXTURED ONE SIDE, EXCLUDING PACKAGE

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.7	1.3	.7	.2	.3	3.3	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.5	99.8
3	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
4	23	GAS DEP. & DIFF.	.0	1.7	1.0	.6	.3	.3	3.9	99.0
5	73	ETCH STOP APPLY	.0	.9	.7	.4	.2	.3	2.6	99.8
6	72	DIELEC ETCH(WET)	.0	.4	.8	.5	.0	.0	1.8	99.6
7	14	TEXTURIZE NA-OH	.0	1.0	2.4	1.0	.1	.1	4.6	99.6
8	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
9	45	SILICON NITRIDE	.0	1.0	1.0	.6	.3	.3	3.1	99.8
10	15	PR APPLY	.0	1.1	4.0	1.6	.7	1.0	8.4	99.5
11	72	DIELEC ETCH(WET)	.0	.4	.8	.5	.0	.0	1.8	99.6
12	16	PR REMOVE	.0	2.1	.6	.4	.1	.1	3.3	99.7
13	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.3	99.5
14	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.5	99.8
15	8	CENTRIFUGE	.0	.1	.4	.3	.0	.0	1.0	99.8
16	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
17	40	ELECTROLESS PLTN	3.0	2.6	1.4	.9	.1	.1	8.2	99.6
18	43	SOLDER COATING	2.2	.0	.1	.2	.0	.0	2.7	99.8
19	60	ELEC. TEST CELLS	.0	.0	.8	.5	.1	.1	1.5	99.8

DATA AFTER FACTORING BY YIELDS

PRO #		DESCRIPTION	MAT	EXP	LAB	OVR	INT	DEP	TOT	YIELD
1	1	BRUSHING	.0	.8	1.4	.7	.2	.3	3.5	99.5
2	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.6	99.8
3	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
4	23	GAS DEP. & DIFF.	.0	1.8	1.1	.6	.3	.3	4.1	99.0
5	73	ETCH STOP APPLY	.0	1.0	.7	.5	.2	.3	2.7	99.8
6	72	DIELEC ETCH(WET)	.0	.5	.8	.5	.0	.0	1.9	99.6
7	14	TEXTURIZE NA-OH	.0	1.0	2.5	1.1	.1	.1	4.8	99.6
8	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
9	45	SILICON NITRIDE	.0	1.0	1.1	.6	.3	.3	3.3	99.8
10	15	PR APPLY	.0	1.1	4.2	1.6	.8	1.0	8.7	99.5
11	72	DIELEC ETCH(WET)	.0	.5	.8	.5	.0	.0	1.9	99.6
12	16	PR REMOVE	.0	2.2	.6	.4	.1	.1	3.4	99.7
13	28	ION IMP ADVANCED	.0	.1	.2	.3	.7	1.0	2.4	99.5
14	6	STANDARD SOLNS.	.0	.4	.6	.4	.1	.1	1.6	99.8
15	8	CENTRIFUGE	.0	.1	.4	.4	.0	.0	1.0	99.8
16	20	DRIVE-IN DIFFUSN	.0	1.0	1.0	.6	.3	.3	3.2	99.5
17	40	ELECTROLESS PLTN	3.1	2.6	1.5	.9	.1	.1	8.2	99.6
18	43	SOLDER COATING	2.2	.0	.1	.3	.0	.0	2.7	99.8
19	60	ELEC. TEST CELLS	.0	.0	.9	.5	.1	.1	1.5	99.8
		TOTALS	5.3	14.9	19.6	11.0	3.4	4.4	58.5	99.5
		%	9.1	25.4	33.4	18.7	5.9	7.5	100.0	

3.7 COST LIMITS, PROJECTIONS, AND PROCESS AREAS REQUIRING ADVANCED DEVELOPMENT

Direct processing costs can be conveniently separated into the three distinct categories of labor, material, and capital. If, as is the goal of Task IV, an automated factory with a high volume throughput is realized in the 1980's, some definitive statements can be made concerning each of these direct cost categories. First, if a truly automated factory is achieved, direct labor costs will be minimized and will not form a major cost contribution. Second, if the automated equipment can achieve a high volume throughput, the capital cost per unit will be low. Finally, material costs will be optimized by achieving maximum material utilization, but costs cannot be below some minimum value needed to physically form the solar cells. In the limit of these arguments, if labor costs approach zero and capital equipment throughput approaches infinity, the limiting cost factor is the cost of consumed materials in manufacturing solar cells.

The effect of this arugment is apparent when the cost data presented in this report are scrutinized. Labor is a major factor in the costs based on today's technology, with capital costs also being high. For processes up to encapsulation, projections look reasonable for ERDA goals for 1985. (Encapsulation costs, however, appear less promising and will require considerable innovation to reach the goals.) It can be stated at this time, however, that certain technology areas require advanced development in order to ensure processing cost goals. These areas are:

1. Ion implantation with increased beam current.
2. Plasma etching and cleaning processes to eliminate wet chemistry steps.

3. Printed metallization technology to reduce costs and increase reliability.
4. Plated metallization to increase control and reduce costs.
5. Spray-on technologies to ensure effective coatings for any solar cell substrate, geometry, and surface condition.

Development of both printed and plated metallization techniques is recommended at this time, to ensure that at least one metallization system with superior reliability can be found and advanced to the state of economical processing. Such a system is necessary to assure long term terrestrial reliability utilizing projected encapsulation materials and technologies.

3.7.1 DEVELOPMENT OF AUTOMATION AND SCALE-UP CONCEPTS

Cost studies included in this report have assumed that a machine in the process line will be utilized less than 100% of the time due to operator breaks and lunch hours as well as machine maintenance and repair time. Each piece of equipment in the processing factory will be inoperative for random and varying periods of time due to repairs and maintenance. It is an obvious objective to ensure, that if one piece of equipment is inoperative, the overall rate of production through the processing line should not be halted as a result. The factory design, thus, should allow for equipment downtime.

Equipment failure or routine downtime can be eliminated if, for each process step, many machines operate in parallel with a queuing area before it. As each machine becomes available for processing, materials from the queuing areas are fed to it. Any machine that is inoperative is merely by-passed until it is again available for processing. This is a necessary concept for proper utilization of all equipment and minimization of capital equipment and facility investment.

4.0 CONCLUSIONS

This program has emphasized the evaluation of individual processing steps and complete process sequences for technical feasibility and cost effectiveness. The overall conclusion from this study is that no fundamentally new development in processing technology is required to meet the long range LSSA Program goal of large scale solar panel production at a selling price of $0.50/peak watt. In order to achieve that goal, however, it will be essential to further develop (and subsequently automate) existing technologies. Some highly promising processing areas, including ion implantation, plasma etching and cleaning, plated contacts, and printed metallization, should be the subjects of specific advanced development work to permit full evaluation of their potential technical and economic contributions. An understanding of cost effective control limits on process steps is also necessary.

5.0 RECOMMENDATIONS

No specific recommendations, other than technological areas identified and recommended in Sections 3 and 4 for further development, are made in this report period.

6.0 CURRENT PROBLEMS

No specific problems have occurred to the date of this report.

7.0 WORK PLAN STATUS

The work plan is on schedule.

8.0 LIST OF ACTION ITEMS

No items requiring unusual action have come to light during this report period.

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