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CM-458/U Signal Comparator

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CM-458/U SIGNAL COMPARATOR

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ABSTRACT

This report describes the development history, the physical and functional characteristics, and the production activity of the CM-458/U Signal Comparator. The CM-458/U Signal Comparator is a test device used to verify proper delivery by the aircraft control equipment of the unique signal used in the prearming of modern nuclear weapons. CM-458/U monitors voltage levels, pulse widths and signal sequence to verify correctness.

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CM-458/U SIGNAL COMPARATOR

INTRODUCTION

The advent of the intent strong link safety concept in weapons resulted in the development of a unique signal pattern transmitted from cockpit to weapon. Because the signal generator required verification, the Air Force requested Sandia National Laboratories to develop and provide a receiving device that would respond to a proper unique signal but would reject an improper signal. The receiving device, or tester, is designated the CM-458/U Signal Comparator. The unique signal checked is a fixed pattern many seconds long comprised of pulses that activate a mechanical switch device in the weapon. The pattern, shown in Figure 1, is always the same, is unclassified, and the system is provided only for safety reasons. The mechanical switch is designated the MC2969. During use, the CM-458/U is connected to the weapon cable at the aircraft pylon and thus checks out the aircraft cabling system as well as the source of the unique signal. The source of the signal presently is the DCU-201 or DCU-218 Aircraft Controller.

HISTORY OF DEVELOPMENT AND PRODUCTION

The requirement for design was established in January 1975. In June 1975, Sandia National Laboratories proposed a design for the T1550 Unique Signal Analyzer. The design was approved and development was begun. The T1550 design was similar to the T1549 Decoder-Programmer, used to check the Category B and Category D PAL patterns. However, complementary metal oxide semiconductor (CMOS) technology was employed rather than the higher powered transistor-transistor logic (TTL). Two prototype units were fabricated in the laboratory. In conjunction with the prototype development the PT3078 was adapted and programmed to provide production test capability. Sparton Southwest, Inc. of Albuquerque, was asked to quote on tooling and fabrication of ten development units. This quote was made in October 1975 and the order was approved and placed in November. Sandia furnished a shopmade board tester for in-process testing. In February 1976 some changes to pulse lengths in the basic unique signal were necessary, due to an incompatibility of the original pulse lengths and the

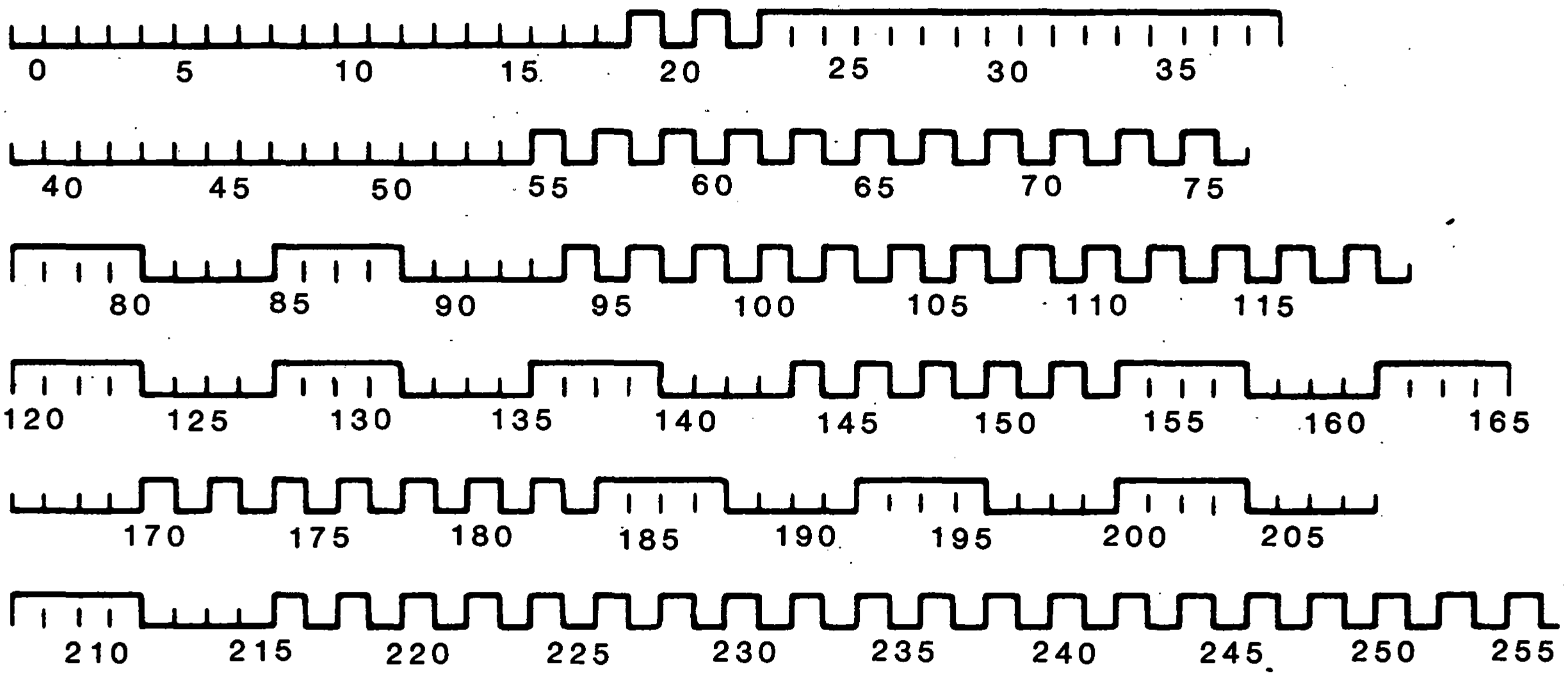

FIGURE 1 - USG PULSE SEQUENCE (PATTERN)

mechanical capabilities of the MC2969 switch device. The T1550 logic was altered to accommodate the revised pulse train. Crystal oscillators for the T1550 development were evaluated from Vectron and Q-Tech from sample quantities. The Vectron unit did not survive vibration testing so the Q-Tech unit was used for all production. The ten development units were produced by Sparton and were used to prove-in the tooling, testing, and case sealing techniques. A separate contract with Sparton Southwest was negotiated for a production tester for use in the in-process testing of logic boards and the complete assembly test. This test, controlled by means of the INTEL 8080 Central Processor Unit, was designed and fabricated by Sparton.

In conjunction with an Air Force agreement to fund production under a reimbursable program, the Air Force asked and Sandia agreed to redesignate the T1550 device as the CM-458/U Signal Comparator. The drawings were made in the Air Force format per MIL-STD-100 and MIL-D-1000, and all development effort, drafting, and ten development units were done with ERDA funding. Continual liaison with the Special Weapons Group of the San Antonio Air Logistics Command was maintained to discuss drawing definition, spare parts policy, and maintenance problems.

Sparton Southwest was awarded a cost plus contract in November 1975 for the production quantities of the CM-458/U. In September 1976, the first units were assembled. Several people from Kelly Air Force Base representing ALC/MME and ALC/SWP came to participate in the First Article Configuration Inspection. The design, workmanship, and test program were approved. The various environmental tests defined in Table 1 were done on two sample units with no failures, so production was begun, with first shipment occurring in January 1977. The production was smooth with only minor problems involving test equipment. The final shipment was in September 1977. The production cost per unit was approximately $4500 for a total of 56 units to the Air Force.

PHYSICAL DESCRIPTION

The CM-458/U is 8 x 8 x 10 inches and weighs 10.5 pounds. Photographs of the unit are shown in Figures 2a and 2b. The front panel is a heavy machined aluminum piece that serves as a heat sink for the power electronics and as a base for the internal structure. The logic section is composed of two wirewrap boards of CMOS dual in-line packages. The two boards are cantilevered to the front panel on spacers. All high heat-generating components are mounted on the front panel. The rear cover is a deep drawn aluminum can with a stiffner strap around the edge. After assembly of the front panel and rear cover, the seam is sealed with PR1201-Polysulfide adhesive and a pressure test is performed to assure a good seal. This assembly also provides a good electromagnetic shield. Eight corner-mounted rubber shock absorbers provide vibration and shock protection. The finish is gray enamel. Electrical access through the case is by means of a Bendix-made connector, MS20029-P17A-99S; inside the case the active lines are filtered with low-pass RF filters. Table 2 identifies the connector pin assignments and identifies the filtered lines.

TABLE 1

ENVIRONMENTAL TESTS

a. Low temperature, -59°C

b. High temperature, +76°C

c. Humidity - ten days

d. Salt fog - two days

e. Rain - 4 hours at 4 inches per hour

f. Altitude - sea level to 60,000 ft.

g. Temperature shock, -59°C to 76°C

h. Static charge - 20,000 volts

i. Electromagnetic radiation - 4000 volts/meter

j. Vibration - 3g, 10 to 500cps

k. Mechanical shock - multiple 24 inch drops on concrete.

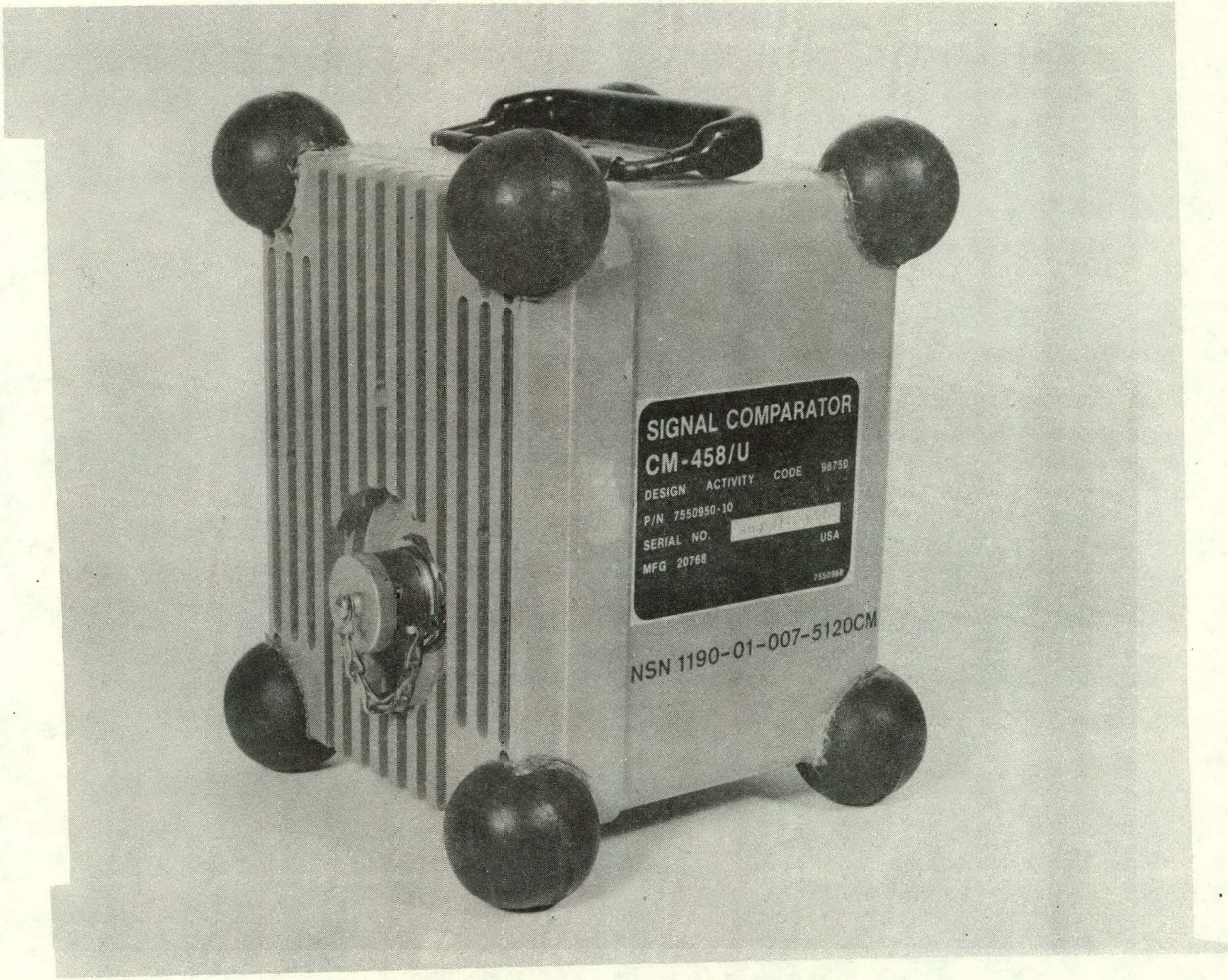

FIGURE 2A - CM-458/U

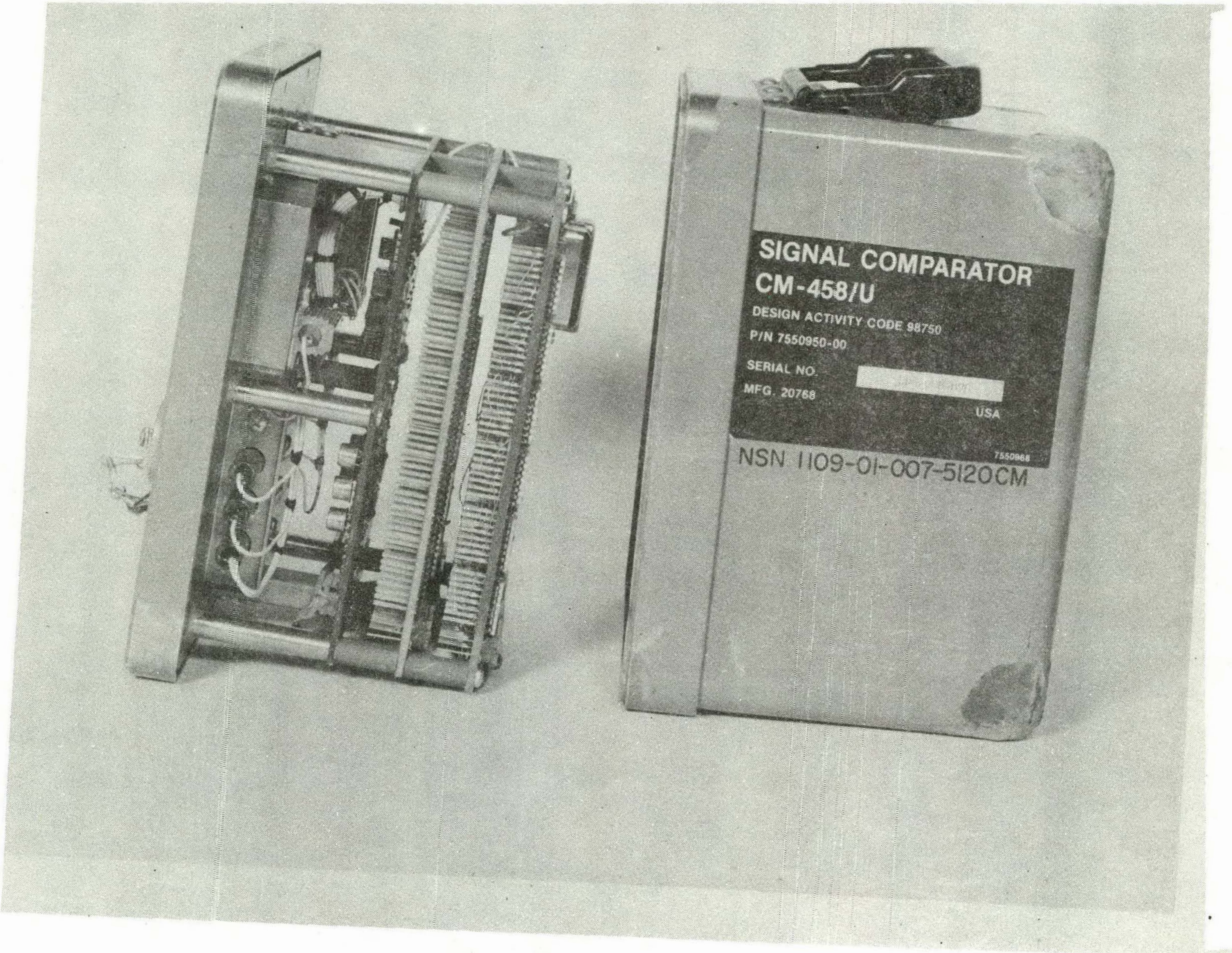

FIGURE 2B - CM-458/U

TABLE 2

CONNECTOR PIN ASSIGNMENTS

PIN	FILTERED	INPUT/OUTPUT	DESIGNATION
C	F	Output	Monitor Normal, System A
D	F	Output	Monitor Common, System A
E	F	Input	PRESET-ARM (PREARM), System A
F	F	Input	dc Power (25-30Vdc), System A
H	F	Input	dc Power for Arm Operation, System 1
S	F	Input	Dual Purpose; 1. dc Power for SAFE Operation; 2. SAFE Signal Input, System 1
P		Output	Press-to-Test Common, System A
R	F	Input	RESET-SAFE Signal, System A
T	F	Output	SAFE MONITOR Signal, System 1
U			Power and Signal Common, System 1 and System A
V	F	Output	ARM MONITOR Signal, System 1
Y	F	Input	PRESET-ARM (PREARM), System 1

FUNCTIONAL CHARACTERISTICS

The CM-458/U contains sophisticated electronic circuits which measure voltage levels on appropriate lines, measure pulse widths of incoming signals, and determine if the correct sequence of signals are generated on lines at the weapon interface. The CM-458/U simulates the nuclear weapon unique signal device by generating an appropriate output monitor response to the unique signal generating (USG) device in response to an input from the unique signal generating device. The primary elements of the CM-458/U are depicted in the block diagram, Figure 3. The four input lines; System A, ARM Power 1, Reset/Safe, and Safe Power in the upper left corner of the diagram are all diode coupled to the logic power regulator, a series voltage regulating circuit providing +10 volts to the internal circuitry.

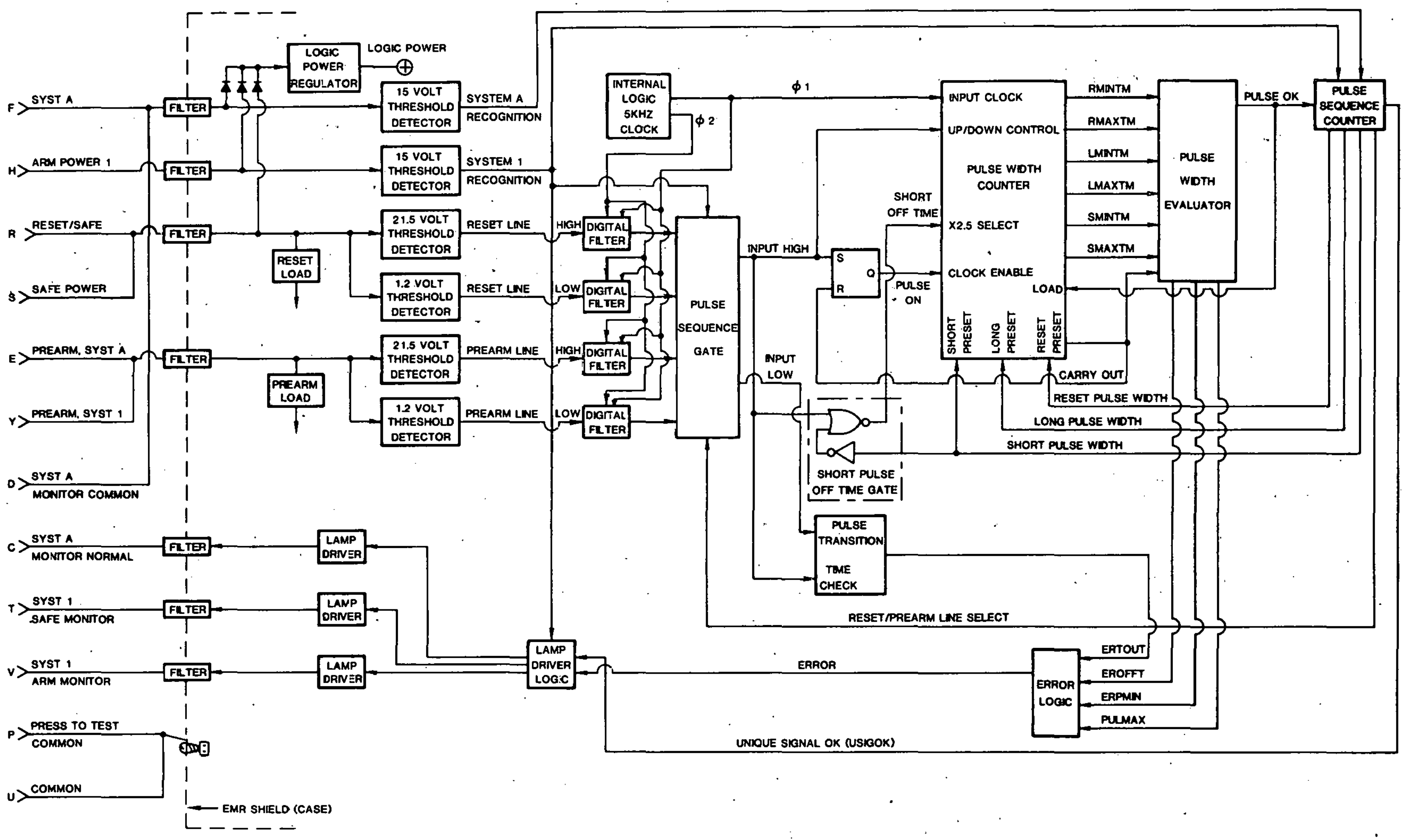

FIGURE 3 - CM-458/U BLOCK DIAGRAM

Thus, power is obtained for the logic of the CM-458/U on one or more of these four lines. A minimum of 15 volts continuous power input to the regulator is required to ensure correct operation of the unit. If power to the unit is interrupted, a 15 volt operational amplifier threshold detector will sense the low voltage condition and generate a reset to the logic. The reset will preclude a correct operating sequence of the unit and a system monitor indication of a faulty operation will occur. Resistive loads of 30Ω are present on the RESET/SAFE and Prearm lines to simulate unique signal device solenoid loads.

All input lines to the CM-458/U are sensed for proper operating voltage levels by an array of operational amplifier voltage threshold detectors. Two 15 volt threshold detectors sense minimum supply voltage for either System 1 or System A arming of the unique signal device. A 21.5 volt threshold detector and a 1.2 volt threshold detector on both the Prearm lines and the RESET/SAFE lines of the unit ensure both a minimum "on" voltage of 21.5 volts and a maximum "off" voltage condition of less than 1.2 volts. This is done to ensure pulses are delivered to the unique signal switch which will not only actuate USG device solenoids, but will also release them after the activating pulse is over. Each of the four lines coming from these four threshold detectors; Reset high, Reset low, Prearm high, and Prearm low, are input to separate digital filters like the one shown in Figure 4.

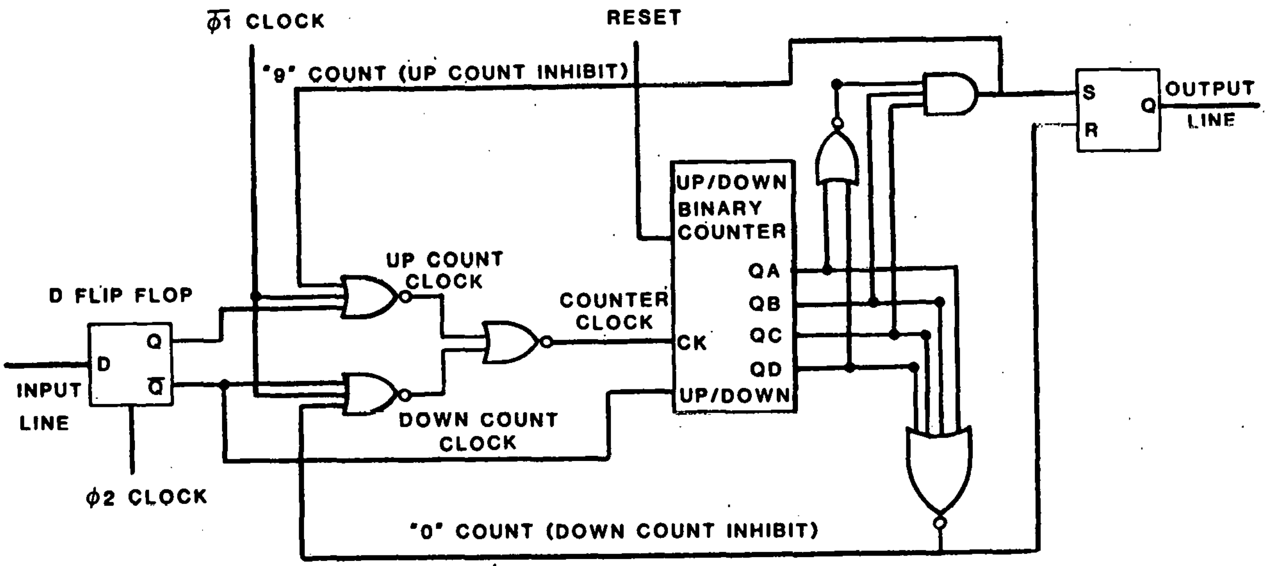

FIGURE 4 - DIGITAL FILTERS

A brief description of the digital filter follows. The up/down binary counters of the digital filters are initially reset to a count of zero. With a logic low input on the filters input line the input "D" flip flop will enable the down count clock signal except when the down count inhibit signal of the feedback term inhibits the clock from getting to the counter. As soon as a logic one signal is applied to the input line, the down count clock is inhibited by the "D" flip flop and the up count clock signal is enabled. Since the up count inhibit signal occurs only at a count of nine, the Phase 1 clocks will increment the up/down counter each 0.2 ms. After the input signal has been present continuously on the input line for ten successive clock counts, the binary counter will be at a nine count and the up count inhibit signal will set the RESET/SAFE latch and the output line will go high. At the same time, the up count inhibit signal will stop the up count sequence. If a dropout in input voltage occurs during the up count sequence, the up count clock will be inhibited by the "D" flip flop and the down clock will be enabled. This will start the binary counter counting down. Thus, a dropout reverses the count on the counter and enough dropouts will prevent the output of the counter from responding to an intermittent input signal. Normal input pulse operation of the filter with no dropouts will delay the output pulse response 2 ms from the occurrence of the input pulse. The negative transition of the input line will cause the down count clock to be enabled by the "D" flip flop and the down count mode of the binary counter to be enabled. The binary counter will decrement each 0.2 ms and when it arrives at a count of "0" the down count inhibit signal will reset the RESET/SAFE output latch and drop the previously high output line signal. In addition, the down count inhibit line will inhibit further down count clocks holding the binary counter at "0". Thus, a normal input pulse turnoff will also be delayed 2 ms at the output of the filter. The filter is designed to eliminate internal logic circuitry from responding to spurious pulses or dropouts on the RESET/SAFE and Prearm lines that are less than 2 ms in duration. This closely simulates the actual response of the electromechanical solenoids of the unique signal devices.

The Reset and Prearm on and off signals thus generated are input to the pulse sequence gate shown in Figure 3. The pulse sequence gate evaluates whether the CM-458/U is responding to a System 1 or System A unique signal pulse train by looking at the System 1 recognition line. Additional information provided by the pulse sequence counter tells the pulse sequence gate where in the pulse train the pulse being evaluated is.

The pulse sequence gate then connects its output to either the Reset or the Prearm inputs, whichever input is for the pulse being measured. The output of the pulse sequence gate for a correct sequence of pulses is a logical sum of all input pulses to the pulse sequence gate. The system will ignore pulses which are out of sequence or which occur on the wrong lines.

The input high signal of the pulse sequence gate enables a RESET/SAFE latch to the pulse width counter in Figure 3 which in turn enables the clock to the counter. At the same time, as long as the input high signal is present, the up/down control will be in the up count position and the counter will increment.

The pulse width counter is a counter which evaluates whether pulses meet minimum and maximum on and off time specifications. The counter measures pulse on-times as an up counter and pulse off-times as a down counter. Immediately after power is applied to the CM-458/U and after each successful pulse occurs and is counted, the pulse width counter is preset to one of three initial counts which are controlled by the reset pulse width, the long pulse width, or the short pulse width signals generated by the pulse sequence counter. These Presets are such that a minimum time output from the counter for the type pulse selected will occur before the pulse which is being evaluated is over; this assumes the pulse being evaluated has an on time which lasts at least the minimum required time. If a pulse minimum time does not occur, an ERPMIN error is generated to the error logic and the cycle is aborted. If the pulse ON time is longer than the maximum permissible on time for the pulse selected, a maximum time output will occur on the output of the pulse width counter and the pulse width evaluator in Figure 2 will generate a PULMAX error to the error logic which also will abort the cycle. If, however, a minimum time output occurred and no maximum time output and the pulse being evaluated goes low, the pulse width counter will begin to count down (because the input to the up/down control is the input high signal which goes low selecting a down count when the pulse goes low). If the pulse sequence counter thinks it is evaluating a short pulse and the pulse goes low after an adequate ON time, the short OFF time signal is generated which causes the counter to count down at 2.5 times the rate it counted up. This is done to satisfy a requirement that the short pulse OFF time be 0.4 times the short pulse ON time. The reset and long pulses

OFF times are counted at the normal counting rate of the counter. If the OFF time of the pulse being evaluated is sufficiently long, a carry out will occur from the PULSE WIDTH COUNTER. This signal will reset the INPUT HIGH latch and turn off the clock enable to the PULSE WIDTH COUNTER. At the same time, if the proper minimum signal occurred to the PULSE WIDTH EVALUATOR and the maximum time signal did not occur, a PULSE OK signal will be transmitted to the PULSE SEQUENCE COUNTER and its counter will increment and set up the PULSE WIDTH COUNTER for the next expected pulse. If a carry out does not occur, the EROFET error will be generated to the error logic and the cycle will be aborted.

The PULSE TRANSITION TIME CHECK circuit shown in Figure 3 is a binary counter which measures the time between the disappearance of the input high signal and the occurrence of the input low signal, i.e., the pulse transition time from high to low. If this time exceeds 1.6 ms a time out error will occur which will trigger the ERROR LOGIC circuit and abort the cycle.

If the proper sequence of short, long, and reset pulses occurred on the proper input lines and all pulses had satisfactory ON and OFF times and transition times, the PULSE SEQUENCE COUNTER will generate an output to the LAMP DRIVER LOGIC (indicating the unique signal is ok). This in combination with no abort errors having been generated by the error logic will cause the LAMP DRIVER LOGIC to generate a signal to the lamp driver controlling the System A monitor normal line to turn off and stop sinking current to the disagree monitor light (providing the system being tested is a System A configuration).

The absence of a disagree monitor signal on the System A monitor normal line indicates that the function requested of the CM-458/U was successfully performed. In the event that the system under test is a System 1 configuration and a successful arming operation occurred, the System 1 arm monitor lamp driver would be turned on and it would sink current to the System 1 ARM monitor indicator and the System 1 SAFE monitor indicator would be turned off. If the attempted System 1 arming operation was unsuccessful, the System 1 SAFE lamp driver would sink current into the System 1 SAFE monitor indicator and the System 1 ARM monitor indicator would be turned off. In the event of a successful System 1 safing operation, the System 1 SAFE monitor lamp driver would sink current into the SAFE monitor indicator and the ARM monitor lamp driver would be turned off. If the safing operation were unsuccessful, the SAFE monitor lamp driver will remain off and an ARM monitor indication will remain. The three monitor lamp drivers of the CM-458/U are all current limited to 50 mA maximum current into their respective interface connector pins.

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