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OVERVIEW ON RADIATION EFFECTS IN ELECTRONICS*

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INTRODUCTION

Electronic components in many applications may be exposed to radiation from sources such as nuclear reactors, the natural space environment, or nuclear weapons. Each of these sources has a unique radiation spectrum that generally has a differing impact upon microelectronic components. A nuclear weapon environment for example, offers a radiation spectrum that is characterized by X-ray, gamma, neutron, and other reaction debris constituents, typically occurring within a short time span. The X-ray and prompt gamma deposition from a nuclear weapon typically occur within 20 nanoseconds, while the remaining radiation generally occurs within a matter of seconds. The nuclear reactor spectrum is characterized as primarily gamma, beta, and neutron over a time frame of years. In the event of a LOCA the ionizing dose (gamma and beta) may reach approximately 2E7 and 2E8 rads(Si) respectively, within 30 days. Finally, the natural space environment, similarly to the reactor environment, does not contain the high dose rate pulse characteristic of a weapon, but still may accumulate a high total ionizing dose (total dose) from electrons and protons over an extended time frame, usually several years depending upon the satellite orbit. The most radiation intense earth orbit includes the Van Allen belt where electron doses of 100 rads(Si)/hour and proton doses of 10 rads(Si)/hour are available. A unique constituent of the natural space environment is cosmic rays, which include massive ions, such as oxygen and iron, with energies exceeding hundreds of GeV.

To summarize, the radiation spectrum constituents of interest to microelectronics are prompt gamma or X-ray, total dose, neutrons (or protons), and cosmic radiation. Each of these constituents has a unique effect upon microelectronic components and requires unique techniques to improve the microelectronic radiation tolerance to such an exposure.

DISCUSSION

This paper reviews the radiation effects associated with the natural space and nuclear reactor radiation environment, that is to say, total dose, neutrons, and cosmic rays. For completeness however, some mention

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DISCLAIMER

dose, neutrons, and cosmic rays. For completeness however, some mention should be made concerning the radiation effects due to prompt gamma (frequently referred to as gamma dot) and X-rays on electronic circuits. Prompt gamma is a result of either a nuclear detonation or DEW, and is expressed in rads(Si)/sec. In silicon, ionizing radiation generates hole-electron pairs at a rate of 4.3E13 hole-electron pairs/rad(Si)/cm^3, and the high dose rate associated with prompt gamma, typically 1E8-1E12 rads(Si)/sec, initiates unique responses in semiconductor devices. In particular, the high dose rate produces transient photocurrents in semiconductor materials that initially cause logic upset and in some technologies, such as junction isolated bipolar and bulk CMOS, may result in a condition known as latch-up. Latch-up occurs when parasitic bipolar elements, existing in all junction isolated bipolar and bulk CMOS circuits, are configured as a parasitic SCR (Semiconductor Controlled Rectifier) as a result of the radiation induced photocurrents and subsequently initiate SCR action. The parasitic SCR action is usually terminated either when the power supply is interrupted or when device failure occurs. For conventional silicon technologies, logic upset occurs for gamma dot levels on the order of 1E8 rads(Si)/sec, and for sensitive technologies, such as junction isolated bipolar or conventional bulk CMOS, latch-up may occur at approximately 1E10 rads(Si)/sec. Fortunately, there are techniques available for both improving the logic upset level and for providing latch-up immunity to normally sensitive circuits.

Total dose is the accumulated ionizing radiation received by a material and the effect of total dose is to generate hole-electron pairs in the material. The ionizing radiation may result from exposure either to gamma radiation or from charged particles, such as electrons or protons. Ionizing radiation resulting from particle exposure is usually accompanied by displacement damage, which will be discussed in a latter section. In semiconductor devices the major impact of total dose is upon the dielectric layers used either for active gates (MOS devices) or field isolation (virtually every semiconductor device, including many III-V structures). In the semiconductor materials, the radiation induced hole-electron pairs will dissociate into individual holes and electrons that, depending upon the material, will be either minority or majority carriers. If the minority carriers do not diffuse to a region where they become majority carriers, then they will exponentially decay at a rate determined by the minority carrier lifetime. The majority carriers represent a photocurrent that eventually is passed to the power supply, usually without deleterious effects to the semiconductor device. As the total dose exposure from gamma radiation approaches 1E6 rads(Si), displacement damage within silicon will become noticeable.

The impact of total dose upon dielectric layers is considerably more complex than within the semiconductor substrate. In fact, the major total dose degradation mechanisms in semiconductor devices are associated with radiation induced changes within the dielectric. In a dielectric, such as SiO_2, hole-electron pairs are formed by the ionizing radiation, as they are in the bulk semiconductor material. Electrons however, quickly sweep through the oxide due to their significantly higher mobility and reduced trapping cross-section, leaving a net positive

charge in the oxide from the remaining holes. These holes then migrate to either the oxide-semiconductor or oxide-electrode interface at a rate that is dependent upon temperature, electric field, and the oxide process parameters. Generally, holes that transit the electrode-oxide interface do not degrade the device characteristic. Holes trapped in metastable states at the oxide-semiconductor interface however, can cause a significant change in the oxide characteristics at short times following a radiation pulse.

A fraction of the holes traversing the interface are trapped, representing a net positive charge in the oxide. Another fraction of the holes generate interface states in the oxide which, depending upon the material polarity and gate bias during irradiation, will become negatively or positively charged for n-channel and p-channel transistors, respectively. Since the trapped charge and interface generation are a strong function of the number of holes traversing the interface, it is expected that there will be a strong field dependence upon the charge state. This manifests itself as a threshold voltage shift for MOS devices. Figures 1 and 2 illustrate the threshold voltage shift for a hardened oxide as a function of dose and gate bias (Dressendorfer, 1981). The turn around in the n-channel device is due to the negatively charged interface states dominating the positively charged trapped charge at approximately 2-5E5 rads(Si). For p-channel devices, both the interface charge and trapped charge are positive. For n-channel devices, the interface charge buildup also significantly degrades the device mobility; typically, for a hardened device, a 1E6 rads(Si) exposure will result in an approximate 10-50% mobility degradation. The effect is considerably smaller for p-channel devices.

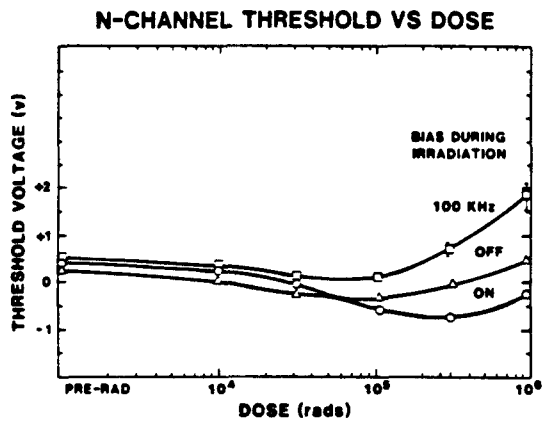

FIGURE 1

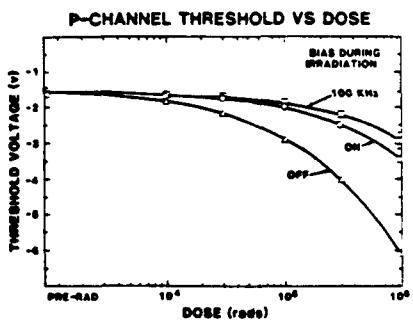

FIGURE 2

Another characteristic of total dose exposures to MOS devices, especially silicon gate n-channel transistors, is a long term annealing phenomenon referred to as rebound (Schwank, 1983). Rebound, illustrated in Figure 3, represents the post irradiation gradual annealing of the

oxide trapped charge, which causes the n-channel threshold voltage to increase, frequently exceeding its initial preirradiation value. The rate of rebound is a strong function of bias and temperature, with a thermal activation energy of about 0.4 eV. For an ambient temperature of 125°C and a +10 volt bias, saturation occurs after approximately 100 hours. This effect is naturally a great concern for long term, low dose rate exposures, such as space or reactor applications.

The effect of total dose on gate oxides is a strong function of oxide thickness, typically a power of 2 to 3. For this reason, MOS radiation hardening techniques usually start by using thin gate oxides, consistent with the reliability concerns. The thickness dependence will saturate at approximately 1200 A, but considerable threshold shifts will still occur in the field oxide regions, which may be on the order of 1 micron. The problem is usually confined to p-type surfaces (n-channel devices) since the positive trapped charge tends to drive the surface n-type. N-type surfaces become more strongly accumulated, and thus are not typically a problem. Field inversion usually causes commercial devices to fail before radiation induced threshold voltage shift, typically at approximately 1E4 rads(Si). Figure 4 illustrates the magnitude of the radiation induced field threshold voltage problem. For reference, a typical circuit will exhibit field failure if the field threshold voltage shifts approximately 10-20 volts toward inversion.

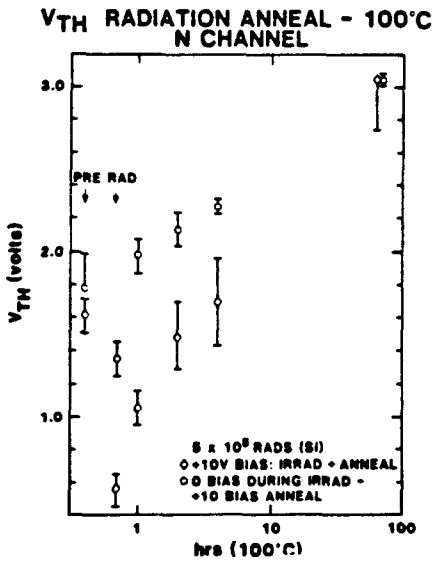

FIGURE 3

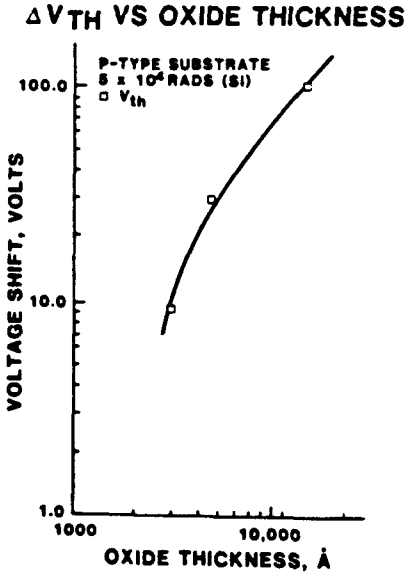

FIGURE 4

Similarly to the problem with the gate oxide radiation response, there are techniques for hardening field oxides. Although the discussion primarily dealt with MOS devices, field inversion may also destroy bipolar functionality, as well as significantly increase diode leakage currents.

The effect of neutron irradiation upon semiconductors is to introduce damage clusters which result from the collision of the neutron with a

lattice atom and the secondary collisions from the recoiling atom. Displacement damage is also associated with proton irradiation, and to a lesser extent, with electrons and gamma irradiation. There is annealing associated with the damage cluster, and it is a strong function of temperature, carrier density, and time. But in general, a significant fraction of the damage (>1/2) is unannealed under normal operating conditions. The damage clusters have several effects in semiconductor materials, the most important is the reduction of minority carrier lifetime. For example, a 1E14 n/cm^2 (1 MeV equivalent) exposure in silicon will result in a minority carrier lifetime on the order of nanoseconds, whereas its preirradiation value may have been on the order of milliseconds. The second major effect of damage clusters in semiconductor materials is carrier removal. A general rule of thumb for silicon is that every 1 MeV equivalent neutron will remove 10 carriers.

The consequences of a minority carrier lifetime reduction is to degrade those device types, such as bipolars, dependent upon minority carrier lifetime for functionality. MOS devices are generally not sensitive to minority carrier lifetime. The neutron sensitivity of bipolar devices is a function of the base width, which is inversely proportional to the maximum frequency of operation. This is illustrated in Figure 5. The implication of this is that high voltage bipolar devices, which need long base widths to support the voltage, will be very sensitive to displacement damage.

Displacement damage induced carrier removal will become a factor in device performance when the carrier removal becomes comparable to the sensitive doping levels. For MOS devices, this is typically on the order of 1E15 carriers. High voltage devices, including high voltage bipolar or diodes, usually have high resistivity regions to support high voltage breakdown voltages; the doping levels on these regions is usually on the order of 1E14 carriers, thus these devices are very sensitive to modest neutron fluences, such as 1E13 n/cm^2.

Cosmic radiation is a source of circuit malfunction referred to as SEU (Single Event Upset) and is illustrated in Figure 6.

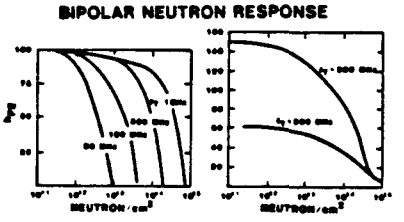

FIGURE 5

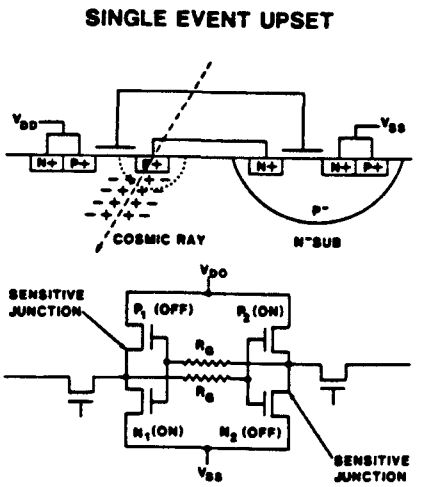

FIGURE 6

SEU results from a high energy heavy ion striking a sensitive node and depositing a charge on that node. Note that the ion energy, which can range to hundreds of GeV, precludes shielding as a practical technique for SEU prevention. For MOS circuits, the charge discharges the gate, which is a capacitor, resulting in a transient change of state for that node. If the recovery time at the node is less than the circuit response time, then there will be no logic upset. If however, the circuit response time is less than the nodal recovery time, then there will be a logic state change. Bipolar circuits generally do not rely on capacitive nodes, but current levels instead. In this case, the SEU induces a logic state change by the current spike resulting from the ion hit. In general, the SEU phenomenon is a characteristic of the natural space environment, and for typical 2 micron design rule MOS SRAM circuits, the error rate in space due to SEU is on the order of 1E-6 errors/bit/day. It should also be noted that the transient charge spikes from cosmic ray hits are also capable of inducing latch-up, a disagreeable effect usually associated with prompt gamma radiation from a weapon spectrum. Since the atmosphere shields the Earth from heavy cosmic rays, such as oxygen and iron, SEU is generally not a problem for terrestrial applications. There is one exception to this however, and that is the alpha radiation from ceramic packages, which is capable of inducing SEU in high density DRAM circuits. Fortunately, alpha particles have a limited range and are easily stopped by thin chip coatings. Similarly to the other radiation effects previously discussed, there are solutions to the SEU problem.

SUMMARY

The radiation spectrum from sources such as nuclear weapons, the natural space environment, and nuclear reactors includes prompt gamma and X-rays, total dose, neutrons, and cosmic radiation. Succinctly, prompt gamma and X-rays may produce transient upset and latch-up in microelectronic circuits, while total dose typically causes threshold voltage shifts and mobility degradation. Since the threshold voltage shifts also impact field isolation, the effect may manifest itself as increased junction leakage. Neutrons generate displacement damage with its ensuing degradation on minority carrier lifetime and carrier removal. Finally, cosmic rays may cause SEU, and in some cases, latch-up. For all these radiation events, there are both process and circuit techniques that vastly improve the radiation tolerance of microelectronic circuits.

REFERENCES

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