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CADMIUM SULFIDE - COPPER SULFIDE HETEROJUNCTION CELL RESEARCH

Quarterly Progress Report

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1. ABSTRACT

The development of the planar junction CdS/Cu_2S solar cell has been continued. Experiments have been conducted with varying thicknesses of Cu_2S to determine whether the need for light trapping can be reduced by utilizing thick Cu_2S layers. Further optical analysis of the influence of texturing on light trapping in the cell have been conducted. In Task 2, the development of a (CdZn)S/Cu_2S cell, a major effort has been expended in determining the details of the junction morphology. A wide range of analytical work has continued under Task 3. Preliminary data has been obtained on cells sealed behind sheet glass and cells with integral electron beam evaporated glass coatings.

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3. INTRODUCTION

The cell development efforts have concentrated on the achievement of high short circuit currents with a planar junction of high open circuit voltage. It has been found that both the optical and electronic properties of the Cu_2S layer are changed significantly when using the solid state rather than the solution reaction process. Systematic investigation of the optical behavior using various reflection measurements has been continued. Detailed studies of the effects of the solid state formation process on the resulting Cu_2S layer are providing direction for the improvement of key Cu_2S properties.

The methodology for the development of (CdZn)S cells has been to modify the cell design and production procedures until the mixed sulfide cell resembles as closely as possible the high efficiency CdS/Cu_2S cells. During this quarter it has been found that the Cu_2S morphology in the mixed sulfide cell is considerably different to that in the CdS cell and a plausible correlation with observed mixed sulfide cell properties has been made. Further attempts will be made to produce a junction and Cu_2S morphology more closely matching that of the CdS cell.

Detailed modeling and analysis and the application of loss minimization continue to drive the cell development efforts. Progress has been made in developing techniques to determine the hole trap population in the CdS junction region. This work will be progressively extended to the mixed sulfide.

Some preliminary data has now been obtained on cells sealed behind sheet glass and also encapsulated by electron beam deposition from a special glass frit. As may have been anticipated the first attempts at providing total hermetic enclosures have not succeeded and will require further technology development.

4.1 Task 1 Development of CdS/Cu_2S Solar Cells

Work has continued on the first two phases of this task, the development of a planar junction with the necessary open circuit voltage and fill factor, and the development of a satisfactory anti-reflection technology. The production of cells with high short circuit currents by combining these two phases has been delayed by the realization that light trapping as well as low first surface reflection must be achieved.

4.1.1 Phase 1: Develop planar junction to achieve V_{OC} and FF design goals

Status: The above goals were reached during first quarter.[1] However ongoing cell production for experiments addressing the goals of other activities has shown that CdS substrate material of poor quality is being produced. This is evidenced by low V_{OC} and J_L in conventional solution reacted-textured cells as well as by below design V_{OC} in solid state-untextured cells being intermittenly observed.

4.1.2 Phase 2: Reduce the photon losses of the planar cell to the level of the textured cell by developing an improved front surface AR structure and overall light trapping technology.

Status: Three concepts are under development to improve the overall photon economy of the planar cell:

1) Increasing the active layer (Cu_2S) thickness

2) Modifying diffuse reflection from the CdS/Brass interface in order to increase "light trapping"

3) Increasing the texture of the AR coating/Air interface to decrease both reflected and re-emitted photon losses.

The progress and problems in each area are as follows.

a) Effect of Cu_2S thickness on J_{sc} of planar cells.

Results to date: Optimization of J_{sc} in "dry" Cu_2S cells made with various Cu_2S thickness yields the results shown in Figure 1. These results reveal that the optimum Cu_2S thickness for planar cells lies in the range 0.1 μm < $\overline{d}$ < 0.2 μm, where $\overline{d}$ is the effective thickness determined by the electrochemical method.[2] For the above $\overline{d}$ range, total reflectance losses exceed those for textured cells (≃ 6%) even after AR coating application (Figure 2). While this points to a fundamental limitation in the photon economy of planar cells, the currents achieved in most cases are even lower than would be predicted on the basis of photon losses alone. Table I summarizes the results obtained for the highest current planar cells produced by solid state reaction and compares them to a high current textured cell. After correcting for reflection losses, the difference between the currents observed is reduced to ca. 10%.

Table I

Average Reflectance (R) of CdS/Cu_2S cells with SiO_x AR Coating

Cell	Junction	Substrate	Reflectance (R)	J_{sc}(AM1) [mA/cm^2]	J_{sc}(AM1)/(1-R) [mA/cm^2]
686 A14	Solid State	Smooth	0.17 ± 0.03	20.5	24.7
462 D1	Solid State	Rough	0.12 ± 0.03	20.2	23.0
690 B13	Solution	Rough	0.04 ± 0.01	24.8	25.8

Finally, major differences exist between measured and calculated reflectance losses for planar cells. At this time, the differences are believed to arise from "light trapping" induced by diffuse reflection at the CdS/Brass

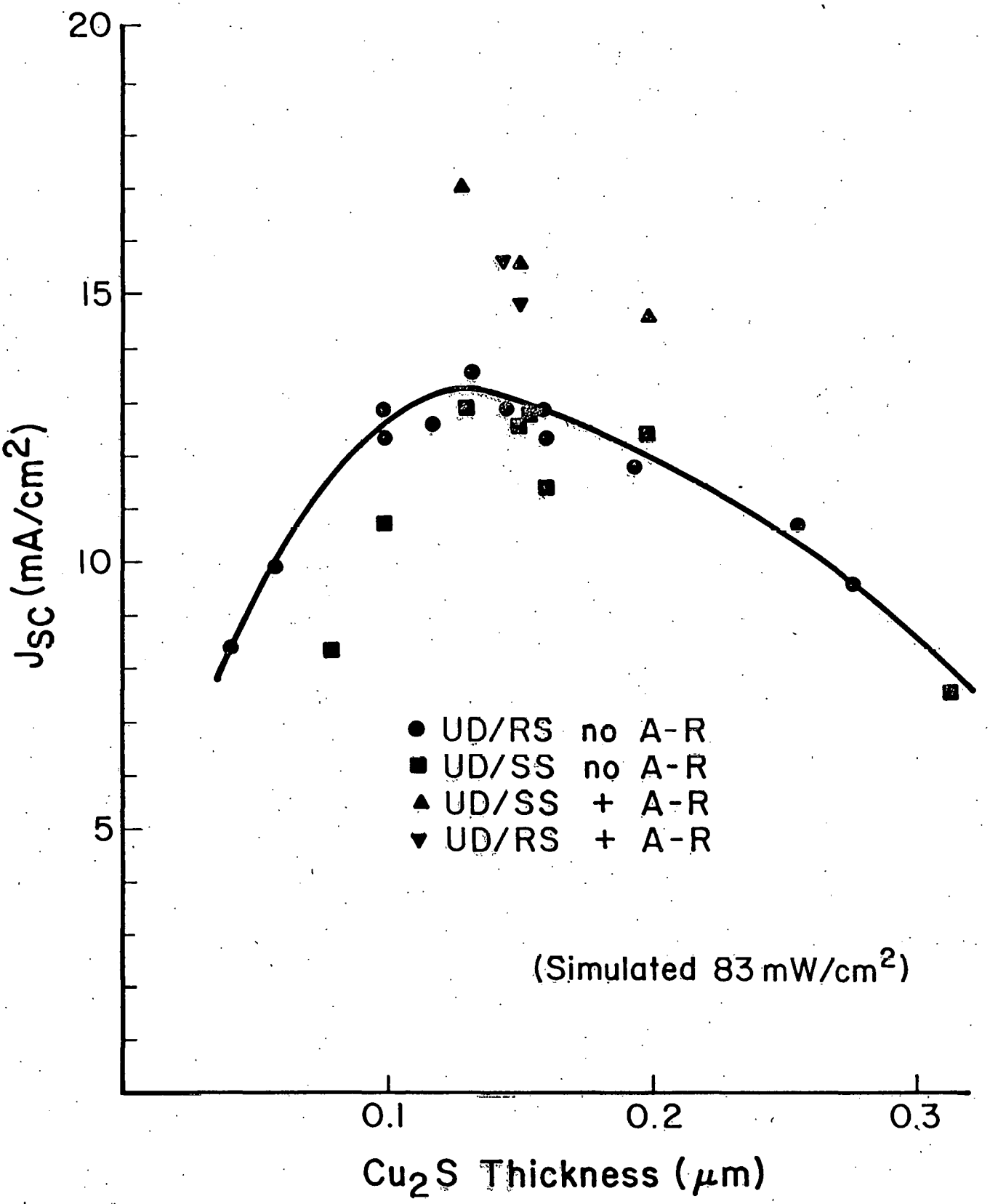

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Fig. 1 The influence of Cu_2S thickness on short circuit current for various planar junction cells.

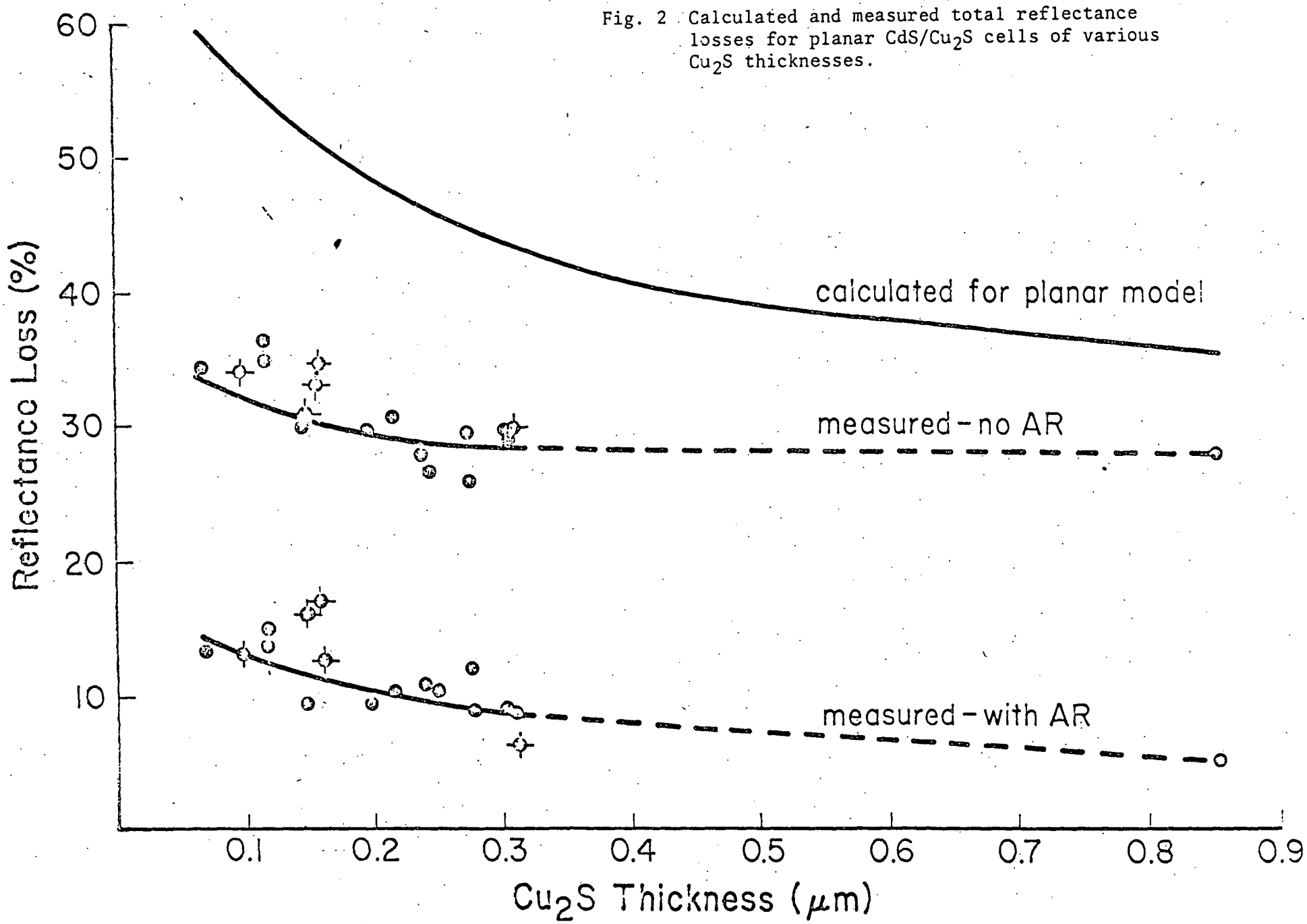

Fig. 2 Calculated and measured total reflectance losses for planar CdS/Cu_2S cells of various Cu_2S thicknesses.

interface. This occurs for cells made on either the rough or smooth side of the Cu substrates, suggesting that even the presence of striations in the smooth substrate is sufficient to cause significant improvement in the photon economy. Modeling to quantitatively account for the effects of substrate texture is in progress.

Problems and Proposed Solutions: The major problem encountered has been the fluctuation in materials quality described in relation to Phase I. Preliminary measurements show that the J_{sc} losses in planar cells due to junction recombination can be neglected. This points to bulk and surface recombination as the most likely mechanisms to account for excessive non-optical losses. Accordingly, analysis and development of solid state Cu_2S and improvement in the quality of the CdS substrate material will be pursued. A high J_{sc} in conventional textured cells is used to monitor the effective "quality" of the CdS.

b) Development of New Textured Substrate

Results to date: Preliminary experiments have shown that the smooth side of the Cu substrate can be textured by etching in a solution containing HNO_3, H_2SO_4 and ZnO followed by etching in $Na_2Cr_2O_7$ to smooth out large features and introduce small ripples. Figure 3 shows the resulting optical behavior.

Texturing of the substrate results in a decrease in reflectance of CdS/Brass samples obtained by applying standard process to etched Cu. This decrease is higher than the changes in the bare brass reflectance, thus demonstrating that light trapping is taking place. (Figure 4). However, as is shown by comparing the data in Table 2 with Figure 3 the degree of diffuse reflectance achieved with any etched surface is less than that arising from the matte side of the electroformed copper.

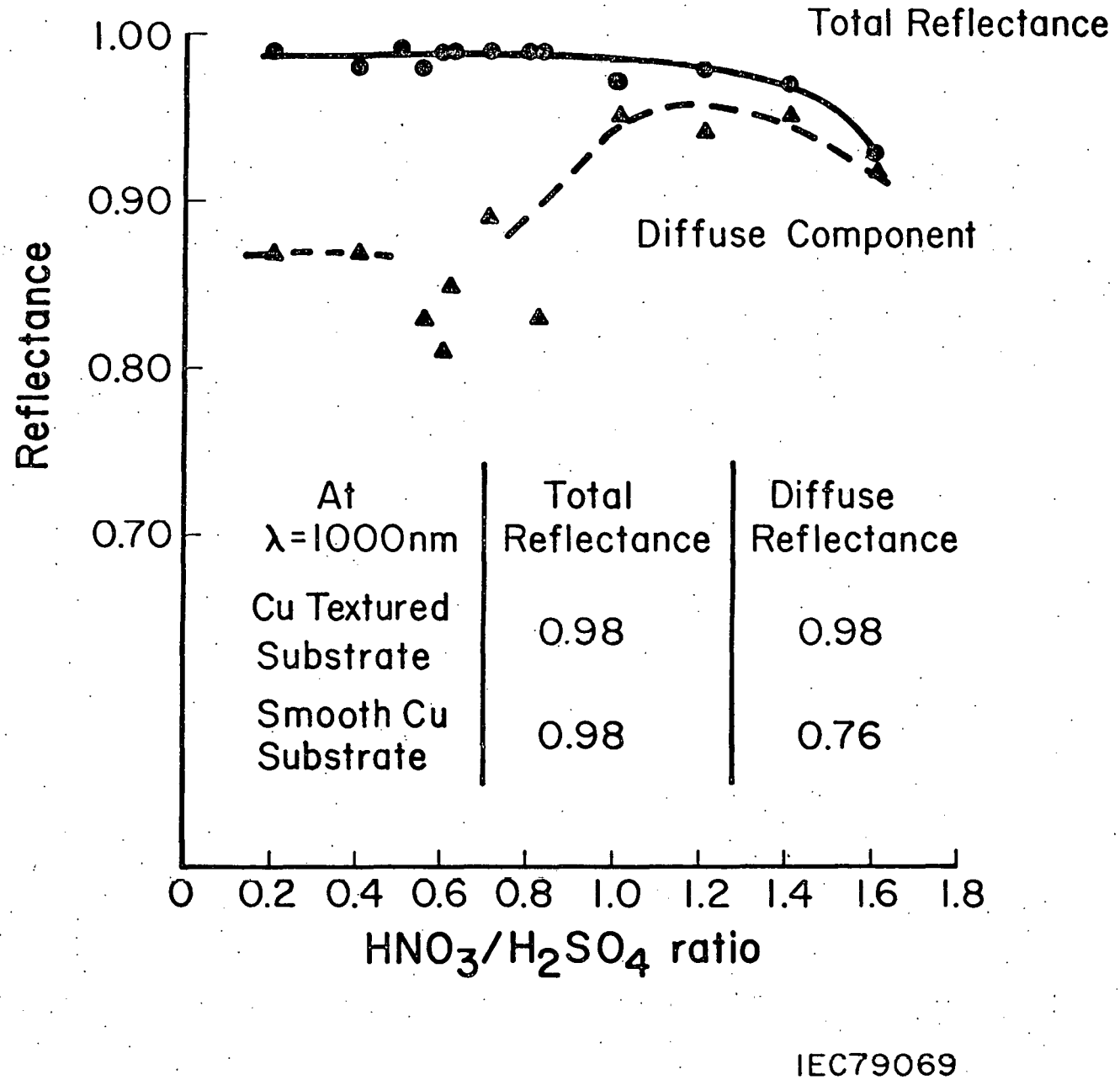

Fig. 3 Measured total and diffuse reflectance as influenced by the amount of etching performed on the copper substrate.

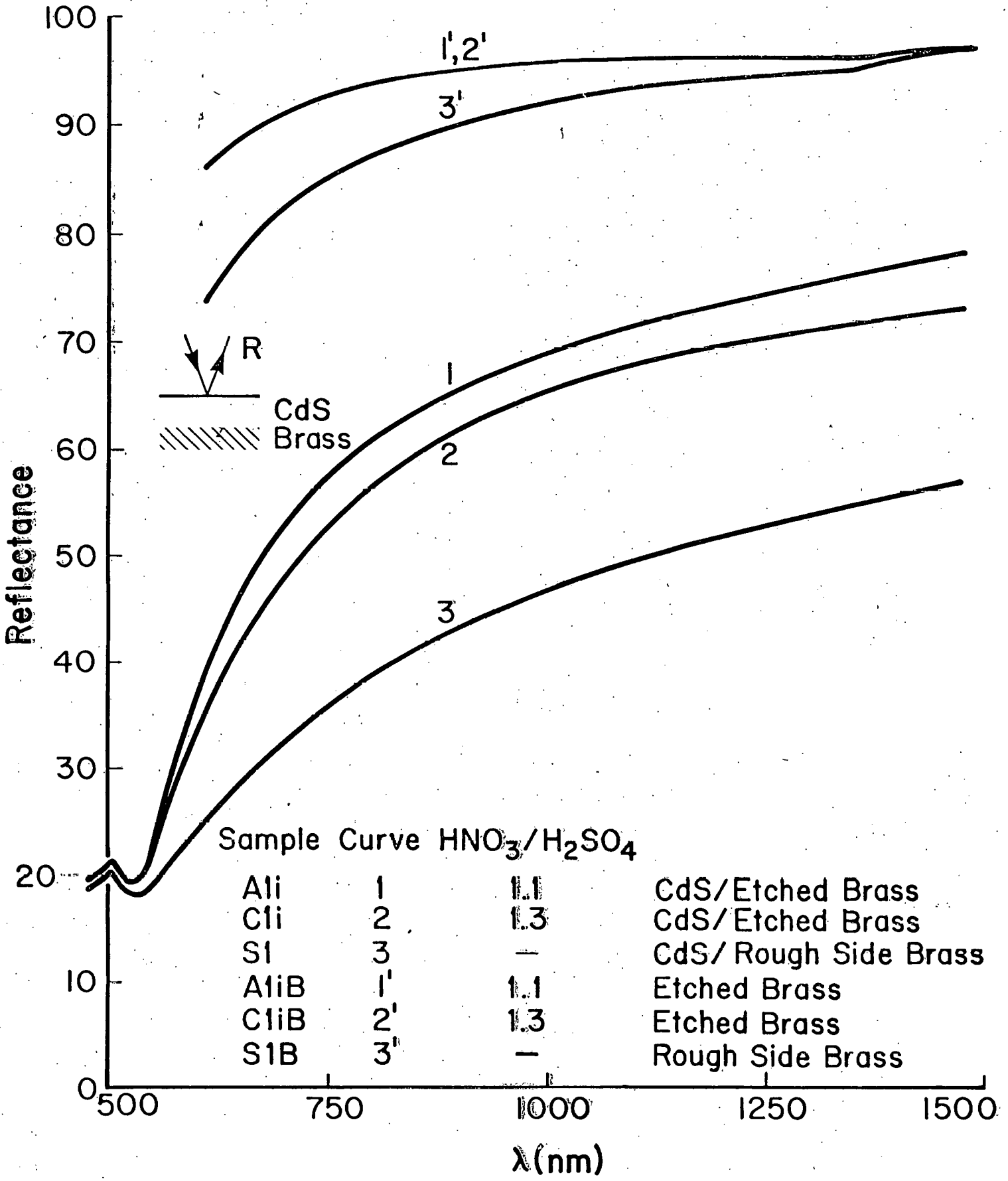

Fig. 4 Total reflectance from a brass surface with and without an overlying CdS layer. The various surface morphologies on the brass were produced by etching the starting copper substrate surface. IEC79070

Table 2

Diffuse Component and Total Reflection from the Smooth and Matte Side of The Electroformed Copper Substrate Measured at 1000 nm

	Total Reflectance	Diffuse Reflectance
Matte Surface	0.98	0.98
Smooth Surface	0.98	0.76

Scanning electron microscopy has shown that a smooth CdS surface can be produced by growth on a finely textured (etched) copper surface. It is tentatively concluded that the goal of a high voltage planar junction in a structure giving good light trapping is therefore achievable.

Problems and Proposed Solutions: The main problems in this area are the lack of a quantitative model relating "light trapping" to texture and in the ability to carry out measurements of bidirectional reflectance to evaluate the results of various texturing processes. However a technique has been developed to evaluate the influence of substrate texture on light trapping by applying a dielectric (CdS) to the substrate and measuring the total reflectance of the system dielectric/substrate. Variations in substrate roughness do induce reflectance variations as shown in Figure 4. A second technique, comparing specular and total reflectance using the Gier-Dunkle integrating sphere, provides a first order approximation to the evaluation of the directional reflectance of the substrates investigated.

Future work will address both the modeling and measurements problems as well as that of extending the etching techniques to large textured AR cover.

c) Development of a Textured AR cover

Results to date: This activity has been delayed by lack of a quantitative model to guide the reduction to practice of this concept. A preliminary design for this structure consisting of a thin (5 μm) glass layer deposited on the Cu_2S and textured by chemical treatment or sandblasting has not yet been successfully applied to cells. Shorted cells resulted in the case of chemical attack, while sandblasting has been observed to increase the absorption of the glass layer (Figure 5). Future work will be closely integrated with Task 4.

Work on the other phases in this Task is being deferred pending the successful completion of the first two phases.

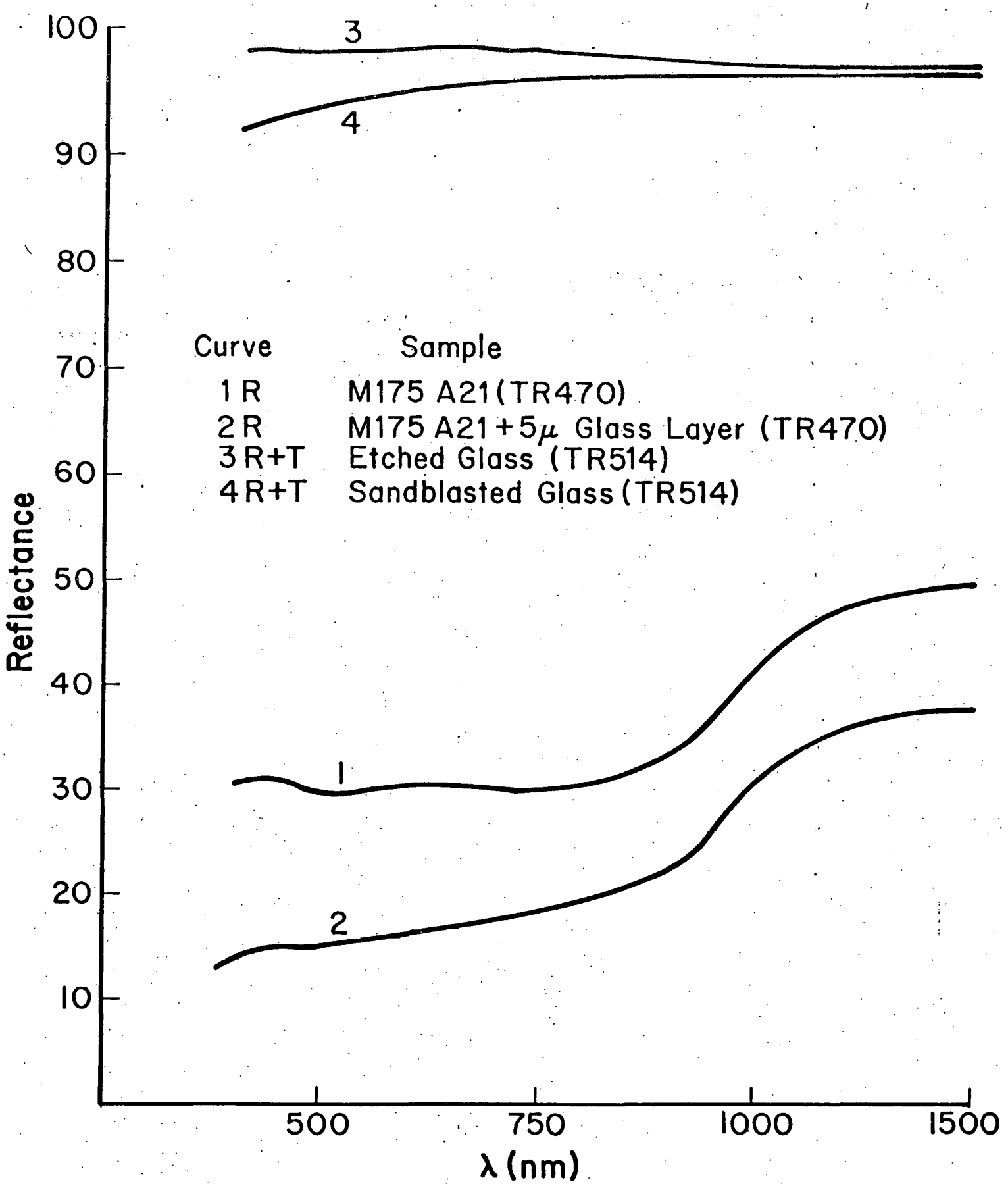

Fig. 5 Total reflectance and transmission for various samples.

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4.2 Task 2 Development of (CdZn)S/Cu_2S Solar Cells

Attention has focused on the differences between the Cu_2S and junction morphology in CdS and (CdZn)S solar cells. The specific phase of Task 2 addressed during the past quarter has focused on an investigation of the Cu_2S morphology. The cell design strategy has been to prepare Cu_2S on (CdZn)S films with zinc concentrations between 10-15% by the technique known to achieve high currents[3] in CdS/Cu_2S. The goal is to verify that comparable short circuit currents can be obtained from a (CdZn)S/Cu_2S cell.

4.2.1 Phase 1 Growth of Optimized (CdZn)S Films

Status: Good control has been achieved over morphology, resistivity and photoluminescence. The results reported during the last quarter suggested major differences in junction morphology and attention was therefore focused on this aspect of cell development

4.2.2 Phase 2 Development of Good Heterojunctions in (CdZn)S/Cu_2S

Whereas short circuit currents in excess of 15 mA/cm^2 (ELH simulator at 83 mW/cm^2 equivalent) have been observed for the textured (CdZn)S solution grown Cu_2S, the open circuit voltages of these devices decay with time.[1] Optical cross sections of these devices revealed the existence of intrusions presumably Cu_2S, into the (CdZn)S at the Cu_2S-(CdZn)S interface. Intrusions have been reported in the past for CdS/Cu_2S cells, and were tied to the long term V_{oc} decay of those cells.[4] The optical cross section of a range of (CdZn)S compositions indicate that the linear density of intrusions and their average depth increase with increasing zinc concentration. Optical microscopy does not reveal these intrusions into the (CdZn)S when either the morphology of the (CdZn)S film is changed (i.e. (CdZn)S grown on the smooth side of copper),

or the method of Cu_2S formation is different (i.e. solid state reaction process). However, the V_{oc} instability of devices prepared using these latter fabrication designs still persist but to a much lesser degree.

A scanning electron microscope technique has been described by Szedon[5] which reveals the Cu_2S morphology with high resolution after the CdS has been removed. This technique has been applied to an IEC textured (CdZn)S - solution grown Cu_2S cell and revealed 6-8 μm long cone-like structures in the Cu_2S morphology.

The plan for the ensuing reporting period will be to continue the characterization of Cu_2S intrusion for a variety of junction formation designs. In addition, an investigation to determine the microstructural defects which permit intrusion formation and their specific impact on cell parameters will be undertaken. As the results of these investigations are analyzed, appropriate modifications to material preparation will be instituted to eliminate or passivate the microstructural defects. Work on the remaining two phases of this Task must await the successful outcome of the junction studies.

4.3 Task 3 Electro-Optic Analysis and Modeling

4.3.1 Phase 1 Feedback Analysis

A significant fraction of the effort in this Task is the routine testing of cells to provide information and direction to the other tasks. Although referred to as routine, these testing procedures go well beyond I-V testing under simulated sunlight. Photocapacitance as a function of intensity, spectral response measurements and I-V testing under a range of intensities and spectral content are carried out for diagnostic and loss minimization purposes.

4.3.2 Phases 2 and 3 Map Junction Field CdS, CdZnS

Modifications and improvements to the photocapacitance system have continued. A lower limit to the capacitance that can be measured due to instrumental and lead capacitances is 1 nF. A break in the 1/C versus $1/\eta_c$ curves which are used to determine S_I/μ near AM1 intensity was seen in recent work. This break would imply much higher values of S_I/μ - 5 x 10^4 V/cm as compared to - 5 x 10^3 V/cm reported previously. Such high values would lead to greater current losses at the interface ($\tilde{}$ 20%) as compared to previous loss estimates (<5%). A careful study of all components of the system is being undertaken to determine whether this effect is real or instrumental.

4.3.3 Phase 4 Quantify Interface Recombination

The losses at the interface are field dependent through the field dependence of the light generated current J_L,

$$J_L = J_{LO} \frac{\mu_2 F_2}{S_I + \mu_2 F_2}$$

The determination of S_I/μ from the photocapacitance and collection efficiency measurements uses this equation. The field is varied by varying the white light intensity which changes the trapped hole population and measuring J_L at zero voltage. Another way of studying these effects and also fill factor losses is to determine J_L as a function of voltage. The technique for doing these measurements utilizes the spectral response apparatus.

Figure 6 shows a schematic representation of the experimental set-up which is used. Light from an ELH lamp powered by a stabilized DC source passes through a grating monochromater. An image of the exit slit is focused on the surface of a silvered light-chopping blade placed at 45° to the path of the incoming light beam. The transmitted beam illuminates the cell under test through an appropriate lens system. The beam reflected from the chopper is monitored to give a continuous measurement of the primary beam intensity. The light-chopper control provides a reference signal for the lock-in amplifier which is used to measure the AC output of the cell. An ELH tungsten-iodide lamp driven by a stabilized DC supply provides the bias light. The cell under test is mounted on a thermoelectric temperature-controlled block with the necessary electrical connections to allow for application of a bias voltage and measurement of cell output. Output from the lock-in amplifier and the voltage-biasing power supply are manipulated by a PDP 1103 and the output fed to an x-y recorder for display.

Marked differences in the fraction of current lost due to voltage-dependent junction effects have been noted for cells of differing performance characteristics. Figure 7 shows J_L/J_{LO} at AM1* as a function of bias voltage for two cells of significantly different performance. A table of current-voltage parameters has been included and it can be seen that while the open-circuit voltages (V_{OC}) are within 5% of each other, and the short-circuit

*AM1 is set on the ELH lamp simulator using NASA standard reference cells.

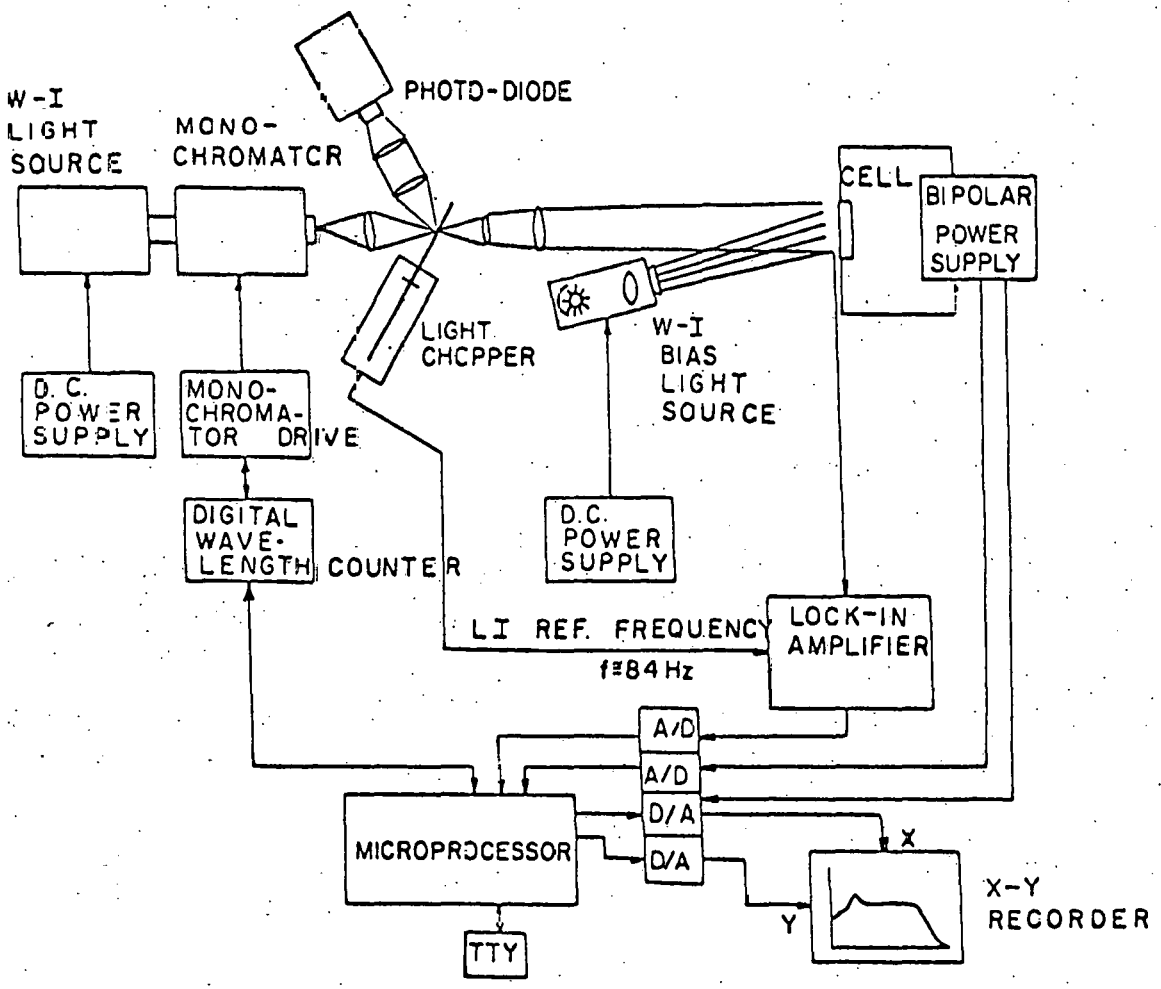

Fig. 6 Block diagram for the spectral response equipment.

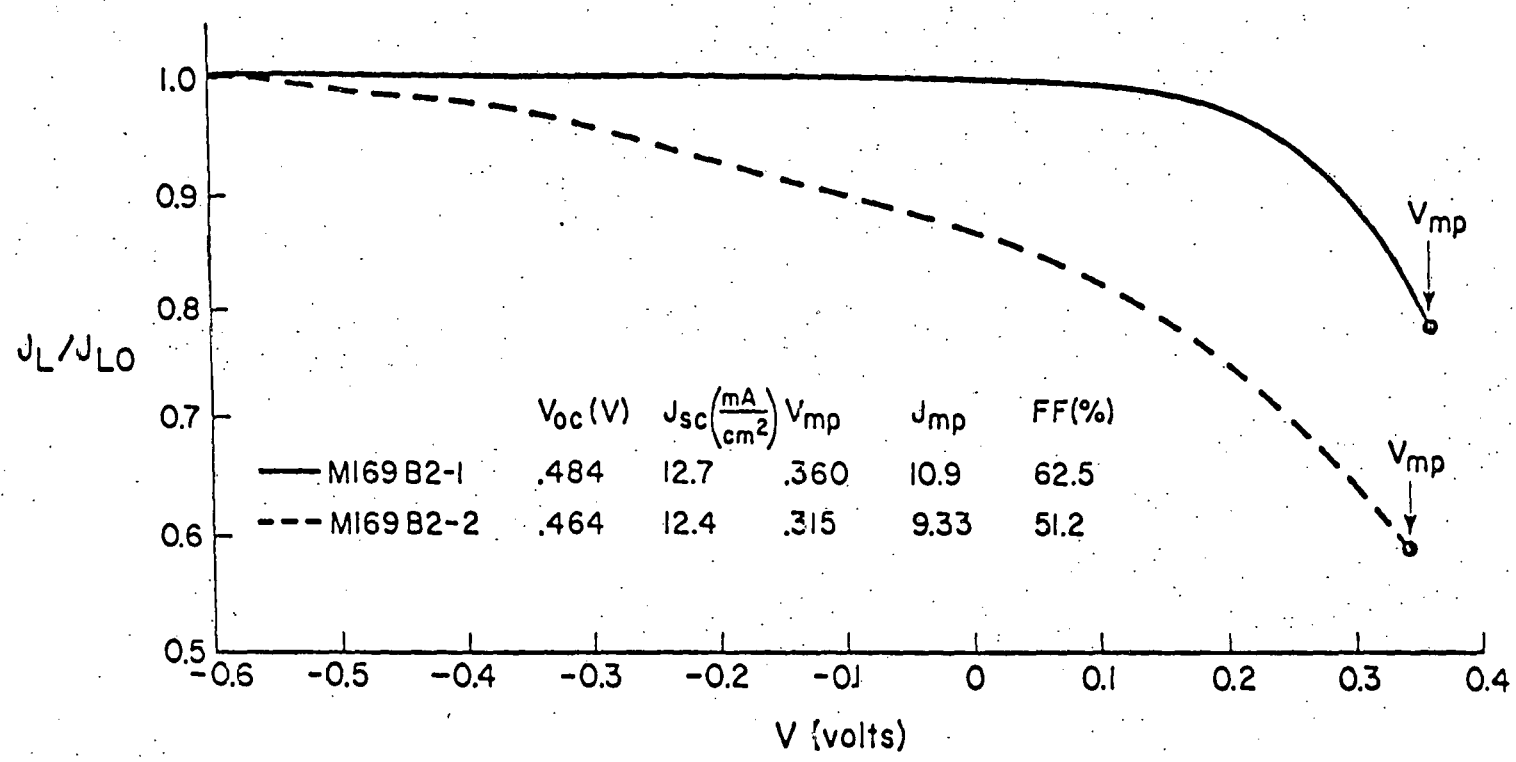

Fig. 7 The influence of bias voltage on light generated current for two cells showing significantly different fill factors.

currents (J_{SC}) are within 3%, the fill factor (FF) of cell M169B2-2 is nearly 20% less than that of cell M169B2-1. This disparity in fill factor is clearly mirrored by the J_L behavior of the two cells.

For cells of generally good performance characteristics the variation of J_L with voltage is not so pronounced under normal AM1 conditions. For these cells, however, it is possible to induce strong voltage dependence by varying the junction field via the bias light. Figure 8 shows J_L/J_{LO} vs. voltage for cell #810A1-4 under three different conditions of bias illumination. The top curve was taken under standard AM1, while the two bottom curves were obtained using color filters which limit the shorter wavelength portions of the spectrum.† From the included table of current-voltage parameters measured under corresponding bias light conditions we see that the J_L/J_{LO} behavior clearly mirrors the progressive loss in fill factor observed for longer wavelength illumination. This lowering of the fill factor, along with corresponding changes in photocapacitance, has been reported previously.(6)

The extension of this technique to variation in bias white light intensity and spectral intensity will be carried out. The results will be compared to theory to determine S_I/μ and the variation of F_2 with voltage.

4.3.3 Phase 5 Identify Degradation Mechanisms

Studies of the time dependence of V_{oc} in (CdZn)S/Cu_2S cells have continued. All evidence still continues to point to the deep intrusions of Cu_2S into the CdZnS layer as the cause of the decay.

† Corning sharp cut orange filter C.S.3-68(507 nm < λ < 574 nm) and sharp cut red filter C.S.2-73 (558 nm < λ < 618 nm)

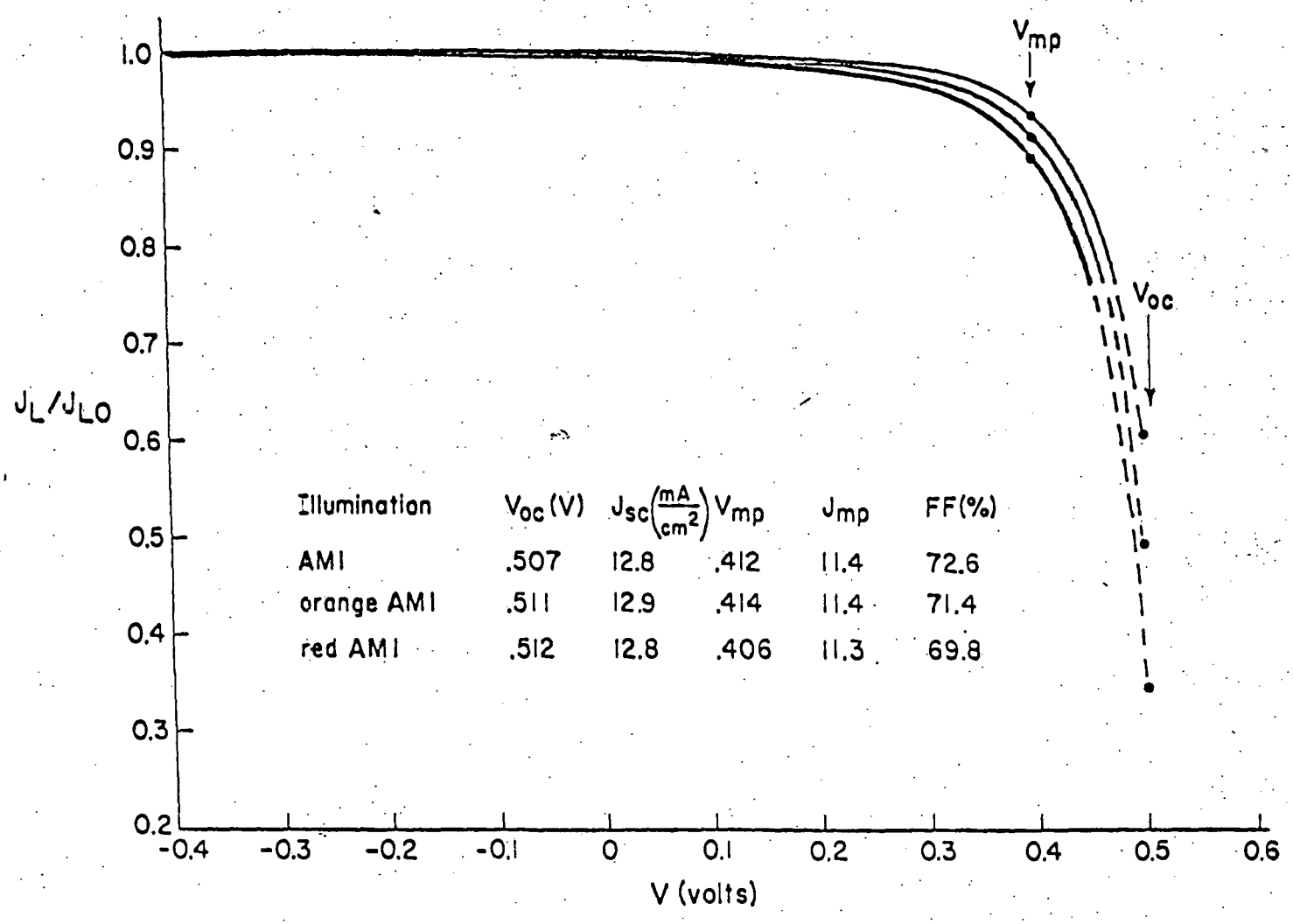

Fig. 8 The influence of the spectral content of the bias illumination on the voltage dependence of the light generated current.

4.3.2 Phase 6 Identify Trap Levels

As part of a program to identify the defect levels in CdS time dependent studies of photocapacitance build up and decay at under various illumination conditions were started. Figs. 9 and 10 show the preliminary results of these studies.

4.3.5 Phase 7 Theoretical Modeling

a) Optical losses in Cu_2S/CdS cell. The observed changes[1] in optical absorption in Cu_2S can be related to expected changes in short circuit current by consideration of the main optical loss mechanism within the cell, namely absorption at the back contact. If we assume that the reflection coefficient at the back contact is r, and all light reaching the front surface after being reflected from the back is totally internally reflected, then the collection efficiency ($j_L(\lambda)/\Phi(\lambda)$) is given by

$$\eta_c(\lambda) = \frac{\eta_{cFw} + r \exp(-\alpha d)\, \eta_{cBw}}{1 - r \exp(-2\alpha d)}$$

where η_{cFw} is the collection efficiency calculated for a front wall mode cell η_{cBw} is that for a backwall cell, and α is the absorption coefficient of the Cu_2S and d is the Cu_2S thickness. For thin layers $\eta_{cFw} \simeq \eta_{cBw} = 1 - \exp(-\alpha d)$, neglecting other losses and η_c can be written as

$$\eta_c = (1 - \exp(-\alpha d)) \left(\frac{1 + r \exp(-\alpha d)}{1 - r \exp(-2\alpha d)}\right)$$

As $r \to 1$, $\eta_c \to 1$, independent of αd. For $r < 1$, η_c and hence j_{sc} becomes very sensitive to α for fixed d. For the Cu_2S/CdS solar cell $d \simeq 0.1\ \mu m$, $\alpha d \leq 1$ for most λ of interest. For $r = .9$ and $\alpha d = 0.5$, $\eta_c = 0.91$ or 9% losses, while for $\alpha d = 0.25$ $\eta_c = 0.83$ or 17% loss. Hence a factor of 2 change in α for $r = 0.9$

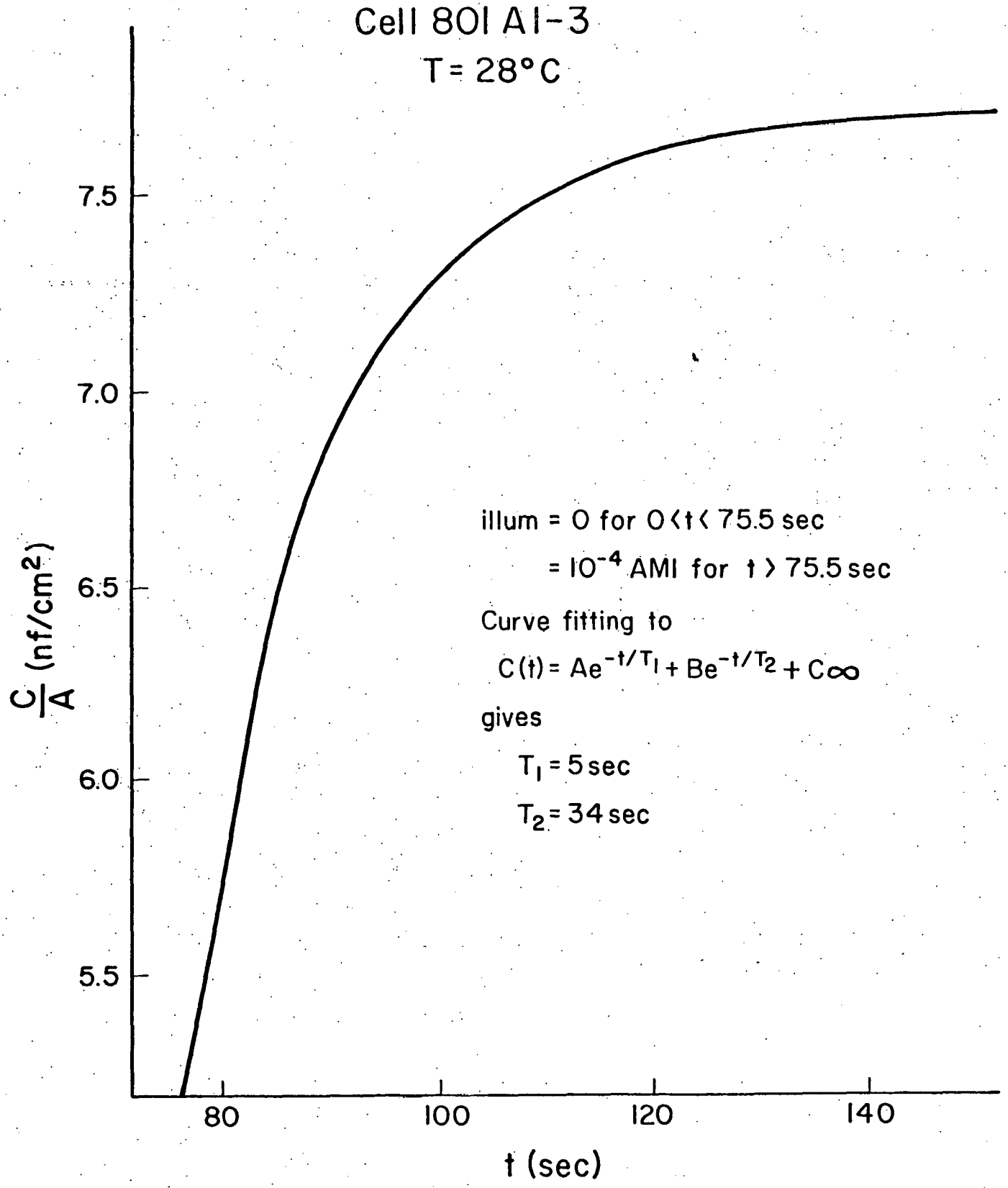

Fig. 9 Transient capacitance behavior for cell 801A1.3.

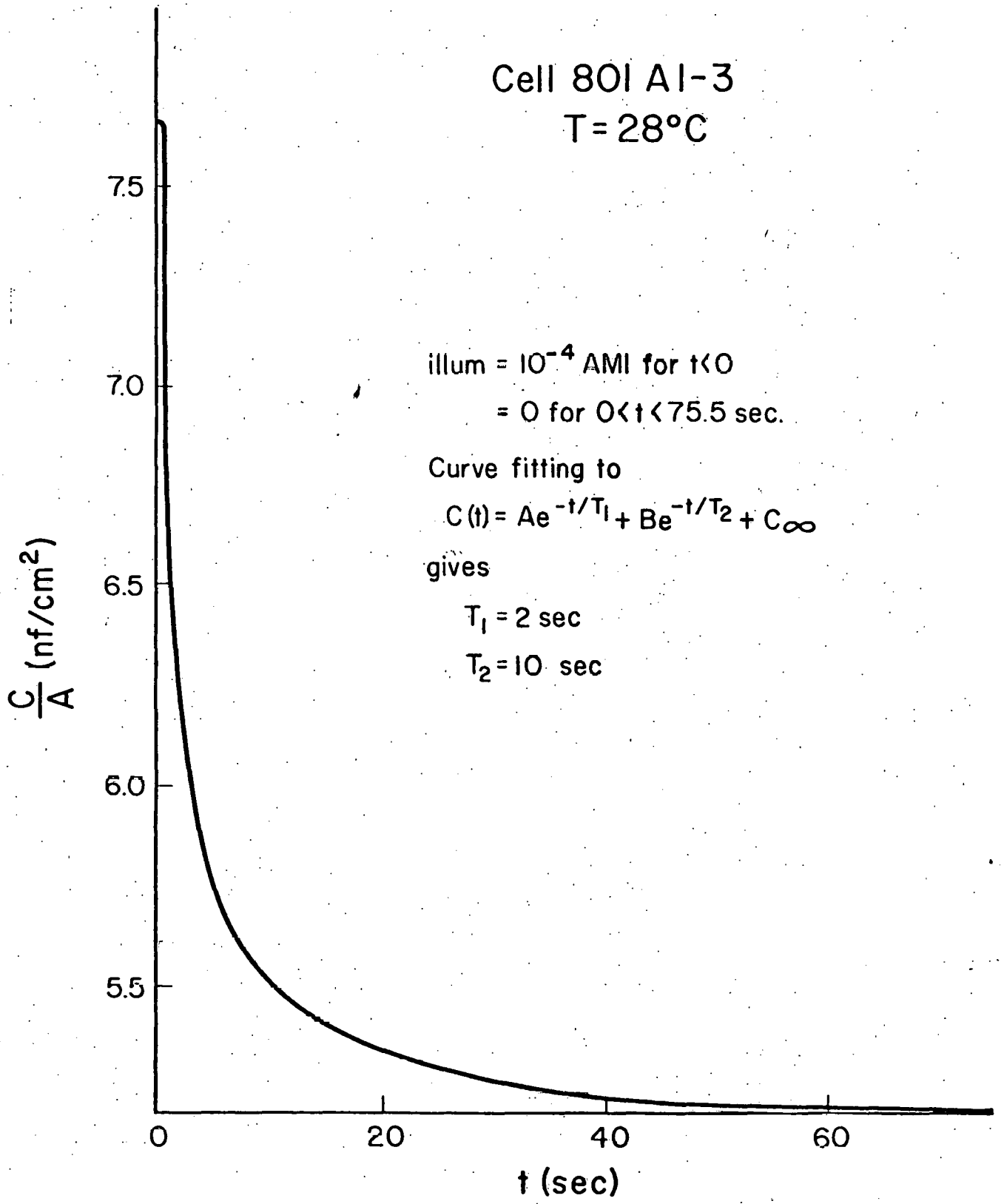

Fig. 10 Capacitance decay for cell 801A1.3.

nearly doubles the losses due to absorption at the back contact. The experimental data on the changes in αd as a function of sheet resistance indicate 25-50% values. This will result in changes in j_{sc} for an AM1 spectrum of 30-40%, over the range of ρ/d values seen in cells (10^3-$10^4\Omega$).

b) Possible effects of tunneling upon cell characteristics

It has been noted previously[7] that there is experimentally an apparent relationship between barrier height Φ and j_{oo} such that j_{oo} exp($-\Phi$kT) at room temperature is nearly constant. The range of measured values was 0.75 - 1.0 eV. The theoretical model neglecting tunneling indicates that the cell current should be given by

$$j = j_{oo} \exp(-\Phi/kT)[\exp qV/kT - 1] - j_{sc}$$

with $j_{oo} = qN_{c2}S_I$ where S_I is the interface recombination velocity and N_{c2} is the effective density of states in CdS.

If tunneling through a narrow portion of the space charge region occurs to the same interface state path we would expect the current to be given by

$$J = qN_{c_2}S_I \exp(-cd') \exp(-\Phi'/kT) (\exp \frac{qv}{kT} - 1] - j_{sc}$$

where Φ' is the new activation energy as determined by V_{oc} vs T measurements and the exp(-Cd') represents the effects of the tunneling on the current. Obviously if the tunneling mechanism is dominant over the interface recombination at the band edge, then a requirement is that $\frac{\Phi'}{kT} + cd' < \Phi/kT$. If we assume that the cd' term is independent of temperature the inequality will only be true for temperatures below the value $T_o = (\Phi-\Phi')/k$ c d'. Hence if tunneling is occuring we would expect it to be dominant at low temperatures.

c) Two dimensional current flow in the CdS/Cu_2S cell.

Results on the analysis of the two dimensional flow problem in relation to the dependence of series resistance on sheet resistance ($\frac{\rho}{d}$), light generated current density, J_L, and grid spacing, L, can be summarized as follows:

With R_sA_1 the lumped parameter for the series resistance due to the Cu_2S layer one has in the active (3rd) quadrant

$$\frac{1}{\alpha J_L}\left(\frac{1}{\tanh \ell} - 1\right) \leq R_sA_1 \leq \frac{\rho}{d}\,\frac{L^2}{8}$$

where $\ell^2 = \frac{\alpha J_L\, \rho L^2}{4d}$; $\alpha = \frac{q}{kT}$

for small ℓ

$$\frac{\rho L^2}{12d} < R_sA_1 \leq \frac{\rho L^2}{8d}$$

Fill factor loss due to R_s can be expressed as

$$\Delta FF_{R_s} = \frac{C\, J_L}{V_{oc}}\left(\frac{\rho L^2}{10.3d}\right)$$

where

$$C = \left(1 - \frac{\ln qV_{oc}/kT}{qV_{oc}/kT}\right)/\left(1 + \frac{kT}{qV_{oc}}\right)$$

These approximations hold for fill factors greater than 0.55.

4.4 Encapsulation for Improved Stability

Cells have been selected and a technique developed for sealing the cells behind a sheet of glass. Roof top exposure has been initiated for two mounted cells.

4.4.1 Phase 1 Review of L.S.S.A. Experience

Current reports are monitored as they are issued. The conclusion that an inorganic glass is necessary to provide total hermetic sealing is unlikely to be changed.

4.4.2 Optical Quality Encapsulant

Preliminary depositions have been made by electron beam evaporation from a specially prepared Barium Alumino-Borosilicate glass frit, IEC 9658. Approximately 5 μm thick layers were deposited. The behavior of the cells indicate that the glass is electronically compatable and has good optical transmission but is not providing complete hermetic sealing in its present form. Table 3 shows some of the performance data obtained with these cells.

Table 3

Performance of CdS/Cu_2S cells Coated with 5 μm of Electron Beam Evaporated Glass

Tested under ELH simulation at 83 mW/cm^2 equivalent intensity

Cell #	Date	V_{oc}(V)	J_{sc}(mA/cm^2)	FF(%)	η%	Condition
799A13	1/19/79	0.488	16.0	66.5	6.26	Heat treated 16 hrs./170° CO
	1/19/79	0/489	13.3	69.8	5.48	Glass Encapsulated
	1/23/79	0.494	14.5	72.1	6.24	16 hrs/170° Vacuum
	1/29/79	0.503	13.1	70.3	5.56	Stored in Air
	2/2/79	0.503	12.9	70.1	5.47	Stored in Air
800A13	1/19/79	0.474	15.5	66.9	5.93	Heat treated 16 hrs/170° CO
	1/19/79	0.473	13.0	66.8	4.93	Glass Encapsulated
	1/23/79	0.481	14.0	72.1	5.84	16 hrs/170°C Vacuum
	1/26/79	0.490	12.6	70.9	5.28	Stored in Air
	2/2/79	0.493	11.6	69.3	4.78	Stored in Air

The two cells put out for roof top test are 695.B13 and 688.A11. They were in storage since June 1978. At that time they had the following electrical characteristics:

Cell	V_{oc}	J_{sc}	V_{mp}	J_{mp}	FF	EFF	RS	GSH	J_L	J_o
695.B13	.473	20.9	.344	17.89	62.3	7.39	3.556	4.396	21.23	23.23
688.A11	.523	19.8	.399	18.2	69.9	8.71	3.01	7.67	19.9	3.44

These cells after retrieval from storage (11/18/79) were cleaned in trichloroethylene and tested for possible degradation during storage. Following results were obtained.

Cell	V_{oc}	J_{sc}	V_{mp}	J_{mp}	FF	EFF	RS	GSH	J_L	J_o
695.B13	.486	18.65	.366	15.79	63.8	6.96	3.247	4.698	18.93	12.461
688.A11	.530	18.11	.401	16.06	67.1	7.76	3.686	2.249	18.26	2.348

The encapsulation of the cells were made in several steps. These steps are given below:

- Setting of the insulator tab on the copper plate
- Bonding to the copper plate with silver filled epoxy
- Setting epoxy in the laminator. 30 min. 190°C in vacuum followed by 1 hr. 190°C in H_2 + Ar atmosphere. Tests performed showed unstable current-voltage characteristics.
- Spreading of the potting compound on the copper plate
- Mechanical clamping of the glass plate
- Vacuum heat treatment 16 hrs. 170° 10 μm Hg
- Painting of a window on the glass plate to eliminate light pipe effects.

The glass plate used is Corning 757 and the potting compound is a silicone semi-gel which does not set hard (Elastomeric) made by TRANSENE Corp. It is possible that the potting compound had exceeded its recommended shelf life.

Tests were made to find out possible degradation of the glass and the potting compound under the influence of temperature and UV exposure. The transmittance of the glass/potting compound/glass sandwich structure was measured before and after heating in air at 170°C for 72 hrs. No change in transmission was observed. The transmittance was also unchanged after 6 hours of exposure to UV (43 mW/cm^2). This sandwich structure is exposed to the atmospheric agents along with the encapsulated cells to monitor the possible long term degradation of the optical properties. The glass cover did not have an AR coating.

During roof top exposure the cells are shorted. The changes on the electrical parameters are measured periodically. The results obtained to date are presented in Table 4.

Table 4

Behavior of Cells Under Roof Top Exposure

Cell # 688.A11

Date	V_{oc}	J_{sc}	V_{mp}	J_{mp}	FF	EFF	RS	GSH	J_L	J_o	Comment
11/18	.530	18.11	.401	16.06	67.1	7.76	3.686	2.249	18.26	2.348	Retest after storage
11/20	.502	20.16	.356	17.72	62.3	7.60	4.614	2.394	20.38	7.754	Initial in Package
11/21	.506	20.31	.367	17.56	62.7	7.76	4.132	3.661	20.62	6.505	Retest
11/27	.510	20.00	.381	17.32	64.7	7.95	3.484	3.685	20.26	5.460	Retest
01/9	.524	19.61	.397	17.17	66.3	8.21	3.324	3.112	19.81	3.151	Retest
01/24	.525	19.29	.399	16.93	66.7	8.14	3.300	2.959	19.48	2.990	Retest

Cell # 695.B13

Date	V_{oc}	J_{sc}	V_{mp}	J_{mp}	FF	EFF	RS	GSH	J_L	J_o	Comment
11/18	.486	18.65	.366	15.79	63.8	6.96	3.247	4.698	18.93	12.461	Retest after storage
11/20	.473	20.53	.333	17.59	60.3	7.06	4.377	3.899	20.88	23.500	Initial in package
11/21	.476	21.20	.362	17.82	63.9	7.77	2.517	5.875	21.52	20.593	Retest
11/27	.490	20.30	.379	17.59	67.0	8.03	2.325	3.908	20.49	11.917	Retest
01/9	.497	19.25	.381	16.77	66.8	7.70	2.762	3.389	19.43	8.697	Retest
01/21	.499	18.72	.383	16.17	66.3	7.46	2.841	3.747	18.92	7.738	Retest

Further tests will be performed using different potting compounds. Four candidate compounds were obtained from Dow Corning:

- Silicone dielectric gel Q3-6527 A & B
- Sylgard 184 resin
- An experimental compound QL2577

Specifications for the first three compounds are available. However, no specifications for the experimental compound QL2577 were given by the manufacturer although Dow Corning personnel have indicated that the QL2577 might be the best material for our purpose.

The compounds Q3-6527 A & B and Sylgard 184 have a major drawback which is the curing inhibition in the presence of sulfur compounds.

5. Future Developments

Solutions to the problems revealed in the formation of planar Cu_2S layers will be sought by detailed analysis of the structure and properties of these layers. A procedure for rapidly evaluating each CdS substrate by making a standard textured cell is being designed.

Further studies of the junction morphology in the (CdZn)S/Cu_2S cells are expected to provide direction to the substrate growth and cell production efforts in Task 2.

Progress is being made and will be continued during the next quarter on the development of a quantitative measure of photoluminescent character.

The monitoring of the roof top cells will be continued.

6. REFERENCES

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