Light-Triggered Thyristors for Electric Power Systems (Phase 2)

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Research Project 669-2

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ABSTRACT

This report marks a milestone in the development of light triggered thyristors suitable for HVDC applications. Three devices were constructed with 5, 4, and 2 amplifying stages respectively with several sub-variations. Of these the 4 amplifying stage GE3 type D device and all variations (A, B & C) of the two stage GE4 design proved sufficiently reliable for a one for one replacement of the normal, electrically triggered 2.6 kV HVDC cell. These devices proved the usefulness of the n^+ alignment band, a feature design to ensure even turn-on, and the interrupted n^+ metal, a feature to enhance rapid spreading away from the initial turn-on line.

Important device characteristics other than a typical 160A/μsec or better di/dt at 105°C and 1800 volts include the following: (1) typical forward breakdown voltage of 2900 volts; (2) typical reverse breakdown voltage of 3100 volts; (3) dv/dt capability of 2000V/μsecond to 2200 volts; (4) forward drop at 105°C, 1000 amperes of 1.3 volts and, finally, (5) a typical photo threshold of 10 to 20 nanojoules of incident photo energy. Surge capability and other device ratings are similar to the original electrically fired device.

It is also significant that both the fabrication and packaging of these devices took place in a production facility and that the light triggered thyristor could be fabricated with the same process, apart from the extra sensitivity etch, as the regular electrically triggered device. Further, the package is a relatively simple one which requires only a few cents worth of extra parts.

EPRI PERSPECTIVE

PROJECT DESCRIPTION

A key factor in gaining the benefits of high-voltage, direct-current (HVDC) transmission systems is the availability of simple, inexpensive converter valves. Use of electrically fired thyristors has provided the first step in this direction. Substitution of light-fired thyristors will be a major added step in the evolution of simpler, more reliable, and less expensive valves.

This study, EPRI Research Project (RP) 669-2, was preceded by RP669-1, which established the feasibility of a 2.6-kV, 1000-A, light-fired thyristor. EPRI Report EL-932 issued in November 1978 documents the success of this effort and defines the direction of continued research. RP669-2 describes the follow-up effort in which light-fired thyristors were fabricated and packaged in a production facility.

At the conclusion of RP669-2, a third and final report will be issued to document continuing work with the goals of: (1) higher voltage rating per thyristor, (2) further simplification of the protective electronic circuitry, and (3) fabrication of a panel for installation in an existing HVDC converter currently using electrically fired valves.

PROJECT OBJECTIVE

The objective of RP669-2 was the development of a commercially acceptable 2.6-kV, 1000-A, light-fired thyristor. This objective having been met, the next phase of this project will encompass: (1) development of an integral 5-kV, light-fired thyristor, (2) development of self-protection features that would eliminate most of the

remaining external circuitry, and (3) installation of a 10-voltage-level panel using 2.6-kV, light-fired thyristors with ZnO protection in an existing HVDC system now using electrically switched devices.

PROJECT RESULTS

The work described in this report has brought the industry closer to the use of light-fired thyristors in HVDC converters. The fabrication and packaging of 2.6-kV, 1000-A thyristors in a commercial facility provides the devices and the confidence to prepare for a field installation to replace a panel of electrically fired thyristors. Development of an improved redundant light-firing system using laser diodes gives added reliability to the trigger circuit. In addition, some of the work reported herein will be used as groundwork for the next phase of the project, which will provide further advances in voltage level and reliability.

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SUMMARY

INTRODUCTION

The work described in this report is a continuation of the Light Triggered Thyristors for Electric Power Systems program initiated by EPRI in 1976 with the ultimate objective of developing a directly light triggered thyristor for electric utility application. The earlier program funded under EPRI Contract RP669-1 is described as Phase I and the current program, funded under EPRI Contract RP669-2, is denoted as Phase II. In this section an introduction to the light fired thyristor program will be given followed by a brief review of the results of Phase I and a summary of the more important results of the activities of Phase II.

BACKGROUND

The object of this program is to develop a light triggered high power thyristor of the type useful in electric utility applications and to ultimately demonstrate it in a utility application. One example of an intended use is in solid state High Voltage Direct Current (HVDC) conversion stations. These stations convert large blocks of power from 60 Hz to dc and back again for long distance transmission or asynchronous ties between utility systems. The thyristor development centers on an existing high power electrically triggered thyristor characterized by the diameter of the silicon wafer which is 53mm (~2 inches). This device is presently rated at 2600 volts and 1000 amperes and is used in HVDC stations currently under construction. This thyristor is being redesigned such that it is triggered into conduction by a beam of light instead of the conventional conducted gate current. In addition, it is intended to apply new thyristor gate designs to obtain a measure of internal cell protection. This internal self-protection

is intended to reduce the probability of device failures when triggered into conduction either by excess anode voltage or by an excessive rate of rise of applied anode voltage. The new light sensitive device will be housed in a modified press pak production package. Suitable modifications to the package are being made to permit entry and registration of the trigger beam of light, with the package installed in a typical HVDC module.

The highly interdependent nature of the thyristor characteristics and the final HVDC system architecture requires a thorough knowledge of potential light sources and the fiber optics used to channel and control the light beam. As a result, review of the present state-of-the-art in applicable light sources and fiber optics or coupling media is required. Final device tests with a suitable light source are being run to characterize operational parameters important to HVDC system operation. Particular emphasis is placed on testing those cell parameters currently specified for HVDC module operation.

The additional goals of the Phase II efforts ultimately involve a transfer of the thyristor process and design capability into production, the fabrication of a production package and testing of the light fired devices in a two thyristor assembly.

PHASE I HIGHLIGHTS

Phase I efforts were expended in several major areas - design and fabrication, device testing, light source and light pipe assessment and, finally, package modification. In the design phase, two computer programs were developed, one to predict photo-current in the thyristor for any light source and for any thyristor forward blocking voltage and one to shape the turn-on line periphery for optimum di/dt. In addition, a number of dv/dt correction factors were identified to increase our ability to predict and design to a specific dv/dt capability. In fabrication, three runs of light fired devices were made with several sub-variations in design, all with a relatively high yield of testable

devices. In device testing, xenon flash lamps, cw YAG lasers, solid state lasers and LED's were all used to turn-on the thyristor. Turn-on threshold incident photo-energies at blocking voltage of 100 volts ranged from 10 to 30 nanojoules with threshold dc gate power levels from 5 to 10 milliwatts. Measurements proved dv/dt capability to be within 10% of the design point of 2000V/μsecond at 105°C. Forward drop, leakage current and blocking voltage were comparable to the original electrically fired device while delay time and turn-on time were somewhat reduced.

Di/dt capability varied widely as a function of snubber design and operating temperature. Room temperature turn-on tests show di/dt's from a low value of tens of amperes per microsecond to thousands of amperes per microsecond. However, elevated temperature tests ultimately degraded the device blocking capability, most often temporarily, but occasionally catastrophically. Tests made in a hybrid circuit configuration indicated that the slower turn-on at higher temperatures generated excessive turn-on line temperature excursions during turn-on.

Packaging and light pipe - light source assessment were begun. Several prototype packages with axial package entry were considered and several were successfully fabricated. In the light source - light pipe area low loss glass fibers coupled to solid state laser light sources were tested satisfactorily as triggering systems.

For a more detailed account of Phase I, the Phase I Final Report can be consulted.

PHASE II HIGHLIGHTS

This section of the report summarizes progress in developing a light fired thyristor from the conclusion of Phase I under Contract RP669-1 to the end of Phase II. The major effort of this period was the development of three

new series of light fired thyristors with integrated light fired amplifying stages. These designs evolved from a three pronged effort which included a concerted series of experiments to zero-in on the high temperature di/dt problem, the evolution of a turn-on model capable of comparing new designs and finally the selection and detailed analysis of the new designs. To help evolve new thyristor designs some method had to be found to predict temperature excursions in turn-on. This was a difficult task and for practical reasons a computer model was developed. The initial turn-on region was described by four linear circuit elements and one non-linear one. Temperature and turned on area are calculated in a consistent manner using a simple expression describing the spreading of the on-region from a pre-set turn-on area. With this model designs with up to 19 amplifying stages can be analyzed for turn-on properties including the essential one of temperature excursion. By the end of the first quarter of Phase II thyristor designs with one to six stages had been investigated theoretically.

The culmination of the foregoing efforts was the design of three series of devices, the first series designated EPRI-GE2A, B and C; the second series designated EPRI-GE3A, B, C and D; and the third series designated EPRI-GE4A, B and C. The GE2 series has 5 amplifying stages, the GE3 series has 4 amplifying stages and the GE4 series has two amplifying stages. The devices were all designed to have a gate sensitivity of 2 to 5 milliamperes (d.c.) and a dv/dt capability of 2000V/μsecond. They were all designed in accordance with the computer program results so that they theoretically have a suitably small temperature excursion in the light sensitive gate stage under di/dt test conditions. Two design improvements were incorporated into some of the designs. For example, all "C" designs have an "n^+ alignment band". This is believed to be a new contribution to thyristor design as is the "interrupted n^+ emitter metallization" also possible in some of the sub-variations. These designs and calculations of their expected properties were the main accomplishments of the second quarter of Phase II.

In the third quarter the major effort was the manufacture and test of approximately 40 devices. These tests were chiefly concerned with elevated temperature di/dt capability which was the single shortcoming of the EPRI-GE1 light fired thyristor. In order to perform meaningful di/dt tests at and above HVDC stress levels, a high power di/dt tester was designed and built at CRD. This was used on 17 devices including a number of test devices other than the EPRI-GE devices. Results were encouraging but inconclusive with a few devices passing the HVDC stress tests at elevated temperature. Additional devices were tested at SPCO in Philadelphia which now has the capability of testing LTT devices.

In addition to these tests, 15 devices were oven tested at 100°C with a .5μfd, 10 Ω snubber with nearly 100% survival. Unfortunately, this particular set-up could only be used to 25 Hz. The second major activity of this quarter was the evolution of three prototype packages and some hardware for inserting the light pipe into the package through the heat sink assembly. One radial entry package and two axial entry packages were considered. In both the oven tests and di/dt stress tests performed in the third quarter, devices were physically if not electrically degraded by a new device failure mode which was called "local channel burn" and ascribed possibly to surface arcing. This prevented "true" di/dt capability from being reached and necessitated experiments and theoretical analysis to determine the failure mode. The cause of this failure mode was later determined to be excessive interstage current flow in the p base layer of the thyristor.

The experiments and theory done to pinpoint the cause of the channel failure plus the fabrication of over 50 new devices comprised the major work effort of the fourth quarter. New devices consisted of the best of the 10 device types (EPRI-GE2A, B, C, etc.) fabricated in the second quarter and tested in the third quarter. In addition, 10 L1A and L1B test devices were fabricated, these devices being free of channel failure but prone to normal di/dt failure.

The experimental analysis of the Run 1 device channel arcing problem consisted of a series of measurements of interstage or "channel" voltage turn-on transients measured between successive stages during turn-on. It was found that interstage voltages of the order of 100 volts and more occurred during high voltage turn-on which, with the sharp edge of the n^+ alignment band, caused the surface arcing.

Theoretical analysis also predicted sizeable interstage voltage transients but not accurately enough to be confidently used in further designs. This led to a re-examination of the turn-on model and a new attempt at predicting initial current flow in light fired thyristor turn-on. A charge control model normally used in transistor modelling and occasionally in thyristor modelling[2,3] was expanded to apply to light fired as well as electrically fired thyristors[4]. We now have a model which, for the first time, is able to accomodate the essential differences between a light fired and or electrically fired device - namely, that in a light fired device both the n and p bases receive gate current whereas in an electrically fired device only the p base is gated. Initial results of the model are encouraging up to about 10 amperes where two dimensional charge spreading effects, not contained in the present model, dominate the turn-on process.

Preliminary tests on 15 of the Run 2 devices showed not a single device with any channel arcing failures after being tested at 25°C and 100°C with a .5μF, 10 Ω snubber. This was expected and meant that the di/dt tests that were the main effort of the fifth quarter would not be compromised by surface arcing failure.

During the fifth quarter the major effort was the di/dt testing of the Run 2 devices. This testing was of two sorts. The first we termed "integrated device testing" where the light fired device is tested by itself. The second is the so-called "hybrid" approach where a small light fired device is connected through a series resistance between the anode and gate of a regular electrically fired device. For the small light fired device we used the inner stages (280 mils in diameter) of the EPRI-GE Run 2 devices. For the electrical device, which

carried the main current, we used the original electrically fired 53mm HVDC device used in present generation HVDC valves.

The results of both types of tests were successful. In the integrated tests (no separate gate device), approximately 85% of the type GE3 and GE4 devices passed the one minute, minimum HVDC stress test as did about 60% of the type GE2 devices and 75% of the type L1 devices. This result indicates that the GE3 and GE4 designs are suitable, at this point, for HVDC applications at least to the extent that they pass all of the same HVDC screening tests as the original electrically fired device. However, it should be stated here that the best designs, the EPRI-GE3 and GE4 series, still have a di/dt distribution that is below that of the electrically fired device and will ultimately be less reliable under stress conditions. It appears that the typical one minute device di/dt capability will be about 80% of that of the electrically fired device and about 4 times rather than 5 times the minimum HVDC di/dt screening level. This implies that higher voltage devices may require an additional development effort.

The hybrid or "separate gate" di/dt tests were even more successful. In this realization of the direct light firing system, the amplifying stages of the integrated light fired device are incorporated into a separate device so that a two watt series current limiting resistor can be inserted between the cathode of the light fired device and the gate of the electrically fired main device. Since the anode of the light fired gate device is connected to the anode of the main device, all of the normal advantages of direct light firing are preserved. What we pay for is a separate package and the small device (perhaps, ultimately, 150 to a 3" wafer). What we gain is chiefly overall capability, reliability, and system mechanical flexibility as well as an overall yield improvement. Actual di/dt test results showed that in a separate firing scheme, the di/dt capability of the devices would be increased to at least the limit presented by the main electrically fired device. At first the HVDC stress tests were done at 160A/μsecond. When no failures occurred, this was increased until the present

test circuit limit of 425A/μsecond was reached. Every light fired gate passed this test as well as 80% of the electrically fired devices used as the main stage. This result indicated two things: first that the light fired device will have an extremely high reliability if the initial turn-on current from circuit and stray capacitance can be limited, and second, that the part of the turn-on stress absorbed in the separate gate device lowers the turn-on stress of the main device which in turn is responsible for perhaps as much as a 50% increase in its di/dt capability.

Finally it was decided to produce a further run (Run 3) of the EPRI-GE4 device type as a supply for packaging, testing and possible application. Fabrication of an additional 20 EPRI-GE3 type devices was also begun using a slight mask modification to relieve a particularly high channel voltage transient between the second and third amplifying stages. It was considered possible that with this mask change that the four amplifying stage GE3 type device would be the most successful integrated light fired device. In fact it is the GE3D option with the "interrupted n^+ metallization" which provided the most successful four amplifying stage device.

During the sixth quarter three major activities were undertaken. The first of these was the fabrication and partial testing of a number of Run 3 devices. These consisted of approximately 20 type GE3D devices and 20 type GE4B devices. A further quantity of type GE4B devices was still in process. The partial testing refers to testing on a subset (10) of these devices which were taken past the critical di/dt test at 160A/μsecond, 1700 volts. None of these devices failed on di/dt which tends to confirm the success of our 2600 volt design(s). A second major effort was undertaken in the device packaging area with the packaging of a number of devices which was to be followed, during the next quarter, with packaged device tests in single and double level stacks. A

third effort involved generating a rather ambitious outline of some of the possible technical paths to a 5000 volt, integral light fired device and some possible VBO self-protected thyristor structures. Many of the proposed methods are believed to contain patentable concepts and will not be discussed in detail until they are reduced to practice. These methods and the general thyristor design philosophy will be discussed, however, in general terms in the next sub-section of this report which deals with the goals of Phase III.

The final quarter of Phase II was devoted to tying up loose ends. All of the untested Run 3 devices were di/dt tested with 100% yield at twice the test HVDC stress level. Devices were packaged and successfully tested in the package. Tests of two devices in series were done with similarly successful results. In this case success meant suitably small differences in delay time.

SUMMARY OF PHASE II AND GOALS FOR PHASE III

From the beginning of the light triggered thyristor program it has been clear that our goals were very ambitious - in short, to develop a directly light triggered device which would be sufficiently rugged to serve as a one-for-one replacement for its electrically triggered counterpart. Beside the fundamental problem of over a thousand-fold smaller available triggering energy, we had to deal with triggering system (light source and light pipes), package and process modification. These problems were gradually overcome during Phase I and II so that we can now package a 2600 volt, 1000 A, HVDC grade thyristor which can be triggered on with only 20 nanojoules of incident photo energy. Despite this low gate energy, we can, with the help of a partially optimized amplifying gate design, achieve all of the dv/dt capability and 80% of the di/dt capability of the original electrically fired device. This device has already passed all HVDC tests which the electrically fired device needs to meet and with essentially equal yields. The device in all but its earliest production runs was manufactured not at GE's Research and Development Center, but on production equipment at SPCO in Collingdale. This fact makes this device an immediately marketable device.

Part of the original goal of RP669 was to develop devices immune to certain types of catastrophic failure, the most damaging being known as VBO (Voltage Break Over). VBO is a term describing the turn-on of a thyristor resulting from device voltage exceeding the avalanche breakdown voltage. Turn-on is extremely localized and occurs at perhaps 2.5 times the normal turn-on voltage. The combination of small area and high available system energy results in a melting of the silicon and a shorted junction. During the course of Phase II approximately 30 thyristors were fabricated with a special VBO region whose location would allow the amplifying stages to somewhat alleviate the VBO turn-on stress. Experiments on these devices and on a dozen 5 kV devices with the EPRI-GE4 design led to the development of a concept we have called "controlled turn-on".

In the 5 kV light triggered thyristor the problem is degradation of di/dt capability. In essence the problem is that higher voltage gives higher system di/dt but the device has inherently smaller di/dt capability. For example in going from a 2.6 kV device to a 5 kV device system di/dt doubles but device di/dt capability goes down a factor of more than two and as much as four.

With "controlled turn-on" initial current flow is controlled in the device. Turn-on losses are larger but spread out over a much, much larger volume of the device so that excess thermal excursions are avoided. This, at least, is the theory that we will be investigating in Phase III which, if successful, will result in a practically fail-safe 5 kV HVDC type light triggered thyristor.

Section 2

ANALYSIS OF PHASE I DEVICE PROBLEMS

BACKGROUND

During Phase I we developed a two amplifying stage light triggered device with good sensitivity and good dv/dt capability. Our success in this trade-off, essentially between gate sensitivity and noise sensitivity, was the result of perfecting design equations and pre-turn-on models of the device. What we could not anticipate were the dynamic characteristics resulting from about a 100 fold smaller gate stage. Late in Phase I high temperature di/dt tests revealed an apparent inability of the very sensitive light gate stage of the device to withstand repeated turn-on. Evidently the initial power dissipated in the short ($\sim$1/10 as long as in the electrically gated device) gate stage turn-on line led to unacceptable temperature excursions in the turn-on region estimated at about 80°C. The symptoms were a slow increase in turn-on delay time and a gradually increasing leakage current followed by thermal runaway and a loss of blocking capability. The level of leakage current at which total blocking capability was lost was low enough to suggest that it was indeed the small gate stage which was being degraded. Our difficulty was that, if we made the gate stage larger we would lose our required gate sensitivity.

Perhaps the best way to summarize light triggered device design is to observe that high input light intensity (energy per unit area) allows us to design with very high dv/dt capability while high total input light energy allows us to achieve devices with high di/dt capability. Neither high intensity nor high energy is easily achievable with inexpensive, highly reliable, solid state sources. Our answer was to use solid state laser sources whose intensity, at least, was sufficient for getting high dv/dt capability and to go to an extra internal amplifying stage to try to offset the small total energy available

in the laser pulse. Since there existed no experience in multi-amplifying gate thyristors, it is not surprising that we should observe some rather different device failures.

The remainder of this section is devoted to a description of the experiments, the device analysis and the modelling undertaken to understand multi-amplifying stage device behavior and to improve future designs. We first describe elevated temperature di/dt experiments perhaps more accurately described as elevated temperature stability tests. These results are analyzed and then a computer model is proposed, solved and results presented which tend to confirm the hypothesis of an 80°C temperature excursion in the gate (first) amplifying stage of the EPRI-GE1.

EPRI-GE1 TURN-ON EVALUATION

The design of the EPRI-GE1 is fully described in the Phase I Final Report. Briefly it is a two amplifying stage device with gate threshold levels of 5mA and 50mA with a main stage sensitivity of about 250mA. About 50 devices were fabricated and tested. Figure 2-1 is a photograph of the EPRI-GE1 device. As described in the Phase I report, device capability met or exceeded specifications in every characteristics except high temperature turn-on.

To investigate this shortcoming new turn-on experiments were evolved to try to isolate the turn-on action of the gate and pilot amplifying stages, the presumed weak links in high temperature turn-on. Figure 2-2 shows the test circuit. Incidentally, a version of this circuit can be used to extend thyristor turn-on capability. The major purpose of the test circuit shown in Figure 2-2(a) was to be able to examine di/dt in the gate and pilot amplifying stages with some degree of control over the power dissipated in the light fired thyristor under test. This thyristor was connected at K1 and A1 with the main thyristor region bypassed as shown in Figure 2-2(b). Instead, the main thyristor stage was replaced by the regular electrically fired 2600V, HVDC cell,

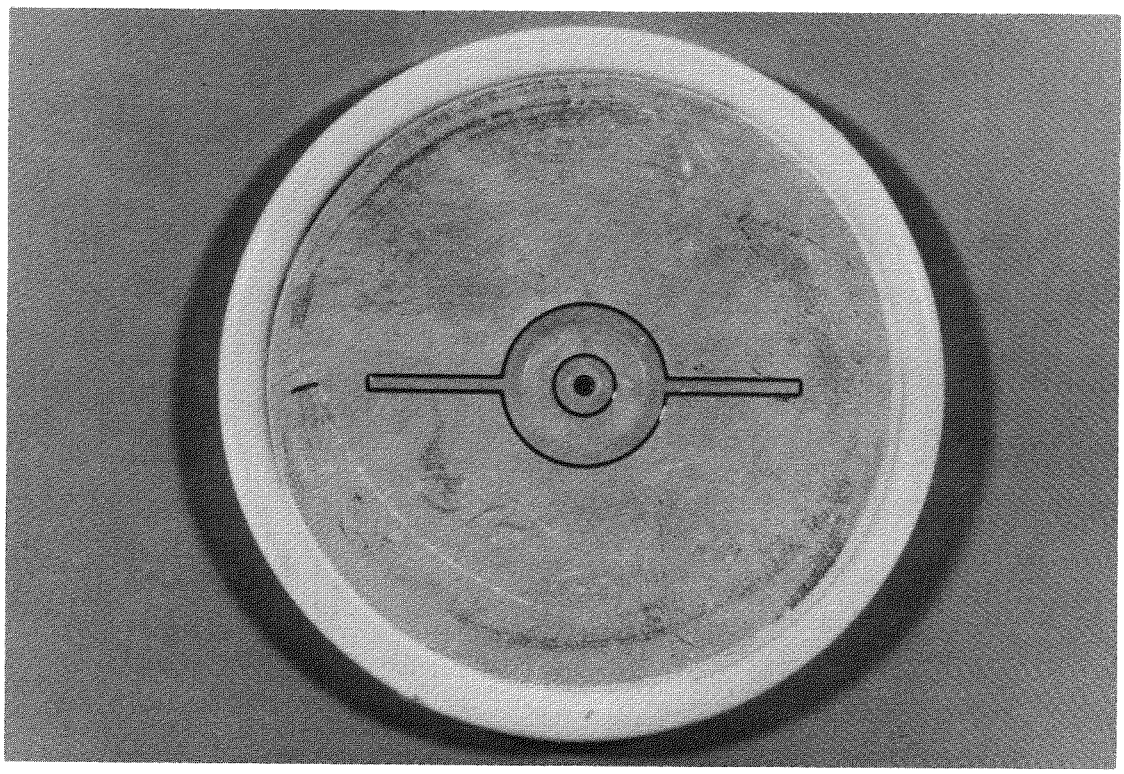


Figure 2-1: Photograph of the EPRI-GE1
Light Triggered Thyristor.

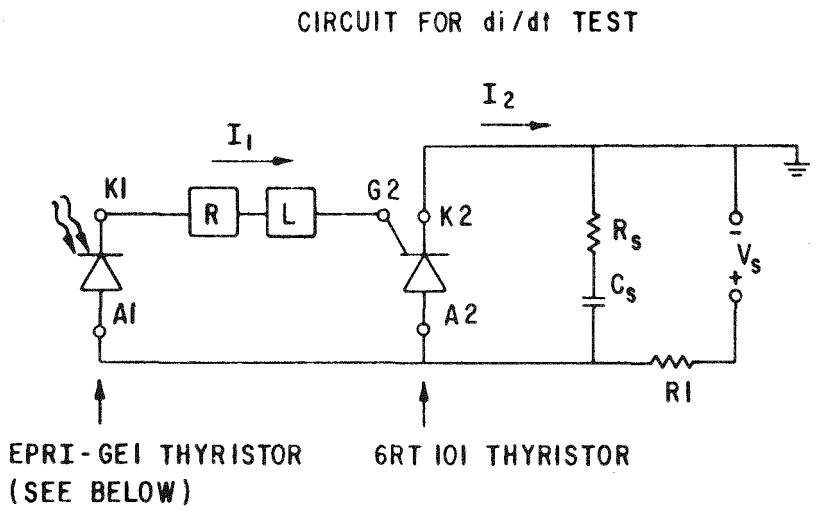
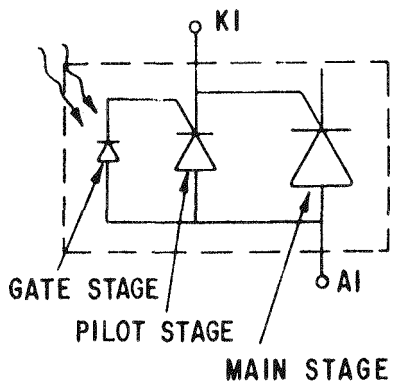


Figure 2-2(a): The test circuit for the inset photographs in Fig. 2-3 and 2-4. Incident photons trigger the light sensitive device at A1-K1. Current I_1 subsequently triggers the main device which was chosen to be the regular 6RT101 electrically fired thyristor.



ELECTRICAL ANALOG OF THE EPRI-GE1 THYRISTOR SHOWING THE PILOT STAGE BEING USED FOR THE CATHODE

Figure 2-2(b): Schematic showing how the main stage of the devices is by-passed in the light fired device to allow us to investigate the inner two stages more accurately.

properly packaged and mounted. All of the elements were put inside an oven whose temperature could be regulated. A series of tests were then performed at different anode voltage, different oven temperatures and with different snubber resistances and different combinations of R and L.

In one of the more significant tests a thermocouple was attached to the thyristor approximately in the center of the pilot thyristor emitter. Turn-on tests were performed from 1200 and 1800 volts at 25, 50 and 70°C oven temperatures with R = 0, 10 or 100 Ω and L = 0. The tests were continued until the thermocouple temperature reading stabilized or exceeded 125°C.

Two typical results are shown in Figure 2-3 and 2-4. Each figure shows the temperature rising above the oven temperature as a function of time, first firing at 1200 volts and then firing at 1800 volts. The photographs included in each figure show the currents, I_1 and I_2, and the voltage, V_{K1-A1} and V_{K2-A2}, across the two thyristors. In all cases, the top trace is the current I_1 (positive downward) and the bottom trace, the current I_2 (positive upward). V_{K1-A1} can be distinguished from V_{K2-A2} as it is slightly displaced vertically and falls off in voltage first.

The higher temperature results show that the best performance in terms of highest stabilized average device temperature was R = 100 Ω, shown in Figure 2-3, in which the 1800 volt turn-on test stabilized at approximately 85°C. For R = 0 and R = 10 Ω, no temperature stabilization was obtained at the 70°C oven temperature although the device operated successfully for several minutes. At 25°C the temperature stabilized for all three resistance values. Note that the standard di/dt stress test is of one minute duration. The stress level is between 2 and 100 times that seen in normal operation.

What was usually observed at that point would be an increase in leakage current and a drop off in anode firing voltage as marked along the curve in Figure 2-4. There, each 100 volt drop marks an increase in leakage current of about 2.5mA.

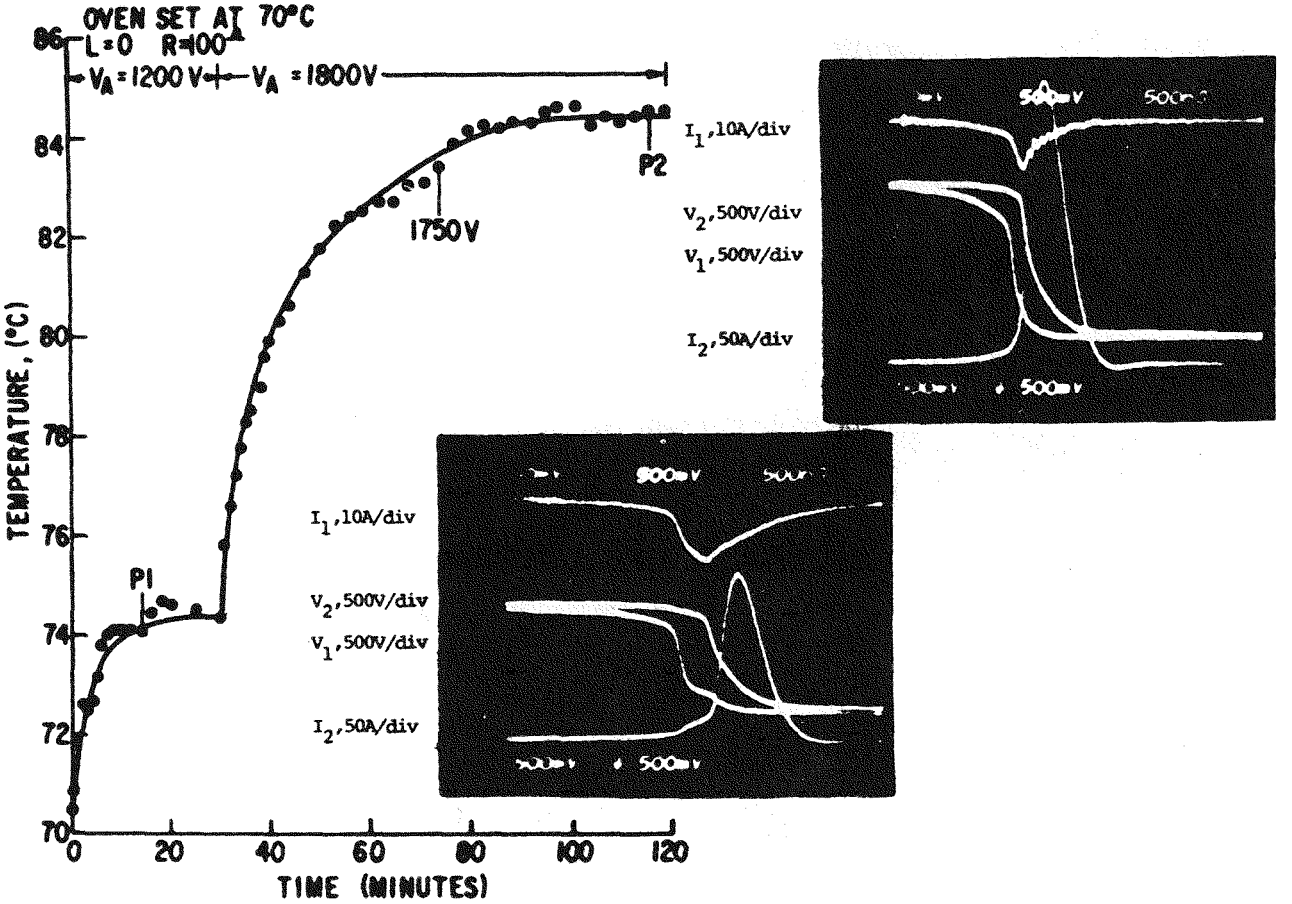


Figure 2-3: Prolonged di/dt test using the test circuit in Figure 2-2. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 70°C. A series resistance of 100 Ω was used. The snubber was .1μf, 1.25 Ω. The time scale is .5μsec/div.

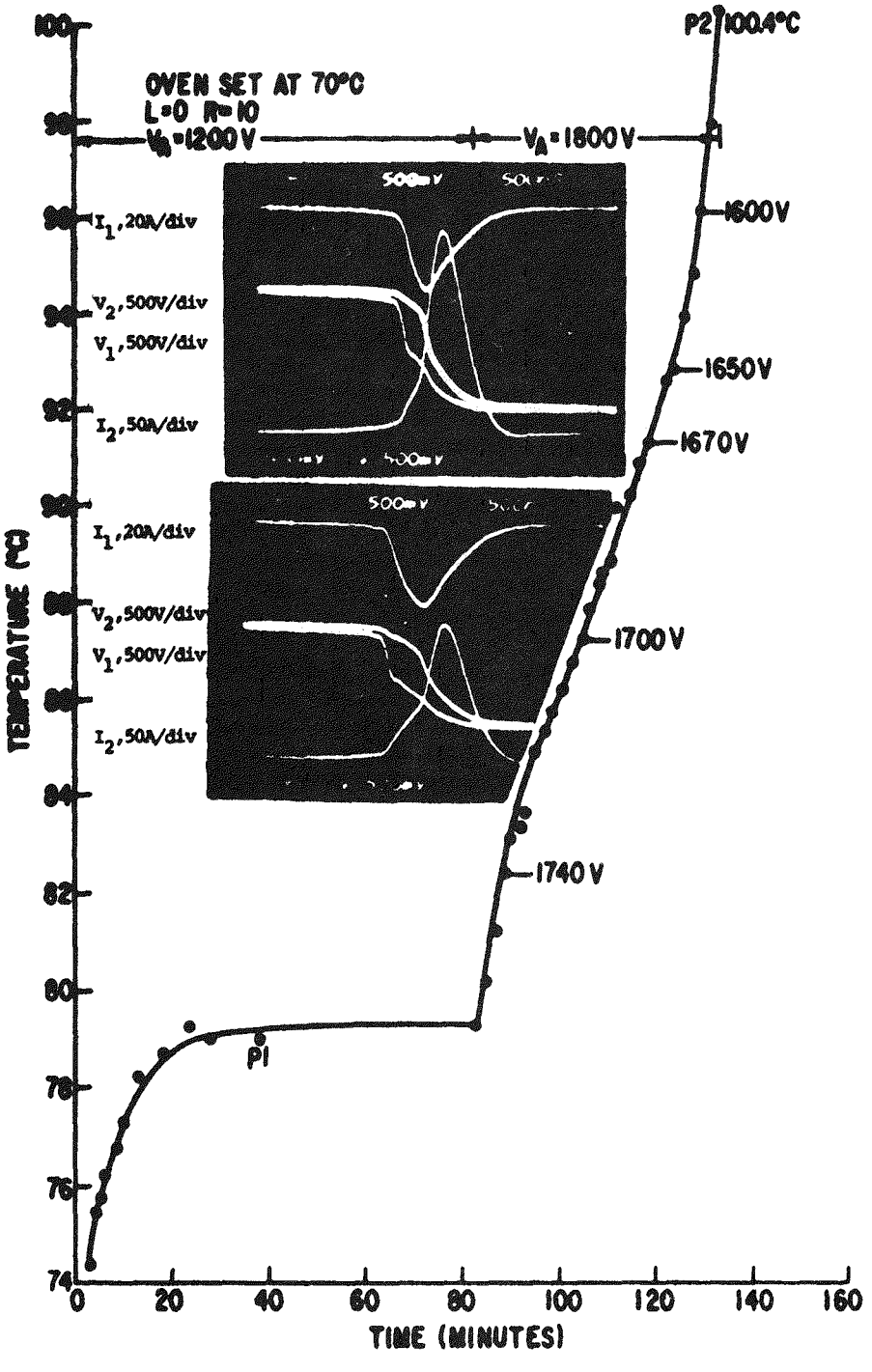


Figure 2-4: Prolonged di/dt test using the test circuit in Figure 2-2. P1 and P2 indicate the points at which the inset photographs were taken. The oven temperature was 70°C. A series resistance of 1Ω was used. The snubber was .1μf, 1.25Ω . The time scale is .5μsec/div.

If the process had not gone too far, the device would recover on removal of the photo-gate pulse and the temperature would fall due to the removal of the turn-on energy dissipation stress. If the process had gone further, it would require a reduction in voltage for the thyristor to recover.

TURN-ON CALCULATIONS

This section deals with the evolution of a turn-on model which is in part determined by the known physics of the device and in part known from previous experimental data. The simplest form of the model is that shown in Figure 2-5. As can be seen, the model explicitly includes the lateral p-base resistances R_G, R'_G, etc., the voltage dependent capacitances C_{G2}, C_{P2} and C_{M2} of the forward blocking (n_{base}-p_{base}) junction and the capacitances C_{G1}, C_{P1} and C_{M1} representing the diffusion capacitances of the $n+$-p_{base} junction. These latter capacitances can be readily calculated or can be determined experimentally from the observed threshold charge required to fire that particular emitter stage. Looking at the model from the gate region to the main emitter, we see first a current source representing the photo-gate current and then three similar blocks depicting the gate, pilot and main thyristor stages of the device. On the right is attached a simple snubber circuit. The main circuit connects to A and K where provision is made for the source supply and a series R-L network to represent the load. The elements of the model which are not as well established are the switches S1, S2 and S3. While we know when, in the turn-on, to close the switches, at the time we did the first calculation we were forced to model the subsequent impedance of the switches by a time dependent admittance of the form given in equation (2-1) below:

$$Y = Y_o + Y_1 (t - t_s) + Y_2 (t - t_s)^2 + \ldots \qquad (2\text{-}1)$$

Y_o models the leakage current. Y_n is identically zero until $t>t_s$ where t_s is the switching time. After t_s, the Y values are constant and selected to fit the observed turn-on. The results shown in Figure 2-6 use only Y_1, all other Y_n being set to zero. The Y_1 values for S_1, S_2 and S_3 themselves were simply selected to match experiment.

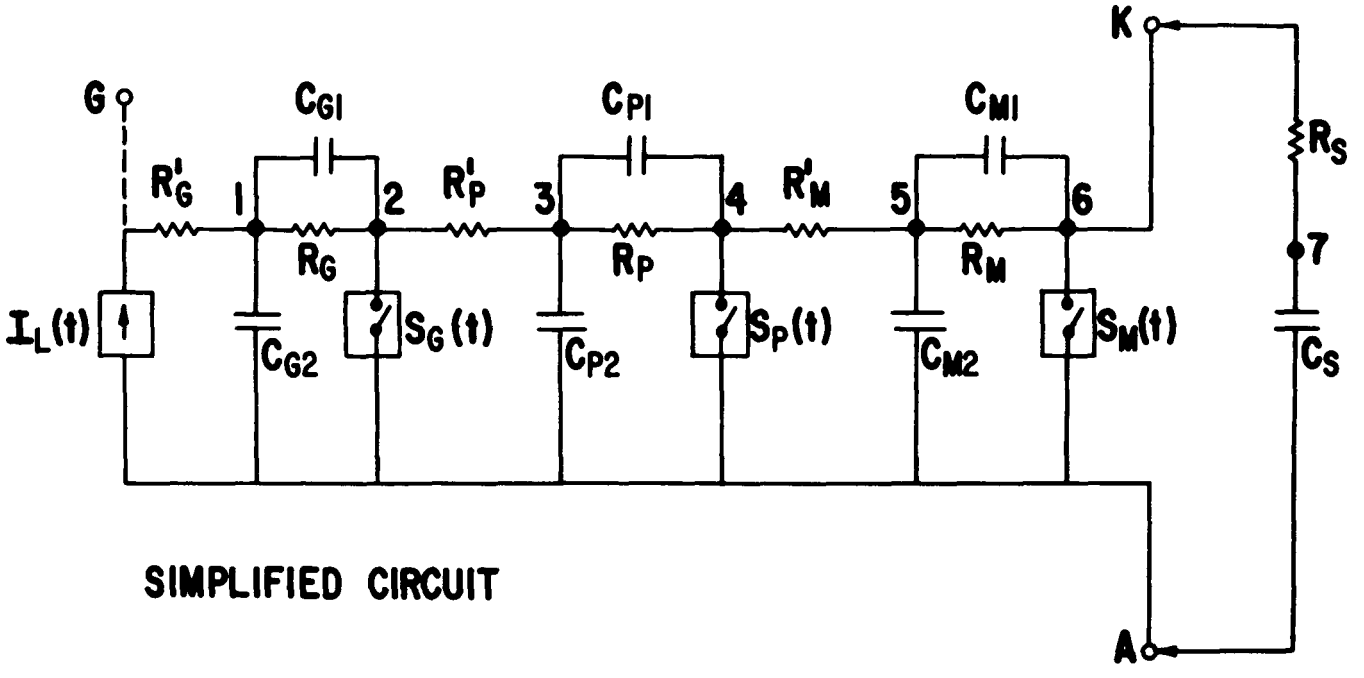
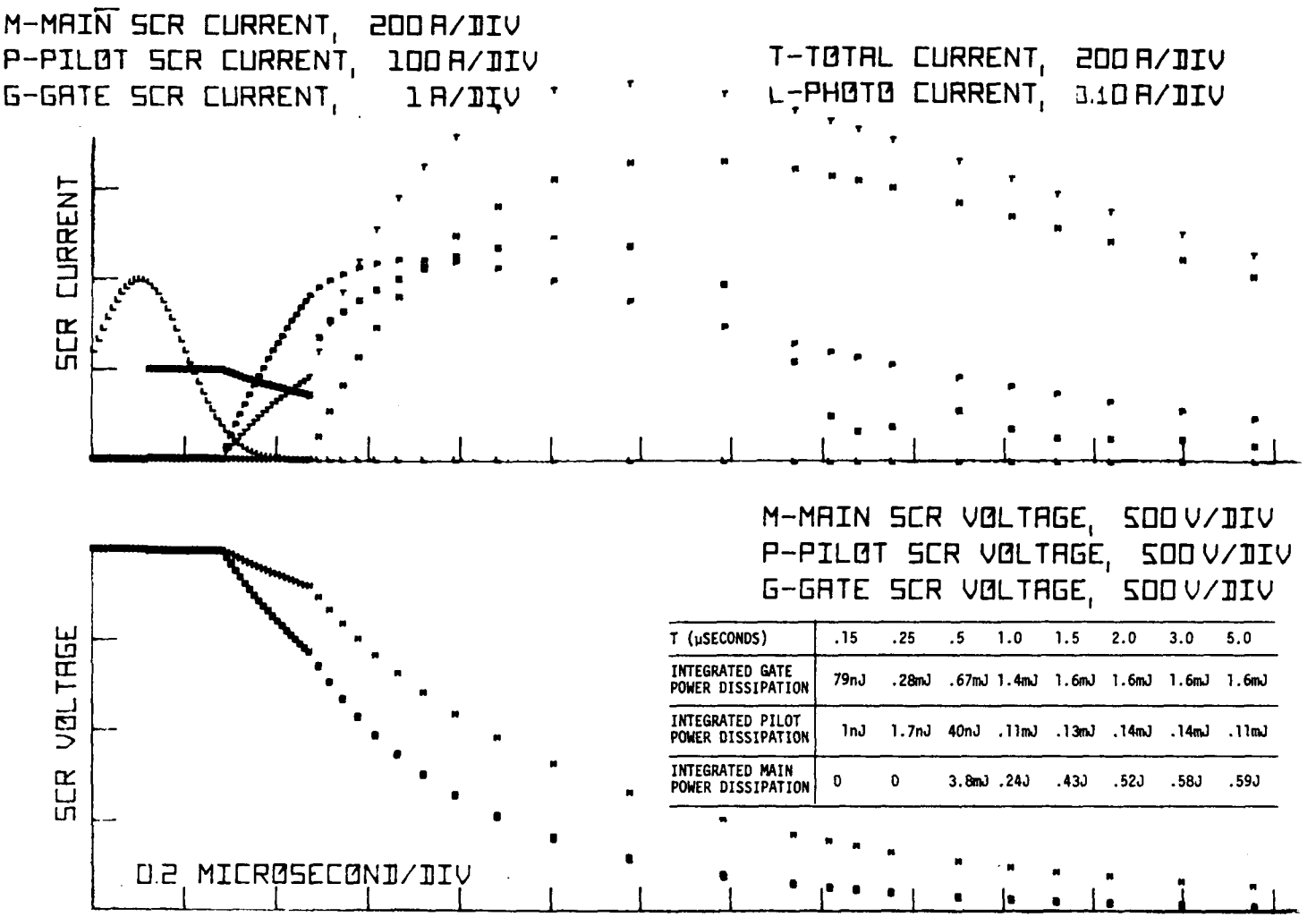


Figure 2-5: Simplified circuit depicting the turn-on model used in the computer program. See Figures 2-14 to 2-19 for typical outputs of the computer program. Note that $S_G(+)$, $S_p(+)$ and $S_\mu(+)$ are the only non-linear elements presently used in the model. These elements consist of a charge controlled ideal switch in series with a time dependent admittance.

Figure 2-6 is a typical result. It represents the turn-on of the present EPRI-GE1 device with a 1μfd, 1 Ω snubber circuit and no load. The currents are shown in the upper graph, L being the gating photocurrent, G, P and M being the currents in each thyristor stage, and T being the total current. The voltages on each of the thyristor stages are represented by G, P and M, respectively, on the lower graph. In this case, P and G are so close as to be indistinguishable on the voltage scale used. Note that in the experiment or in a real application it would be "T" for total current in the upper graph, and "M" for main emitter voltage in the lower graph, that would be of greatest interest. For example, this particular turn-on shows a di/dt of 2000A/μsecond, a delay time of .46μseconds and a net turn-on time of 2.38μseconds after the initiation of a short, 200nseconds gate signal of 40njoules of absorbed photo-energy.

One of the most important considerations is, in fact, the turn-on power dissipated in each of the gate and pilot thyristor stages. These are given in Figure 2-6 in the inset table which shows that, of the 2 joules stored in the snubber capacitance and dissipated during turn-on, 1.5mJ was dissipated in the gate thyristor, all of it in the first 1.5μseconds. Similarly, .14 joules was dissipated in the pilot thyristor all of it in the first 2μseconds. The main thyristor dissipation was only .59 joules. Finally, before leaving Figure 2-6, observe that the gate, pilot and main thyristor turn-on can be easily and separately identified at .12, .29 and .46μseconds, respectively, each with a characteristic di/dt reflecting the Y_1 values chosen for the model.

Table 2-1 is a collection of the similar data for other circuit values. It can be seen from the items listed in the table that we have considered placing a 100 Ω series impedance either between the gate and pilot stages or between the pilot and main stages. In the first location, series impedance does not lessen the pilot stage dissipation as it does if located between the pilot and main stages. However, longer turn-on delay time may result.



T (μSECONDS)	.15	.25	.5	1.0	1.5	2.0	3.0	5.0
INTEGRATED GATE POWER DISSIPATION	79nJ	.28mJ	.67mJ	1.4mJ	1.6mJ	1.6mJ	1.6mJ	1.6mJ
INTEGRATED PILOT POWER DISSIPATION	1nJ	1.7nJ	40nJ	.11mJ	.13mJ	.14mJ	.14mJ	.11mJ
INTEGRATED MAIN POWER DISSIPATION	0	0	3.8mJ	.24J	.43J	.52J	.58J	.59J

Figure 2-6: Computer calculation of the EPRI-GE1 turn-on process showing the current and voltage of each thyristor stage. The inset table shows integrated power dissipation (energy) at a number of time points. The snubber was 1μfd, 1 Ω.

TABLE 2-1

Energy Dissipated During Turn-on
in Devices with Different Series Resistances

CASE	GATE THYRISTOR		PILOT THYRISTOR	
	NET ENERGY DISSIPATED	* TIME TO TURN OFF	DISSIPATED	* TIME TO TURN OFF
1. R_S = 1Ω No series R	1.6mJ	1.5 μsec	.14J	2.0 μsec
2. R_S = 10Ω No series R	.55mJ	1.3 μsec	28mJ	1.5 μsec
3. R_S = 1Ω R'_P = 100Ω	1.1mJ	1.3 μsec	.14J	2.0 μsec
4. R_S = 1Ω R'_M = 100Ω	.34mJ	.5 μsec	2.0mJ	2.0 μsec
5. R_S = 10Ω R'_P = 100Ω	.50mJ	1.0 μsec	28mJ	1.5 μsec
6. R_S = 10Ω R'_M = 100Ω	.34mJ	.5 μsec	1.7mJ	1.0 μsec

* Time to turn off is the time at which no appreciable power is being dissipated in the thyristor stage. Time is measured from the incidence of the photo-gate pulse.

CONCLUSION

Turn-on experiments and computer calculations confirm that excessive energy was being dissipated in the gate and pilot thyristor stages. Both theory and experiment point to this excessive energy as being dissipated in the first few microseconds of turn-on. The results of these and further calculations indicated that the EPRI-GE1 design could be improved to give a device with a higher di/dt capability. This design was the next goal of Phase II.

Section 3

PHASE II DEVICE DEVELOPMENT

DESIGN FOR HIGH DI/DT CAPABILITY

In this section the various methods by which di/dt capability in thyristors can be increased will be discussed. It will be understood in these discussions that the basic n^+-p-n^--p^+ structure will not be subject to change. For example, it will be assumed that the thickness of the n^--p region and the n^- region resistivity will be chosen as thin as possible given a specific breakdown voltage need. Further, it will be assumed that carrier lifetime will already have been fixed to meet a specified forward voltage requirement.

What allows the thyristor to turn-on with a power gain of over 12 orders of magnitude is the fact that only a small area is initially turned on. This area subsequently spreads to cover the entire main emitter. Generally, the more sensitive the thyristor the smaller the initial turn-on region must be. Further, the more sensitive the device the more dv/dt constraints force the gate region to smaller and smaller enclosed area. This is spelled out mathematically in Section 4 of the Phase I Final Report.

The turn-on di/dt problem exists because in the turn-on period both thyristor current and thyristor voltage are high at the same time. Anode current (coming first from the snubber circuit) is forced to flow in a constrained region along what is termed the turn-on line. Excess local temperature excursions may result in a "di/dt" failure. Physically, for center gating, this occurs at the inner periphery of the n^+ emitter of the stage that is being turned on. The failure is termed a di/dt failure because it is seen that reducing the rate at which anode current is allowed to rise ultimately results in no further device failures. Simply stated, one way to prevent di/dt failure is to prevent

the initial current from increasing too rapidly for the given condition of thyristor voltage and on-area.

There are, it seems, three general methods to improve di/dt turn-on capability. These are fairly obvious and consist of (i) turning on a larger initial area, (ii) increasing the spreading rate of the on-area and, (iii) controlling current amplitude and/or current di/dt until that point in the turn-on process at which the device can take the full circuit di/dt. All of these methods are possible to some extent but almost all implementations call for some trade-offs. A number of implementations are believed to be new contributions to thyristor gate design.

In the next three subsections each general approach will be discussed. Following that, a "stage 2" version of the computer turn-on model will be presented and some of its capabilities demonstrated. These capabilities include modelling up to 19 amplifying stages and calculating turn-on areas and temperatures as a function of time given a relatively small number of assumed input parameters.

Increased Initial Turn-on Area

Most devices designed for high di/dt capability use an interdigitated gate structure to achieve extremely long turn-on lines. While this would be possible for the main thyristor stage, it is not possible to incorporate any large degree of interdigitation into gate stages with high gate sensitivities. Another way to increase initial turn-on area which, incidentally, has the useful properties of decreasing turn-on delay time and voltage fall time is to increase the gate overdrive factor. This, too, while very effective unfortunately requires more light.

Using a computer program and a pre-turn-on model described in Section 4 of the Phase I report, calculations were done to compare the initial effect of electrical gate overdrive in the moment prior to actual turn-on. Figures 3-1

and 3-2 are plots of a small section of the turn-on line of typical shorted emitters. This could in fact correspond to the turn-on line of any emitter in the following respects. First it shows that the actual area turned on (injecting current at a sufficient level) is small and located precisely at the inner edge of the emitter. The numbers 1, 2 and 3 on the figures indicate the injection levels which can be seen to vary very rapidly over small distances. This is the second observation that can be made. In comparing Figures 3-1 and 3-2 it can be seen that although Figure 3-2 with its 1.8 volt gate signal does not turn-on much more area than with a 1.5 volt gate signal, the total injected current (which helps govern delay time) is substantially higher.

There is, however, some possibility of increasing initial turn-on area by having serial gates. Figure 3-3 is a preview of one of the final designs which will be more fully discussed in the next section of this report. Suppose the first two amplifying stages have a d.c. turn-on threshold current of 3 and 5ma and corresponding threshold energy (or threshold charge Q = Energy/1.1 volts) of 30 and 50 nanojoules, respectively. In normal circumstances the input gate energy would be 3 to 10 times the 30nJ required for the first stage if only for uniformity of delay time so it can be seen that the first and second stages turn-on more or less at the same time (at least within 10 to 50ns). This tends to have the effect of <u>adding</u> the separate turn-on lines of these two stages. Hence one of the goals in multistage designs is to have the second amplifying stage as sensitive as possible.

Figure 3-4 illustrates the concept of the n^+ alignment band. Essentially the n^+ alignment band assures an even turn-on line potential and thereby the maximum possible di/dt rating for a given geometry. For a small sacrifice in device area one can ensure complete relief from the necessity for perfect alignment. This is important because normally the misalignment between the n^+ emitter mask and the contact metal mask will result in uneven turn-on and to a wide spread in di/dt capability in any fabrication lot.

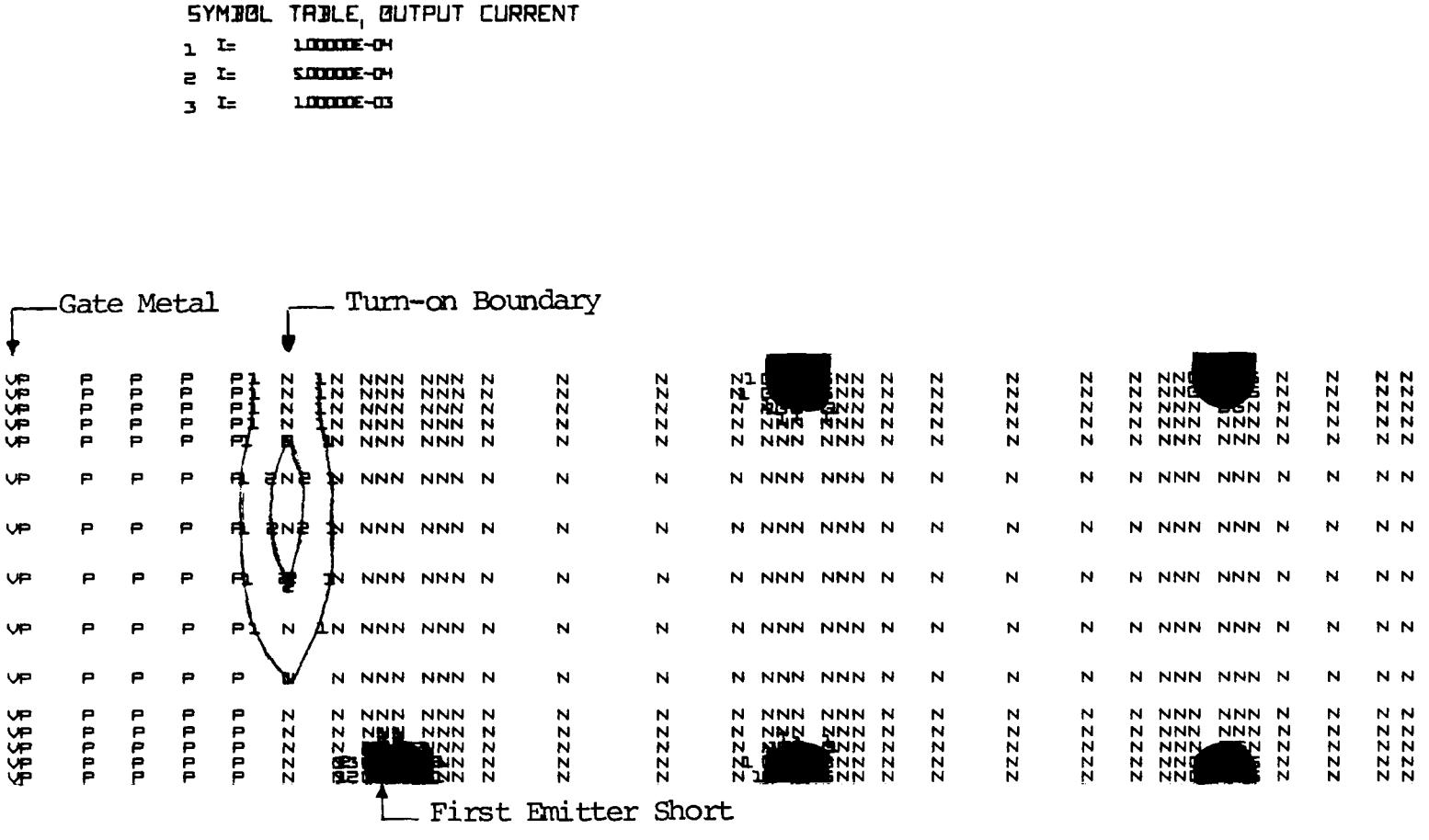


Figure 3-1: Two dimensional plot of a section of turn-on line for a shorted emitter. "V"s denote an applied gate voltage of 1.5 volts. The n^+ emitter is represented by "N"s. Emitter shorts are shaded in. Numbers 1, 2 and 3 show injection current density.

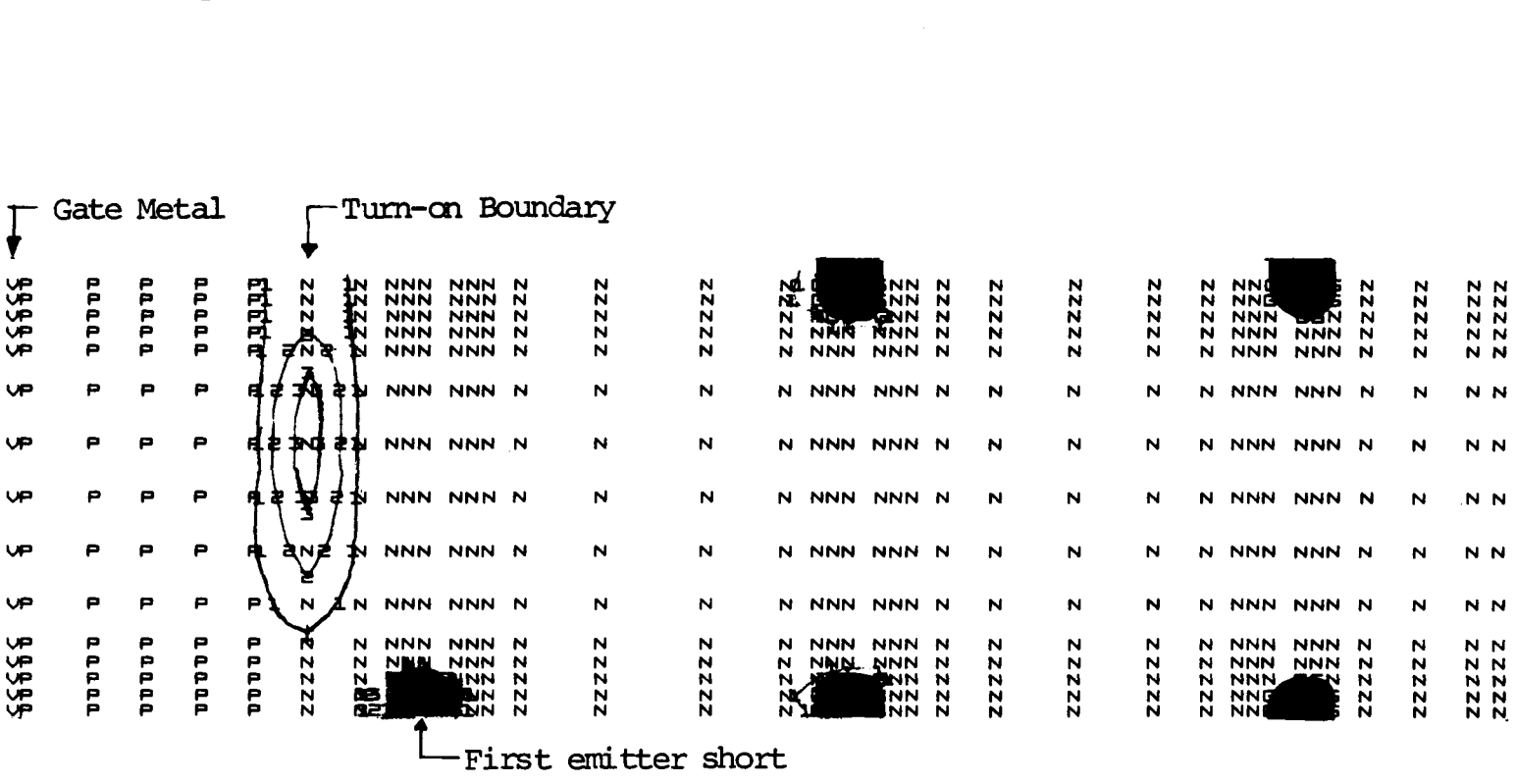


Figure 3-2: Two dimensional plot of a section of turn-on line for a shorted emitter. "V"s denote an applied gate voltage of 1.8 volts. The n^+ emitter is represented by "N"s, Emitter shorts are shaded in. Numbers 1, 2 and 3 show injection current density.

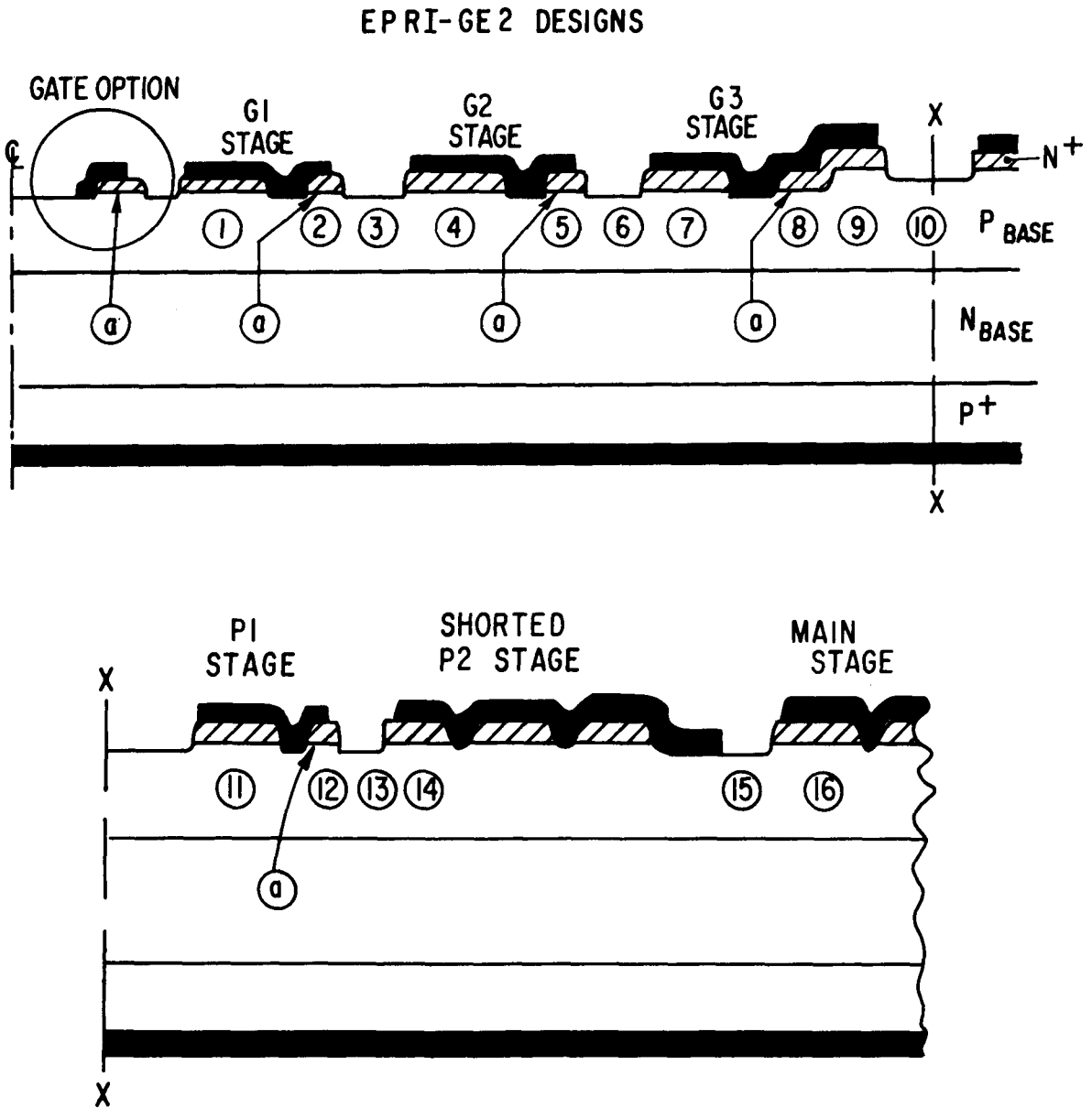


Figure 3-3: Partial radial cross-section of a typical multi-stage amplifying gate thyristor. Letters 'a' refer to an "n+ alignment band" described in the text.

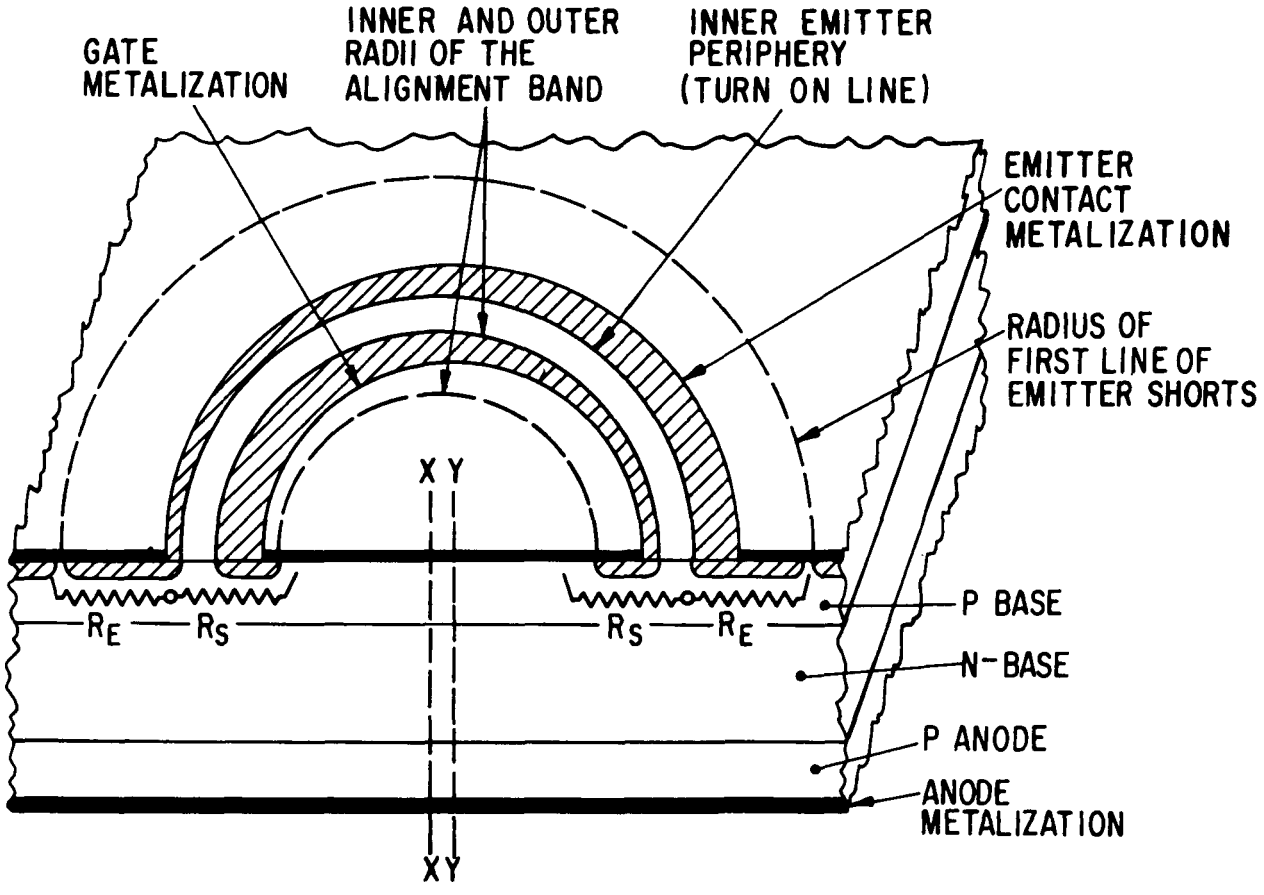


Figure 3-4: View of a thyristor with misaligned n^+ definition and contact metallization masks (represented by the non-coincidence of X-X and Y-Y) but with perfect turn-on line voltage equalization (represented by equal R_S and R_E everywhere along the turn-on line).

It is also probable that in a perfectly aligned device or, as in Figure 3-4, in a device with effectively perfect alignment that less gate overdrive would be needed to obtain maximum turn-on di/dt capability.

On Region Spreading

A second general method to increase di/dt capability is, in some manner, to increase the rate at which the on-area spreads. Since the on-area spreads at a rate proportional (to first order) to the boundary between the on and off region, it would seem that this boundary should be as large as possible for a given amount of input gate energy. In the absence of gate amplification, the turn-on spreading velocity is normally a function of current density alone. However, in the presence of gate amplification tremendous increases in on-area spreading are possible. What occurs is that some of the anode current is used to charge up the much larger turn-on line of the next stage. This stage turns on and the on-region spreads from the new turn-on line. The effect is a jump in the on-area as each amplifying stage is turned on.

One of the excellent ideas for speeding on-region spreading was the FI gate[5] so called because it forced on-region spreading to be enhanced by a lateral field developed between the initial turn-on line and the emitter metallization. This technique, however, never fulfilled all of its expected promise because of excess heating which now seemed to occur in the unmetallized n^+ region. Figure 3-5 illustrates an improvement which is termed "interrupted emitter metallization", taking its name from the purposely left gaps in the n^+ emitter metallization. The function of these gaps and the lateral field produced thereby is to cause the field assisted spread of the on-region from the turn-on line to the far side of the gap. One of the consequences of the gap is that injection current from the vicinity of the initial turn-on line is now limited in a predictable fashion through sheet resistance of the n^+ in the gap and by the gap size. Obviously if the gap resistance was .01 Ω a current across the gap of 10 amperes would induce a voltage drop of .1 volts and a lateral field of .1/W, W being the

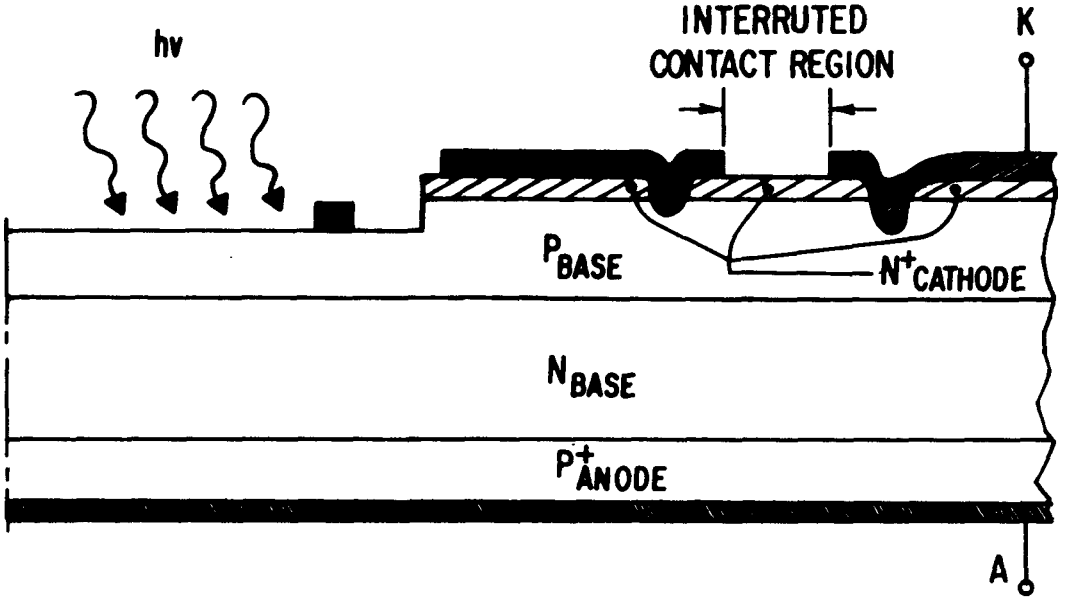


Figure 3-5: Interrupted n^+ emitter metallization concept.

width of the gap. It would also infer an order or so of magnitude drop in the injection current on the turn-on line which would reduce power dissipation there. The nice thing about this technique is that at low anode current, say below 1A (1 ampere might be the current which best gates the main emitter) where maximum injection is called for, the injection efficiency would be relatively unaffected.

Initial Anode Current Control

The third general method for improving device turn-on reliability is to retain control of the anode current until enough area has been turned on and until the rate of on-region spreading is sufficient to prevent excessive temperature excursions. Obviously an external light fired gate stage such as that of Figure 2-26 is very attractive. Control through simple series resistance or through more sophisticated circuitry would be possible even to the extent of circuits which would let through a specified current or current pulse. Should simple series resistance be an adequate measure, such a resistance could eventually be incorporated into an integrated structure.

Actually the requirement that we are looking for is one of controlled power dissipation during turn-on. In a sense, amplifying stages do this for they can be used to reduce the duty cycle of the prior amplifying stage. The less "gain" between stages, gain referring to the ratio of the turn-on threshold currents, and the more series impedance the sooner the current flow in the prior stage falls off. This point will be demonstrated in some of the computer calculations performed in Section 4 of this report.

NEW THYRISTOR DESIGNS

Improved Turn-on Model

Because our new designs anticipated more than two amplifying stages, the turn-on model discussed in Section 2 and shown in Figure 2-5 was extended to allow more amplifying stages. The new computer program is also an improvement

over the former one in its inclusion of power density and temperature calculations. For this the spreading velocity vs. current density given by equation 3-1 below has been assumed using results[6] obtained on similar thyristors with microwave probes.

$$V_{SP} = K1 \ln(J/J_o) \qquad (3\text{-}1)$$

The initial turn-on area is assumed to be the turn-on line length times the p base region diffusion length and power dissipation is assumed to be constant in the on-region through the wafer from anode to cathode. These two reasonable assumptions enable a time dependent calculation to predict instantaneous on-area, spreading velocity, on-area current density and temperature for each amplifying stage. The new model is shown in Figure 3-6.

General Design Aims

The section describes the Phase II series of EPRI thyristor designs. These devices embody the general design concepts for improved di/dt that were discussed earlier in this report. There are three series of devices: EPRI-GE2, EPRI-GE3 and EPRI-GE4. For convenience these will be referred to as the GE2, GE3 and GE4 series and subvariations by the addition of letters A, B, C, etc. The three series differ in two main ways. The GE3 and GE4 versions have a larger light sensitive inner gate region than the GE2 version while GE2 and GE3 have 5 and 4 amplifying gate designs compared to the GE4 which has two amplifying stages as the EPRI-GE1[1].

Implementation of the new design N^+ alignment band, the interrupted N^+ metal, and series resistance are possible in most of the designs as is evident in Table 3-1. Note that Table 3-1 also includes calculated dc gate sensitivity and dv/dt capability. The "gate ring" option (column 4) refers to a photocurrent gathering metallization inserted between the photosensitive region and the emitter of the first amplifying stage. This feature was not commented upon in Section 3 of this report because it was developed and described in earlier work[1,7].

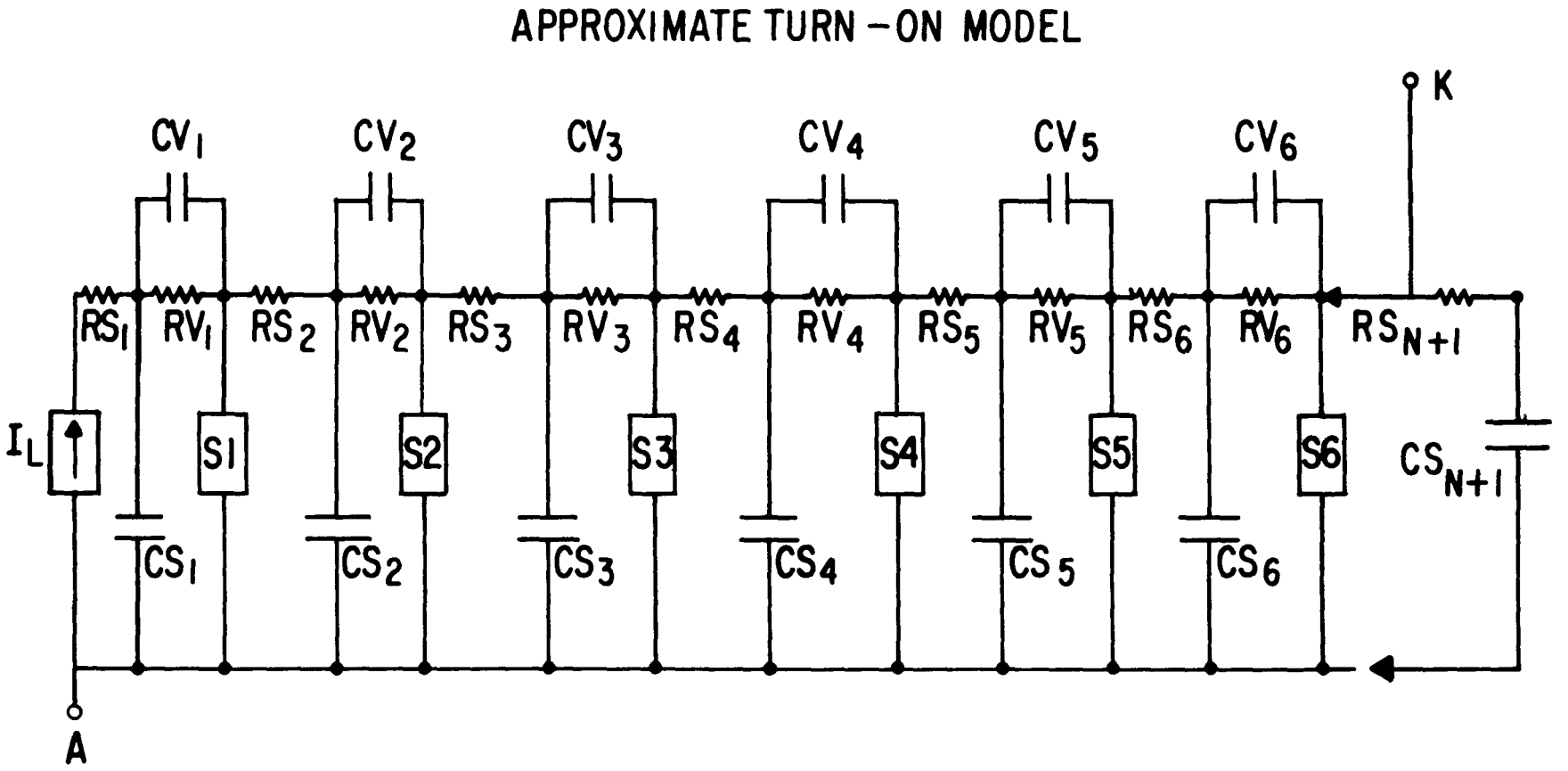


Figure 3-6: Curcuit model for generating turn-on current-voltage transients. Up to 19 amplifying stages can be included. Numerical subscripts identify the amplifying stage that each element is a part of.

TABLE 3-1: THYRISTOR DESIGN VARIATIONS*

DESIGN	NUMBER OF AMPLIFYING STAGES	Features Included				dc GATE SENSITIVITY (mA)	dv/dt CAPABILITY (V/μsec)
		N^+ ALIGNMENT BAND	GATE RING	INTERRUPTED N^+ METAL	SERIES R		
EPRI-GE2A	3 Gate + 2 Pilot	No	No	No	No	3.0	2000
EPRI-GE2B	" "	No	Yes	No	No	3.0	2000
EPRI-GE2C	" "	Yes	Yes	No	No	3.0	2000
EPRI-GE3A	2 Gate + 2 Pilot	No	No	No	No	3.2	2020
EPRI-GE3B	" "	No	Yes	No/Yes	No	3.2	2020
EPRI-GE3C	" "	Yes	Yes	No	No	3.2	2020
EPRI-GE3D	" "	Yes/No	Yes	Yes	No	3.2	2020
EPRI-GE4A	1 Gate + 1 Pilot	No	No	Yes/No	Yes/No	2.3	1995
EPRI-GE4B	" "	No	Yes	Yes/No	Yes/No	2.3	1995
EPRI-GE4C	" "	Yes	Yes	Yes/No	Yes/No	2.3	1995

* Device processing started on 80 wafers (total possible variations ∿34)

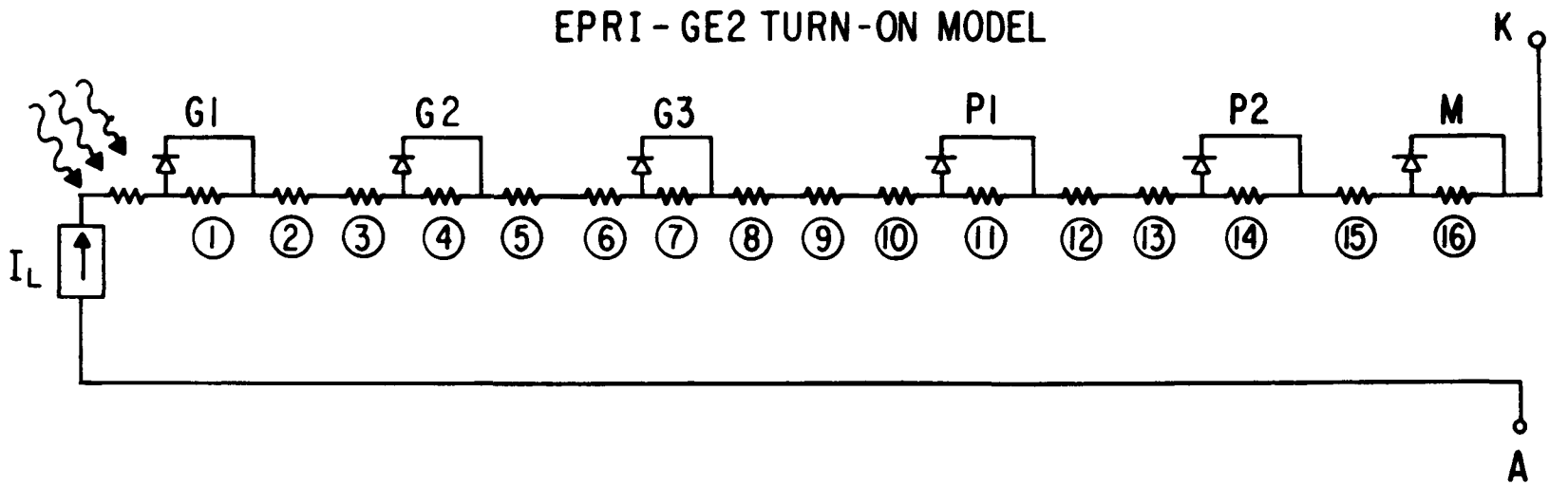


Figure 3-7: Model used to calculate gate and dv/dt turn-on thresholds for the GE2 design. Results are tabulated in Table 3-2.

TABLE 3-2: GE2 CALCULATIONS

ZONE	R (Ω)	ρ (Ω/□)	L_{on} (cm)	Thermal Rise for lateral current (1) (^{o}C/mJ)	I_G Threshold (mA)	dV/dt (V/μsec)	ΔT on Turn-on line(2) (^{o}C/mJ)	ΔT on Turn-on line(3) (^{o}C/mW)
1 (G1)	236	2300	.25	5.6	3.0	5990	19	.56
2	21	2300	-	26.3	-	-	-	-
3	49	2900	-	12.1	-	-	-	-
4 (G2)	67	2300	.64	5.2	10.5	5360	7.4	.52
5	14	2300	-	17.4	-	-	-	-
6	33	2900	-	8.2	-	-	-	-
7 (G3)	49	2300	.93	5.0	14.3	3930	5.1	.50
8	11	2300	-	13.4	-	-	-	-
9	4.1	1200	-	17.3	-	-	-	-
10	14	1600	-	6.3	-	-	-	-
11 (P1)	30	1200	1.20	1.7	23	3390	4.0	.17
12	6.0	1200	-	6.4	-	-	-	-
13	18	1600	-	2.6	-	-	-	-
14 (P2)	17	1200	1.68	1.8	42	3480	2.8	.17
15	11	1600	-	.81	-	-	-	-
16 (M)	6.5	1200	3.75	.98	94	2000	1.3	-

(1) Assumed to dissipate power in the p-base only.

(2) Assumed to dissipate power in a 2 mil annular zone from anode to cathode.

(3) Averaged over silicon volume for that emitter.

In the following, the main design series are treated separately and in some detail. Finally the new turn-on model is applied to the various designs to assess, if possible, whether the specific problem of excessive thermal transients at the turn-on line would be lessened by the new designs and whether additional amplifying stages might have any positive effects.

The EPRI-GE2 Design

The chief feature of the basic EPRI-GE2 thyristor design shown in radial cross-section in Figure 3-3 is its five amplifying stages. The three inner stages are labeled G1, G2 and G3 for first, second and third gate stages with the final two amplifying stages referred to as the first (P1) and second (P2) pilot stages. These stages act to turn-on the main (M) thyristor. The P2 and M stages intentionally duplicate the design of the pilot and main stages of the basic electrically fired device which it is to replace.

Figure 3-7 shows the simple electrical turn-on model normally used to calculate gate and dV/dt turn-on thresholds. Some of the results of calculations on this model are given in Table 3-2. Note that the calculated turn-on thresholds are given for each amplifying stage. In addition, three slide rule variety calculations regarding temperature effects are also given. The "zones" referred to in the table relate to similar numbers in Figure 3-3.

Key elements in the table that are important to good di/dt capability are "L_{on}", the turn-on line length and the ratio of succeeding "I_G" or gate threshold currents. As noted before, L_{on} should be as large as possible given the constraint of a minimum gate sensitivity and the I_G ratio (I_G [Stage N+1]/I_G [Stage N]) should be low. Comments on dynamic turn-on calculations are reserved for the final part of this section.

The EPRI-GE3 Design

The basic GE3 thyristor design represented in Figures 3-8 and 3-9 is very similar to that of the GE2, even to the extent of stages P1, P2 and M being totally identical. However, there is one less gate amplifying stage and more than twice as large a light sensitive inner gate region for photocurrent generation.

Table 3-3 like Table 3-2, gives turn-on threshold calculations, but for the GE3 design and with the simple turn-on model of Figure 3-9. Note that the four sub-variations, denoted GE3A, B, C and D in Table 3-1, are expected to have identical thresholds but will vary in other respects which will hopefully reduce initial turn-on region temperature excursions.

The EPRI-GE4 Design

Figures 3-10 and 3-11 represent the basic GE4 thyristor. In one way it is like the GE1[1] thyristor in having only two amplifying stages. But it is different from the GE1, 2 and 3 designs in having emitter shorts in the gate thyristor stage. With the series base resistance option included, this design would be the closest to that recommended at the end of Phase I. At that time, it was felt that a larger total first stage emitter area would be needed to accomodate initial on-region spreading. Now, in light of the measured spreading velocity vs. current density data[6] made in similar devices using microwave techniques, the GE4 versions become less important except in so far as comparing possible 4A, 4B and 4C sub-variations. This will be reinforced by dynamic turn-on calculations discussed in the following.

TURN-ON CALCULATIONS

In this section results of computer calculations using the turn-on model in Figure 3-6 are described. As indicated earlier, these calculations allow the inclusion of up to 19 amplifying stages and, in addition, predict such things as current density, on-region spreading velocity, on-region area, power

EPRI–GE 3 DESIGNS

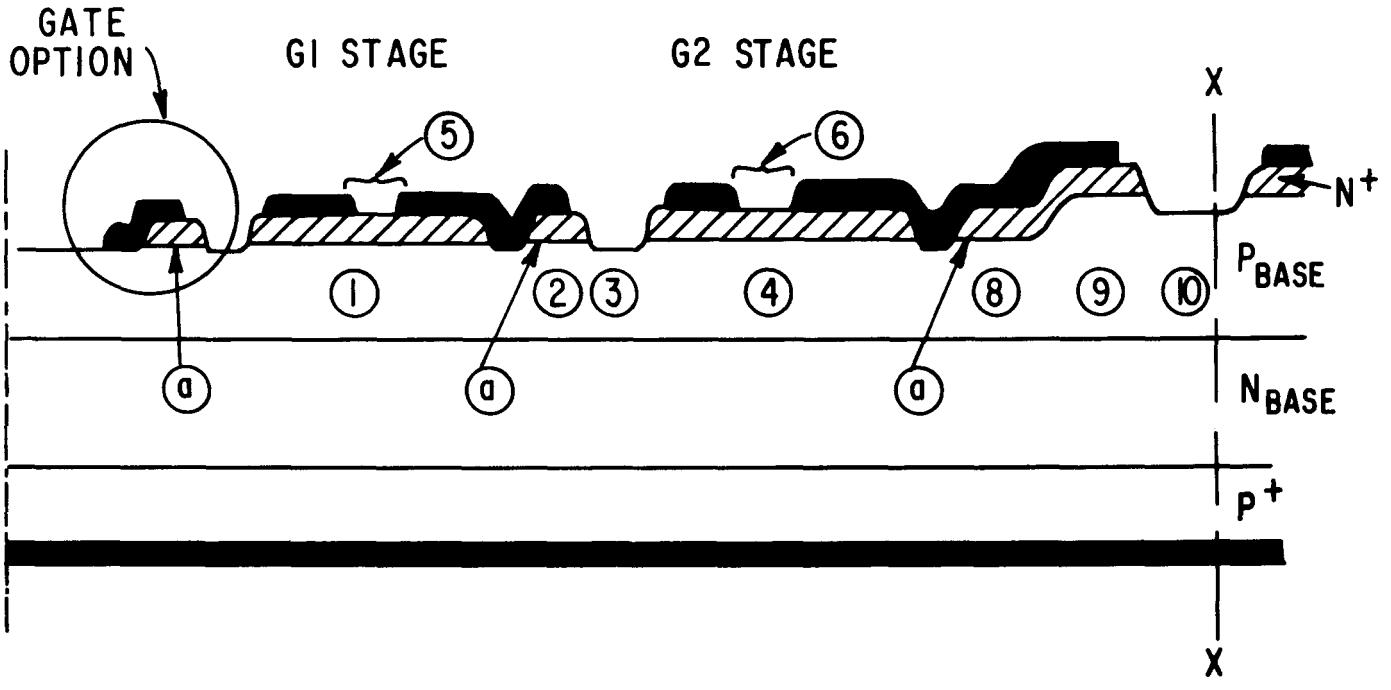


Figure 3-8: Partial radial cross-section of the basic GE3 design. The letters 'a' denote the n^+ alignment bands while the circled numbers refer to the base region "zones" whose resistance values are given in Table 3-3.

EPRI–GE 4 DESIGNS

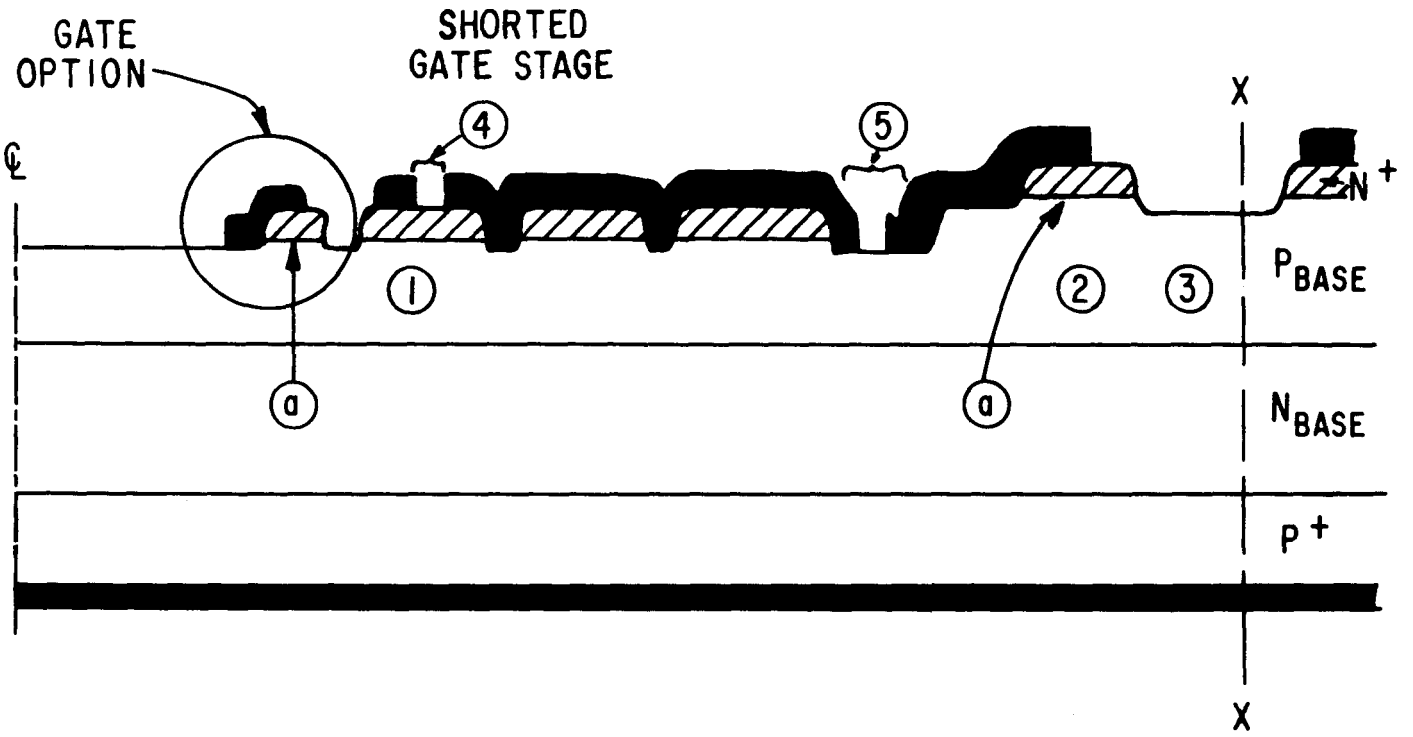


Figure 3-9: Model used to calculate gate and dv/dt turn-on thresholds for the GE3 design. Results are tabulated in Table 3-3.

TABLE 3-3 GE3 CALCULATIONS

ZONE	R (Ω)	ρ (Ω/□)	L_{on} (cm)	T for Lateral Current(1) (°C/mJ)	I_G Threshold (mA)	dV/dt (V/μsec)	ΔT_{on} (2) (°C/mJ)	ΔT_{on} (3) (°C/mW)
1 (G1)	218	2200	.35	3.1	3.2	3300	13.6	.31
2	15.2	2200	-	20	-	-	-	-
3	37.7	2900	-	9.4	-	-	-	-
4 (G2)	79.5	2200	.81	2.5	8.8	2670	5.9	.25
5	.02	1	-	144	-	-	-	-
6	.0055	1	-	159	-	-	-	-
8	11	2300	-	13.4	-	-	-	-
9	4.1	1200	-	17.3	-	-	-	-
10	14	1600	-	6.3	-	-	-	-
11 (P1)	30	1200	1.20	1.7	23	3390	4.0	.17
12	6.0	1200	-	6.4	-	-	-	-
13	18	1600	-	2.6	-	-	-	-
14 (P2)	17	1200	1.68	1.8	42	3480	2.8	.17
15	11	1600	-	.81	-	-	-	-
16 (M)	6.5	1200	3.75	.98	94	2000	1.3	-

(1) Assumed to dissipate power in the p-base only.

(2) Assumed to dissipate power in a 2 mil annular zone from anode to cathode.

(3) Averaged over silicon volume for that emitter.

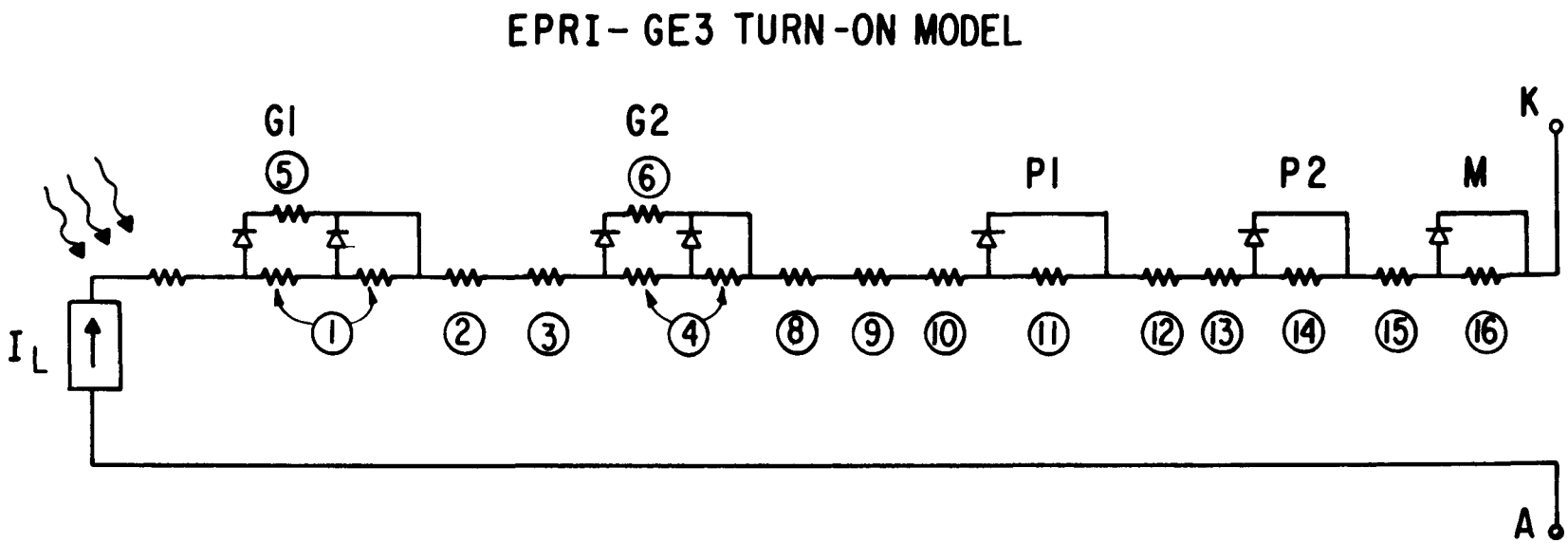


Figure 3-10: Partial radial cross-section of the basic GE3 design. The letters 'a' denote the n^+ alignment bands while the circled numbers refer to the base region "zones" whose resistance values are given in Table 3-4.

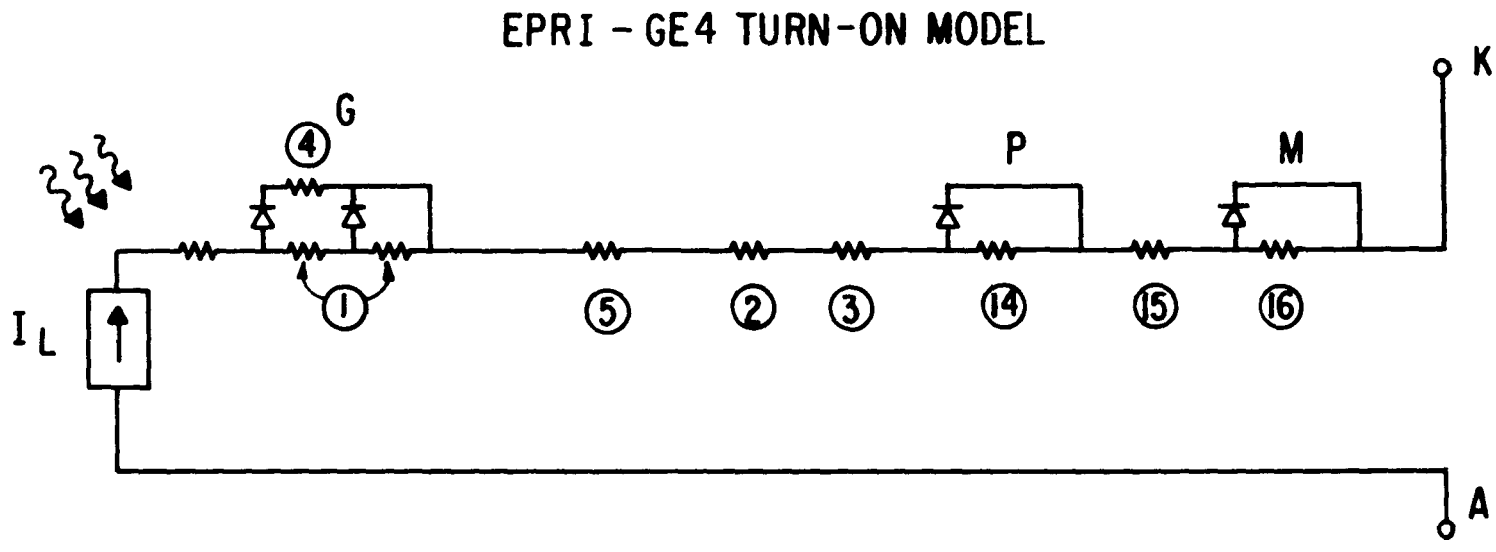


Figure 3-11: Model used to calculate gate and dv/dt turn-on thresholds for the GE4 design. Results are tabulated in Table 3-4.

TABLE 3-4: GE4 CALCULATIONS

ZONE	R (Ω)	ρ (Ω/□)	L_{on} (cm)	(^{o}C/mJ)	I_G Threshold (mA)	dV/dt (V/μsec)	ΔT_{on} (2) (^{o}C/mJ)	ΔT_{on} (3) (^{o}C/mW)
1 (G)	303*	2200	.32	3.1	1.75*	2630*	.32	.31
2	4.9	1200	-	6.3	-	-	-	-
3	6.6	1600	-	3.6	-	-	-	-
4	.011	1	-	300	-	-	-	-
5	22	2900	-	5.4	-	-	-	-

The Pilot and Main are identical to Zones 12 - 16 of Fig. 3-3

* Includes 25% increase in sensitivity due to short radius.

(1) Assumed to dissipate power in the p-base only.

(2) Assumed to dissipate power in a 2 mil annular zone from anode to cathode.

(3) Averaged over silicon volume for that emitter.

dissipation and instantaneous temperature. Table 3-5 is a condensation of some of the more important data which can be found in such output.

Each of the 13 cases treated give the key results of the important first 5 or 10μseconds of the turn-on transient. This is generally a large enough time period to establish the maximum turn-on line temperature excursions of all the thyristor stages. These key variables are rather obvious ones enabling prediction of such things as turn-on delay, voltage fall time, and transient temperature excursions for a given snubber and initial di/dt. Enough data is given to also establish how long each stage dissipates power during the turn-on process and what each stage's maximum power dissipation and maximum current density might be during that time. Although spreading velocity is not specifically listed, its maximum value can be recalculated taking J_{max} and using equation (3-1) with parameter values given in Reference 6. Appendix A can be consulted for turn-on model parameter values.

All of the thirteen cases treated in Table 3-5 relate to EPRI-GE1, 2, 3 and 4 designs. All of the cases treat turn-on from 2000 volts which is slightly above the required voltage for the actual di/dt test. The first column describes which design the case treats and gives the gate photocurrent pulse used for that case. It should also be noted that the program is flexible enough to allow for turn-on calculations with any one or more of the amplifying stages omitted.

Cases 1, 2 and 3 describe the turn-on action of the basic GE2 design for a 200n-second laser type gate current of three different amplitudes. Case 1, the middle amplitude at .2 amperes (corresponding to an incident photoenergy of 40-120nJ) shows a turn-on delay time of ∿.191μseconds and voltage fall time also at ∿1μsecond. Case 3 with 5 times larger amplitude than Case 1 had the shortest turn-on delay at .1μsecond but the same 1μsecond fall time. The bottom line, of course, is the ΔT value given in the last column. Only the first gate stage,

TABLE 3-5: TURN-ON CALCULATION DATA

CASE	GATE STAGE	t_{on} (μsec)	$V(t_{on})$ (V)	$t_{.9V}$ (μsec)	$t_{.1V}$ (μsec)	$I_G(t_{on})$ (A)	I_{max} (A)	$t_{I_{max}}$ (μsec)	$t_{.37I}$ (μsec)	E_{tot} (mJ)	$t_{.1E}$ (μsec)	$t_{.9E}$ (μsec)	P_{max} (kW)	$t_{P_{max}}$ (μsec)	J_{max} (A/cm²)	$t_{J_{max}}$ (μsec)	$A_{on}(o)$ (mm²)	$A_{on}(P_{max})$ (mm²)	$A_{on}(t_{.9E})$ (mm²)	ΔT (°C)
GE2 Design. All stages utilized. Turn-on from 2000V with .2A, 200nsec gate pulse	G1	.114	1963	.128	.209	.198	2.38	.152	.215	.155	.126	.182	3.37	.142	1637	.150	.143	.145	.148	.94
	G2	.140	1791	.146	.227	2.13	3.25	.176	.275	.160	.149	.217	3.36	.158	847	.175	.376	.381	.390	.37
	G3	.148	1750	.154	.255	3.74	4.88	.188	.362	.275	.159	.262	4.41	.168	1032	.189	.465	.472	.490	.51
	P1	.152	1802	.158	.314	4.94	8.70	.216	.577	.772	.169	.334	7.80	.180	1184	.212	.715	.725	.772	.92
	P2	.158	1864	.168	.494	9.47	23.4	.330	1.39	4.43	.193	.735	18.9	.109	2165	.300	1.00	1.02	1.28	3.55
CASE 1	M	.176	1823	.191	1.22	25.4	142	1.19	~5.5	~80	.317	3.10	69.8	.305	5435	.616	1.85	1.99	5.27	24.7
GE2 Design. Same as above. Except .1A 200nsec gate pulse	G1	.296	1996	.309	.394	.015	2.47	.334	.398	.165	.309	.363	3.62	.326	--	--	--	--	--	1.0
	G2	.326	1763	.331	.412	2.25	3.22	.362	.461	.153	.333	.398	3.26	.342	--	--	--	--	--	.35
	G3	.330	1783	.335	.439	3.26	5.10	.371	.540	.285	.341	.439	4.56	.349	--	--	--	--	--	.53
	P1	.336	1785	.341	.501	5.59	8.76	.397	.766	.750	.353	.551	7.72	.366	--	--	--	--	--	.89
	P2	.342	1858	.352	.681	9.21	23.5	.518	1.57	4.34	.376	.910	19.1	.382	--	--	--	--	--	3.48
CASE 2	M	.362	1833	.374	1.32	24.4	142	1.40	~6.0	~80	.50	3.6	69.8	.488	--	--	--	--	--	24.7
GE2 Design. Same as Case 1 except 1A 200nsec gate pulse	G1	.028	1863	--	--	.772	1.89	.060	--	.099	.038	.083	2.56	.054	--	--	--	--	--	.60
	G2	.048	1758	--	--	2.31	3.03	.082	--	.135	.056	.119	3.09	.064	--	--	--	--	--	.31
	G3	.054	1768	--	--	3.50	4.92	.095	--	.268	.064	.161	4.31	.073	--	--	--	--	--	.50
	P1	.060	1777	--	--	5.86	8.61	.124	--	.730	.076	.262	7.12	.090	--	--	--	--	--	.87
	P2	.064	1874	--	--	8.16	23.6	.242	--	4.40	.098	.610	19.6	.105	--	--	--	--	--	3.53
CASE 3	M	.086	1825	.098	1.15	25.3	142	1.1	--	~80	.226	~3.4	69.6	.213	--	--	--	--	--	24.7
GE3 Design. All stages utilized. Turn-on from 2000V with .2A, 200nsec gate pulse	G1	.156	1977	.171	.276	.171	3.29	.198	.297	.260	.172	.239	4.62	.190	1844	.198	.175	.177	.183	1.29
	G2	.182	1814	.191	.303	2.60	4.50	.225	.395	.306	.195	.299	4.49	.205	1091	.225	.405	.409	.427	.66
	P1	.190	1821	.197	.357	3.02	9.35	.253	.597	.867	.207	.377	8.93	.219	1514	.248	.600	.608	.657	1.23
	P2	.196	1883	.207	.558	7.46	23.5	.369	1.42	4.52	.230	.763	19.8	.235	2580	.336	.840	.856	1.11	4.26
	M	.215	1833	.231	1.38	24.2	142	1.23	.730	~82	.357	3.96	69.9	.343	5435	.650	1.85	1.99	6.23	25.0
CASE 4																				

TABLE 3-5 (CONT.)

CASE	GATE STAGE	t_{on} (μsec)	$V(t_{on})$ (V)	$t_{.9V}$ (μsec)	$t_{.1V}$ (μsec)	$I_G(t_{on})$ (A)	I_{max} (A)	$t_{I_{max}}$ (μsec)	$t_{.37I}$ (μsec)	E_{tot} (mJ)	$t_{.1E}$ (μsec)	$t_{.9E}$ (μsec)	P_{max} (kW)	$t_{P_{max}}$ (μsec)	J_{max} (A/cm^2)	$t_{J_{max}}$ (μsec)	$A_{on}(o)$ (mm^2)	$A_{on}(P_{max})$ (mm^2)	$A_{on}(t_{.9E})$ (mm^2)	ΔT (°C)
GE4 Design. All stages utilized. Turn-on from 2000V with .2A 200nsec gate pulse CASE 5	G	.142	1994	.188	.467	.185	6.69	.223	.672	1.39	.176	.430	10.0	.207	3661	.220	.175	.181	.205	6.57
	P	.184	1906	.200	.531	4.77	26.2	.332	1.29	5.38	.217	.700	25.8	.226	2898	.311	.840	.858	1.09	5.11
	M	.207	1857	.223	1.24	17.5	142	1.22	7.44	∿82	.344	3.38	72.3	.325	5456	.629	1.95	1.98	5.57	25.2
GE4 Design. Same as Case 5 except for 22Ω series R between G & P CASE 6	G	.142	1990	.176	.422	.185	6.29	.220	.568	1.12	.174	.384	8.86	.201	3444	.219	.175	.081	.200	5.35
	P	.186	1907	.203	.540	4.74	26.7	.335	1.29	5.60	.220	.699	26.5	.229	2952	.315	.840	.859	1.09	5.31
	M	.210	1852	.228	1.23	18.4	142	1.21	7.4	∿82	.350	3.34	72.6	.328	5460	.632	1.85	1.98	5.52	25.2
GE1 Design. All stages utilized. Turn-on from 2000V with .2A, 200nsec gate pulse CASE 7	G	.116	1990	.158	.383	.198	5.95	.207	.447	.994	.148	.324	8.05	.199	4528	.207	.125	.131	.141	6.69
	P	.154	1936	.175	.457	3.48	19.8	.222	.990	3.78	.185	.562	27.7	.207	3177	.220	.600	.617	.707	5.14
	M	.203	1807	.215	.786	22.7	156	.90	>5	∿58	.282	∿3	84.4	.261	2744	.538	4.23	4.81	10.6	8.0
GE2 Design. Gate Only. Turn-on from 2000V with .2A, 200nsec gate pulse CASE 8	G	.128	1998	.370	7.5	.193	94.5	2.98	>10.	∿350	.84	6.40	84.8	1.38	2918	1.27	.125	.203	1.050	808

TABLE 3-5 (CONT.)

CASE	GATE STAGE	t_{on} (μsec)	$V(t_{on})$ (V)	$t_{.9V}$ (μsec)	$t_{.1V}$ (μsec)	$I_G(t_{on})$ (A)	I_{max} (A)	$t_{I_{max}}$ (μsec)	$t_{.37I}$ (μsec)	E_{tot} (mJ)	$t_{.1E}$ (μsec)	$t_{.9E}$ (μsec)	P_{max} (kW)	$t_{P_{max}}$ (μsec)	J_{max} (A/cm²)	$t_{J_{max}}$ (μsec)	$A_{on}(o)$ (mm²)	$A_{on}(P_{max})$ (mm²)	$A_{on}(t_{.9E})$ (mm²)	ΔT (°C)
GE2 Design. Same as Case 8 except 2A, 200nsec gate pulse CASE 9	G	.020	1988	.123	7.2	1.48	94.7	3.34	>10.	344	.725	6.41	84.8	1.36	2916	1.20	.125	.273	.964	805
GE2 Design. P2 & M only. Turn-on from 2000V with 2A, 2μsec gate pulse with 1μsec rise time CASE 10	P2	.374	1984	.402	.730	.744	29.1	.519	1.31	6.41	.407	.844	32.8	.420	2248	.498	.895	1.26	1.46	4.3
	M	.406	1884	.423	1.35	16.6	142	1.42	∿6.	∿80	.536	3.2	73.8	.519	5476	.824	1.85	1.97	5.17	24.9
GE2 Design. Same as 10 except for 0μsec rise time CASE 11	P2	.106	1972	.124	.45	1.34	28.5	.246	1.06	6.13	.139	.544	31.0	.152	2810	.231	.857	.972	1.17	5.23
	M	.134	1897	.150	1.08	15.2	142	1.15	>5.0	∿80	.263	3.0	74.0	.240	5486	.554	1.85	.236	5.26	24.9
GE2 Design. G1 & M only. Turn-on from 2000V with .2A, 200nsec gate pulse CASE 12	G1	.116	1996	.201	.870	.198	9.24	.363	2.17	4.63	.181	1.05	10.5	.266	5850	.290	.14	.15	.22	24.7
	M	.201	1938	.21	1.23	6.24	147	1.23	∿5.5	∿88	.32	2.9	89.3	.329	5970	.570	1.85	2.00	5.10	27.7
GE2 Design. GL, P1 & M only. Turn-on from 2000V with .2A, 200nsec gate pulse CASE 13	G1	.116	1990	.158	.450	.198	5.51	.203	.658	1.17	.152	.412	7.93	.185	4201	.200	.125	.130	.148	7.7
	P1	.154	1936	.182	.557	3.48	22.5	.320	1.39	5.56	.193	.734	23.7	.203	3147	.290	.600	.616	.809	7.3
	M	.185	1875	.201	1.21	16.3	143	1.21	∿6	∿82	.320	3.0	76.4	.297	5529	.600	1.85	.198	5.25	24.5

G1, is much affected by increased gate amplitude with the 1A gate signal resulting in a .5°C temperature rise as compared to .94 and 1.0°C for the .2A and .1A gates, respectively. In fact, all of the inner gate stage temperature excursions are below 1°C and only the second pilot (P2) and main (M) stages are really of concern. However these, it should be recalled, are identical in design to the pilot and main of the regular electrically fired device. This should be an acceptable di/dt capability for this design with some provisions that are common to all thirteen cases and will, therefore, be discussed at the end of this section.

Case 4 treats the basic GE3 design with the 200nsecond, .2A gate current. This design is somewhat less sensitive than the GE2 design and has an ∿40nsecond longer delay time but still the same voltage fall time. Actually this should be expected because most of the externally observable effects apart from delay time are controlled by the final stages. This is illustrated by the I_{max} (maximum current) column of Table 3-5. It is also expected from the observation of t_{on}, the turn-on time, and $t_{.37I}$, the time the current in a stage has dropped to .37 times its maximum value. These times are tabulated to give a feel for how long a stage is carrying current. The columns $t_{.1E}$ and $t_{.9E}$ reveal how long the stage is dissipating substantial amounts of energy. Both time intervals are very short, of the order of 100nseconds, for the inner amplifying stages.

Case 5 treats the basic GE4 design. Its gate stage thermal excursion (ΔT) is 6 times that of the gate (G1) stage of the GE2 design and 5 times that of the GE3 design. This is the consequence of having to carry current for a longer interval (e.g. $T_{.37I} - t_{on} = .53\mu sec$). This longer period of current flow is due to the fact that the next stage is much less sensitive and requires a lot more charging current to turn it on. There is also a lot less series resistance between the G and P stages of Case 5 than between the G1 and G2 stages of Case 1. This also has some effect. Note that gate stage on-area

starts out at .175mm^2 but, at $t_{.9E}$ is only .205mm^2. This is an indication that in .53μseconds there is insufficient on-region spreading to require a large emitter area with emitter shorts. This infers that the gate stage area would be better utilized by having one or two more amplifying stages as in Cases 1 to 4.

Case 6 also treats the GE4 design with one change, an additional 22 Ω series impedance between the gate (G) and pilot (P) stages. The consequence of that change was a .12°C reduction in temperature excursion. Although this seems small, in reliability terms it could mean as much as an eight fold increase in cycles to failure.

Case 7 treats the old GE1 design. Its gate stage thermal excursion is 6.69°C, much higher than the new GE2 and GE3 basic designs. Note however, the effect of the larger main stage turn-on line is an 8°C main line excursion as compared to 25° for the GE2, 3 and 4 designs. This is due to the fact that the GE1 design had all stages different from the regular 6RT101 electrically fired device in an attempt to increase di/dt capability above that of the 6RT101 whereas, now, the goal is more conservative. In fact, Cases 10 and 11 treat the GE2 design with only the P2 and M stages which makes these cases essentially that of the electrically fired 6RT101 device. Naturally the gate signal is now 2A and 2μseconds (half width). In case 10 the gate current has the normal 1μsecond rise time. In Case 11 it has a zero second rise time. Note that the delay time in Case 10, ∿.4 μseconds, is what is observed in practice. Also note that there is very little difference in ΔT values.

Cases 8 and 9 predict what would happen with no amplifying stages. One shot would fail the device. Note that the gate stage dissipates 344mJ of the 1J stored in the snubber while all 6 stages of the GE2 Case (Case 1) dissipate a total of only 80mJ and the G1 stage of Case 1 only .155mJ. In Case 12 we show what would happen with a single, very sensitive gate stage directly

turning on a main stage of normal sensitivity. The G1 stage ΔT is cut from 800°C to 24.7°C which is still probably unacceptable. In Case 13 a second amplifying stage is added. Now the G1 ΔT value is reduced to 7.7°C. The only conclusion that can be drawn is that more stages with less gain between stages lowers total energy dissipation in the amplifying stage and therefore lowers temperature excursions. Increased delay time between Case 8 (no amplifying stages) and Case 1 (5 amplifying stages) is only 70 nanoseconds while voltage fall time in Case 1 is actually 5μseconds less.

CONCLUSIONS

In the initial stages of Phase II, a number of new design concepts which should reduce temperature excursions and improve di/dt capability were incorporated into three basic designs with a number of variations. The basic designs were investigated with a computer turn-on model and compared in a consistent manner with the GE1 design[1] and with the regular electrically fired 2.6 kV HVDC thyristor. For turn-on at high voltage the new designs were predicted to be superior and the increase in amplifying stages seems to be beneficial. Some other interesting results were also found. First, turn-on delay time is primarily a function of the overdrive of the first stage. Second, turn-on delay time at high voltage is not materially increased by inserting intermediate amplifying stages but these stages can actually reduce the fall time portion of the turn-on characteristic. Third, series base impedance was shown to be beneficial to a lesser degree than one would have expected. Fourth, the total area of inner amplifying stages turned on by spreading effects was generally small, e.g. .005mm^2 for G1 in Case 1.

Finally, it is instructive to restate here some of the provisions and assumptions on which the calculations were based. These start out with the selection of Y_1 values (see Eqn. 2-1) for our "S" elements of the model in Figure 3-6. They include, after this, the assumption that the entire turn-on periphery be turned

on by the gate signal and that the initial turn-on area is assumed to be evenly distributed between anode and cathode and the spread of the on-region is assumed to follow from the relationship in Eqn. 3-1. This last assumption has most effect on non-amplifying gate structures and the final stage (M) of amplifying structures while the other assumptions affect all designs in a roughly similar manner. This is to make the stated ΔT value into an "ideal" or lowest value. It should be noted that Y_1 values (related to S1 values in Appendix A) were taken from a 25°C turn-on trace and are themselves not highly accurate. However it is important to note that comparison between designs are likely to be more reliable.

Section 4

PHASE II DEVICE TESTS

INTRODUCTION

This section of the report deals with test data taken on the Phase II versions of the EPRI-GE1 light fired HVDC thyristor. Test data taken includes measurements of base resistances needed for computer analysis as well as the usual parameters such as blocking voltage, leakage current, dv/dt capability and turn-on threshold levels. However, most of the emphasis of the tests done on the first run of devices is on di/dt capability. To this end, di/dt tests at and above HVDC stress levels were performed at CRD and SPCO. Results indicate much improved performance compared to the EPRI-GE1 of Phase I with most devices surviving a 25Hz, 100°C snubber discharge of .5μ farads through 10 ohms. In the most critical test where a current ramp to 1000 amperes at a specific di/dt is added to a snubber discharge (.5μF, 35 ohms), the survival rate is much reduced. Device failure modes are discussed and improvements in the computer modeling procedure are suggested. The make-up of the second run of devices is also discussed as well as a process modification which would remove one of the two dominant failure modes which were identified.

NON DI/DT TEST RESULTS

After fabrication of the devices a normal test sequence was carried out including forward and reverse blocking capability at room (25°C) and elevated (125°C) temperatures. The results tabulated in Table 4-1 are in the normal range of the electrically fired counterpart. Device dv/dt capability, also listed in Table 4-1, was also found to lie in the normal range. A measurement of the gate thresholds at low and high base current given in Tables 4-2 to 4-4 confirmed that the devices were capable of being turned on with 5 to 7 mA of gate current. These threshold levels were a factor of 2 higher

TABLE 4-1: DEVICE BREAKDOWN VOLTAGE AND dv/dt CAPABILITY

DEVICE NO.	25°C Voltage/Leakage Current FORWARD	REVERSE	125°C Leakage Current at 2600 Volts FORWARD	REVERSE	dv/dt
3A1	2900/>1mA	2800/N.R.	2600/35	1500	2200
3A2	2600/1.5	3040/4→N.R.	2600/40	2600/25	1870
3A3	2800/>1mA	3040/N.R.	2600/35	2000	
3A4	2600/-	3040/2→N.R.	2600/40	2200/50	>2000
3A5	2600/-	2900/N.R.	2600/30	2600/10	1760
3B1	2600/-	2900/7→N.R.	2600/35	2600/15	>2000
3B2	2650/1	3140/10	2600/40	2600/15	>2000
3B3	2600/-	2830/10	2600/40	2600/30	1900
3B4	2600/-	2990/10	2600/35	2600/15	>2000
3B5	2600/-	2930/1.5→N.R.	1000/50	1000/30	1900
3C1	2600/-	3080/N.R.	2600/40	2600/15	1900
3C2	2600/-	3000/N.R.	2600/40	2600/15	1850
3C3	2600/-	3020/8→N.R.	2600/35	2600/20	>2000
3C4	2600/-	3130/10	2600/35	2600/20	1900
3D1	2650/2	2930/N.R.	2600/30	2600/.7	1950
3D2	2600/-	2930/N.R.	2600/35	2600/10	>2000
3D3	2050/1	2550/5	2400/50	1700/30	>2000
4A2	2600/-	3000/3	2600/15	2600/30	2120
2C2	2600/-	2890/10 N.R.	2600/65	2600/15	1880
4B3	2600/-	--	2600/65	--	2020
4A4	2600/-	2770/N.R.	2600/40	2600/20	1920
2C1	2600/-	3000/N.R.	2600/35	2600/20	2050
2C2	2600/10	3000/N.R.	2600/55	2600/20	2000
3A2	2600/-	--	2600/30	--	2010
4C2	2600/0	2940/40 No S.F. 3000/-	2600/40	2600/15	1900
2A3	1500/7 Loop & S.F.	2840/N.R.	1100/20 S.F.	2600/15	--
4C3	2600/-	2900/N.R.	2600/35	1100/15	
4B2	2600/-	2870/N.A.	2600/30	2600/25	2000
2B2	2600/1.5	3000/N.R.	2600/30	2600/20	2020
3A1	2600/-	2830/10	2500/30	900	
2A1	2600/-	2520/20	2600/30 S.F.	2300	
2B1	2600/1.5	2900/N.R.			
2B1	2600/1.5	2900/N.R.	2600/35	2600/15	2000
4C1	2600/-	1500/5	2600/30	--	1880
4A3	2600/-	2750/10	2600/35	2600/20	2100
4B1	2600/-	800/10	2600/35	--	1940
4A1	2600/-	2970/N.R.	2600/35	2600/20	1970

NOTES:
1. N.R. denotes negative resistance.
2. The dv/dt column lists the voltage that a 2000v/μsecond dV/dt ramp was able to reach before the device fired. The measurement is made at 105°C.
3. S.F. denotes self-fire.

TABLE 4-2: MEASURED SENSITIVITY PARAMETERS FOR GE2 TYPE DEVICES

Device	G1 Amplifying Stage R_1, R_2, I_{GT}	G2 Amplifying Stage R_1, R_2, I_{GT}	G3 Amplifying Stage R_1, R_2, I_{GT}	P1 Amplifying Stage R_1, R_2, I_{GT}	P2 Amplifying Stage R_1, R_2, I_{GT}	Main Stage R_1, R_2, I_{GT}
2A1(#15)	No gate ring	-, -, 18.6	-, -, 30.3	-, -, 36	-, -, 72	-, -, 200
2A2(#7)	" " "	-, -, 22.1	-, -, 37.9	-, -, 41.3	-, -, 88.7	-, -, 188
2A3(#9)	" " "	-, -, 18.7	-, -, 29.9	-, -, 33.8	-, -, 75.1	-, -, 175
2B1(#16)	-, -, 6.54	-, -, 19.7	-, -, 34.2	-, -, 32.2	-, -, 71.9	-, -, 200
2B2(#12)	-, -, 6.16	-, -, 19.4	-, -, 32.0	-, -, 36.3	-, -, 78.6	-, -, 191
2C1(#5)	-, -, 6.88	-, -, 23.0	-, -, 40.4	-, -, 53.6	-, -, 79.8	-, -, 217
2C2(#6)	-,225, 6.18	-, 94, 20.2	-, 64, 34.4	-, 44, 35.0	-, 79, 67.7	-, 12, 187
2C3(#2)	-,240, 5.79	-, 96, 19.4	-, 63, 43.5	-, 48, 34.8	-, 31, 65.0	-,13.5,173

NOTES: 1. R_1 and R_2 represent the p base resistances prior to turn-on and after turn-on of the emitter-base junction.

2. I_{GT} is the gate threshold in milliamperes.

TABLE 4-3: MEASURED SENSITIVITY PARAMETERS FOR GE3 TYPE DEVICES

DEVICE	G1 Amplifying Stage R_1, R_2, I_{GT}	G2 Amplifying Stage R_1, R_2, I_{GT}	P1 Amplifying Stage R_1, R_2, I_{GT}	P2 Amplifying Stage R_1, R_2, I_{GT}	Main Stage R_1, R_2, I_{GT}
3A1	No gate ring	90,2.8, 11.5	50,3.5, 32.1	31, 2, 66.2	15,2.8, 171
	" " "	94,3.3, 13.9	44,3.5, 37.1	30,2.3, 77.0	15,2.3, 189
3A4	" " "	98,1.5, 13.2	44, 2, 32.6	31, 2, 67.6	15, 3, 192
3A5	" " "	120,1.5, 8.8	52,2.5, 26.8	33, 2, 69.7	15, 4, 195
3B2	180, 3, 5.3	106, 6, 10.6	47, 6, 36.8	34,4.5, 77.4	14,2.5, 170
3B3	160, 3, 6.2	90, 3, 13.7	42, 2, 37.4	29, 3, 79.4	14, 3, 195
3B4	165, 75, 6.1	90, 4, 12.9	44, 4, 34.2	33,3.5, 72.1	15,2.5, 203
3B5	155,5.5, 6.3	88, 4, 13.7	44, 4, 36.9	32, 3, 76.8	14, 3.5, 193
3C2	190, 4, 5.1	105, 7, 11.5	43, 3, 34.2	25,2.5, 71.7	14, 4, 207
3C3	160 5, 6.6	83, 5, 15.0	45, 6, 40.4	27, 3, 86.0	12,3.5, 195
3C4	200, 4, 5.0	105, 6, 10.8	43, 5, 33.0	30, 3, 73.1	15,3.5, 201
3D2*	160, 6, 6.7	85, 6, 15.4	40, 15, 38.1	28, 7, 84.5	12, 6, 221
3D3*	190, 6, 5.4	100, 10, 12.8	42, 3, 33.7	28, 3, 77.0	11, 4, 224

NOTES: 1. R_1 and R_2 represent the p base resistances prior to turn-on and after turn-on of the emitter base junction.

2. I_{GT} is the gate threshold in milliamperes.

* These devices have an interrupted metal n^+ region measuring 2 and 1.5 ohms, respectively.

TABLE 4-4: MEASURED SENSITIVITY PARAMETERS FOR GE4 TYPE DEVICES

DEVICE	Gate Amplifying Stage			Pilot Amplifying Stage			Main Stage		
	R_1	R_2	I_{GT}	R_1	R_2	I_{GT}	R_1	R_2	I_{GT}
4A1	No gate ring			29	2	70.0	14	2	179
4A2	" " "			27	1.6	73.4	13	2	170
4A3	" " "			29	2.3	80.4	12	2	183
4A4	" " "			25	1.3	89.6	12.5	1.8	186
4B1	210	3	5.3	24	2	74.2	14	12.5	163
4B2	170	2.5	6.5	25	2	92.1	12	2	197
4B3	200	3	5.2	28	1.8	74.6	13.5	1.8	171
4C1	215	2.6	5.8	32	2.8	77.4	13.5	1.8	176
4C2	210	2.5	6.1	27	2	77.5	12.5	2.2	181
4C3	240	2.5	5.0	31	2	76.6	13.5	1.8	171

NOTES: 1. R_1 and R_2 represent the p base resistance before and after turn-on of the emitter-base junction.

2. I_{GT} is the gate threshold in milliamperes.

than we were aiming for but can easily be modified in the next (second) run of devices.

The resistances listed in Tables 4-2 to 4-4 were measured to use in computer analysis of device di/dt. These resistances are simply measured by isolating each amplifying stage in turn and examining the gate-emitter I-V characteristic (anode open circuit). The two slopes measured asymptotically give the pre-turn-on (unmodulated) and after turn-on (modulated) base resistances which play a critical role in the turn-on process.

Parameters exhaustively measured for the EPRI-GE1 device such as delay time as a function of temperature, voltage and gate drive level, were measured only on a few devices. However, a large number of delay time and turn-on time vs. anode voltage characteristics were made for what will be termed the "threshold pulse condition". In this and succeeding discussion the threshold pulse refers to a light pulse of sufficient amplitude to just fire the thyristor at 50 volts at room (25°C) temperature. Figures 4-1 to 4-12 show delay time and turn-on time at 25°C and at elevated temperature for A, B and C versionsof EPRI-GE2, EPRI-GE3 and EPRI-GE4 devices. Basically, all devices tested showed the same basic qualities - first a reduction in turn-on time at 25°C at 1500 to 2000 volts to the 1 to 1.5μsecond region, and second, a voltage fall time (turn-on time minus delay time) which was about 50% larger at elevated temperature than at 25°C. When all curves are compared it is clear that, though the "threshold gate pulse" may be at threshold level at 50 volts, the improved photo-response of the thyristor at elevated temperature turns this pulse into a pulse of several times the threshold level at elevated voltage. The effect of voltage on photo-response shown in Figure 4-13 illustrates this important point. Recall, for example, that it has been critical for electrically gated devices to supply about 10 times the gate threshold energy (current) for safe turn-on under high di/dt stress conditions.

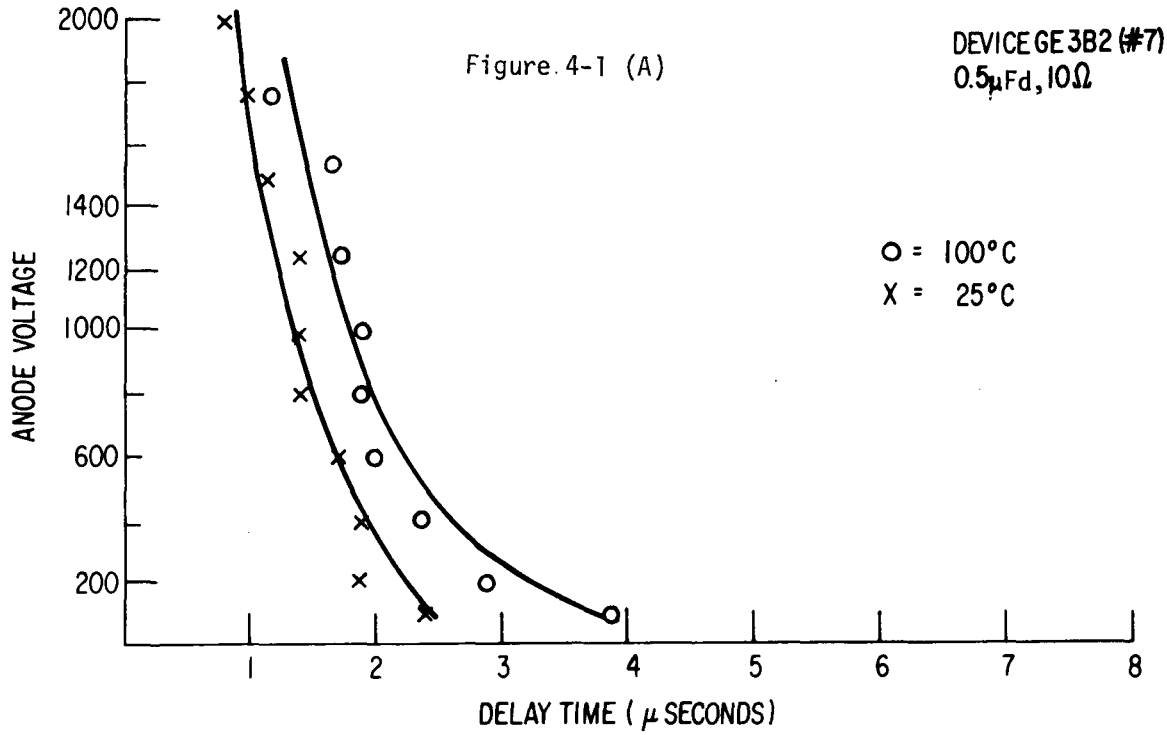


Figure 4-1 (A)

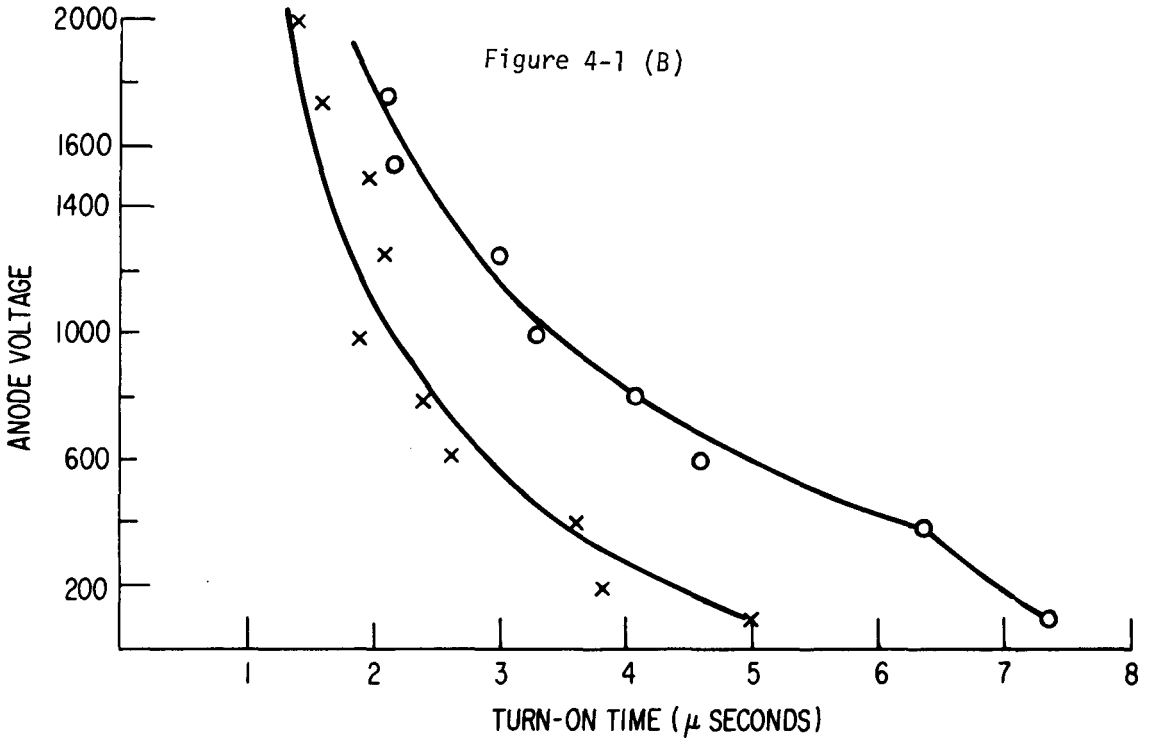


Figure 4-1 (B)

Figure 4-2 (A)

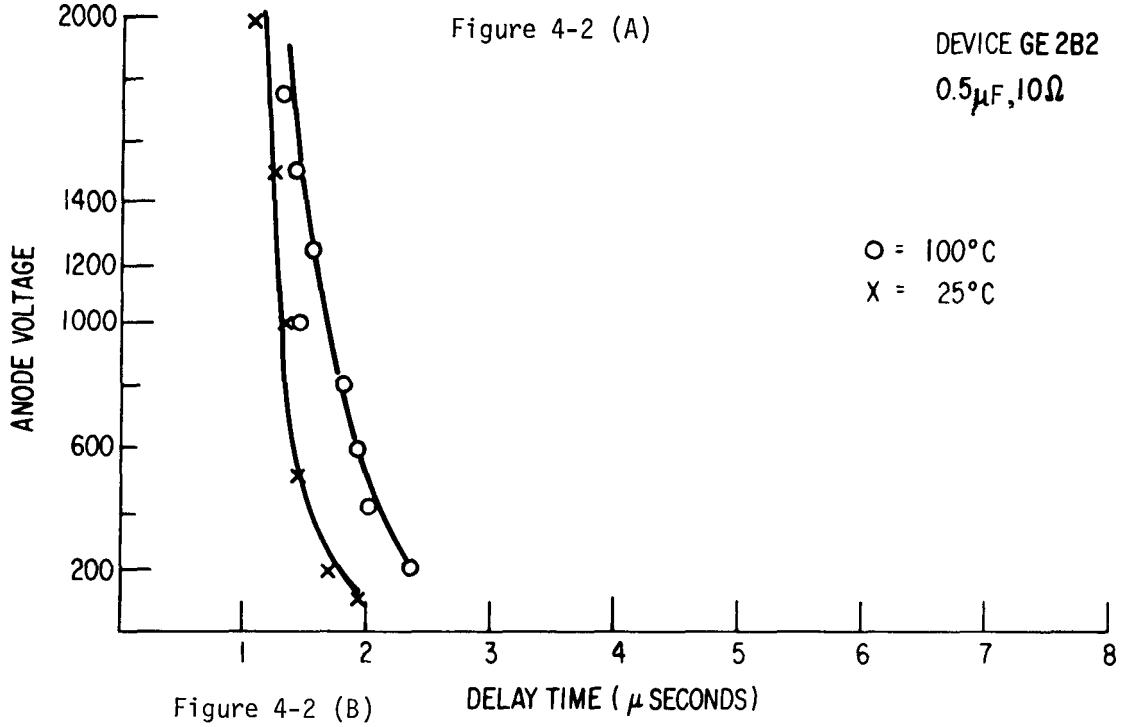


Figure 4-2 (B)

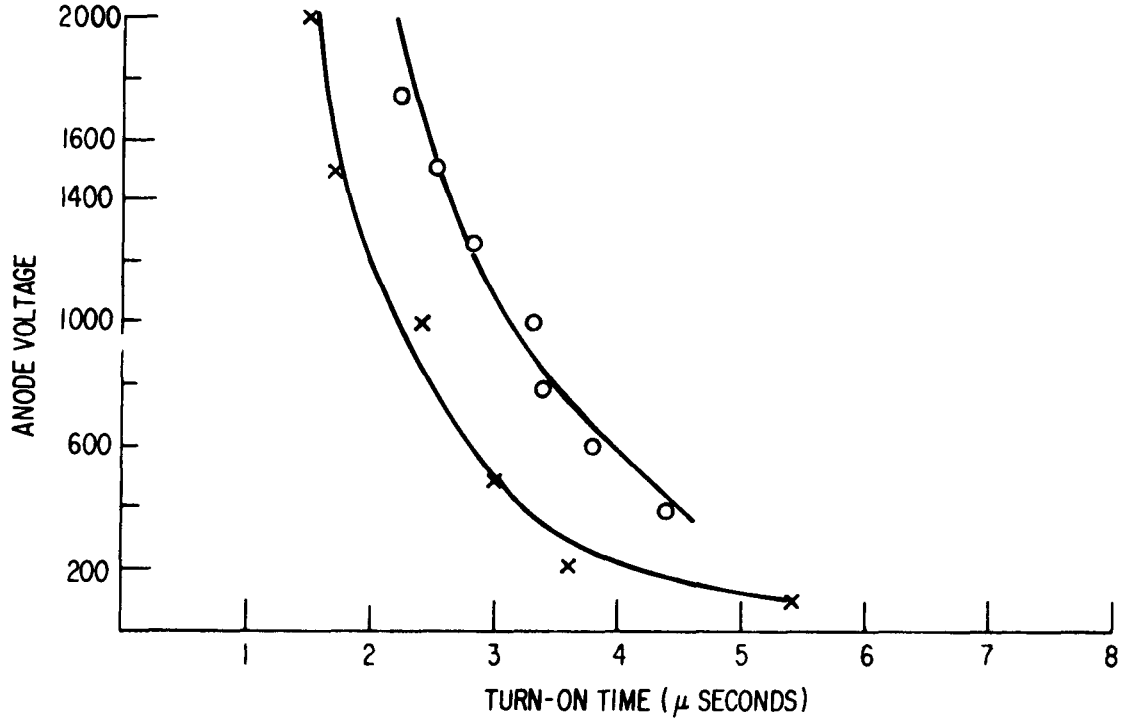


Figure 4-3 (A)

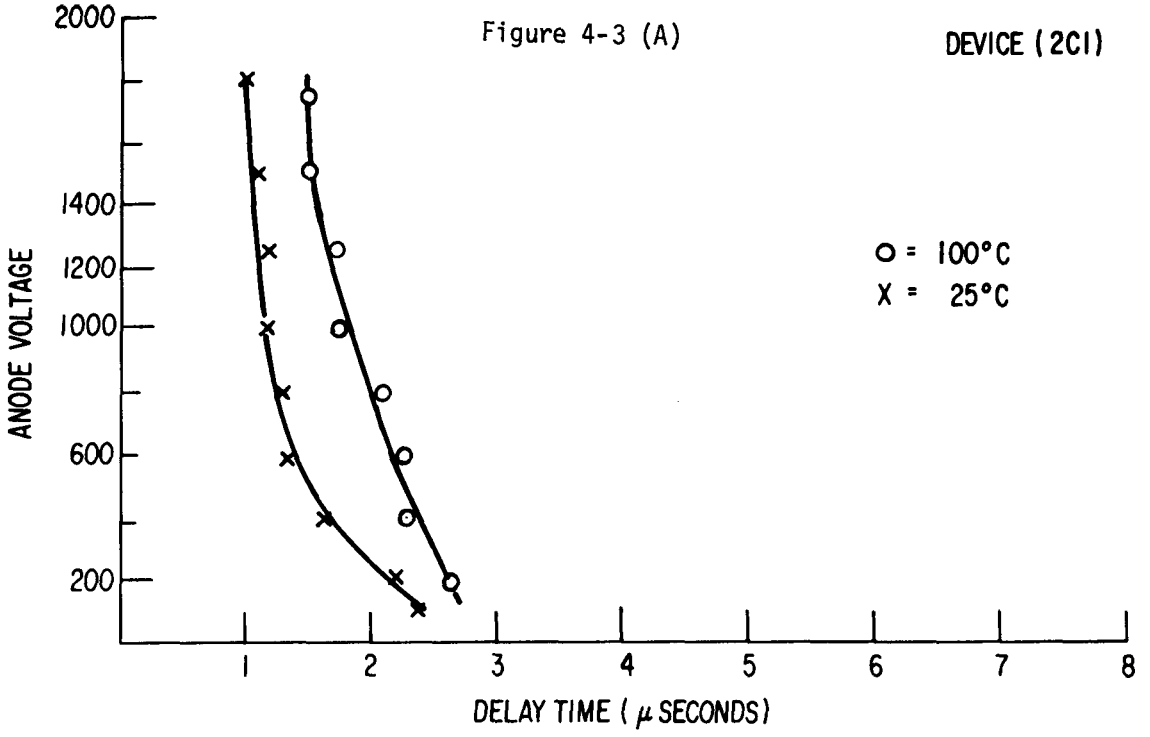
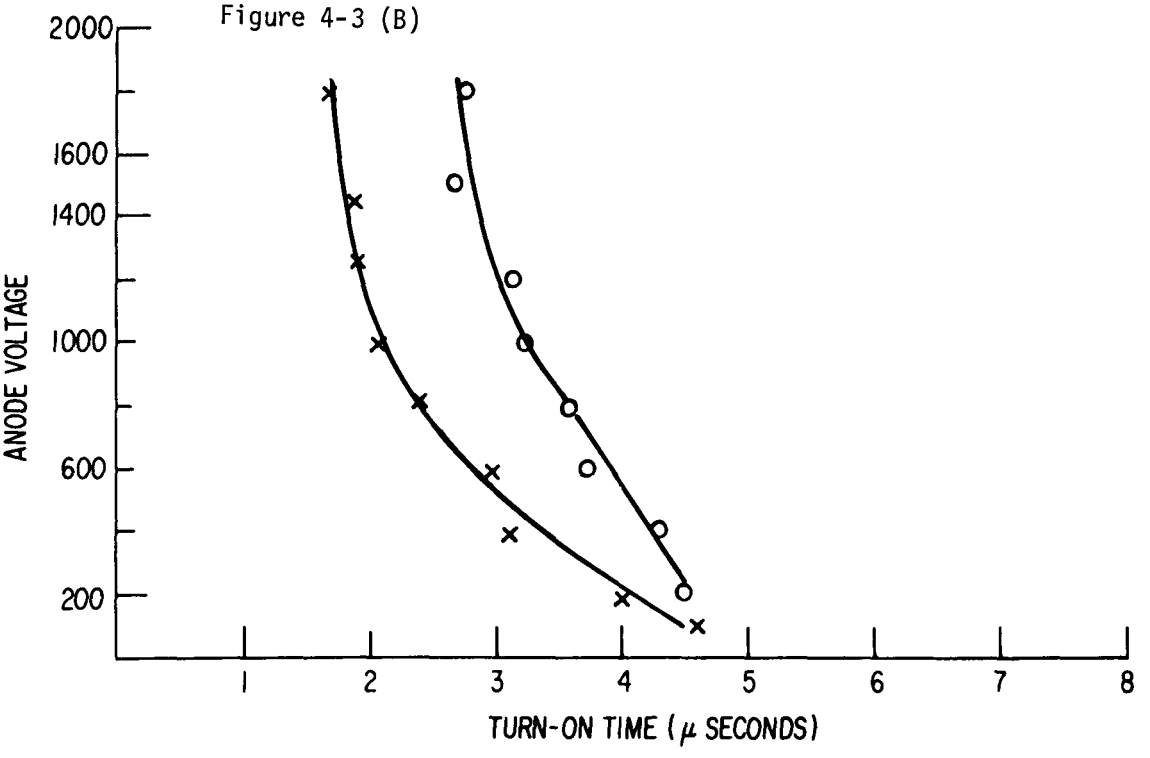


Figure 4-3 (B)



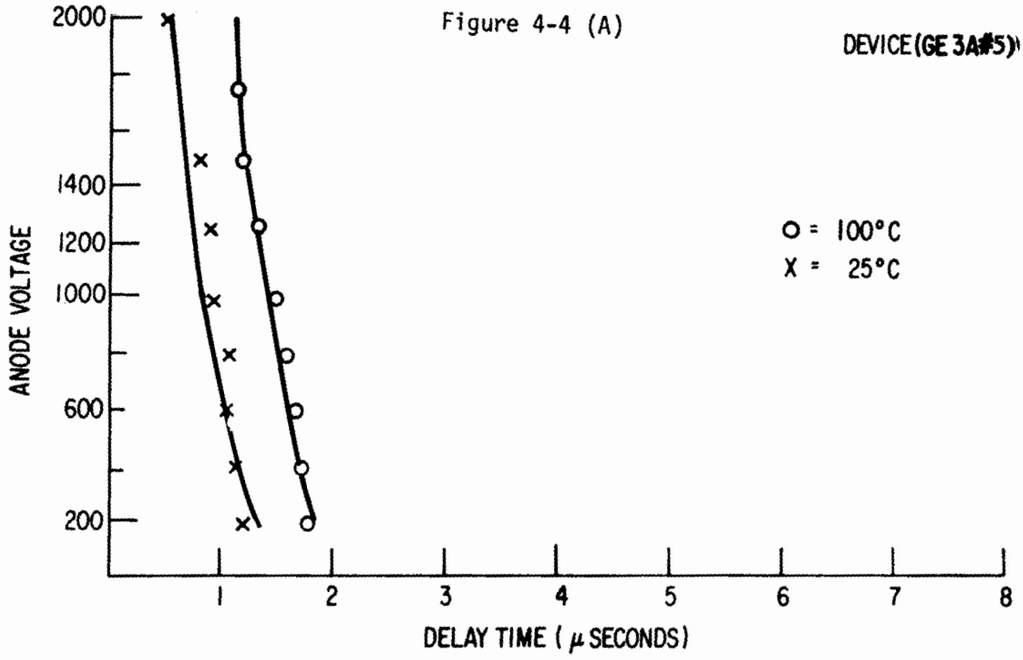


Figure 4-4 (A)

DEVICE (GE 3A#5)

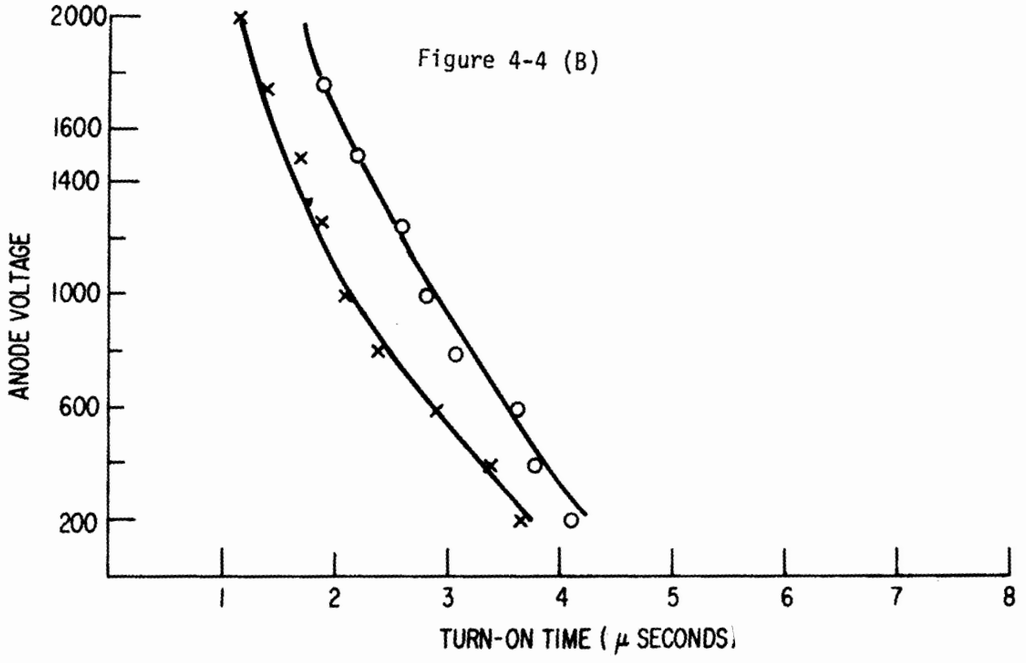


Figure 4-4 (B)

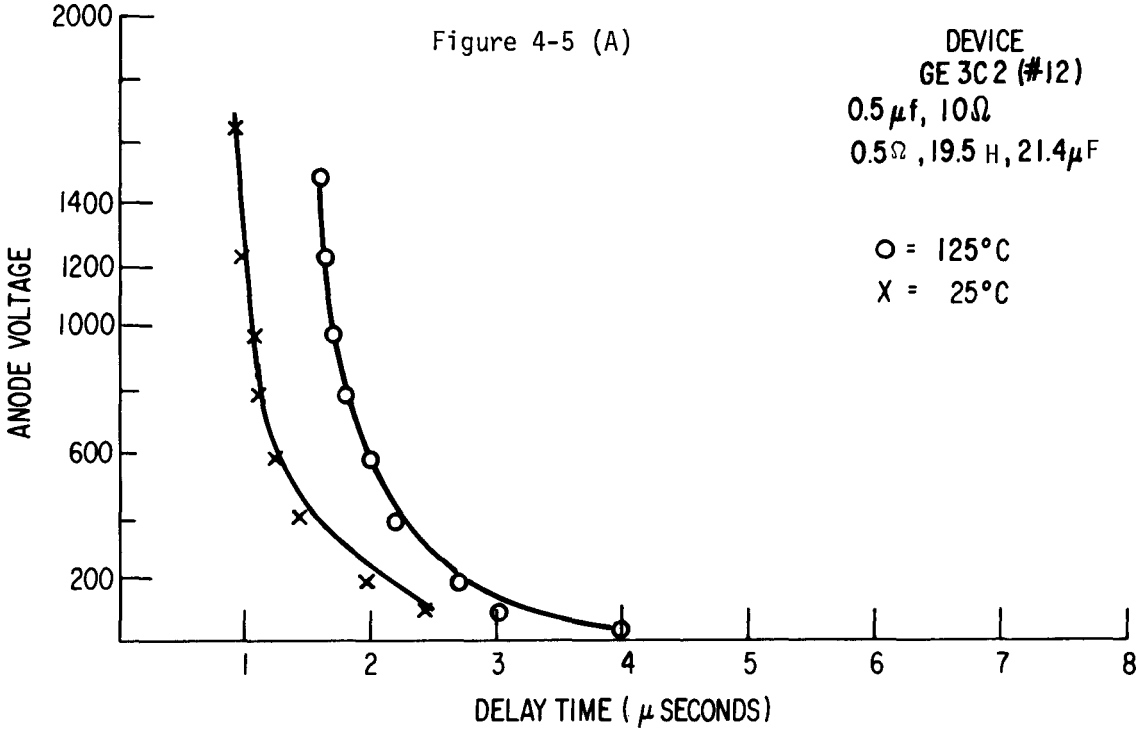


Figure 4-5 (A)
DEVICE
GE 3C2 (#12)
0.5 μf, 10Ω
0.5Ω, 19.5 H, 21.4μF
O = 125°C
X = 25°C
ANODE VOLTAGE
2000
1400
1200
1000
600
200
1
2
3
4
5
6
7
8
DELAY TIME (μ SECONDS)

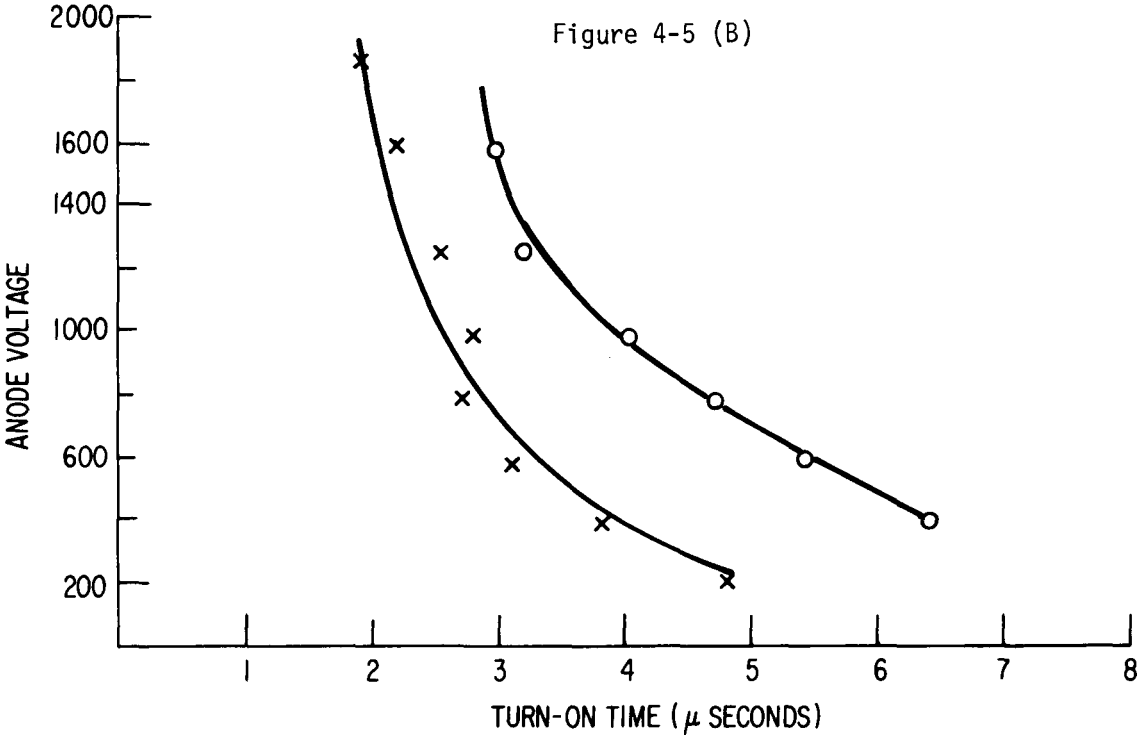


Figure 4-5 (B)
ANODE VOLTAGE
2000
1600
1400
1000
600
200
1
2
3
4
5
6
7
8
TURN-ON TIME (μ SECONDS)

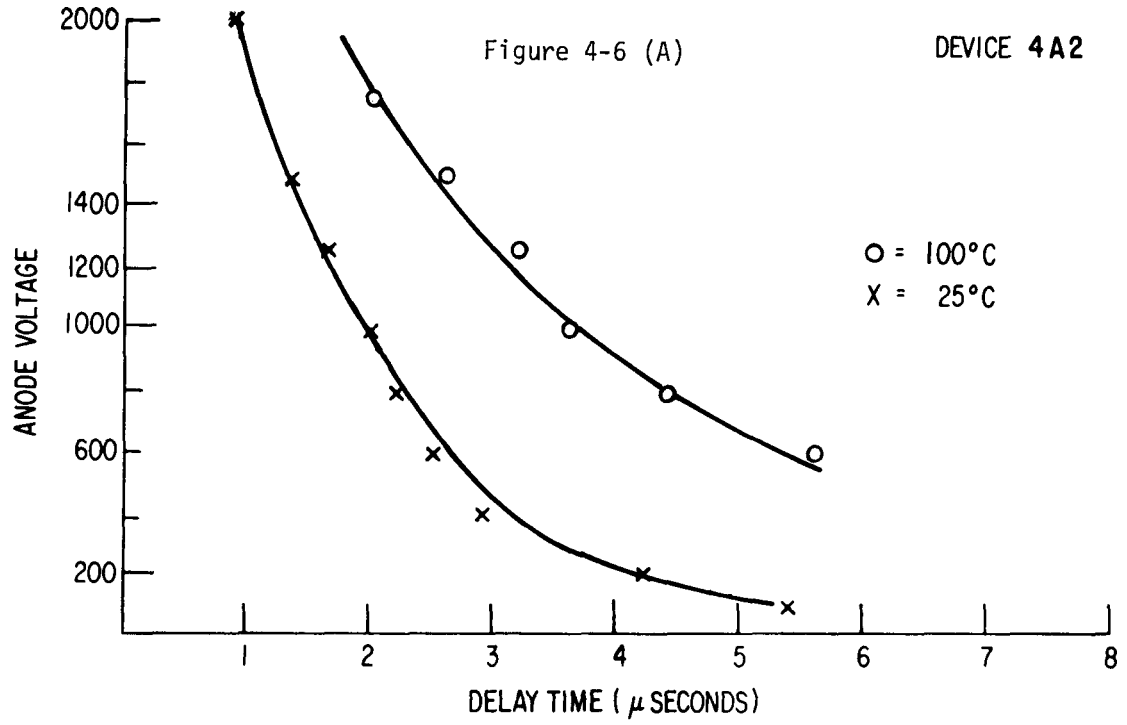


Figure 4-6 (A)
DEVICE 4A2
2000
1400
1200
1000
600
200
ANODE VOLTAGE
O = 100°C
X = 25°C
1
2
3
4
5
6
7
8
DELAY TIME (μ SECONDS)

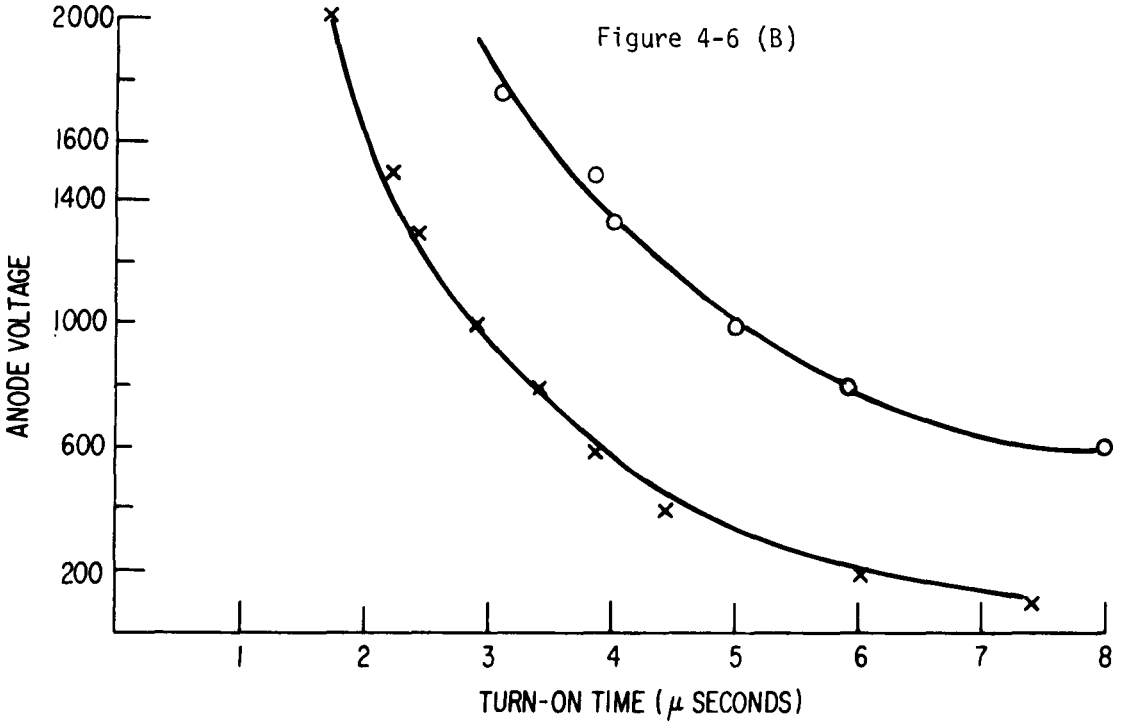


Figure 4-6 (B)
2000
1600
1400
1000
600
200
ANODE VOLTAGE
1
2
3
4
5
6
7
8
TURN-ON TIME (μ SECONDS)

Figure 4-7 (A)

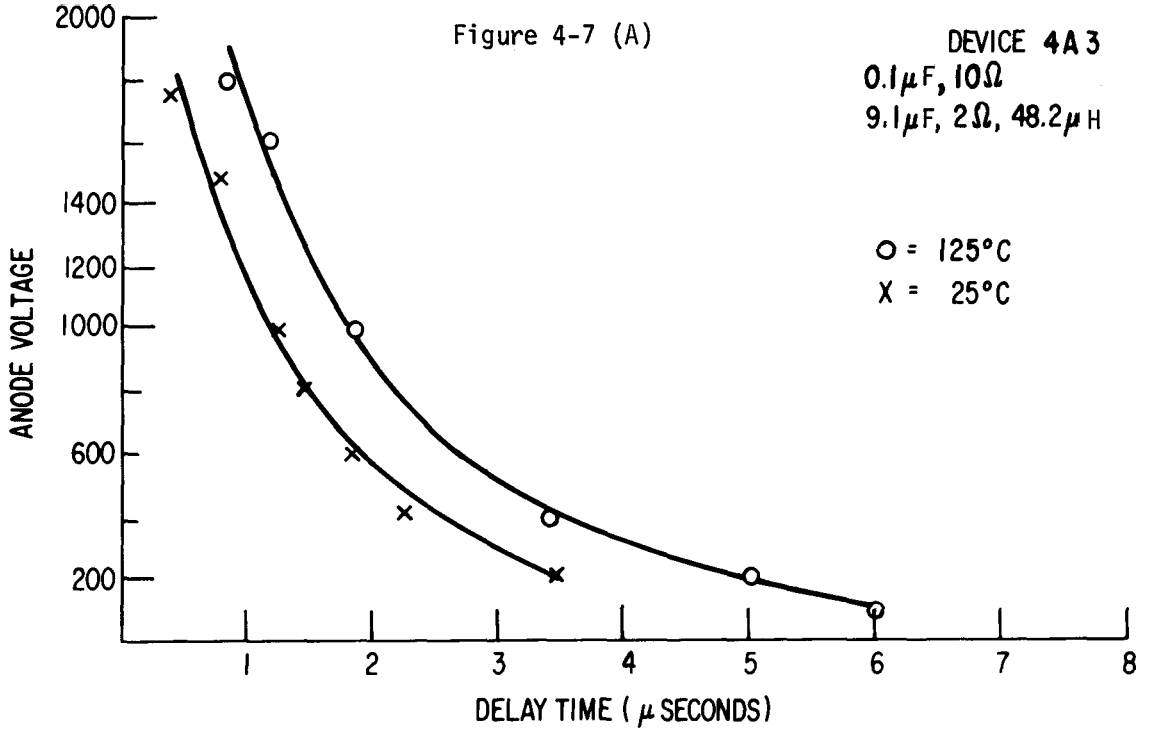
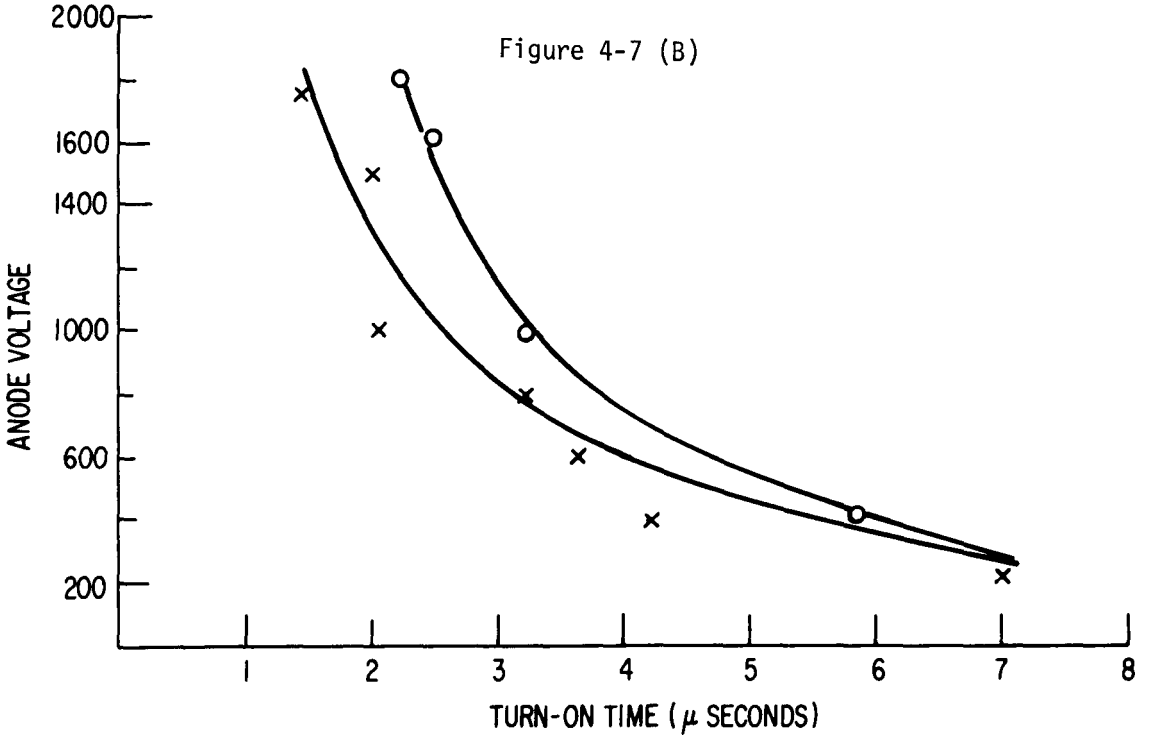


Figure 4-7 (B)



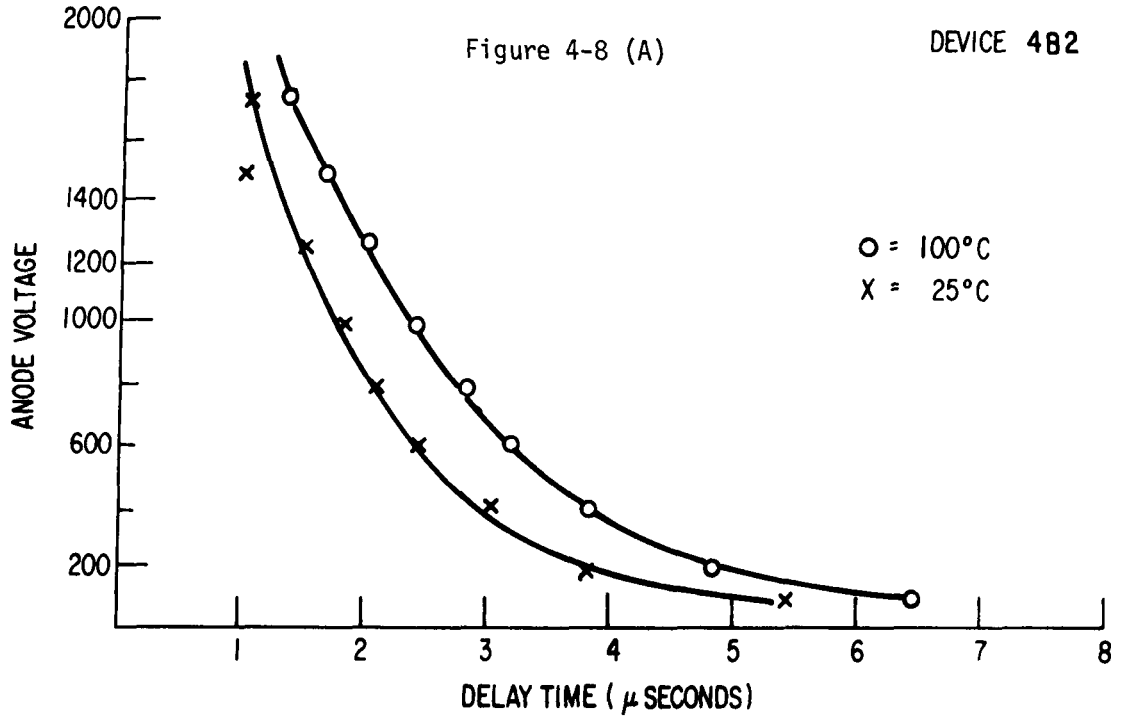


Figure 4-8 (A)
DEVICE 482
2000
1400
1200
1000
600
200
ANODE VOLTAGE
O = 100°C
X = 25°C
1
2
3
4
5
6
7
8
DELAY TIME (μ SECONDS)

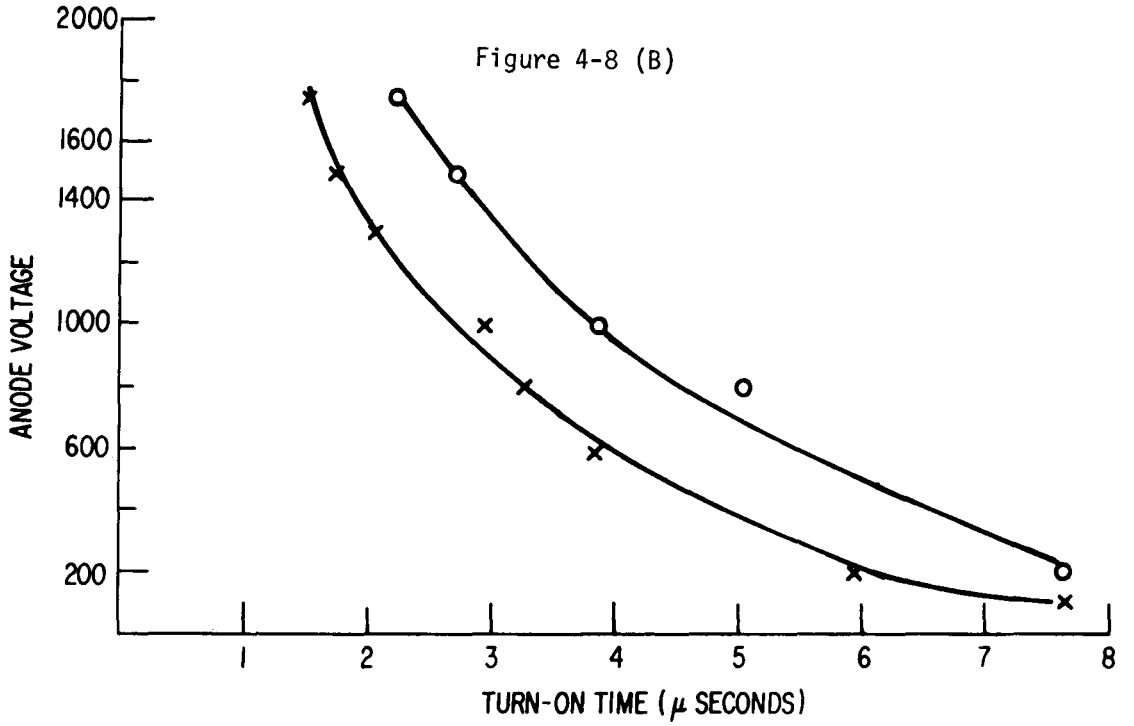


Figure 4-8 (B)
2000
1600
1400
1000
600
200
ANODE VOLTAGE
1
2
3
4
5
6
7
8
TURN-ON TIME (μ SECONDS)

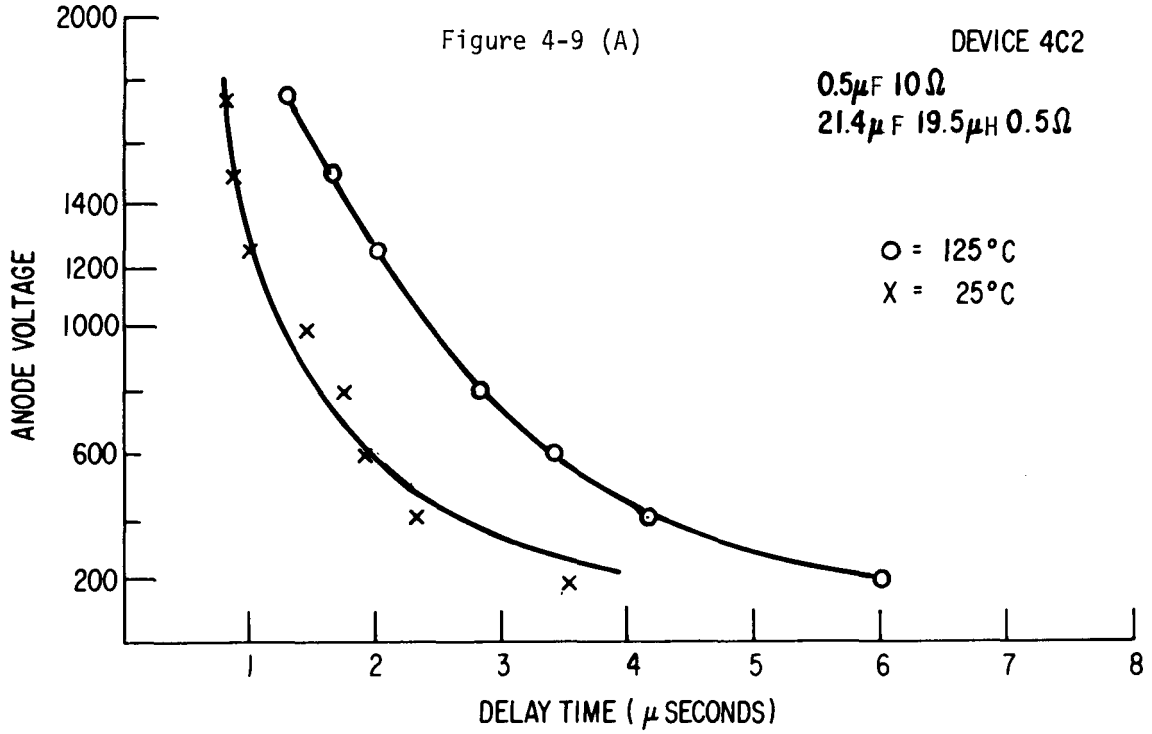


Figure 4-9 (A)
DEVICE 4C2
0.5μF 10Ω
21.4μF 19.5μH 0.5Ω
O = 125°C
X = 25°C
ANODE VOLTAGE
2000
1400
1200
1000
600
200
1
2
3
4
5
6
7
8
DELAY TIME (μ SECONDS)

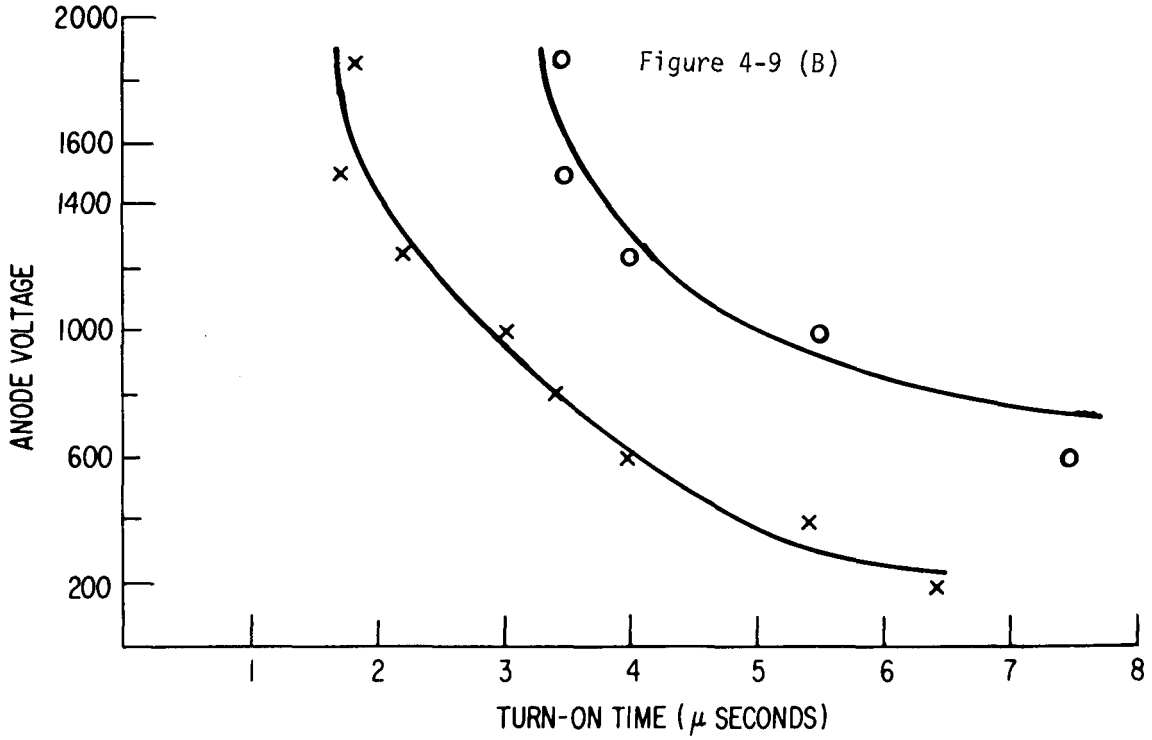


Figure 4-9 (B)
ANODE VOLTAGE
2000
1600
1400
1000
600
200
1
2
3
4
5
6
7
8
TURN-ON TIME (μ SECONDS)

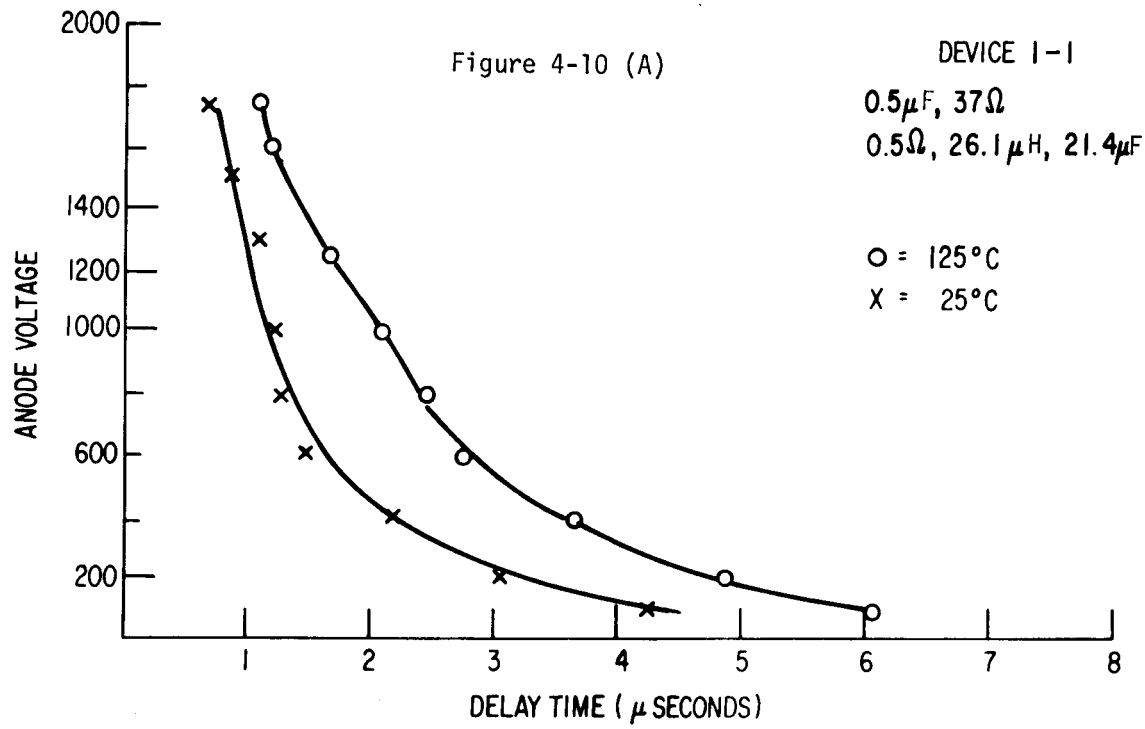


Figure 4-10 (A)

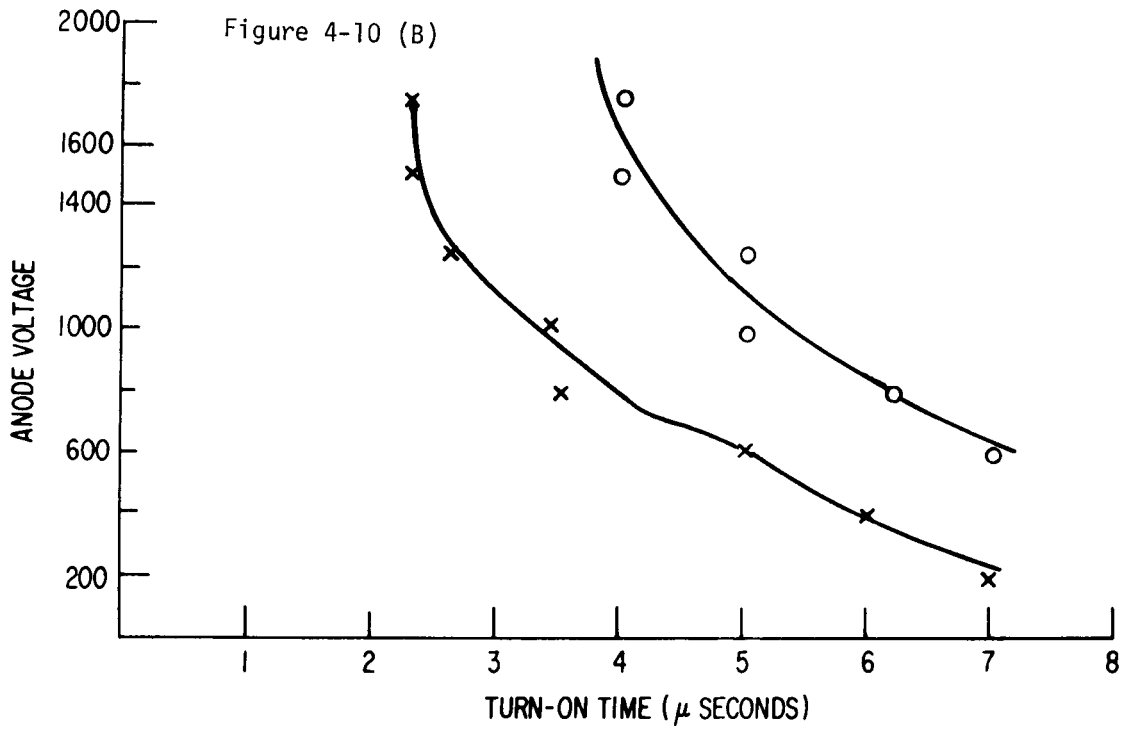


Figure 4-10 (B)

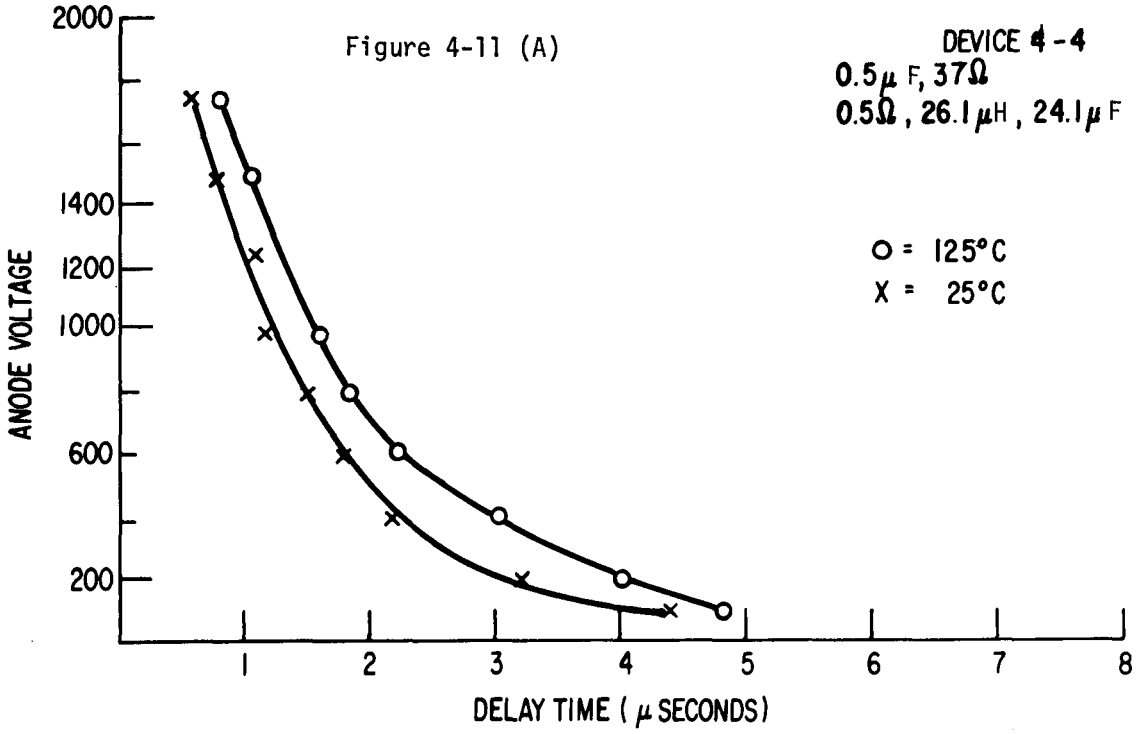


Figure 4-11 (A)
DEVICE 4-4
0.5μ F, 37Ω
0.5Ω, 26.1μH, 24.1μ F
O = 125°C
X = 25°C
ANODE VOLTAGE
2000
1400
1200
1000
600
200
1
2
3
4
5
6
7
8
DELAY TIME (μ SECONDS)

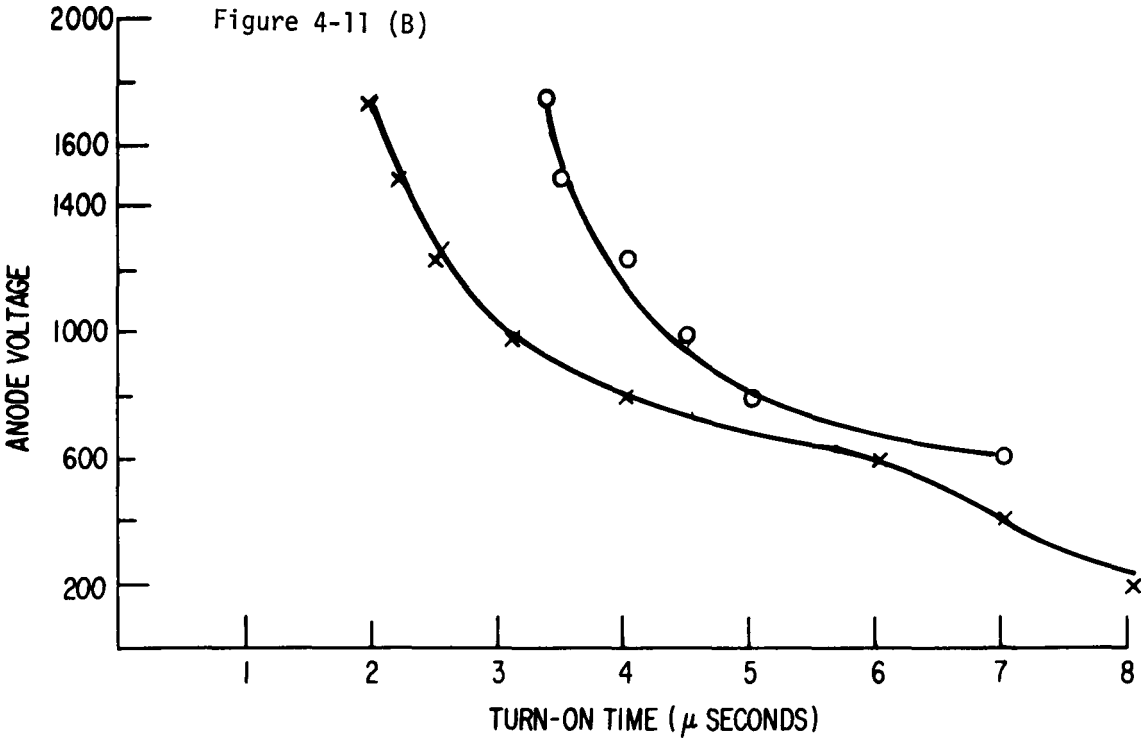


Figure 4-11 (B)
ANODE VOLTAGE
2000
1600
1400
1000
600
200
1
2
3
4
5
6
7
8
TURN-ON TIME (μ SECONDS)

Figure 4-12 (A)

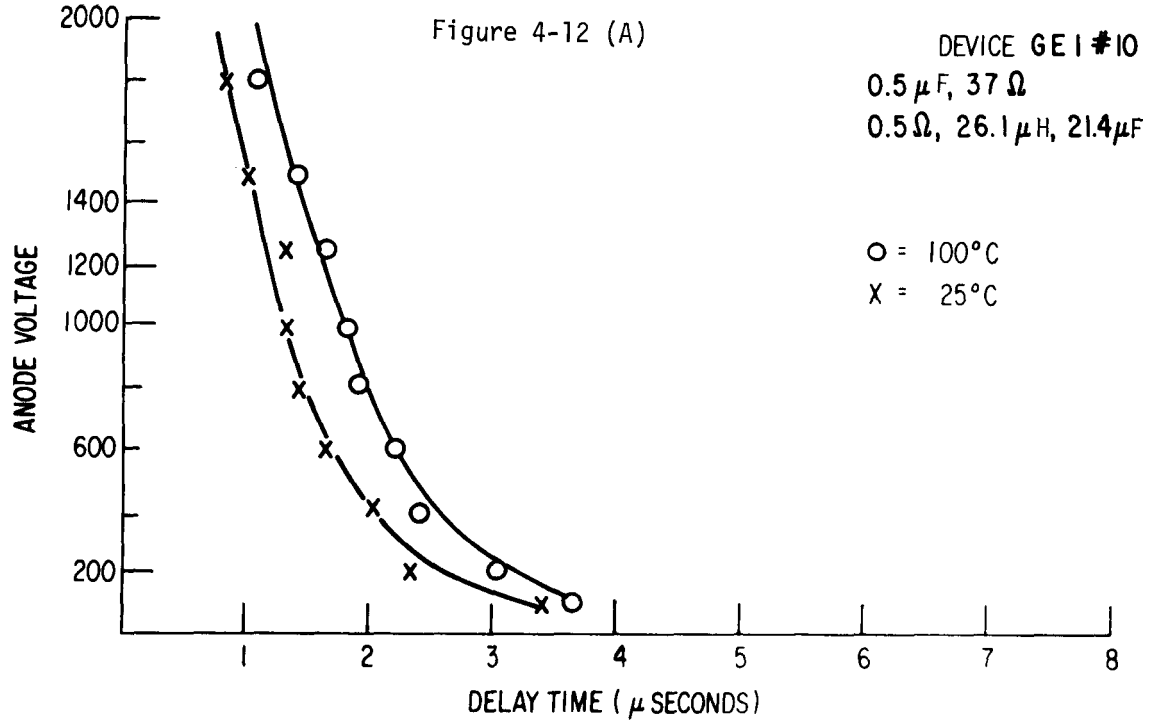
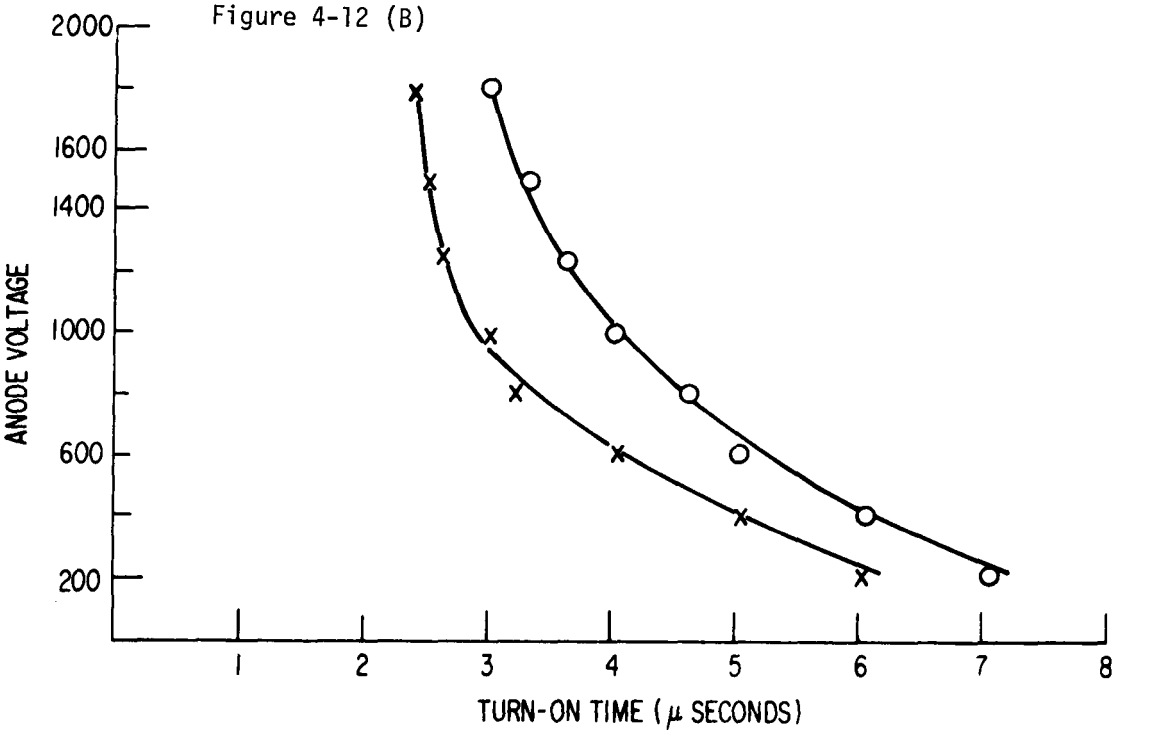


Figure 4-12 (B)



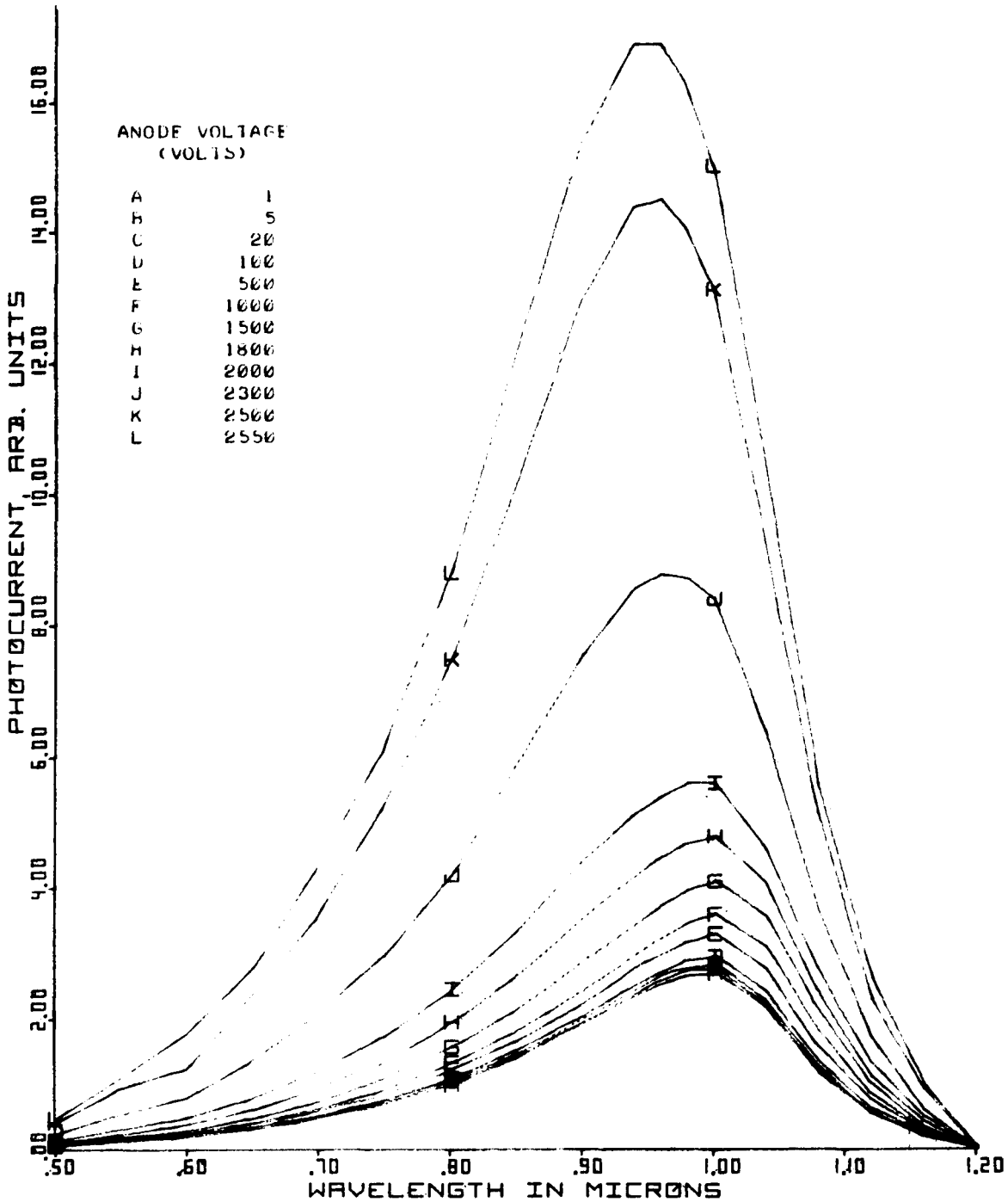


Figure 4-13: Typical EPRI-GE Light Fired Thyristor photoresponse.

DI/DT TESTS AT MODERATE DI/DT

Figure 4-14 shows the di/dt test equipment used in some of the tests discussed in this section. Tests were performed at 11 cycles per second and later at 60 cycles per second. Junction temperatures based on measured case temperatures ranged from 35°C to 120°C.

Examination of the circuit in Figure 4-14 shows that the source of di/dt impulse currents are the snubber capacitor, C_S, with a peak current amplitude of approximately V_A/R_S and the capacitor, C, which supplies a current at V_A/L amperes/μsecond, which, if C is sufficiently large, approaches V_A/R. Figure 4-15 shows a typical test waveform. The current zero is at the top and the voltage zero at the bottom. Scales are marked in the figure. Figure 4-15A shows the current waveform rising to 700 amperes in a 1500 volt turn-on test. The rapidly rising current at the left is the snubber discharge. Figure 4-15B shows the same turn-on at 1μsecond/div. The snubber discharge is approximately 160 amperes peak and the follow-on di/dt from capacitor C is approximately 40A/μsec. With a larger snubber capacitor and a smaller snubber resistor the snubber discharge current peak is more distinct. Figure 4-15C shows turn-on traces from 100 to 500 volts with a .5μF, 1.25 ohm snubber. If the current and voltage waveforms are examined closely it can be seen that nearly the entire turn-on energy dissipation in the device is due to snubber discharge. In an actual HVDC system the snubber may contain a saturable reactor. In that case the largest part of the initial turn-on power dissipation is likely to be the discharge of self and stray capacitance.

Snubber Discharge Tests

Because snubber discharge is so important a concern, a large sample of the devices were pre-screened for snubber discharge alone before being tested in the di/dt test equipment. With an oven temperature of 100°, 13 of 15 devices showed no degradation on being triggered on with the so-called "threshold gate pulse" from an anode voltage of 1750 volts. The devices

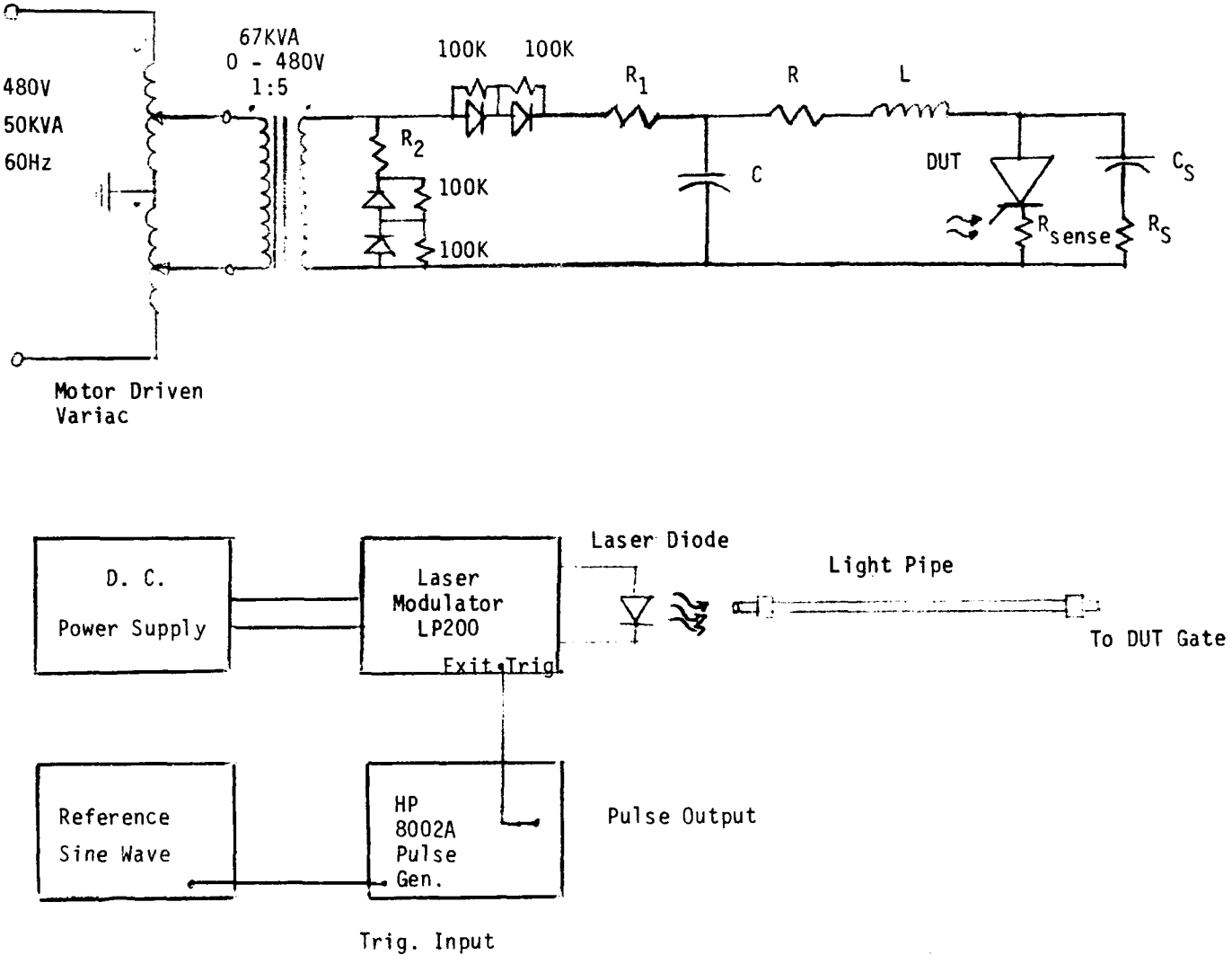
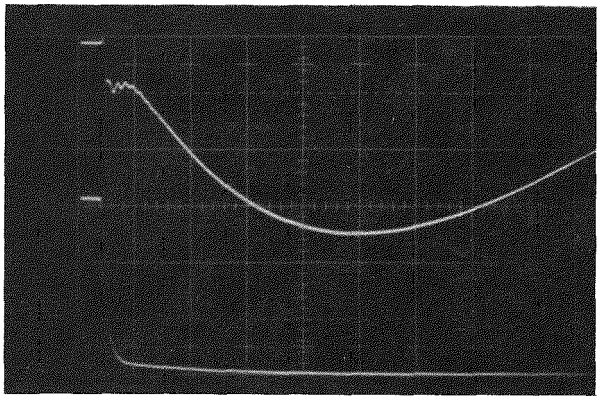


Figure 4-14: di/dt Test Circuit Diagram.



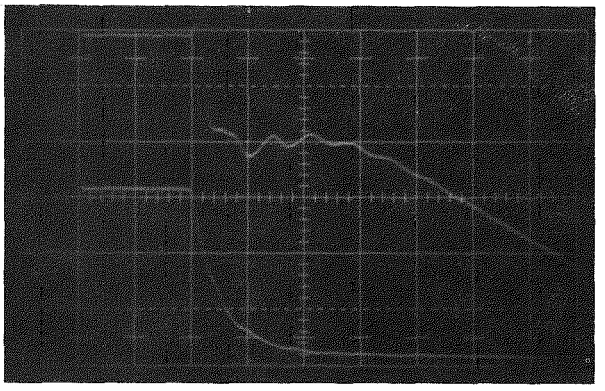
(A) Device 4A3

Snubber = .1μF, 10Ω
R, L, C = 2Ω, 48.2μH, 9.1μF

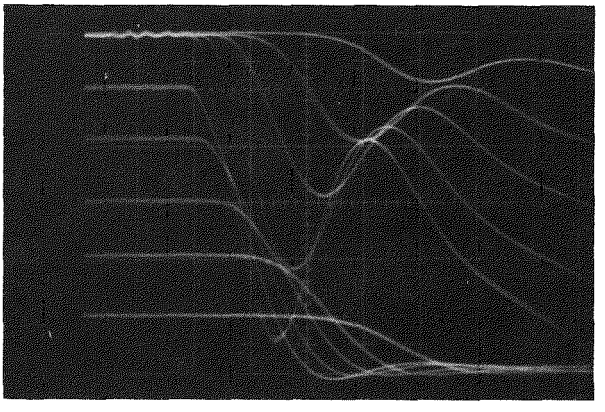
Top Trace: I_{SCR}, 200A/div

Bottom Trace: V_{SCR}, 500V/div

100°C, 5μsec/div



(B) Same as (A) above except
1μsec/div



(C) Same as (A) above except
(i) T = 125°C
(ii) Snubber = .5μF, 1.25Ω

Figure 4-15: di/dt Test Waveforms.

tested, test conditions and results are given in the first section of Table 4-5. Unfortunately the turn-on repetition rate was only 25Hz due to power supply limitations. Note however that no EPRI-GE1 devices passed this same test[1].

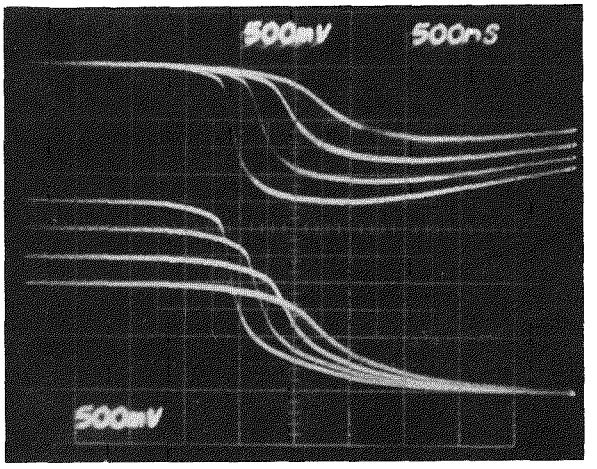
With a sufficiently large C_S, a sufficiently small R_S, and little or no snubber circuit inductance, it is possible to infer device characteristics by carefully examining snubber discharge characteristics. This is because the initial device di/dt is largely controlled by the thyristor physics, in particular the details of the thyristor turn-on process. Less information is contained in the device response to the R, L, C current pulse since its di/dt is largely controlled by inductor L. Consequently a comparison of the EPRI-GE2, GE3 and GE4 devices is best illustrated by snubber discharge tests.

Figure 4-16 shows three 100°C snubber response photographs, each multitrace, and each taken at the threshold gate pulse amplitude. The turn-on traces of Figures 4-16A and B with 5 and 4 amplifying stages, respectively, show snubber current gradually increasing to about 15 to 20 amperes before the rapid current rise denotes turn-on of the pilot and main stage. In Figure 4-16C with only two amplifying stages the current rises to less than 5 amperes before the rapid current rise occurs. The difference is in the larger series base impedance that the current through the first amplifying stage(s) sees on its way to the cathode terminal. These waveforms show, as expected, that the effective impedance of the turned on thyristor changes in a more nonlinear and therefore less lossy manner with the two amplifying stage design. This conclusion has more impact when results of the HVDC di/dt stress tests are analyzed.

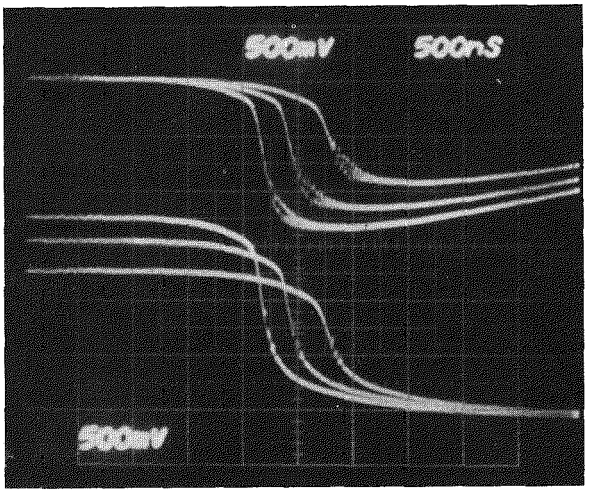
Figure 4-17 illustrates the difference in turn-on speed with device type even more clearly. Plotted are snubber di/dt for all devices tested for three voltages and two temperatures. The GE4 type has clearly the highest turn-on speed and the GE2 the slowest.

TABLE 4-5: SUMMARY OF di/dt TESTS

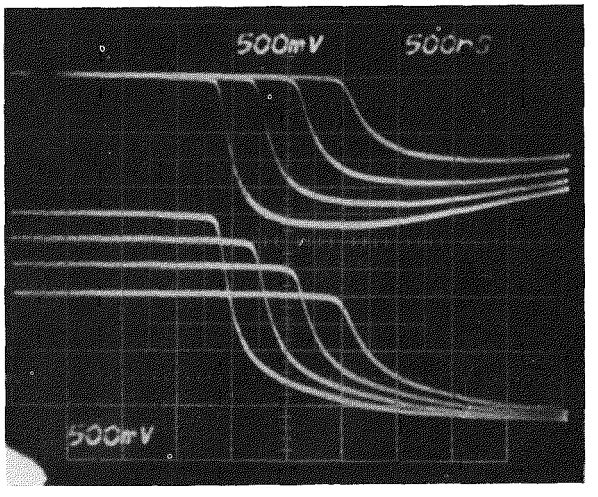
DEVICE	SNUBBER	di/dt NETWORK	TEMPERATURE TESTED	FREQUENCY	COMMENTS
2B2	.5μf, 10Ω	None	25,50,75,100	25	Passes, no noticeable degradation
4A2	" " "	"	" " " "	25	" " " "
3B7	" " "	"	" " " "	25	" " " "
4#18	" " "	"	" " " "	25	" " " "
3A5	" " "	"	" " " "	25	" " " "
3B10	" " "	"	" " " "	25	" " " "
3D17	" " "	"	" " " "	25	" " " "
3D18	" " "	"	25°C only	25	Initially leaky, shorted at 1800V, 25°C
4C1	" " "	"	25,50,75,100	25	Passes, no noticeable degradation
4B2	" " "	"	" " " "	25	" " " "
4A1	" " "	"	" " " "	25	" " " "
4A4	" " "	"	" " " "	25	" " " "
4B1	" " "	"	" " " "	25	" " " "
2C3	" " "	"	" " " "	25	Degraded in test, leaky, could test to 1300V only at 100°C
2C1	" " "	"	" " " "	25	Passes, no noticeable degradation
3#19	.5μf, 1.25Ω	9.1μf, 1Ω, 48.2μh	100	11	Fails to block after 1500V firing; stable at 1000V
4A3	.1μf, 10Ω	9.1μf, 2Ω, 48.2μh	25,100,126	11	Failed on 1800V turn-on test after ∿30 sec
	.5μf, 10Ω	9.1μf, 1Ω, 48.2μh	126		
	.5μf, 1.25Ω	9.1μf, 1Ω, 48.2μh	126		
2B1	.5μf, 10Ω	21.4μf, .5Ω, 19.5μh	25,100,127	11	Device degraded in blocking at 100°C at 1750V
	.5μf, 1.25Ω	" " "	25,103		
3-3	.5μf, 10Ω	" " "	" "	60	Device degraded at 1000V
4C2	" "	" " "	25,102,125	60	Device degraded after 40 sec at 1750V Now VBO fires at 600V
2B2	" "	" " "	25	60	Device degraded now blocks 250V
3#1	" "	" " "	25	60	Device degraded, leakage fires at 1700V
3#9	" "	" " "	25	60	Device degraded at 1500V. Now blocks 10V
3#12	" "	" " "	25,100,125	60	Degraded at 1750V. Now blocks 1000V
2C2	" "	21.4μf, .5Ω, 21.4μh	25,100,124	60	Degraded after 5 sec at 1750V. Now blocks 1500V
1-1	.5μf, 37Ω	21.4μf, .5Ω, 26.1μh	25,105,127	60	Passes, no noticeable degradation
4-2	" "	" " "	25,105,127	60	" " " "
2A2	" "	" " "	25	60	Failed at outer edge
2-3	" "	" " "	25,104.4,127	60	Device failed at outer edge after 30 sec
1-2	" "	" " "	30,105,127	60	Passes, no noticeable degradation
4-4	" "	" " "	25,103,129	60	" " " "



(A) Device 2B2
I_{SCR} 50A/div
V_{SCR} 500V/div
100°C



(B) Device 3B2
I_{SCR} 50A/div
V_{SCR} 500V/div
100°C



(C) Device 4B2
I_{SCR} 50A/div
V_{SCR} 500V/div
100°C

Figure 4-16: Comparison of EPRI-GE2, GE3 and GE4 snubber response.

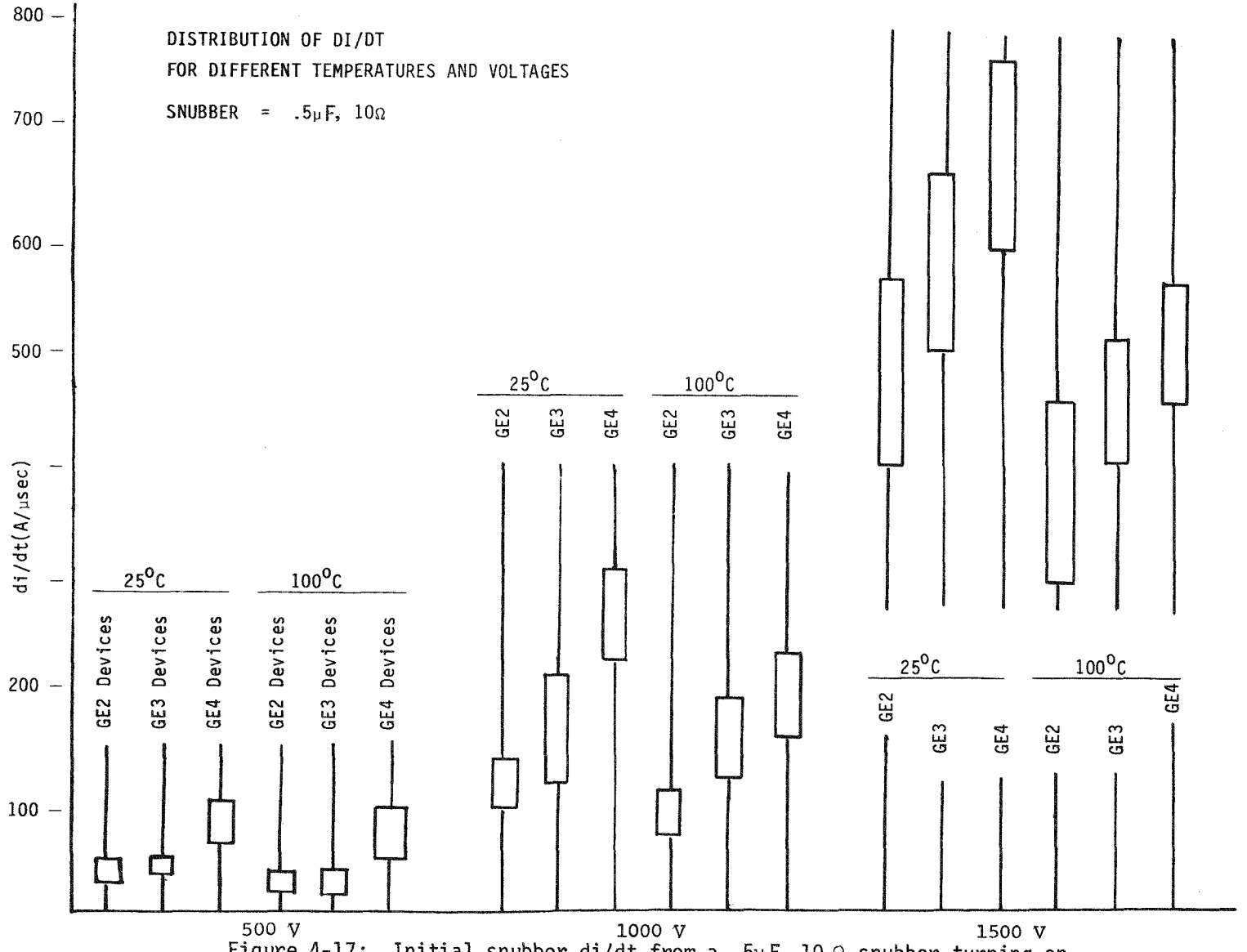


Figure 4-17: Initial snubber di/dt from a .5μF, 10 Ω snubber turning on from 500, 1000 and 1500 volts.

HVDC di/dt Stress Tests

HVDC di/dt stress tests were done with the test circuit shown in Figure 4-14. Various snubber and di/dt pulse forming networks were used at a cathode plate heater temperature of 25°C, 100°C or 125°C. The anode plate temperatures for the same three temperatures were 25°C, 84°C and 106°C and the junction temperatures estimated to be about 10°C above anode temperature at 25°C and 15°C above anode temperature at elevated temperature. A summary of the test results are shown in the second part of Table 4-5.

These results span a range of snubber di/dt as shown in Figure 4-18. It can be seen that the dominant effects are temperature and snubber resistor value. Raising the thyristor temperature slows down device turn-on speed and lowering snubber resistance increases device turn-on speed. Capacitance, provided the snubber time constant is greater than one microsecond, does not seem to matter a great deal as illustrated by the similarity between the .1μF, 10 Ω and .5μF, 10 Ω responses at elevated temperatures. Note also the large size of the initial di/dt which is much larger and considerably less linear than the circuit (R, L, C) di/dt shown in Figure 4-19. The data plotted in Figure 4-19 is just about what would be expected with di/dt slopes closely matching 1/L when plotted against anode voltage.

Figure 4-20 shows typical device current and voltage from turn-on to turn-off of the device under test. The point in time at which the device turns off is sharply marked by a reverse voltage transient beginning at the instant of peak reverse current. This figure is included to show that good reverse voltage characteristics are required so that degradation during di/dt testing is not due to the reverse junction. Note however, that by selecting a larger R value that the reverse voltage transient becomes more damped. It is possible that some of the device failures in Table 4-5 are due to this reverse voltage transient.

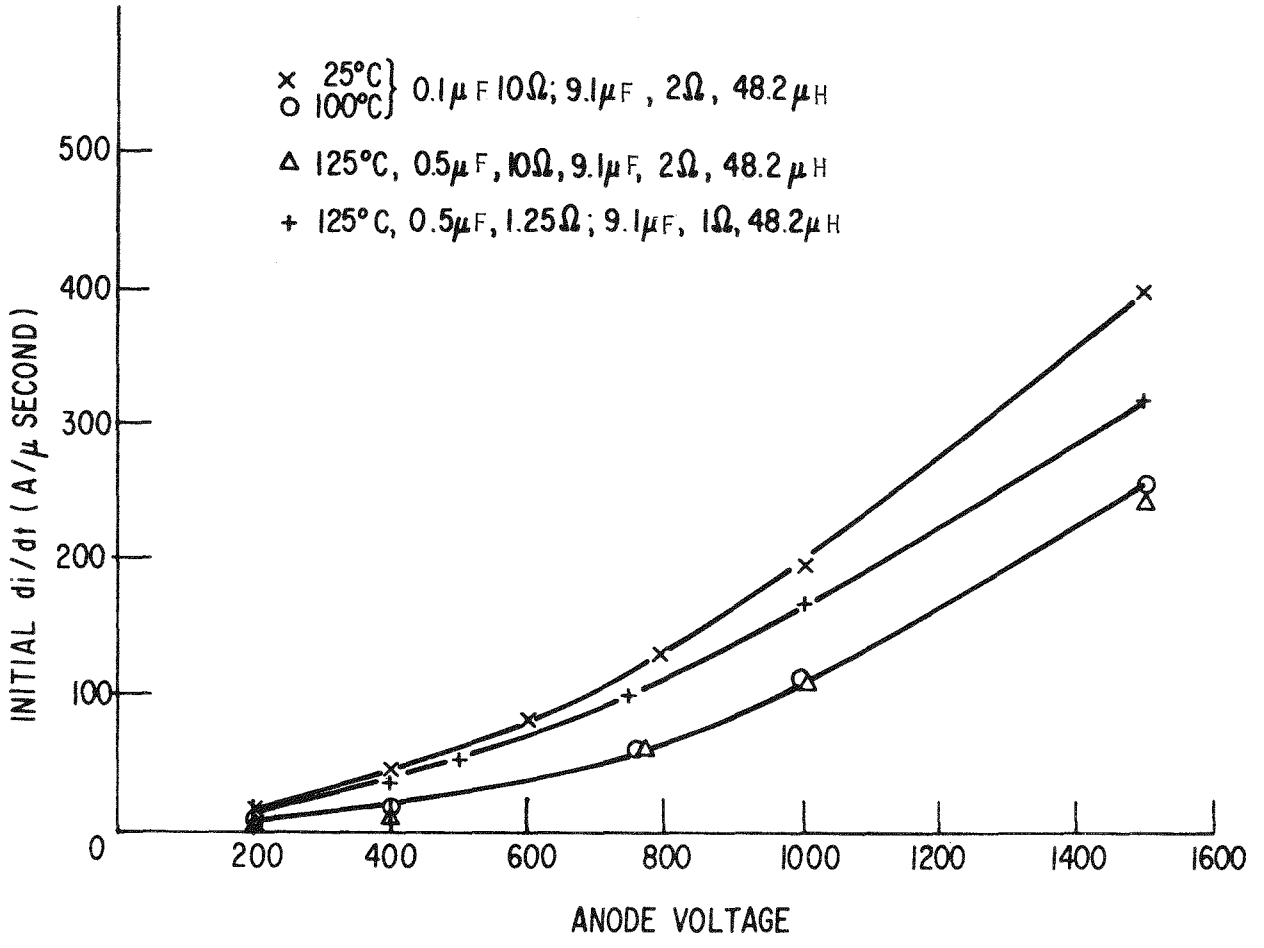


Figure 4-18: Initial (snubber) di/dt as a function of anode voltage for different di/dt test circuit parameters.

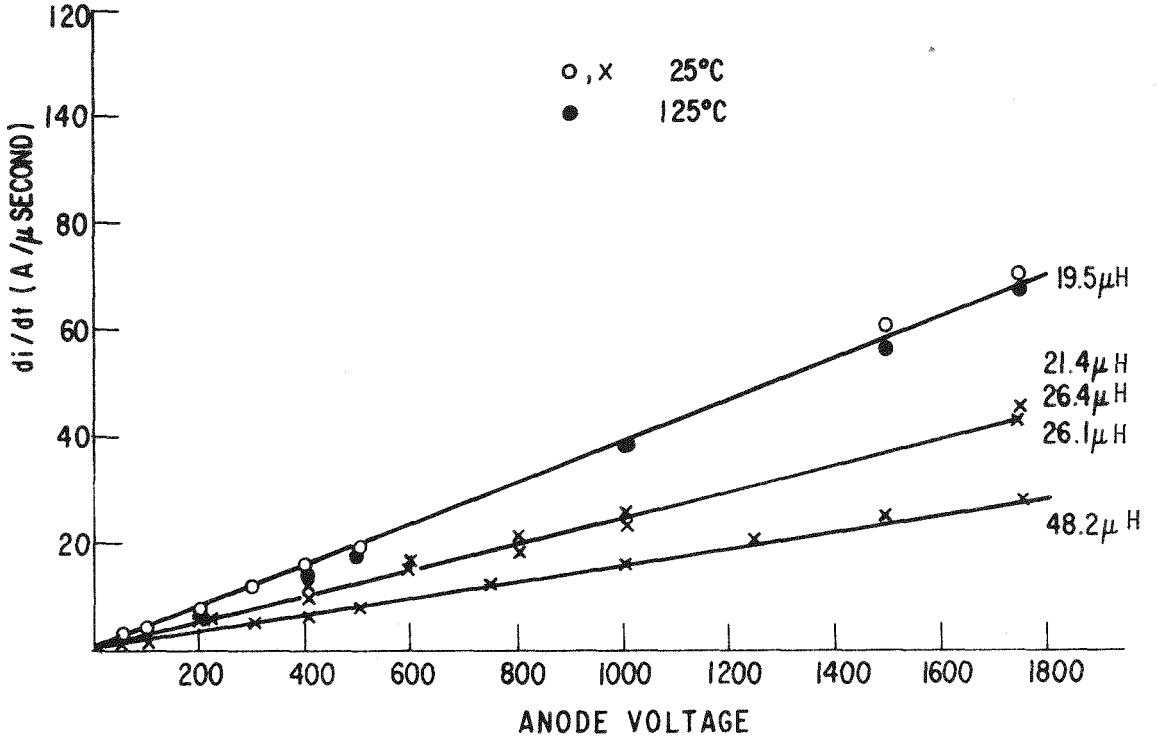
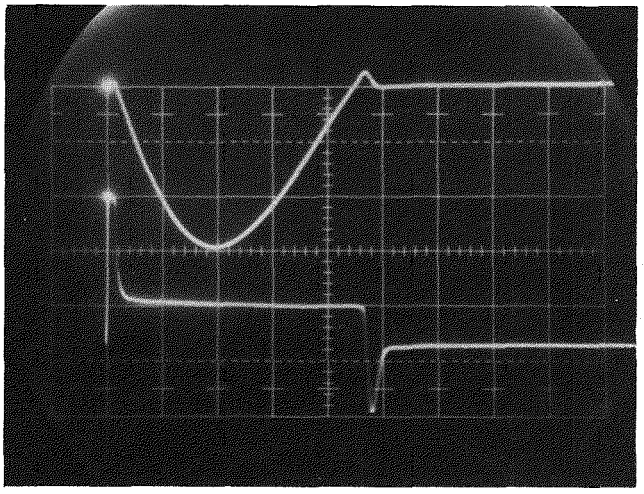


Figure 4-19: Device di/dt for different di/dt test circuit L values.



Test Device #1-2
20μsec/div
125°C
Top Trace: I_{SCR}, 200A/div
Bottom Trace: V_{SCR}, 500V/div

Figure 4-20: Reverse voltage transient after turn-on from 1000 Volts.

Examining Table 4-5 more closely it is apparent that no device survived the full battery of di/dt tests at 60Hz with the .5μF, 10 Ω snubber although some did very well. For example device 4C2 survived the 100°C test at 70A/μsec at 1750 volts as did devices 3C2 and 2C2. It is perhaps significant that these devices (denoted by letter C) had the n^+ alignment band feature. Not until the snubber resistor was increased to 37 Ω did any devices fully qualify. From this point only devices 2A2 and 2-3 failed. Devices 1-1, 4-2, 2-3, 1-2, etc., refer to special double amplifying gate test devices which will be examined at higher stress levels in future tests.

DI/DT TESTS AT HVDC STRESS LEVELS

Light fired device testing at SPCO began with gate threshold tests and delay time vs. voltage and gate pulse amplitude. Results obtained were similar to those obtained for the EPRI-GE1 device described in detail in the Phase I report[1] and will not be discussed here. The more important experimental results all relate to di/dt testing and follow-up failure analysis in which four modes of device failure (defined by noticeable device degradation) were observed. These four failure modes will be referred to as

(1) normal di/dt failure indicated by a crater on the turn-on line of any stage;

(2) channel "bridging burn" in which a lateral burn region reaches between the gate metallization (or emitter metallization of the previous amplifying stage) and emitter turn-on line of the next stage;

(3) edge firing marked by a surface or near surface breakdown under the passivation leading to crater formation at the edge of the main emitter;

(4) "local" channel burns in which channel burns are found near the edge of the gate metal but do not cross the channel.

The locations where these failures would be expected to occur are shown in Figure 4-21. Letter 'b' indicates the points that local channel burns have

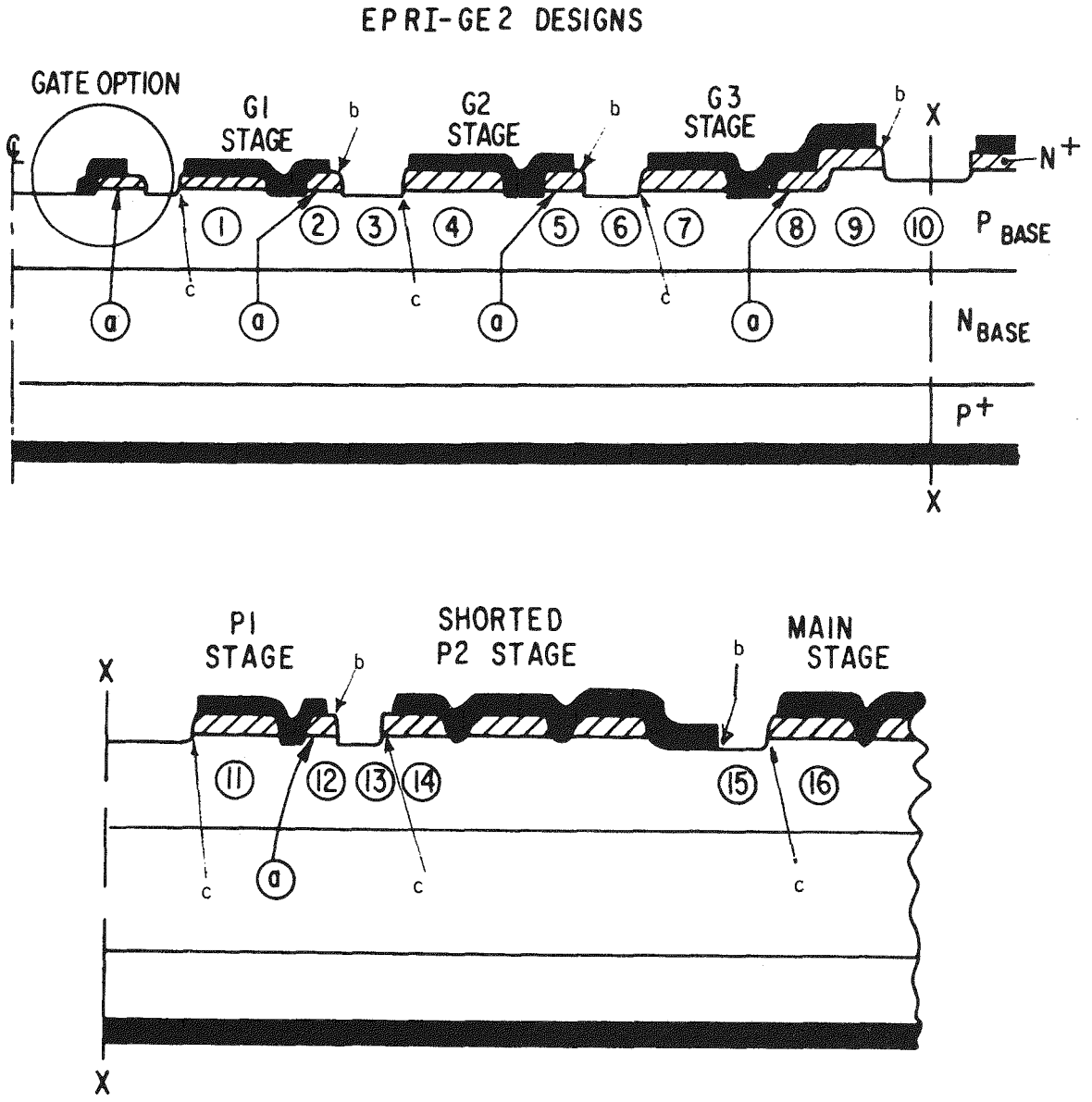


Figure 4-21: Partial radial cross-section of the basic GE2 design. The letters 'a' denote the n^+ alignment bands while the circled numbers refer to the base region "zones" whose resistance values are given in Table 4-2. Letters 'b' indicate the location of the so-called "local channel burn" or surface arcing. The channel burn or "bridging channel burn" would reach right across regions 3, 6, 10, 13 or 15. Normal di/dt failure would occur at points marked 'c'.

been observed. Similarly, letter 'c' indicates the locations in which normal di/dt failure occurs. Bridging channel burns have been observed running across regions 3, 6, 10 and 13, and are possible but have not been observed in region 15. The first three failure mechanisms listed above are observed in standard devices, the last is not. On some devices, modes 1, 2 and 4 are all observed. However, the new failure mechanism seems to be the dominant one, and generally occurs soon enough in testing so that the normal di/dt failure limit is not reached.

Local Channel Burn Failures

Figure 4-22 shows a magnified view of the surface of a failed GE3D device. The dark areas are metal; the light areas are silicon; the dark lines show boundaries between regions of different p-base thickness. In the upper photograph the dark line boundary indicated by the arrow is clean, indicating no local channel burns. In the lower photograph some of the silicon at the corresponding boundary for the next amplifying state is partially pitted. Silicon has vaporized. There are two theories. First, it is possible that during turn-on a transient voltage potential is built-up between successive stages and that the current arcs from the corner 'b' in Figure 4-21 to the p-base below. This hypothesis will be tested by passivating the channel region to see if similar burns do or do not occur. A second possibility is that there is actually enough channel current to cause the observed effect, and that it is local because of some peculiarity of the n^+ definition etch in device processing. If this were true, it would mean that the computer model described in the previous report should be altered and that much more accuracy needs to be achieved in calculating temperature rise due to lateral current flow. We will return to this point later.

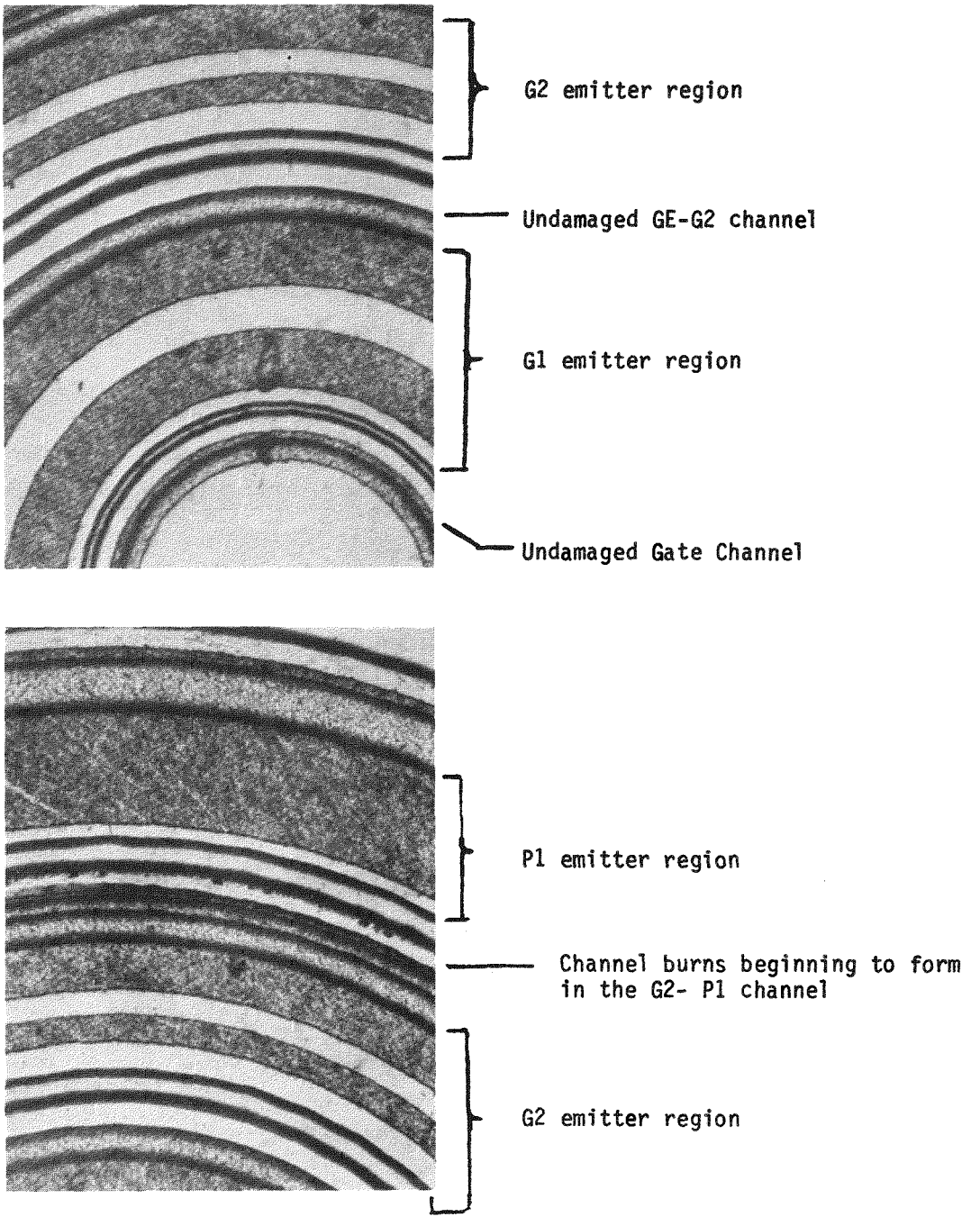


Figure 4-22: Formation of local channel burns in device EPRI-GE3D1 (60X magnification).

Channel Bridging Burn

A more normal sort of channel burn is the burn across the channel as shown in Figure 4-23. In this case the burn was across the G2 to P1 channel of the GE3 type device (4 amplifying stages). With this type of failure it is clear that channel current, at least in this location, has been too high. To be more accurate, the time integrated lateral I^2R loss has been too great. The inference is that the following stages have turned on too slowly and/or the total snubber and gate to cathode resistance is not high enough to hold down I to allowable levels. What these allowable levels were or should be expected to be can be inferred from channel bridging burn level currents measured on the standard device. Figure 4-24 shows several measured gate current vs. pulse widths found to cause channel burns while Table 4-6 lists corresponding values at the wide pulse amplitude calculated for the EPRI-GE3 type device for the same pulse width. It is interesting to note that at a 2μsecond pulse width one would infer an allowable peak lateral current in the G1 - G2 channel of ∿150 amperes.

Edge Failures

Edge failure was observed on a significant fraction of the devices. It is an indication of passivation instability which is often screened out by 5 minute dc forward and reverse blocking voltage tests at elevated temperature. Figure 4-25 shows a typical failure region at 60X magnification.

Normal di/dt Failure

Evidence of normal di/dt failure was seen only once and there accompanied by both local and bridging channel burns so that it is possible that the local channel burns initiated failure.

Summary of Device Failure Analysis

Table 4-7 summarizes the failure analysis results of device di/dt tests performed at SPCO. The prevalent failure (degradation) mechanism was local channel burn, usually worst in the channel between the G2 and P1 stages.

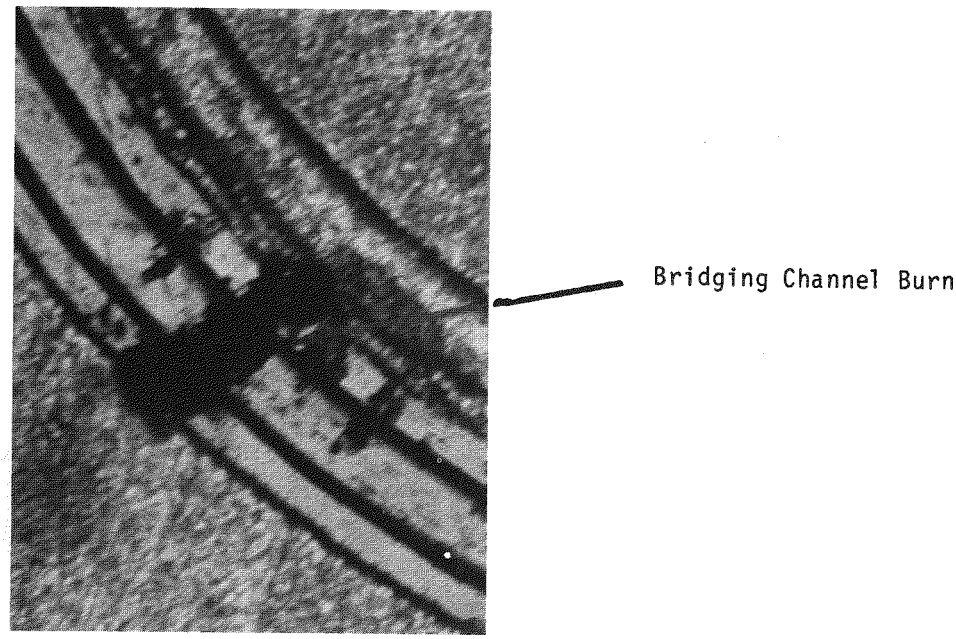


Figure 4-23: Bridging channel burn in device EPRI-GE3A2 after di/dt testing (150X magnification).

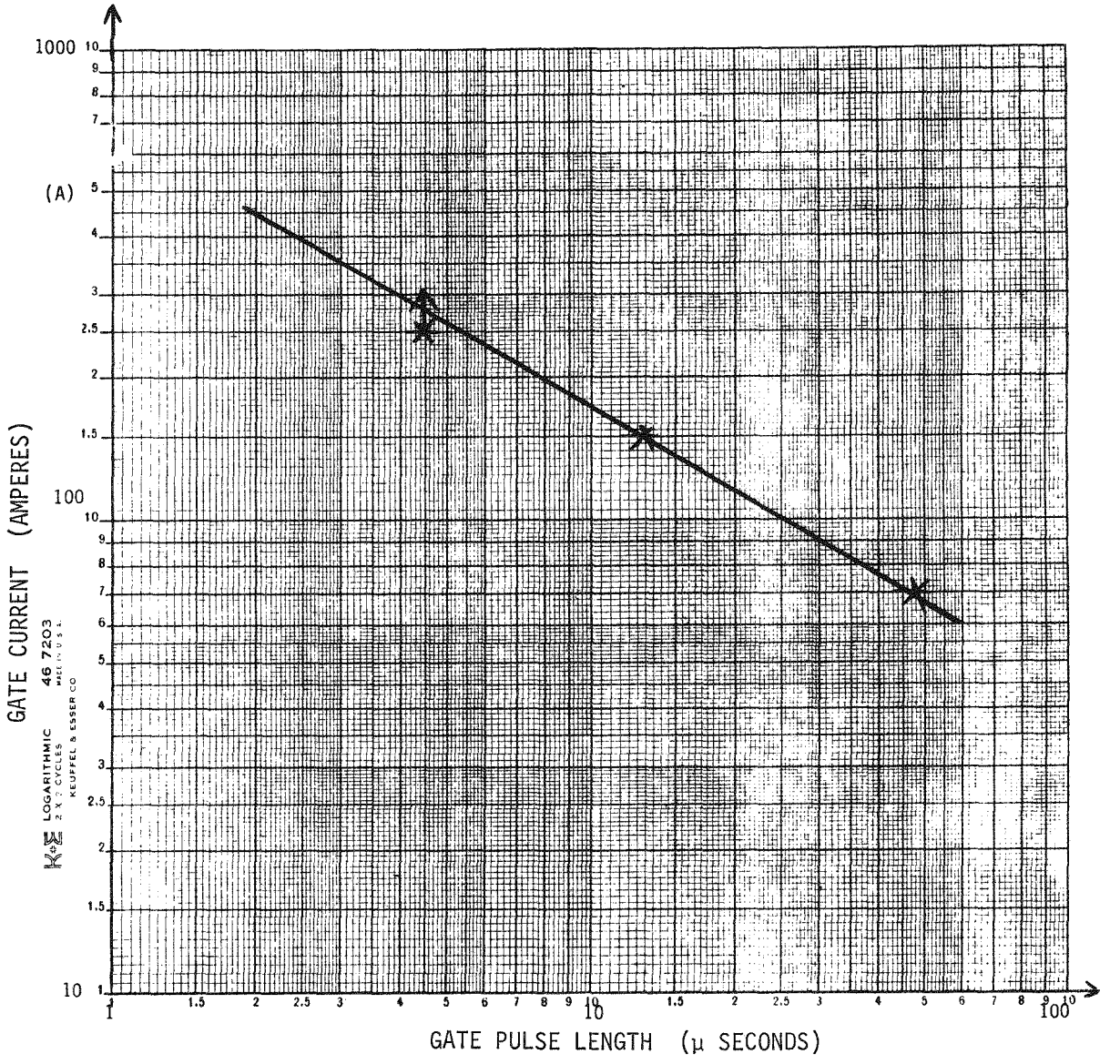


Figure 4-24: Measurement of gate dissipation required to create channel burns on the standard electrically fired cell. Note the point with the arrow attached was for a measurement in which no device failed.

TABLE 4-6: Calculation of current level needed to produce bridging channel burns based on measured standard cell properties and relative channel length for different EPRI-GE3 channels for a 40μsecond pulse length.

Channel Location	Channel Radius (mils)	Destructive Current (A)
Standard cell Gate to Pilot	101	70 (measured)
G1 - G2	36.5	25
G2 - P1	54.5	38
P1 - P2	72	50

TABLE 4-7: Failure analysis of devices tested at SPCO with emphasis on local channel burns.

				FAILURE POINT				
DEVICE NO	G1 - G2 % Burns	G2 - P1 % Burns	P1 - P2 % Burns	V_D	di/dt A/μsec	T_{case} °C	Time (minutes)	Laser Current A
3C3	30	40	80	1500	275	97	∿2	50
3A2	20	80	None	1600	50 to 55	98	∿1	50
3D1	None	10	None	1600	50	35	∿1.5	45
3A4	None	5	None	1600	55	97	∿50sec	50
3B1	None	Some	None	1600	50	42	∿7	33
3C2	None	Some	None	1600	50	42	∿5	35

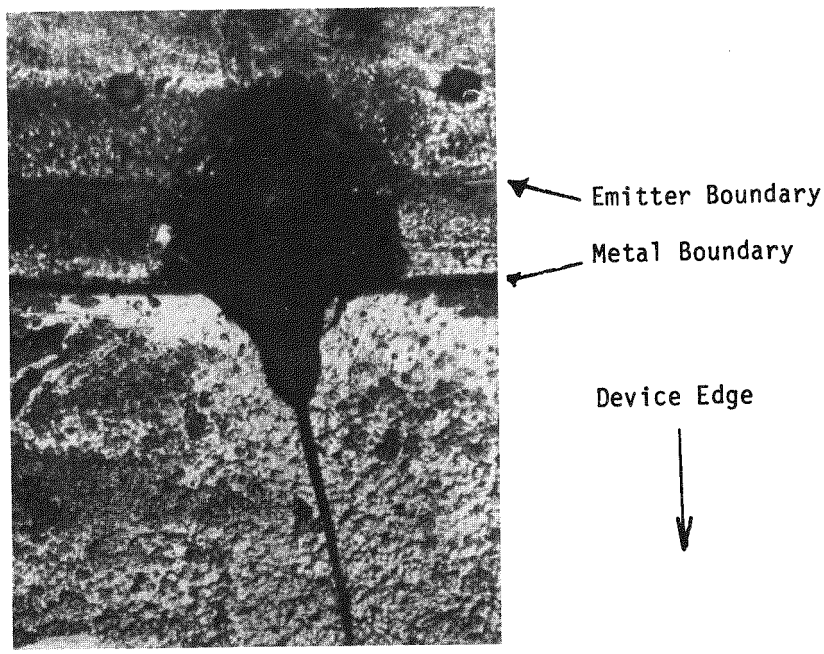


Figure 4-25: Photograph of edge failure region in device GE3A4 (60X magnification).

Columns headed by % burn refer to the percentage of the channel periphery covered by local burn marks like those of Figure 4-22A. The last columns describe the test condition where the degradation in electrical characteristics became noticeable first in a variable delay time and then in self-firing at reduced voltage. Only in device 2C3 was the di/dt value in the typical range of the standard cell.

Table 4-8 shows similar data for EPRI-GE2 and GE4 device types inspected after di/dt tests at CRD. Apart from 2A2, an edge failed device, and 3B4 which had mechanical damage, all devices tested, even device 4A2 with no apparent degradation, showed local channel burn. Comparing results on the basis of local channel burn seems to point to a double amplifying gate design either like type GE4 or like the test device 1-1, for example, which is listed in Table 4-5 as successfully passing the di/dt tests. In fact, examination of device 1-1 shows no local channel burn marks being formed!

Possible Methods to Avoid Local Channel Burn

It is evident from the EPRI light fired device tests that both snubber capacitance and snubber resistance are important in device turn-on tests. Channel burn is seen to occur always with the 10 Ω snubber but not always with the 37 Ω snubber. This leads to the suggestion that a snubber resistor value be identified to prevent this type of failure and allow us to measure the "true" di/dt capability of the design.

Comparison of the devices tested leads to the suggestion that more of the EPRI-GE4 type device and more devices of the L1 test variety[1] be fabricated with their longer channel length between the first and second amplifying stages. It is also possible that burn-out may be avoided by passivating the channels. This would be the case if it were found that surface arcing was occurring at the local burn region. This possibility is suggested by the fact that the burn mark is at a sharp edge. No corresponding sharp

TABLE 4-8: Failure analysis of devices tested at CRD with emphasis on local channel burn.

Device No.	G1 - G2 % Burns	G2 - G3 % Burns	G3 - P1 % Burns	P1 - P2 % Burns	FAILURE POINT				Comments
					V_A	di/dt (A/μsec)	Case Temp (°C)	Snubber	
2C1	1	30	95	30	1750	50	110	.5μF, 37Ω	Device O.K.
3C2	5	90	-	5	1750	50	110	" "	Edge failure
2A2	None	None	None	None	1750	50	25	" "	" "
4C2	-	-	90	-	1500	150	90	" "	Degraded
2C2	None	None	100	99	1750	50	110	.5μF, 10Ω	"
3D4	90	100	-	90	1500	40	110	" "	"
3A4	25	40	-	1	1700	45	25	" "	"
3D3	None	50	-	1	2000	-	25	" "	"
4A2	-	-	80	-	1750	-	100	" "	Device O.K.
2B2	None	100	90	None	2000	55	25	" "	Degraded
3B4	None	None	-	None	1500	40	25	" "	Mechanical Damage

edge exists in the L1A test device (device #1-1, 4-2, 2-3, 1-2 and 4-4 of Table 4-5) which, it is significant, show no channel burn marks.

CONCLUSION

The fabrication and testing of a large number of new devices of multi-amplifying gate design led to a new device failure mechanism which was located in the channel and appeared to be caused by surface arcing between amplifying stages. In some devices channel burn marks indicative of excess channel current were observed. This latter failure is only occasionally seen in electrically fired devices. On the rare device which had normal di/dt failure, i.e. a crater at the turn-on line- the di/dt failure point was high - high enough to pass HVDC qualifying tests.

At this point it was felt that new turn-on tests and modelling would be necessary to understand and predict the channel failures - both surface arcing and channel burn. This subject is discussed in the following sections of this report.

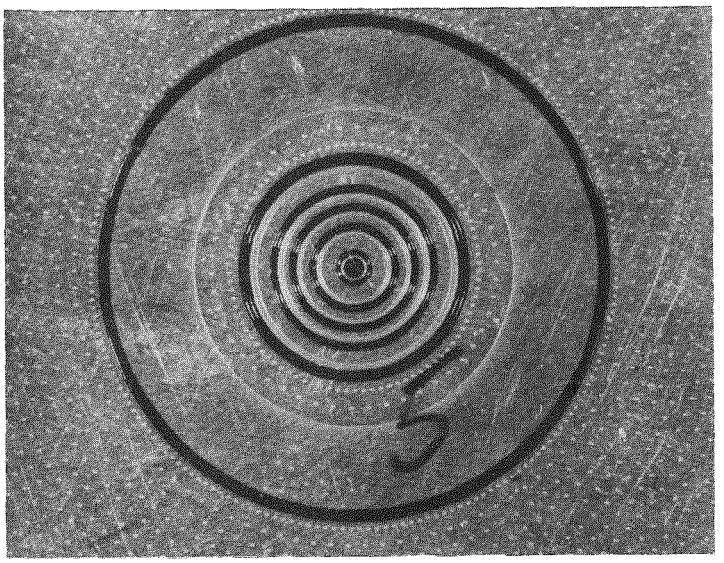
Section 5

FAILURE ANALYSIS OF PHASE II DEVICES

NEW TURN-ON EXPERIMENTS

One of the main difficulties in establishing the di/dt capability of any of the new light fired thyristor devices lay in a pattern of local surface burn marks which appeared at the upper outer corner of each n^+ alignment band. Figure 4-21 showed schematically (location b) where these burn marks appeared. Looking to Figure 5-1 which shows actual photographs of the three main device types, burn marks would appear along the inner edge of the dark bands that mark the bare silicon channel between the various amplifying stages. In Figure 5-2 photographs of successively greater magnification show three of the more prominent local burn features of device 3D1 (Run 1). In these photos the metallization is "grey", the bare silicon light and changes in surface elevation dark in colour. In following from Figure 5-2a to 5-2d we can pick out smaller burn features almost continuously along the inner channel length. These features immediately suggested surface arcing which, at b in Figure 4-21, would require anywhere from 10 to 1000 volts to arc over the interchannel regions depending on the sharpness of the corner "b" and the local dielectric constant and breakdown voltage.

A series of experiments quickly confirmed that there was indeed a momentary interstage voltage transient during turn-on which could reach $\sim$100 volts. Figure 5-3 shows the experimental apparatus assembled to measure channel voltage transients during turn-on, the key features of this apparatus being the ability to either electrically or light fire the device and at the same time, using micro-positionable tungsten probes, to monitor the cathode emitter metallization of each individual stage.



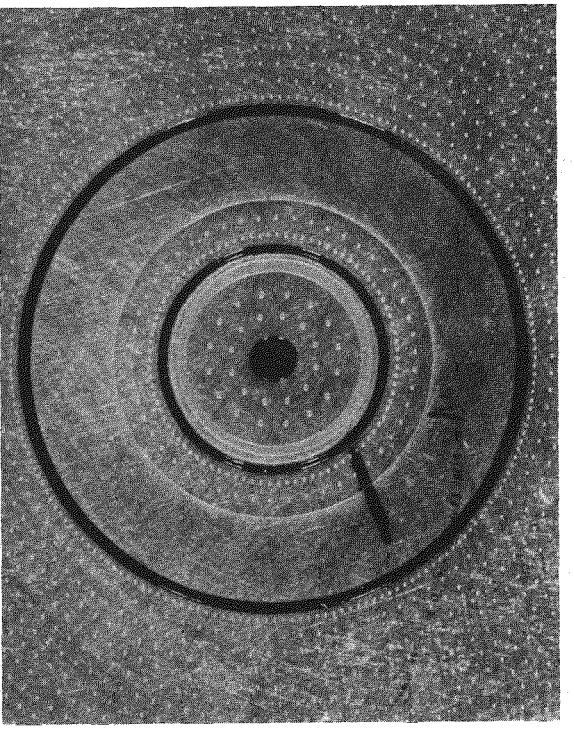


Figure 5-1: Photographs of the inner amplifying stages of the EPRI-GE2 design (left), the EPRI-GE3 design (lower left) and the EPRI-GE4 design (lower right). The dark areas are the so-called channels. The center dark area is the photo-gate region.

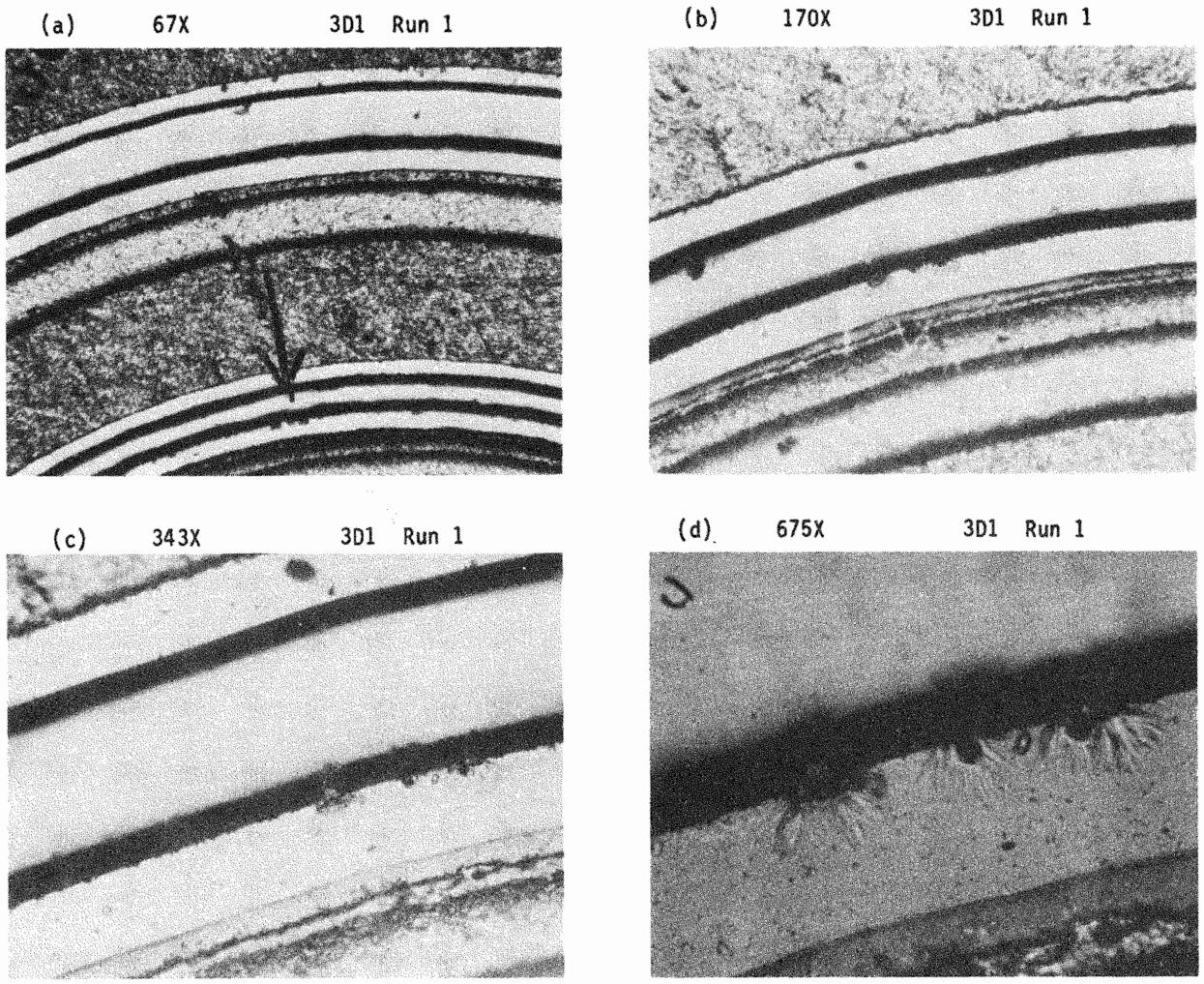


Figure 5-2: Views at increasing enlargement of three more prominent "local burn" features caused by surface arcing.

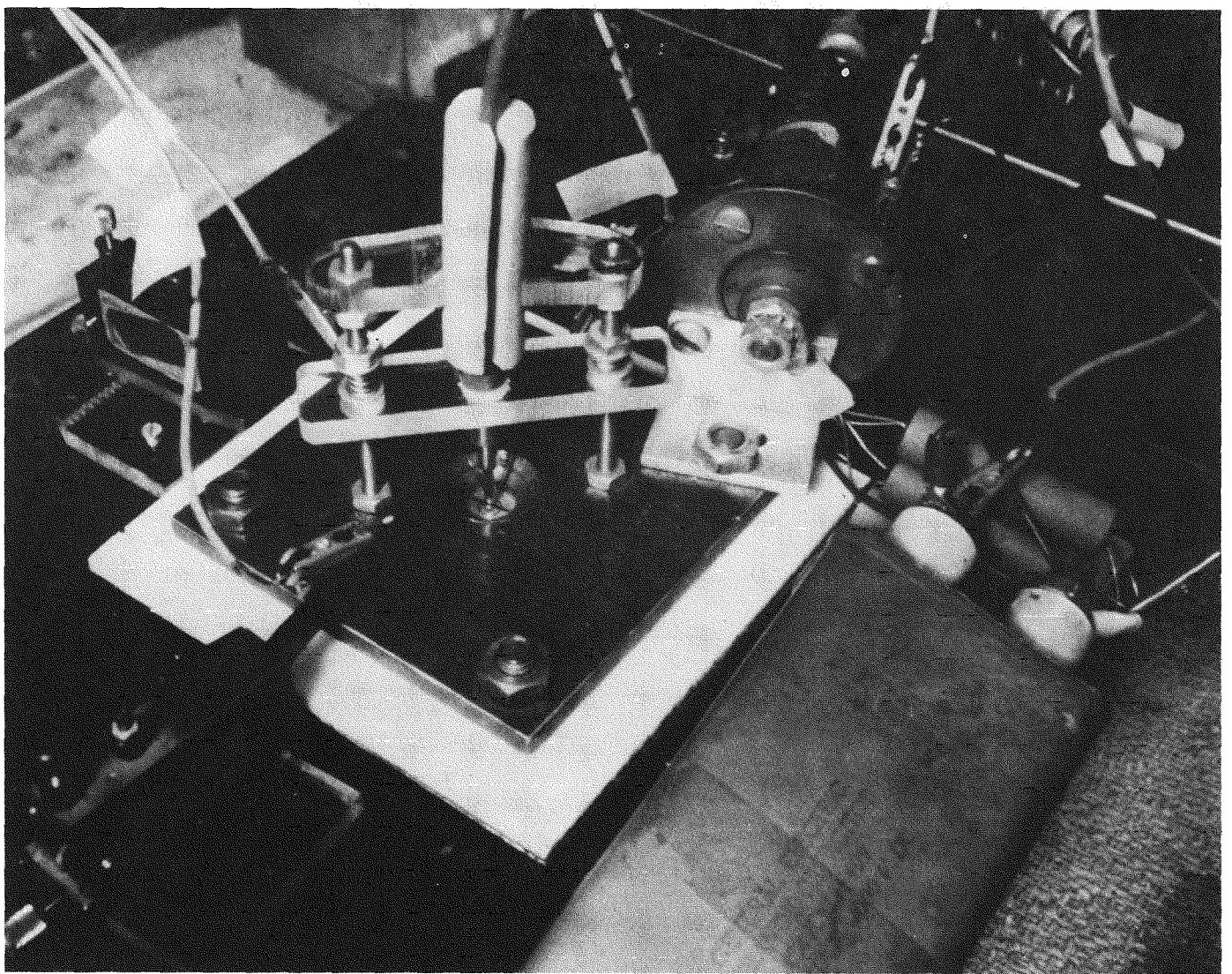


Figure 5-3: Apparatus for channel voltage experiment showing the adjustable light pipe and microprobes for contacting the metallizations of the amplifying stages.

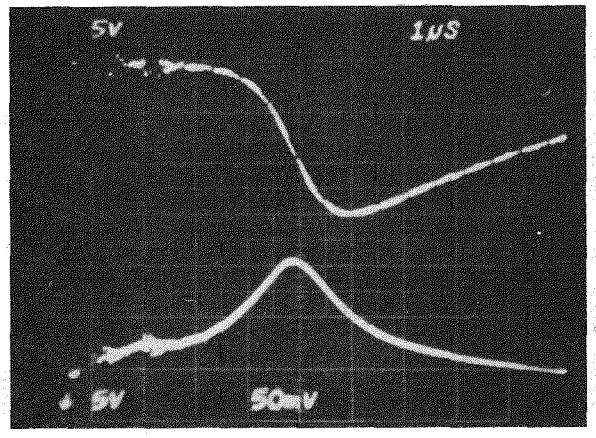
EPRI-GE1 Channel Voltage Experiments

Figures 5-4a to 5-4d illustrate the interstage voltage transient in the EPRI-GE1 device developed and described in Phase I. Figure 5-4d which shows an approximately 95 volt Stage 1 - Stage 2 channel transient had no burn marks. The fact that it had no sharp surface features was also significant.

One of the reasons that the first channel voltage measurements were made with the "old" EPRI-GE1 device is that this device could also be easily electrically fired and the comparison between the electrically fired device and the light fired device made with the least number of complications. This comparison was also believed to be important because, in our experience, no standard electrically fired device had ever displayed "local burn" marks of the type shown in Figure 5-2. Figure 5-5a, b and c show turn-on from the same three voltages as Figure 5-4 with a gate amplitude selected to give the same delay time at 500 volts. The turn-on transients of electrically triggered and light triggered responses were qualitatively similar but several differences appeared which, along with the similarities, are amplified in Figure 5-6.

Since the channel voltage, apart from channel resistivity modulation, is an exact measure of current flow, it is possible to interpret the four regions of the voltage transients of Figure 5-6 as follows: Region 1, the build up of base charge where all we see is the constant gate current times the base resistance of the p-base of the inner (inside channel) stage; Region 2, the turn-on of the first stage with a "slope 1" $R_{channel}$ di/dt; Region 3, both the inner and outer stages on, but the inner stage voltage increasing faster than that of the outer stage; and finally, Region 4 in which the current flow transferred to the outer stage and the voltage falls. A comparison reveals the following things. First an electrically fired device with an identical gate design requires much more gate current to turn it on with the same delay time as a light fired device. Second, the interstage voltage transient in the light fired device is sharper rising to a higher voltage than the electrically fired

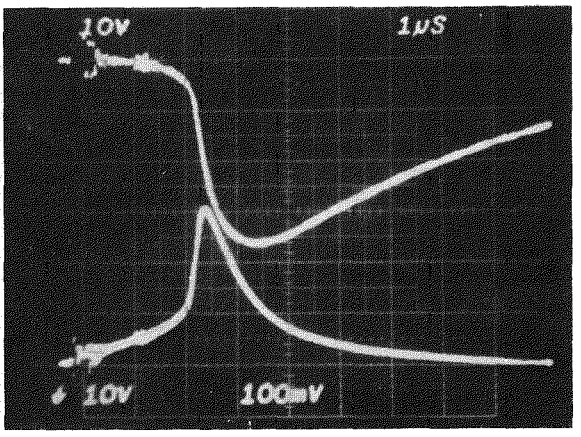
GE1 (L13) Turn-on from 200V



Upper: I_{SCR}, 5A/div Lower: $V_{1,2}$, 5V/div

(a)

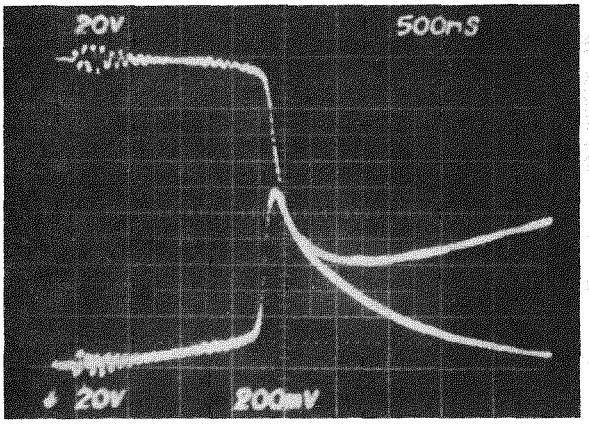
GE1 (L13) Turn-on from 500V



Upper: I_{SCR}, 10A/div Lower: $V_{1,2}$, 10V/div

(b)

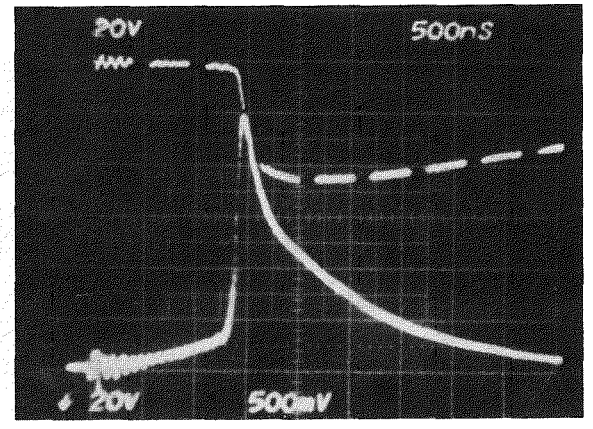
GE1 (L13) Turn-on from 1000V



Upper: I_{SCR}, 20A/div Lower: $V_{1,2}$, 20V/div

(c)

GE1 (L13) Turn-on from 1500V

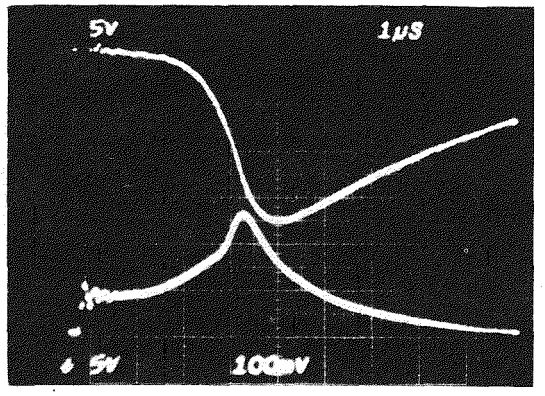


Upper: I_{SCR}, 50A/div Lower: $V_{1,2}$, 20V/div

(d)

Figure 5-4: Turn-on of device EPRI-GE1 L13 from (a) 200V, (b), 500V, (c) 1000V and (d) 1500V. The upper trace is device current, positive downward. The lower trace in each case is the channel voltage between the gate and pilot amplifying stages.

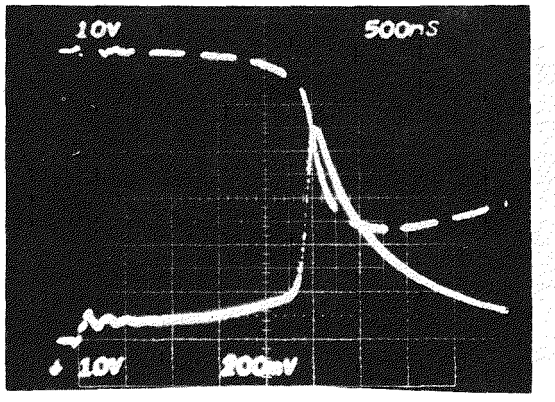
GE1 (LE4) Turn-on from 500V



Upper: I_{SCR}, 10A/div Lower: $V_{1,2}$, 5V/div

(a)

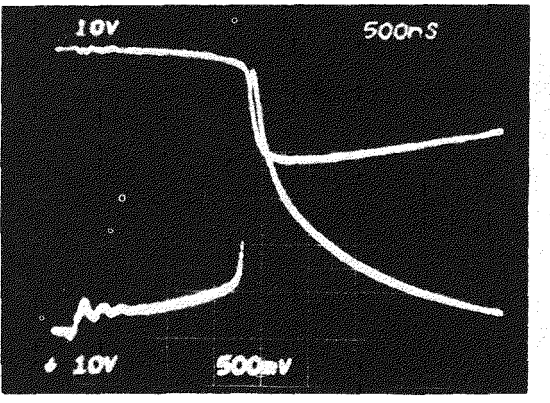
GE1 (LE4) Turn-on from 1000V



Upper: I_{SCR}, 20A/div Lower: $V_{1,2}$, 10V/div

(b)

GE1 (LE4) Turn-on from 1500V

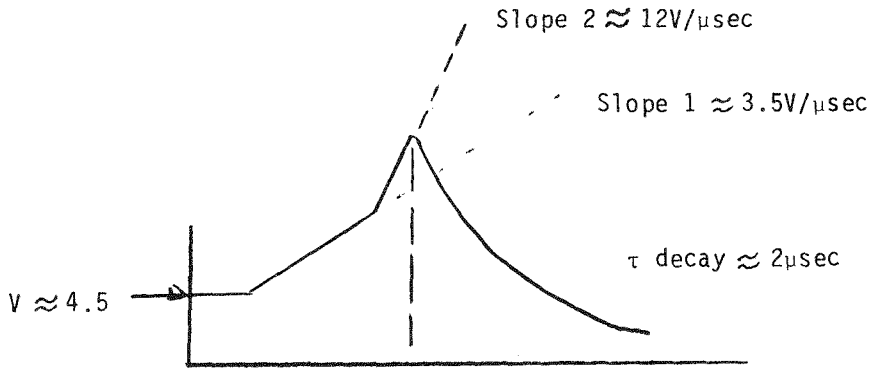


Upper: I_{SCR}, 50A/div Lower: $V_{1,2}$, 10V/div

(c)

Figure 5-5: Device current positive downward and gate-pilot channel voltage for device EPRI-GE1 LE4. This device is the electrically gated counterpart of the device in Figure 5-4.

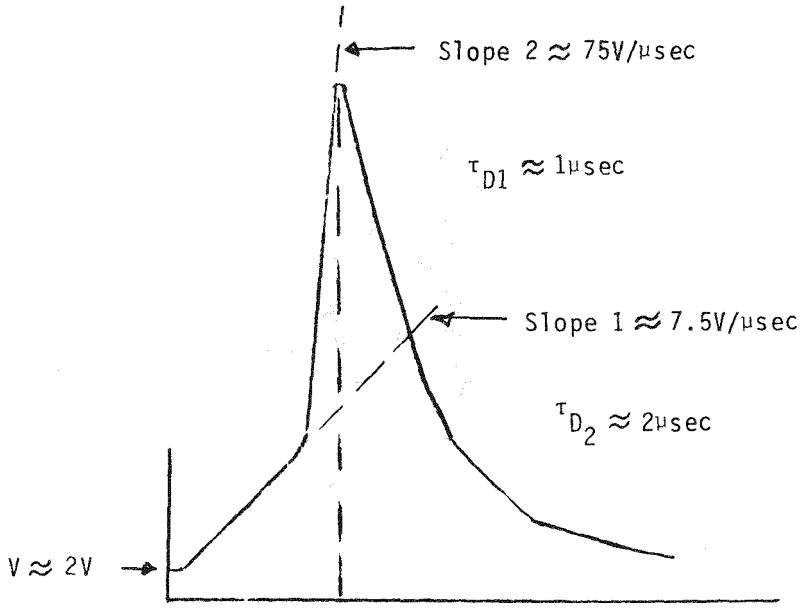
CASE 1: Electrically fired at 500V, 2μsec. delay



NOTE: (i) Slope 2/Slope 1 ≈ 87/23 ≃ the ratio of Pilot to Gate stage turn-on lines.

(ii) Area to peak ≈ 19.4V·μsec

CASE 2: Light fired at 500V, 2μsec delay



NOTE: (i) Slope2/Slope 1 > ratio of Pilot/Gate state turn-on lines

(ii) Area to peak ≈ 17V·μsec

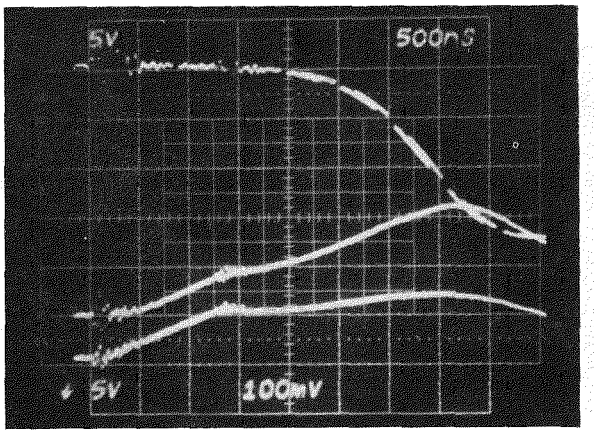
Figure 5-6: Comparison of typical electrically fired (Case 1) and light fired (Case 2) channel voltage transients during turn-on.

device. Yet both devices have approximately the same area under the voltage curve to the point of maximum channel voltage and, after an initial voltage decay which is faster in the light fired case, a very similar decay time. The implications are fairly clear. The light fired stage (inner stage) turns on better and faster than the next stage which is electrically fired by the output of the first stage. The equal areas under the curve to the maximum voltage point occur because the second stages were, in effect, electrically fired in both cases. In terms of power dissipation the evidence points to a peak power (V^2/R) value four times as large where a light fired stage gates the next stage and a total dissipation, $\int V^2/R_{channel}\, dt$, two times as large.

These observations, which resulted from having devices with identical emitter designs which could be electrically and light triggered, have led us to re-examine our turn-on model and, we hope, will lead us to a confident prediction of turn-on properties of future designs. Work on a charge control model for the initial turn-on period, which had always appeared desirable, became necessary as the only mode to easily compare electrically fired device and light fired device turn-on. The next subsection of this report is devoted to the development of this model which is believed to be a unique contribution to light fired thyristor modelling.

The new series of EPRI light fired thyristors, the GE2, GE3 and GE4 types were also tested for channel voltage transients. These device transients, particularly those of of the GE2 with 5 amplifying stages, are more difficult to analyze but show the same qualitatiave behavior as the GE1 device of Figure 5-5. For example, Figure 5-7a-d show the four channel voltage transients for a 500 and a 1000 volt turn-on. At 1000V, the largest voltage transient is the 3,4 channel at 42 volts and the 1,2 channel at 23 volts. Incidentally, the burn marks shown in Figure 5-2 are at the 3,4 channel, i.e., the channel between the third and fourth amplifying stages.

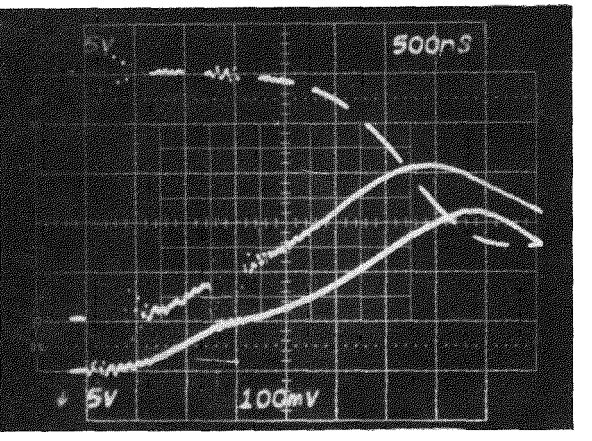
GE3 (C3), 500V Turn-on Upper: I_{SCR}, 10A/div



Middle: $V_{2,3}$, 5V/div Bottom: $V_{1,2}$, 5V/div

(a)

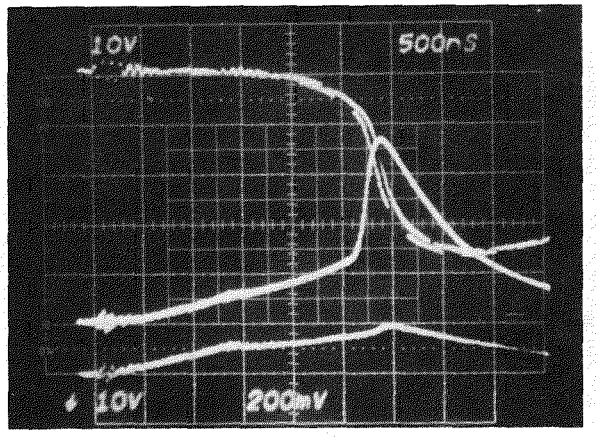
GE3 (C3), 500V Turn-on Upper: I_{SCR}, 10A/div



Middle: $V_{4,5}$, 5V/div Bottom: $V_{3,4}$, 5V/div

(b)

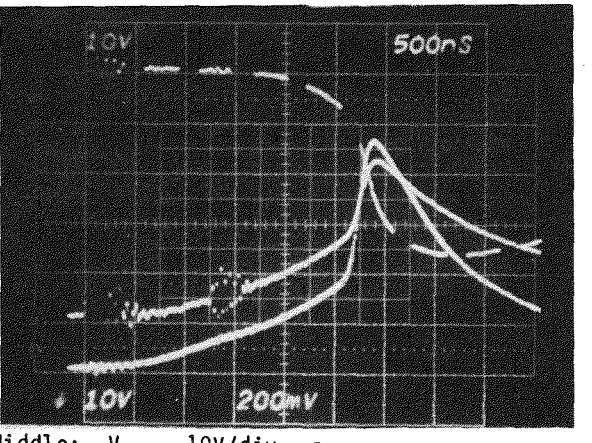
GE3 (C3), 1000V Turn-on Upper: I_{SCR}, 20A/di



Middle: $V_{2,3}$, 10V/div Bottom: $V_{1,2}$, 10V/di

(c)

GE3 (C3), 1000V Turn-on Upper: I_{SCR}, 20A/di



Middle: $V_{4,5}$, 10V/div Bottom: $V_{3,4}$, 10V/di

(d)

Figure 5-7: Device current (positive downward) and channel voltages of device EPRI-GE3 C3 for turn-on at 500V(a&b) and at 1000V (c&d).

Figure 5-8 shows the turn-on transients for the double amplifying gate EPRI-GE4 design at 200, 500 and 1000 volts. Here the voltage transient between stages 1 and 2 is about 55 volts. Naturally, at higher voltages such as 2000V, where at least one turn-on test is made, this would be much larger.

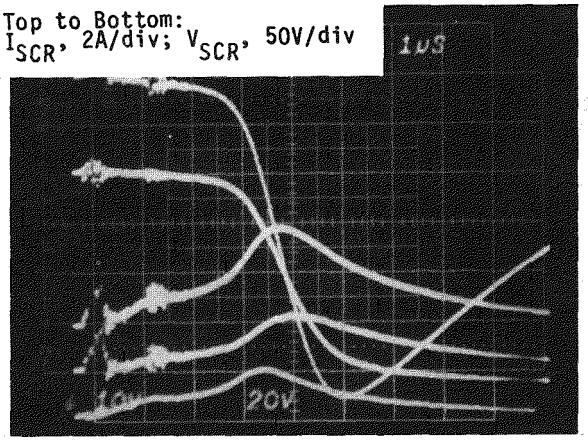
Table 5-1 shows more of the data taken with a normal size gate drive, all results being for a gate drive for which the turn-on delay time at 400 volts was 2 microseconds. Other experiments with a much larger and a much smaller gate drive showed very little difference. In the table three voltages from the transient are recorded: "initial $V_{1,2}$", the relatively constant initial portion; "$V_{1,2}(t_{on})$", the voltage at the point of turn-on; and, "$V_{1,2}(t_{max})$", the maximum value of the transient. Other quantities are self evident.

The first section of the table compares the effect of light and electrical triggering with the channel voltage approximately twice as large in the light fired case. The second section shows the effect of varying the snubber and shows, for example, that the peak channel voltage is dependent on the snubber resistor and relatively independent of the snubber capacitor. The next section shows the effect of multi-stage amplification. Here it appears that there is a somewhat reduced channel voltage peak compared to the GE1(L13) device at the same voltage. It also has a somewhat smaller peak than the double amplifying stage GE4(B3) device.

Finally, before leaving the experimental section on the turn-on channel voltage experiment, it must be noted that the peak channel current values are, for a given device, roughly proportional to peak channel voltages and that the effect of too high a channel current is a channel I^2R loss that will cause a different kind of channel degradation, namely "channel burn" as seen in Figure 4-23.

GE4 (B3), 200V Turn-on

Top to Bottom:
I_{SCR}, 2A/div; V_{SCR}, 50V/div



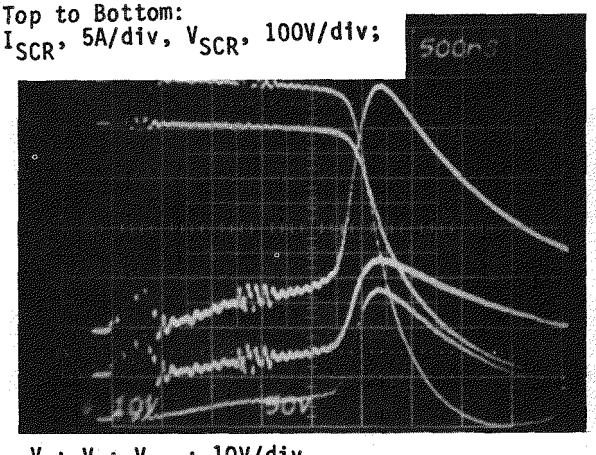
V_1, V_2, $V_{1,2}$, 10V/div

(a)

Figure 5-8: Device current (positive downward) and channel voltage ($V_{1,2}$) for device EPRI-GE4 B3 in turn-on from a) 200V, B) 500V, c) 1000V. V_1 and V_2 are the gate stage and pilot stage voltages, respectively, and $V_{1,2}$ their difference.

GE4 (B3), 500V Turn-on

Top to Bottom:
I_{SCR}, 5A/div, V_{SCR}, 100V/div;

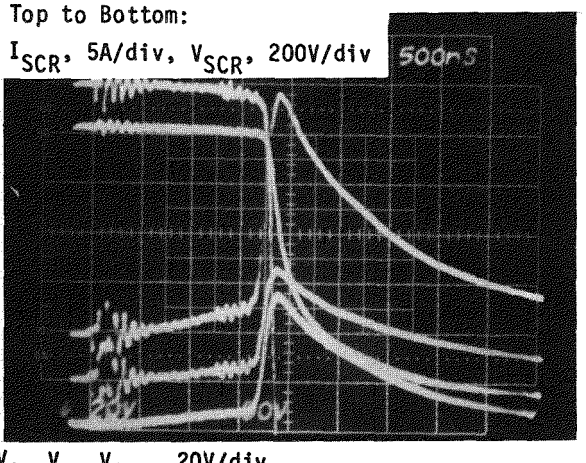


V_1; V_2; $V_{1,2}$; 10V/div

(b)

GE4 (B3), 1000V Turn-on

Top to Bottom:
I_{SCR}, 5A/div, V_{SCR}, 200V/div



V_1, V_2, $V_{1,2}$, 20V/div

(c)

TABLE 5-1: CHANNEL VOLTAGE EVALUATION

Device	Snubber	Gate Pulse	Anode Voltage	Initial $V_{1,2}$	t_{on} (μsec)	$V_{1,2}(t_{on})$	$I_A(t_{on})$	t_{max} (μsec)	$V_{1,2}(t_{max})$	$I_A(t_{max})$
COMPARISON OF LIGHT FIRED AND ELECTRICALLY FIRED DEVICES										
GE1(L13)	10Ω, .5μF	Med.	500	3	2	10	4	2.4	32	25
			1000	3	1.75	11	5	1.9	68.0	44
			1500	3	1.3	11	7	1.45	100	55
			200	3	3	7	2	3.8	11	10A
GE1(LE4)	10Ω, .5μF	Med.	500	4	2.8	8	15	3.2	13V	27
			1000	4	2.3	9	12	2.5	45V	32
			1500	5	1.75	10	8	1.9	58	100
EFFECT OF VARYING THE SNUBBER										
GE1(SE16)	1.25Ω, .1μF	Med.	200	2.5	2.3	7	4	3.3	16	30
			500	3.0	2.0	8	4	2.6	44	80
			1000	4	1.5	9	4	1.7	83	155
GE1(SE16)	1.25Ω, .5μF	Med.	200	3	2.8	7	3	3.4	12.5	12
			500	3	2.2	8	4	3.6	42	44
			1000	3	1.6	10	4	1.8	83	105
			1500	4	1.15	20	4	1.5	200	280
GE1(SE16	10Ω, .1μF	Med.	200	3	2.5	5	2.5	3.2	9	6
			500	3	2.1	7	4	3.1	26	17
			1000	3	1.6	9	4	1.85	54	36
GE1(SE16)	10Ω, .5μF	Med.	200	3	2.7	7	2.5	3.3	10	8
			500	3	2.1	8	3	2.5	28	19
			1000	3	1.6	9	4	1.35	57	44
EFFECT OF MULTI-STAGE AMPLIFICATION (EPRI-GE3 DESIGN)										
GE3(C3)	10Ω, .5μF	Med.	500	5(S)	2.4	5	3	3.5	7	23
		2,3 Stages		4(S)	2.5	7	4.5	3.7	12	28
		3,4 Stages		4.5(S)	2.5	8.5	4.5	3.9	16	34
		4,5 Stages		5(S)	2.4	10	3	3.4	16	17
GE3(C3)	10Ω, .5μF	Med.	1000	6(S)	2.8	8	32	2.95	9.5	54
		2,3 Stages		5(S)	2.6	12	22	2.9	36	52
		3,4 Stages		6(S)	3.6	17	22	2.9	46	52
		4,5 Stages		5(S)	2.65	17	25	2.9	21	52
TURN-ON OF EPRI-GE4 DESIGN										
GE4(B3)	10Ω, .5μF	Med.	200	4(S)	2.5	5	1	3.2	9	4
			500	4(S)	2.2	6	1.5	2.7	26	10
			1000	4(S)	1.65	7.5	1.5	1.85	52	25

IMPROVED LIGHT FIRED THYRISTOR MODEL

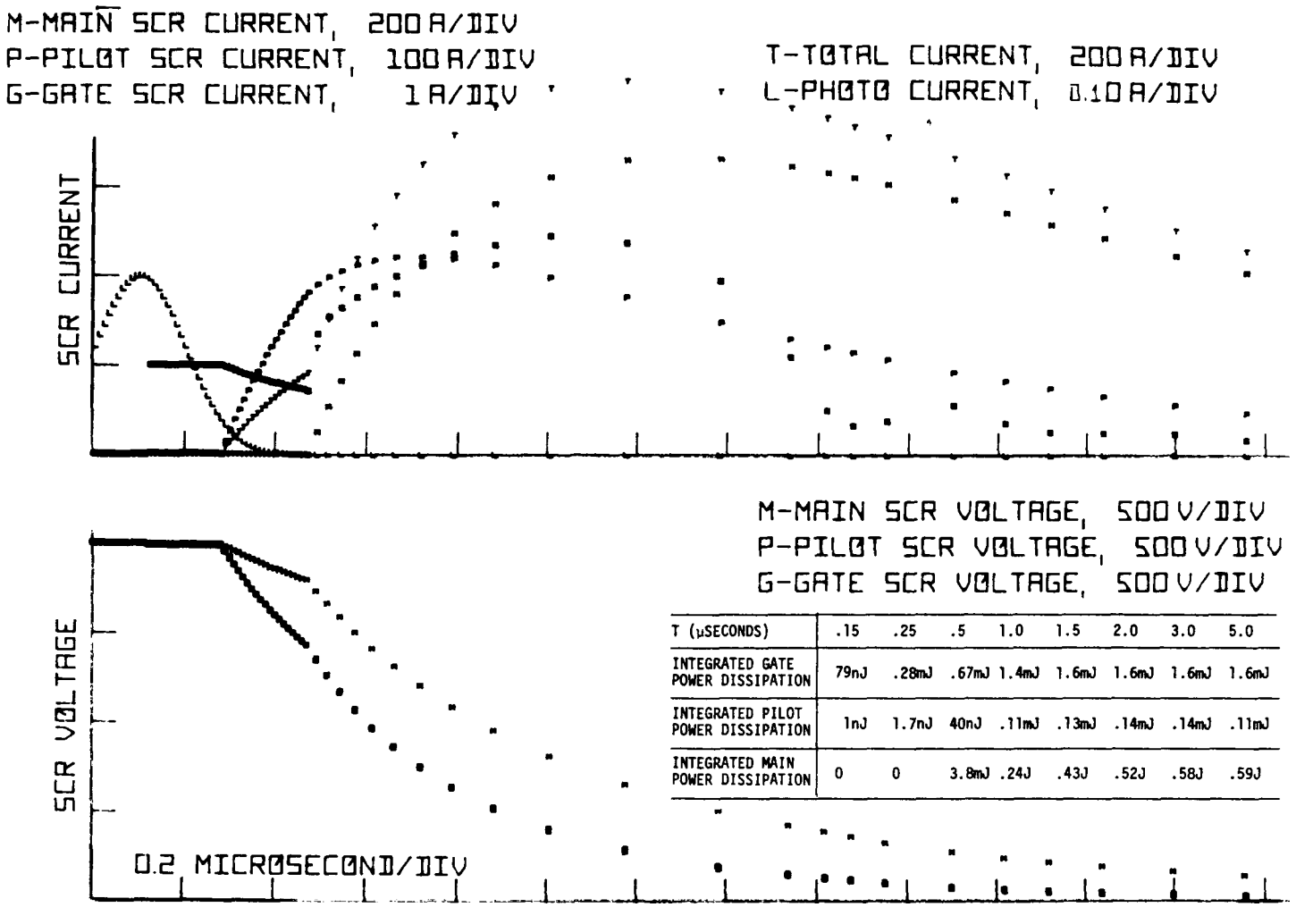
Model with Linear S(t) Admittance

Up to this point in the project our modelling of thyristor turn-on has been confined to a comparison between different device designs with different geometries and different numbers of amplifying stages. The model shown in Figure 3-6 has performed well in predicting turn-on delay time and general device current waveform. This is in part due to the time dependent switching element function $S_n(t)$ being properly chosen. In fact, the S function of each stage to this point has been given as an admittance with a linear time dependence departing from zero when the CV capacitor voltage reaches .7 volts, effectively beginning the electron injection process.

Figure 5-9 shows a typical computer generated turn-on with this model. What is unsatisfactory about these results is the lack of any sizeable G to P stage channel voltage. This would be the difference between the G and P curves in the upper plot. What we know to be true is that a simple linear S(t) function, while it may be excellent for the purposes used for so far, is not accurate in the low current range which comprises a critical part of the turn-on process. The old model is also unable to distinguish any difference between the electrical and light fired gate mechanism. The answer to both of these shortcomings lies in the development of a new charge control model for turn-on, originated for transistors, but adapted here for light fired thyristor turn-on.

Charge Control Model

The object of developing the new charge control model was to replace or augment the S(t) function to more accurately predict thyristor turn-on phenomena. It was intended to especially overcome the two difficulties of the linear S(t) function, namely the poor low current fit and the inability to distinguish between photo gating and electrical gating.

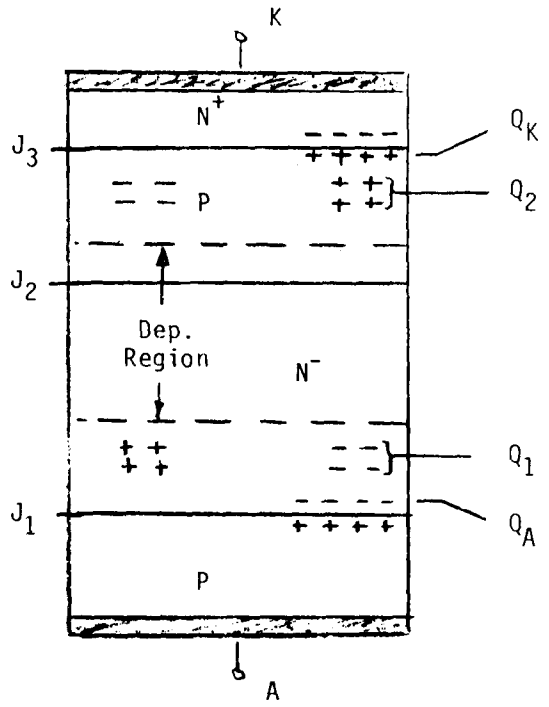


T (μSECONDS)	.15	.25	.5	1.0	1.5	2.0	3.0	5.0
INTEGRATED GATE POWER DISSIPATION	79nJ	.28mJ	.67mJ	1.4mJ	1.6mJ	1.6mJ	1.6mJ	1.6mJ
INTEGRATED PILOT POWER DISSIPATION	1nJ	1.7nJ	40nJ	.11mJ	.13mJ	.14mJ	.14mJ	.11mJ
INTEGRATED MAIN POWER DISSIPATION	0	0	3.8mJ	.24J	.43J	.52J	.58J	.59J

Figure 5-9: Computer calculation of the EPRI-GE1 turn-on process showing the current and voltage of each thyristor stage. The inset table shows integrated power dissipation (energy) at a number of prime points. The snubber was 1μF, 1Ω.

The charge control model developed for transistor analysis was recognized to have a great deal of promise in predicting thyristor turn-on behavior. Various workers[2,3] in the field used the coupled transistor concept of the thyristor in a charge control model for electrical firing. The major shortcoming of the model apart from the one dimensional aspect was its inability to deal with turn-on delay time, though, with only a little extra effort, light triggering could have been considered. These shortcomings have been eliminated in our new charge control model whose parameters are defined below and by inspecting Figure 5-10. In the figure is shown one section of the thyristor. Q_1 and Q_A are the excess majority carriers density (electrons) built up in the n base while Q_K and Q_2 are the excess majority carriers (hole) density in the p base. V_{J1}, V_{J2} and V_{J3} are the various junction voltages. It is believed[2,3] that the model will accurately describe turn-on of a one dimensional thyristor while the center junction remains reverse biased. This and the one dimensional aspects are quite limiting but to compensate we have an ability to predict the pre- and low-current stages of turn-on and have accounted for the light fired-electrically fired turn-on difference.

A brief description of the equation given in the figure is useful before going into a more complete derivation. In equation 1 the build up of Q_K and Q_2, the holes in the p base, is governed by the transit of holes from the p^+ anode through the n base with a transit time τ_{c1} and a loss through decay with time constants τ_2 and τ_K while J_g gives the gate hole density input. Similarly, Equation 2 describes the build up of electrons, Q_A and Q_2, in the n base region. The next subsection deals with the one dimensional C.C. turn-on model more completely.



$$V = V_{J1} + V_{J2} + V_{J3}$$

$$= Q_K/C_K + V_{J2} + Q_A/C_A$$

(1) $dQ_K/dt + dQ_2/dt = Q_1/\tau_{C1} - Q_2/\tau_2 - Q_K/\tau_K + J_g$ (A) (A)

(2) $dQ_A/dt + dQ_1/dt = Q_2/\tau_{C2} - Q_1/\tau_1 - Q_A/\tau_A + J_g^*$ (A) (A) (B)

(3) $J_A = Q_1/\tau_{C1} + Q_2/\tau_{C2} + dQ_A/dt$ (A)

(4) $J_K = Q_1/\tau_{C1} + Q_2/\tau_{C2} + dQ_K/dt$ (A)

Figure 5-10: Charge control model for light fired thyristors. (A) represents terms needed to predict turn-on delay time. (B) represents terms needed to accommodate light triggering.

Program for C.C. Turn-on

A. THEORY

Normal C.C. equations for electrically fired thyristors are given below[1,2]

$$dQ_1/dt = Q_2/\tau_{c2} - Q_1/\tau_1 \tag{5-1}$$

$$dQ_2/dt = Q_1/\tau_{c1} - Q_2/\tau_2 + J_g \tag{5-2}$$

where Q_1 and Q_2 are excess stored n base and p base majority carrier charges and J_g is the gate current density per effective emitter area. τ_c and τ are the base transit times and recombination lifetimes, respectively.

The above equations are modified to apply to a light fired thyristor to the following set.

$$dQ_1/dt = Q_2/\tau_{c2} - Q_2/\tau_1 + J_g^* \tag{5-3}$$

$$dQ_2/dt = Q_1/\tau_{c1} - Q_2/\tau_2 + J_g \tag{5-4}$$

Solutions of 5-1 and 5-2 and to 5-3 and 5-4 can be made in closed form.

$$d^2Q_1/dt^2 + (1/\tau_2 + 1/\tau_1)\, dQ_1/dt + \left(\frac{1}{\tau_1\tau_2} - \frac{1}{\tau_{c1}\tau_{c2}}\right) Q_1 =$$

$$J_g^*/\tau_{c1} + J_g/\tau_1 + \frac{dJ_g}{dt} \tag{5-5}$$

$$d^2Q_2/dt^2 + \left(\frac{1}{\tau_2} + \frac{1}{\tau_1}\right) dQ_2/dt + \left(\frac{1}{\tau_1\tau_2} - \frac{1}{\tau_{c1}\tau_{c2}}\right) Q_2 =$$

$$J_g/\tau_{c2} + J_g^*/\tau_2 + \frac{dJ_g^*}{dt} \tag{5-6}$$

Note that 5-3 and 5-4 differ from 5-1 and 5-2 by including J_g^* which describes the photosupply of electrons to the n base region. Similarly 5-5 and 5-6, if terms J_g^* are dropped, represent solution to 5-1 and 5-2. It is also clear that in a photo generated gate current situation $J_g^* \equiv J_g$; i.e.,

$$J_g^* = J_g \text{ and}$$

$$\frac{dJ_g^*}{dt} = \frac{dJ_g}{dt} \qquad (5\text{-}7)$$

Hence once concludes that a light fired device will have a more rapid build up of charge than an electrically fired device - in Equation (5-5) by a J_g^*/τ_{c1} increase in driving function and in Equation (5-6) by a $J_g^*/\tau_2 + dJ_g^*/dt$ increase in driving function. Note however that the effective dynamics are unchanged, i.e., both charges tend to exponentially increase with a $(\tau_{c1}\tau_{c2})$ time constant when $\tau_1\tau_2 >> \tau_{c1}\tau_{c2}$ as is normally the case. Perhaps the most effective way to solve (5-5) and (5-6) is by LaPlace transform. Equation (5-5) becomes

$$s^2Q_1(s) - sQ_1(o) - \frac{dQ_1}{dt}(o) + (sQ_1(s) - Q_1(o))\left(\frac{1}{\tau_2} + \frac{1}{\tau_1}\right) + Q_1(s)\left(\frac{1}{\tau_1\tau_2} - \frac{1}{\tau_{c1}\tau_{c2}}\right)$$

$$= J_g^*(s)/\tau_{c1} + J_g(s)/\tau_1 + sJ_g(s) - J_g(o) \qquad (5\text{-}8)$$

Similarly, Equation (5-6) becomes

$$s^2Q_2(s) - sQ_2(o) - \frac{dQ_2}{dt}(o) + (sQ_2(s) - Q_2(o))\left(\frac{1}{\tau_2} + \frac{1}{\tau_1}\right) +$$

$$Q_2(s)\left(\frac{1}{\tau_1\tau_2} - \frac{1}{\tau_{c1}\tau_{c2}}\right) = J_g(s)/_{\tau c2} + J_g^*(s) + sJ_g^*(s) - J_g^*(o) \qquad (5\text{-}9)$$

Collecting terms in (5-8) and (5-9)

$$Q_1(s) = \frac{sQ_1(o) + \frac{dQ_1}{dt}(o) + \left(\frac{1}{\tau_1} + \frac{1}{\tau_2}\right)Q_1(o) + J_g^*(s)/\tau_{c1} + J_g(s)/\tau_1 + sJ_g(s) - J_g(o)}{s^2 + s\left(\frac{1}{\tau_1} + \frac{1}{\tau_2}\right) + \left(\frac{1}{\tau_1\tau_2} - \frac{1}{\tau_{c1}\tau_{c2}}\right)}$$

(5-10)

$$Q_2(s) = \frac{sQ_2(o) + \frac{dQ_2}{dt}(o) + (\frac{1}{\tau_1} + \frac{1}{\tau_2})Q_2(o) + J_g(s)/\tau_2 + J_g^*(s)/\tau_2 + sJ_g^*(s) - J_g^*(o)}{s^2 + s(\frac{1}{\tau_1} + \frac{1}{\tau_2}) + (\frac{1}{\tau_1\tau_2} + \frac{1}{\tau_{c1}\tau_{c2}})} \quad (5\text{-}11)$$

The general solution of the above equation for $\tau_{c1}\tau_{c2} < \tau_1\tau_2$ is the sum of a rising and falling exponential. The relevant poles of (5-10) and (5-11) are given by (5-12) below.

$$P_{1,2} = \frac{1}{2}(\frac{1}{\tau_1} + \frac{1}{\tau_2}) \pm \sqrt{\frac{1}{4}(\frac{1}{\tau_1} + \frac{1}{\tau_2})^2 + (\frac{1}{\tau_{c1}\tau_{c2}} - \frac{1}{\tau_1\tau_2})} \quad (5\text{-}12)$$

Unfortunately two charge quantities were not included in Equation (5-1) through (5-12). These charge quantities relate to the hole and electron charges required to charge up the forward biased n^+p base and the p^+n base junction capacitances Q_K and Q_A, respectively. These quantities are necessary to predict delay times and are extremely important in predicting multi-stage thyristor turn-on. Thus, (5-1) should be modified to

$$dQ_1/dt + dQ_A/dt = Q_2/\tau_{c2} - Q_1/\tau_1 - Q_A/\tau_A \quad (5\text{-}13)$$

Similarly, (5-2) becomes

$$dQ_1/dt + dQ_K/dt = Q_1/\tau_{c1} - Q_2/\tau_2 - Q_K/\tau_K + J_g \quad (5\text{-}14)$$

In a similar fashion dQ_A/dt and dQ_K/dt should be added to the left hand sides of Equations (5-3) and (5-4), respectively and Q_A/τ_A and Q_K/τ_K subtracted from the right hand sides.

What is necessary at this point is a further two equations to define the quantities Q_A and Q_K and some information on τ_K and τ_A, the respective majority carrier lifetimes near the n^+p and n^-p^+ junctions, respectively.

For this, two assumptions will be made. The first is that the terms Q_1/τ_{c1} and Q_2/τ_{c2} are not present until the p^+-n base junction and the n^+-p base junction are both sufficiently forward biased to inject the transitting carriers. The second is the way J_g and J_g^* contribute to Q_K and Q_2 in Equation (5-14) and to Q_A and Q_1 in Equation (5-13). In this respect the simplest approach is to assume Q_A and Q_1 (and Q_K and Q_2) build up consecutively. For example

$dQ_1/dt = 0$ until the p^+n^- base junction has built up to $\sim$.7 Volts which corresponds to a specific value of Q_A which we will term Q_{AT} or Q_A Threshold.

Then $dQ_2/dt = 0$ from that point.

Similarly

$dQ_2/dt = 0$ until the n^+p base junction has built up to $\sim$.7 Volts and a corresponding specific value for Q_K, i.e., Q_{KT}.

Then $dQ_K/dt = 0$ from that point.

Interestingly enough this leads to the possibility that Q_1 and Q_2 will begin to grow at different times. It also leads to the possibility of a different set of time constants for Q_1 build up while Q_2 is pinned at zero or for Q_2 build up with Q_1 pinned at zero. These possibilities have not yet been explored.

Making the insertions of Q_A, Q_K, etc., in Equations (5-3) and (5-4) we get the following set of equations:

$$dQ_A/dt = -Q_A/\tau_A + J_g^*; \quad Q_A < Q_{AT}, \quad Q_K < Q_{KT}$$

$$dQ_A/dt = Q_2/\tau_{c2} - Q_A/\tau_A + J_g^*; \quad Q_A < Q_{AT}, \quad Q_K = Q_{KT}$$

$$dQ_1/dt = -Q_1/\tau_1 - Q_{AT}/\tau_A + J_g^*; \quad Q_A = Q_{AT}, \quad Q_K < Q_{KT}$$

$$dQ_1/dt = Q_2/\tau_{c2} - Q_1/\tau_1 - Q_{AT}/\tau_A + J_g^*; \quad Q_A = Q_{AT}, \quad Q_K = Q_{KT} \qquad (5\text{-}15a,b,c,d)$$

$$dQ_K/dt = Q_K/\tau_K + J_g; \quad Q_A < Q_{AT}, \; Q_K < Q_{KT}$$

$$dQ_K/dt = Q_1/\tau_{c1} - Q_K/\tau_K + J_g; \quad Q_A = Q_{AT}; \quad Q_K < Q_{KT}$$

$$dQ_2/dt = - Q_2/\tau_2 - Q_{KT}/\tau_K + J_g; \quad Q_K = Q_{KT}; \quad Q_A < Q_{AT}$$

$$dQ_2/dt = Q_1/\tau_{c1} - Q_2/\tau_2 - Q_{KT}/\tau_K + J_g; \quad Q_A = Q_{AT}, \; Q_K = Q_{KT} \qquad (5\text{-}16a,b,c,d)$$

These can be solved in a piece-wise fashion in closed form by using LaPlace Transforms given J_g (also J_g^*) or they can be solved by computer as discussed in the following subsection.

COMPUTER SOLUTIONS

Like most complex sets of equations a computer solution is preferred because of the speed and convenience and the availability of plotted output. The results are taken from the following pairs of equations derived from Equations (5-15) and (5-16).

Pair 1. $Q_A < Q_{AT}$, $Q_K < Q_{KT}$

$$\frac{Q_A' - Q_A}{dt} = -(\alpha' Q_A' + \alpha Q_A)/\tau_A + (\alpha' J_g{}^{*\prime} + \alpha J_g{}^*)$$

$$\frac{Q_K' - Q_K}{dt} = -(\alpha' Q_K' + \alpha' Q_K' + Q_K)/\tau_K = (\alpha' J_g + \alpha J_g) \qquad (5\text{-}17)$$

Pair 2. $Q_A < Q_{AT}$, $Q_K \geq Q_{KT}$

$$\frac{Q_A' - Q_A}{dt} = \frac{\alpha' Q_2 + Q_2}{\tau_{c2}} - \frac{\alpha' Q_A' + Q_A}{\tau_A} + (\alpha' J_g{}^{*\prime} + \alpha J_g{}^*)$$

$$\frac{Q_2' - Q_2}{dt} = - \frac{\alpha' Q_2' + \alpha Q_2}{\tau_2} - Q_{KT}/\tau_K + (\alpha' J_g' + \alpha J_g) \qquad (5\text{-}18)$$

Pair 3. $Q_A \geq Q_{AT}$, $Q_K < Q_{KT}$

$$\frac{Q_1' - Q_1}{dt} = -\frac{\alpha' Q_1' + \alpha Q_1}{dt} - Q_{AT}/\tau_A + (\alpha' J_g^{*\prime} + \alpha J_g^*)$$

$$\frac{Q_K' - Q_K}{dt} = \frac{\alpha' Q_1' + \alpha Q_1}{\tau_{c1}} - \frac{\alpha' Q_K' + \alpha Q_K}{\tau_K} + (\alpha' J_g' + \alpha J_g) \qquad (5\text{-}19)$$

Pair 4. $Q_A = Q_{AT}$, $Q_K = Q_{KT}$

$$\frac{Q_1' - Q_1}{dt} = \frac{\alpha' Q_2' + \alpha Q_2}{\tau_{c2}} - Q_{AT}/\tau_A - \frac{\alpha' Q_1' + \alpha Q_1}{\tau_1} + (\alpha' J_g^{*\prime} + \alpha J_g^*)$$

$$\frac{Q_2' - Q_2}{dt} = \frac{\alpha' Q_1' + \alpha Q_1}{\tau_{c1}} - Q_{KT}/\tau_K - \frac{\alpha' Q_2' + \alpha Q_2}{\tau_2} + (\alpha' J_g' + \alpha J_g)$$

(5-20)

The solution of the Q_1 and Q_2 values finally allows a calculation of the currents using (5-21) below.

$$I_{GK}(t) + I_{AK}(t) = Q_1(t)/\tau_{c1} + Q_2(t)/\tau_{c2} + dQ_K(t)/dt = I_A(t) \qquad (5\text{-}21)$$

This in turn allows an estimation of the admittance of the various turn-on regions at low levels of injection - specifically for levels at which the center n^-p junction is reverse biased. This is done by estimating the voltage (at low current) as $V_{supply} - I_A \times R_S$ (for the main stage) where R_S is the snubber impedance. The charge control admittance of that stage is then

$$Y_{cc}^{(n)}(t) = I_A^{(n)}(t)/V(t)^{(n)} \qquad (5\text{-}22)$$

where (n) denotes the specific amplifying stage.

Note that in Equations (5-17) to (5-22), primed Q values refer to the Q value at t + dt. The variables α and α' add to 1 and are included to enable one to use numerical solutions from fully implicit to fully explicit. For example

the implicit equation set ($\alpha' = 1$) has the best convergence properties while the explicit set ($\alpha = 1$) is the simplest. The set with $\alpha = \alpha' = .5$ is the most accurate with errorsof the order of dt^2,

Results of the One Dimensional Charge Control Model

Though the one dimensional C.C. model is limited by being one dimensional and by being limited to the low current range, it is capable of being expanded into a two or three dimensional model. Furthermore, the low current range is just the region in which our S(t) function of Fig. 3-6 needs modification.

Figure 5-11 & 5-12 show device current as a function of time for a gate pulse shape similar to that of the room temperature solid state laser. Two gate amplitudes are used: a 200mA peak gate drive ($\sim$40nJ) which is about twice the gate threshold energy and a 400mA peak at $\sim$10 times the gate threshold energy. The time constants and Q_A and Q_K threshold values believed to be applicable to our present device are given in the figures. The curves with $J_g^* = 0$ apply to the electrically gated case which, it can be seen, turn-on more slowly and with a slower initial current rise. In Figure 5-12,where the current is plotted on a log-linear scale, the current vs. time in the electrically fired case eventually becomes parallel at different gate amplitudes as a consequence of the internal device positive feedback quickly overwhelming the gate input current.

Figure 5-13 & 5-14 represent electrical and light triggered turn-on with an exponentially decaying input pulse. Three gate current amplitudes from low to high are included. In Figure 5-13 the model time constants and Q_A and Q_K threshold values are the same as those of Figures 5-11 & 5-12. In Figure 5-14 the value of Q_{AT}, the amount of charge needed at the n-base -p^+ anode junction to cause injection, has been reduced. It is this parameter that is most difficult to measure. Fortunately, Figure 5-14 shows its effects to be less evident at high values of gate drive where devices are usually operated.

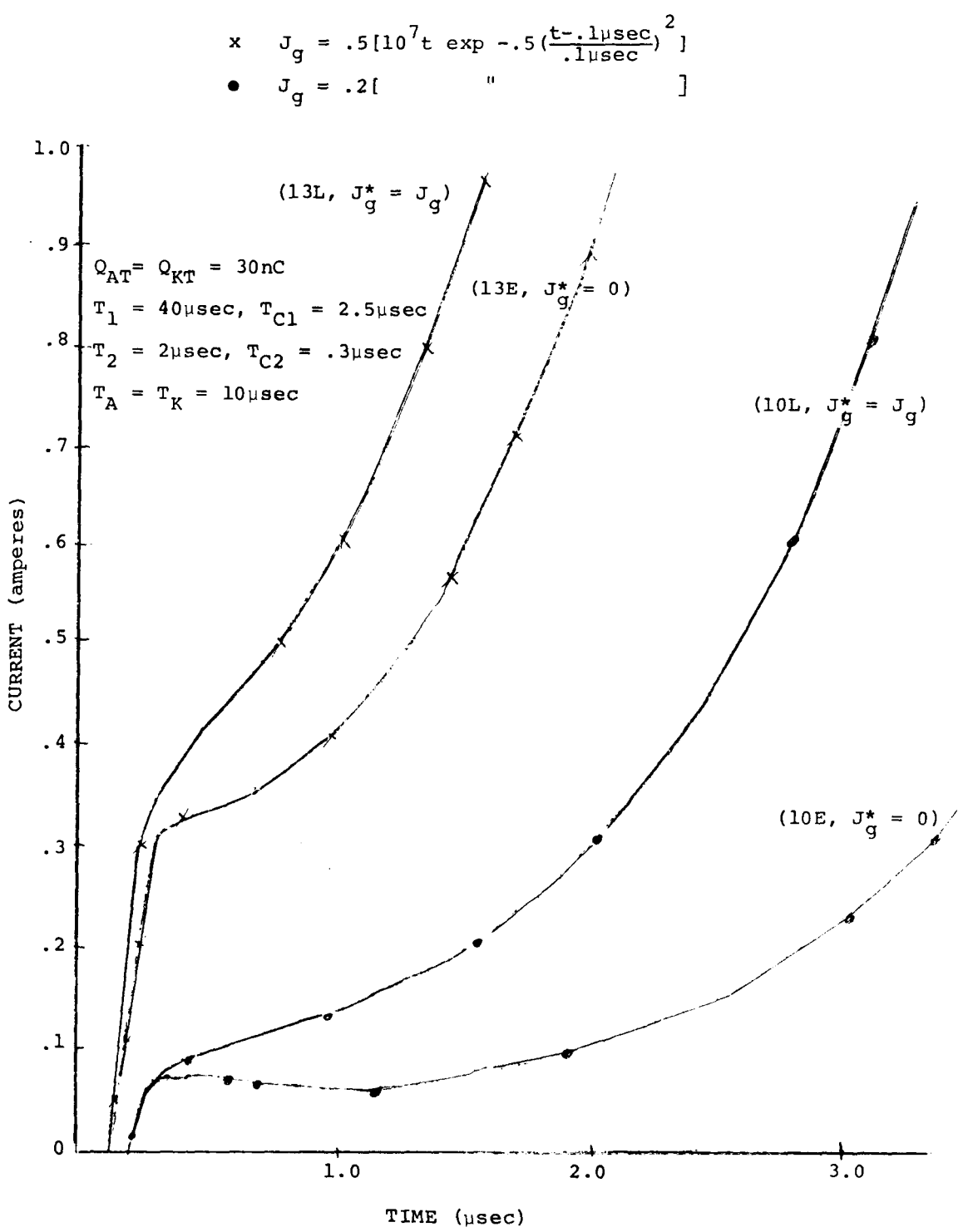


Figure 5-11: Device current predicted by the one dimensional charge control model. Light fired (curves 10L and 13L) and electrically fired (curves 10E and 13E) turn-ons are plotted for a low and a medium gate amplitude.

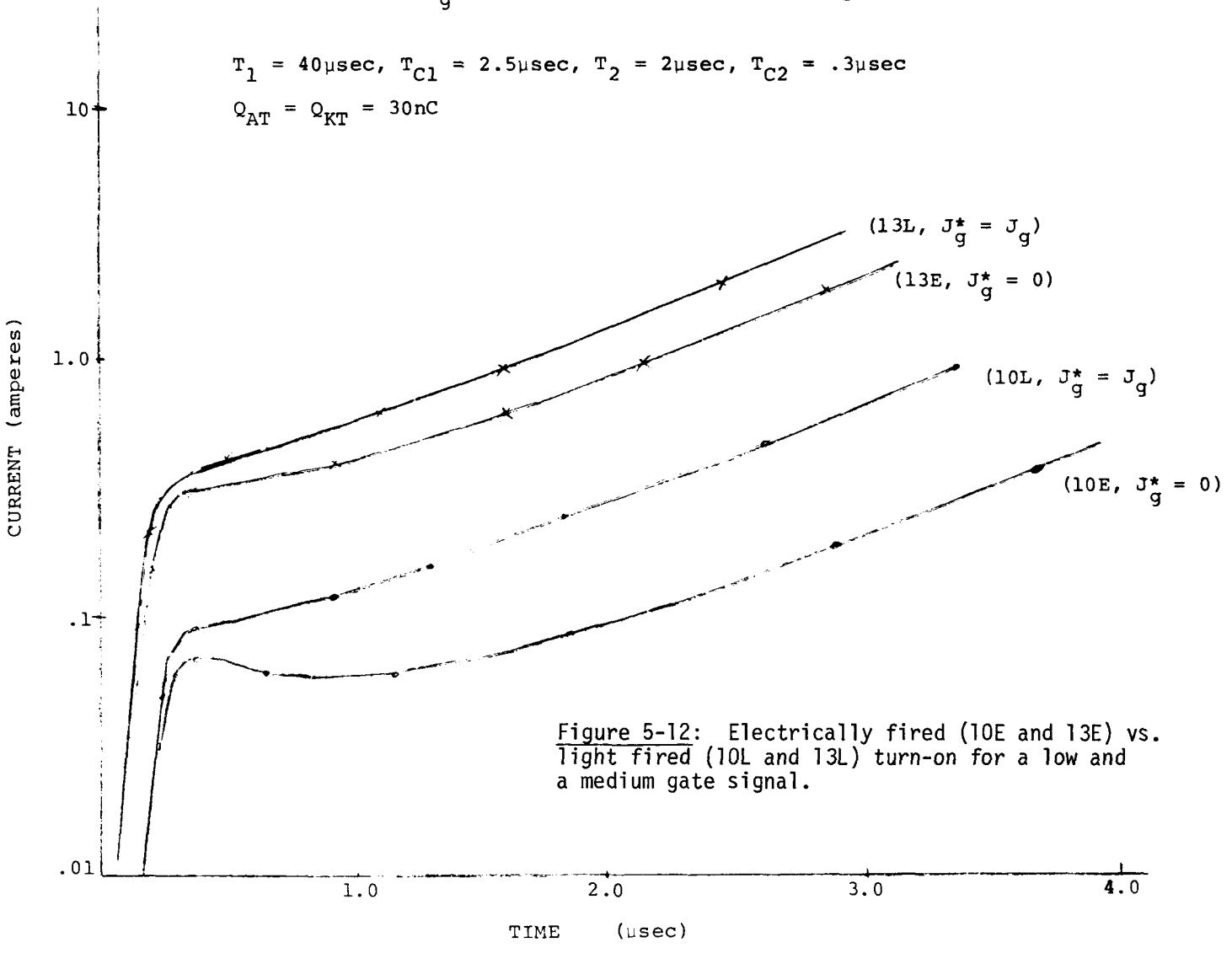


Figure 5-12: Electrically fired (10E and 13E) vs. light fired (10L and 13L) turn-on for a low and a medium gate signal.

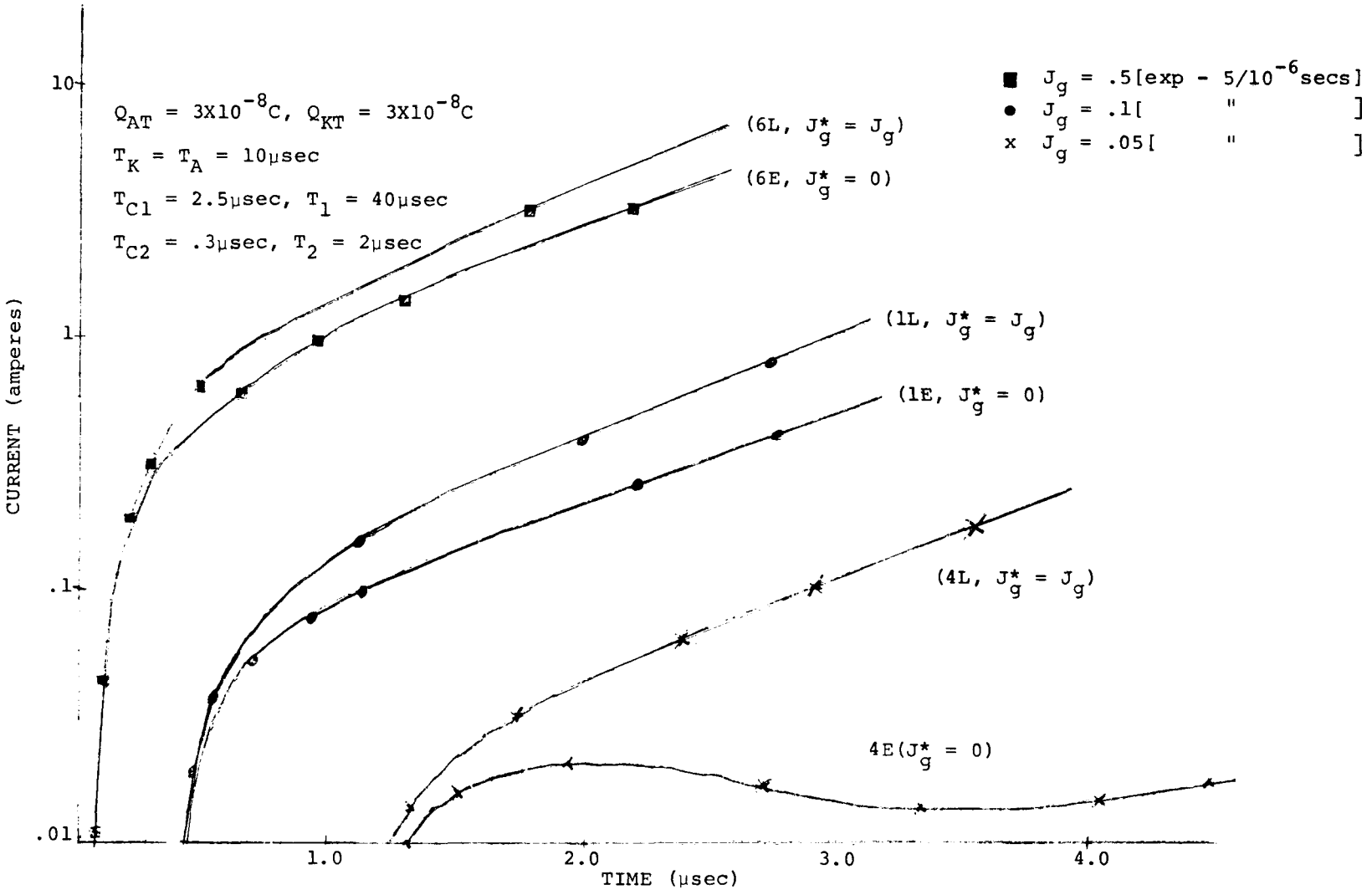


Figure 5-13: Electrically fired vs. light fired turn-on at low, medium and high gate levels.

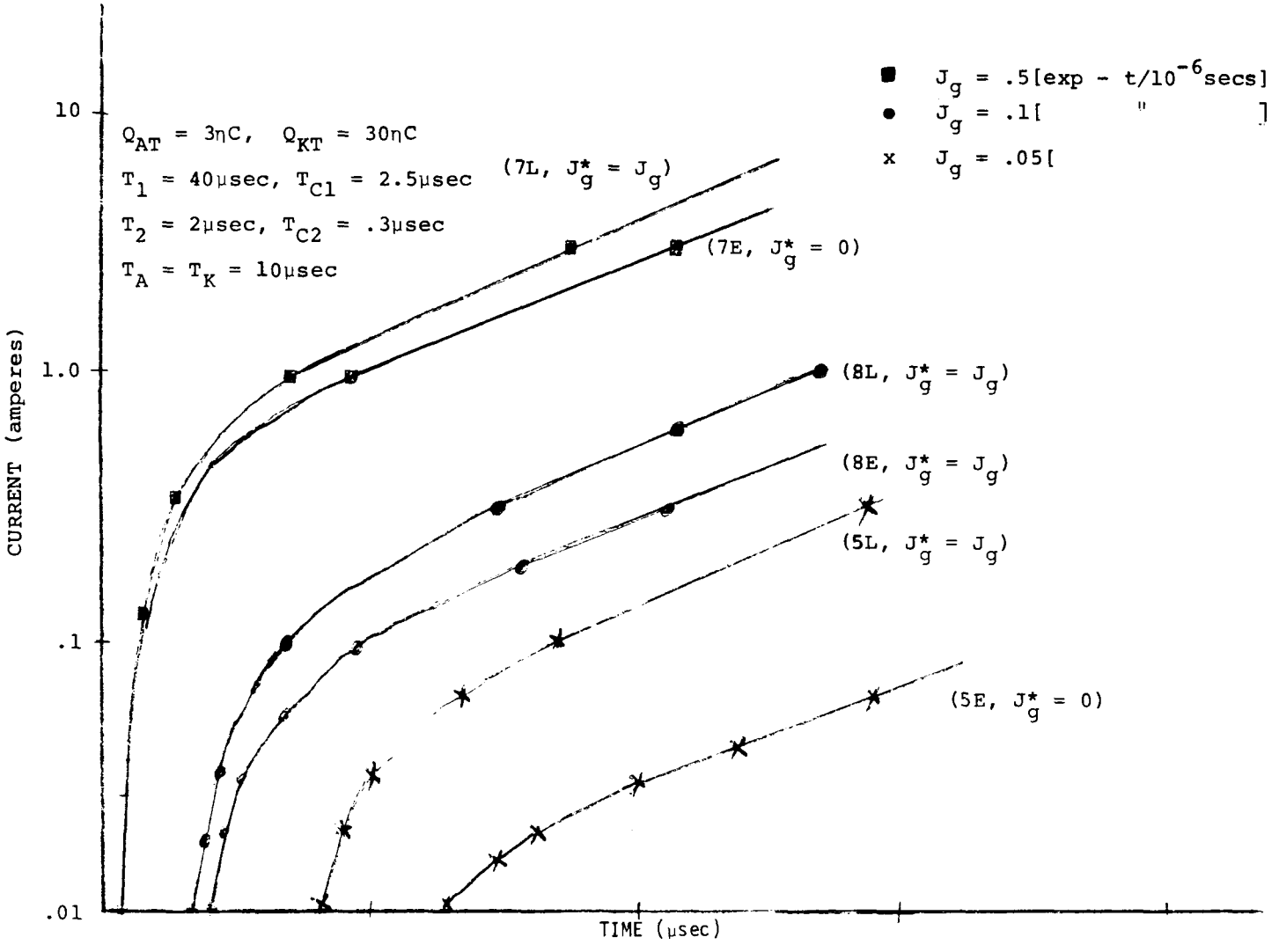


Figure 5-14: Electrically vs. light fired turn-on at low, medium and high gate levels.

However, it is interesting to speculate that a device with the anode junction turning on first, as are the light fired cases in Figure 5-14, might in some way be useful.

Adaptation to the Multi-Stage Model

Once satisfied that the C.C. model was correctly formulated it was included in the S(t) function of Figure 3-6 by simply modifying S(t) admittances as illustrated below:

$$Y_n(t) = Y_o^n + Y_1^n(t-t_{on}) + Y_{cc}^n(t) \qquad (5\text{-}23)$$

Recall that Y_o represents the leakage admittance of stage n while Y_1 which is zero until $t = t_{on}$ gives the best fit to the di/dt of a particular stage. $Y_{cc}^n(t)$ is the charge control admittance of the nth stage. Naturally the input or gate current of that stage is taken from the solution of the model of Figure 3-6. A block diagram is given in Figure 5-15 to show the main outline of the computer program.

Figures 5-16a to f and Figures 5-17a to f show two of the turn-on runs tried so far to fit the 2000V turn-on trace. Figures 5-16a and 5-17a show turn-on voltages of the five stages of an EPRI-GE 3 while (b), (c), (d), (e) and (f) show current, log current, temperature and log Q_1 and log Q_2, respectively. Options built into the program include a simple selection of either light or electrical firing, an option for RV or RS modulated resistance during turn-on and an area feature which tries to extend the applicability of the C.C. model to slightly higher currents by utilizing the known[8] on region spreading velocity of the SPCO built thyristors.

To this point we do not believe that we have reached the best set of parameters for the present device. Separately measuring each stage's turn-on properties should allow for closer fit to experiment and more confident design of future devices.

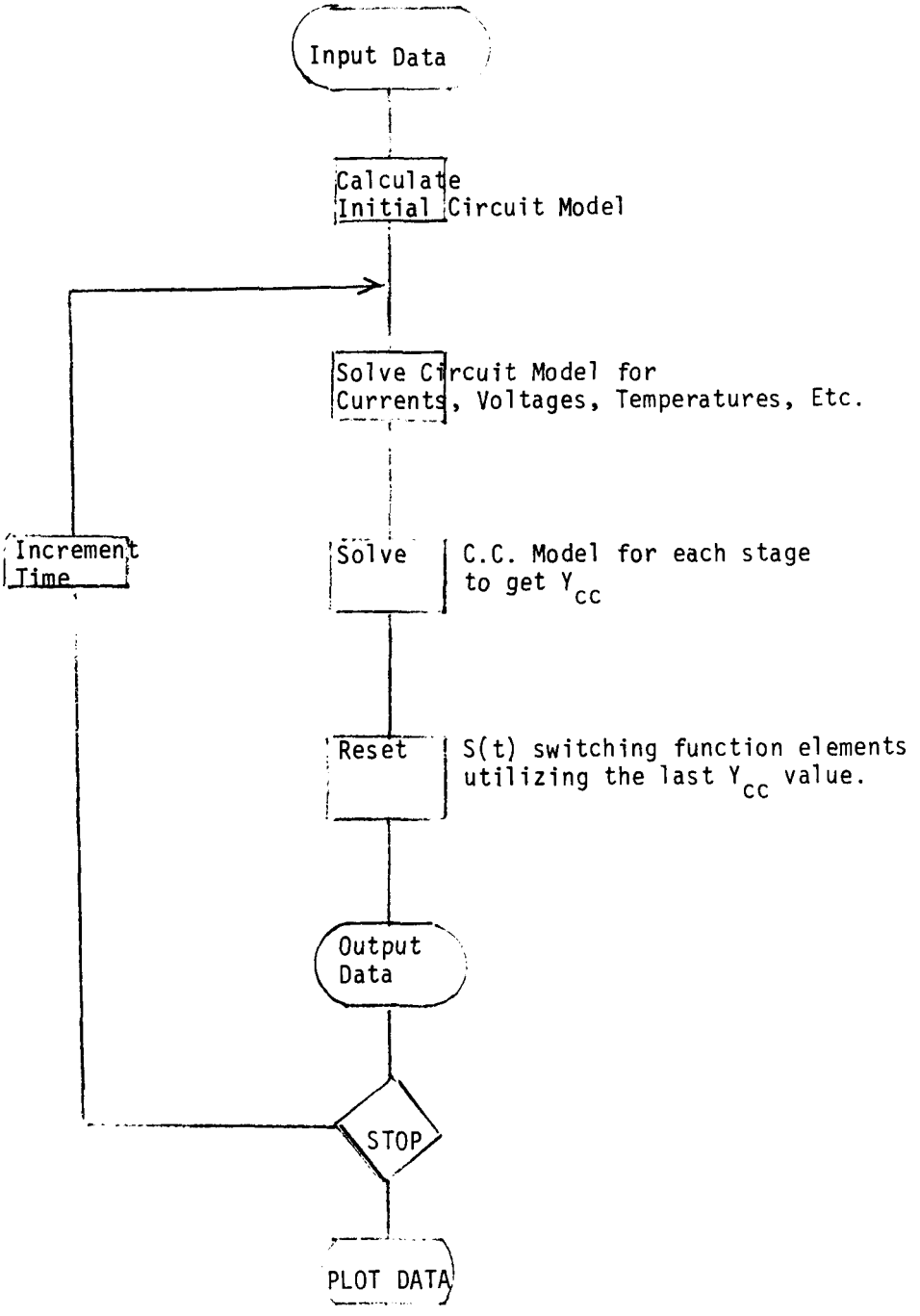


Figure 5-15: Computer program block diagram.

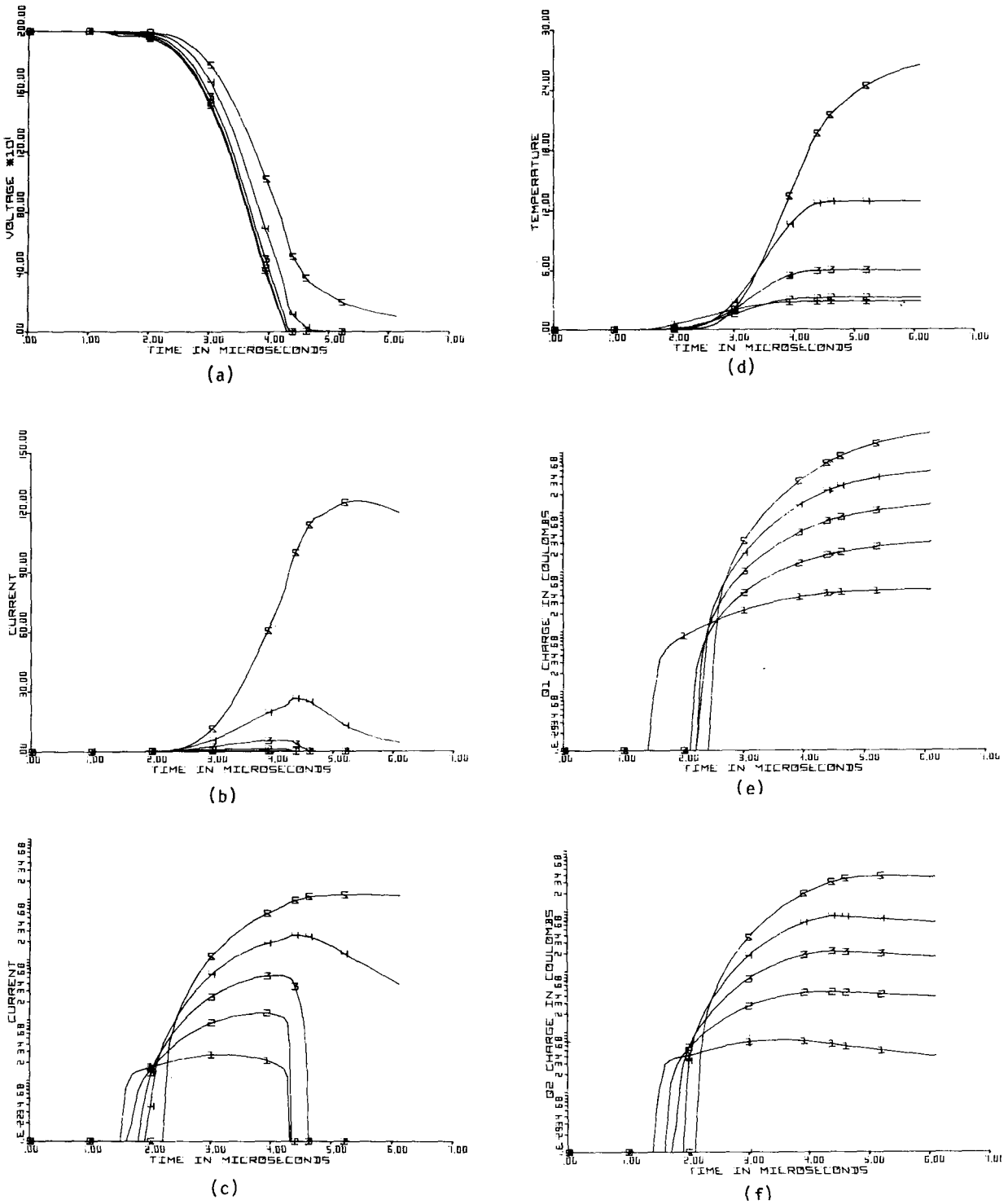
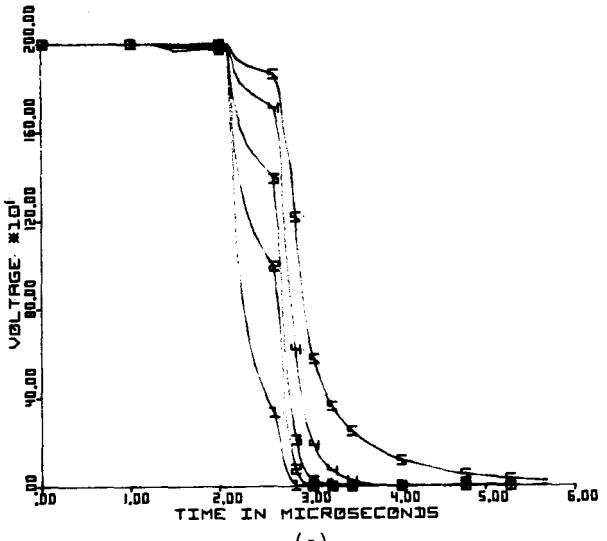
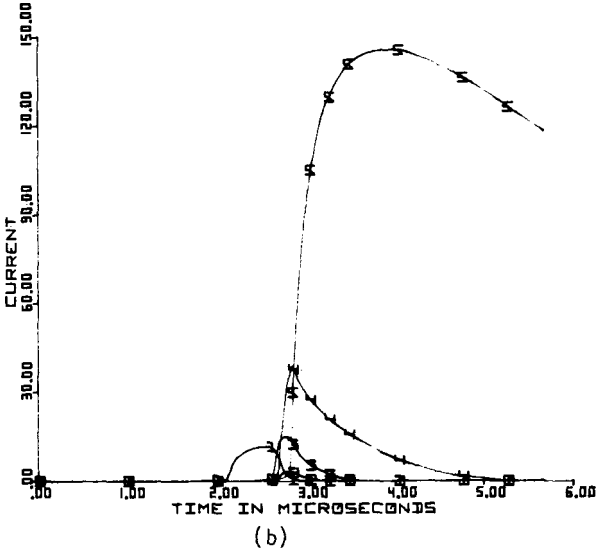


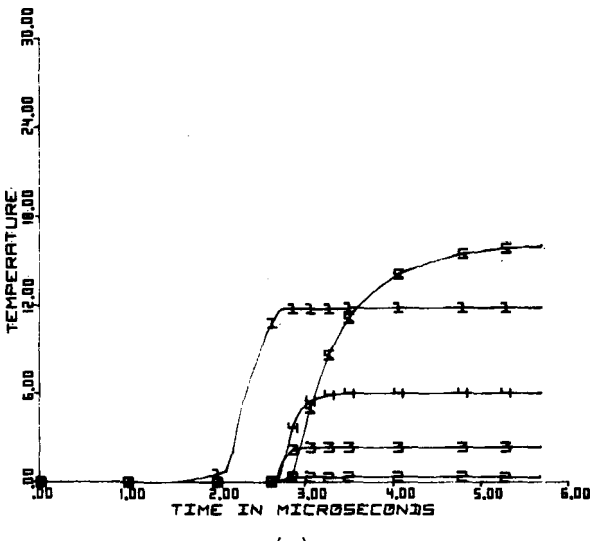
Figure 5-16: Turn-on model (see Fig. 3-6) prediction of voltage (a), current (b), log current (c), temperature (d), log Q_1 (e), and log Q_2 (f) of a four amplifying stage device (such as the EPRI-GE3). Numbers on the curves indicate the stages "1" being the light fired gate stage and "5" being the main stage. The "S" element admittance values contain only $Y_{cc}(t)$ as predicted by the one dimensional C.C. model.



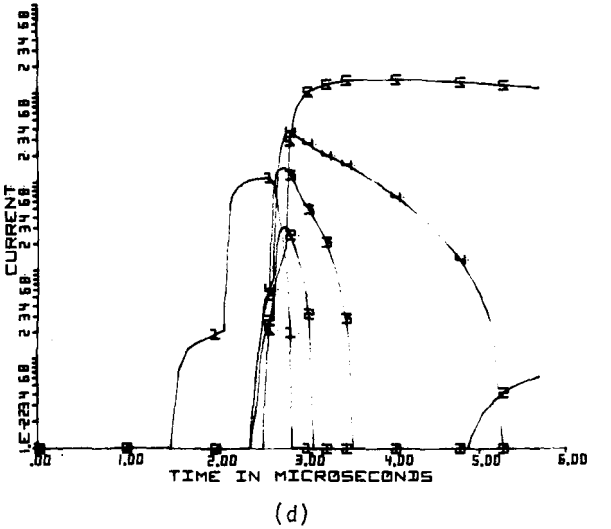
(a)



(b)



(c)



(d)

Figure 5-17: Turn-on model (see Fig.3-6) prediction of voltage (a), current (b), log current (c) and temp. (d) of a four amplifying stage device (such as EPRI-GE3). Numbers on the curves indicate the stages "1" being the light fired gate stage and "5" the main stage. The "S" element admittance values are C.C. model controlled to a current density in each stage of $100A/cm^2$. At that point the linear admittance Y_1 dominates to give the $700A/\mu sec$ di/dt.

CONCLUSION

What we are forced to conclude after working through the experimental results and the theory is that amplifying gate stages, while essential in situations (like ours) where there is a weak gate signal, are susceptible to interstage transients - voltage transients causing the surface arcing and currents causing channel burns. It also appears from the new modelling that the first stage of a light fired device can see a longer than normal on-time due to its inherent turn-on speed advantage over the following stages which are electrically gated.

From the results, however, we did see at least a partial solution to our major problem involving arcing at location "b" in Figure 4-21. An etch to round the surface there and possibly a passivation of the channel would almost certainly reduce surface fields (but not surface voltage or current) by at least an order of magnitude. Therefore a new run of devices was made which incorporated this process variation. This run will be referred to as Run 2. The di/dt capabilities of the Run 2 devices is discussed in the following section of this report.

Section 6

EPRI RUN #2 DEVICE FABRICATION AND TESTING

INTRODUCTION

After the discovery and confirmation of surface arcing problems in the Run 1 devices, fabrication of a second run of EPRI-GE devices was initiated. For this new run of devices the process was altered to prevent a sharp, arc-prone edge from occurring at location "b" as shown in Figure 4-21. This would, it was believed, allow a measure of the true device di/dt capability to be measured without the arc-over complication. The make-up of the Run 2 series of devices is shown in Table 6-1, the overall intention being to make both moderate and high sensitivity devices with various channel lengths and differing numbers of amplifying stages. From this starting array, the number of useful devices for further testing was somewhat reduced. The initial tests are described briefly in the following.

The first tests performed on Run 2 devices are room and elevated temperature breakdown voltages. Where these exceed the 2600 volt device rating, devices are given an elevated temperature dv/dt test at 2000V/μsecond, hopefully to something in excess of 2000 volts. The results of these tests were comparable to similar measurements made on the standard electrically fired device except for the fair number of devices with sub-standard dv/dt values. The cause of this difference is simply the 22 - 25μ etch performed on approximately half the devices to get a higher than usual photo gate sensitivity which also, of course, increases sensitivity to dv/dt turn-on.

The next measurements on the device consist of a measurement on the curve tracer of the electrical gate current needed to trigger the most sensitive stage(s) of the fabricated devices at an anode voltage of 50 volts. The

TABLE 6-1: RUN 2 DEVICES PROCESSED

Devices	Process Options	Comments
L1A-1 to 5	12 to 15μ etch for moderate sensitivity	L1A devices have the longest channel between the first and second stages. Some have a Series R option built-in. None have the n^+ alignment band feature
6 to 10	22 to 25μ etch for high sensitivity	
11 to 15	22 to 25μ etch plus built-in Series R	
L1B-1 to 5	12 to 15μ etch for moderate sensitivity	Same as L1A except for higher sensitivity pilot stage
GE2C-1 to 5	12 to 15μ etch for moderate sensitivity	Largest number (5) of amplifying stages. These devices have the shortest channel.
6 to 10	22 to 25μ etch for high sensitivity	
GE3C-1 to 5	12 to 15μ etch for moderate sensitivity	Device with four amplifying stages.
6 to 10	22 to 25μ etch for high sensitivity	
GE3D-1 to 5	12 to 15μ etch for moderate sensitivity	Device with interrupted n^+ metallization feature. Otherwise identical to GE3C.
6 to 10	22 to 25μ etch for high sensitivity	
GE4A-1 to 5	12 to 15μ etch for moderate sensitivity	Double amplifying gate device. This device has the largest light sensitive gate area. Its channel length is long.
6 to 10	22 to 25μ etch for high sensitivity	
GE4C-1 to 5	12 to 15μ etch for moderate sensitivity	Same as GE4A except for gate ring and alignment band options.
6 to 10	22 to 25μ etch for high sensitivity	

results are similar to those given for Run 1 devices. Note, however, that for device type EPRI-GE4A, no electrical gate sensitivity measurements can be made. The sensitivities are as high as can be achieved with these device designs without losing dv/dt capability. In fact some gate sensitivities were in the 2 to 3 mA rather than the 3 to 5 mA region and the dv/dt's of these devices were less than the desired 2000V/μsecond.

Oven Temperature Turn-on Tests

The first turn-on tests designed to investigate whether the Run 2 process modifications would prevent the local burn-out or arcing problem were performed at 25°C and at 100°C. A liquid nitrogen cooled solid state laser source was used to fire the thyristor at a 25Hz rate. Discharge from a .5μF 10 Ω snubber which was enough to degrade most Run 1 devices, was used in a series of tests from 50 to 2000 volts at room temperature and from 50 to 1750 volts at elevated temperature. The gate pulse amplitude was selected for a 2±.5μsecond delay time at 50 volts at room temperature. Devices L1A-3 and 5, L1B-2, 2C1, 3 and 4, 3C2 and 5, 3D1, 7 and 9 and devices 4A3, 6 and 8 were tested. None of these devices were degraded electrically during the test. Each was carefully inspected and photographed before and after the test at 67X magnification. No evidence of arcing or local burn marks were seen although one device had a metal pattern that could be interpreted as a melt, flow and resolidification of the aluminum contact in one of its channel regions. Re-inspection of the devices at a 600X magnification, however, failed to reveal more than that one instance of the pattern.

With this preliminary success we began an exhaustive series of di/dt tests designed to assess di/dt capability. They involved a rather lengthy test procedure of varying switching voltage, temperature, di/dt and snubber resistance and capacitance. These tests and hybrid di/dt tests on EPRI light fired thyristors are the subject of the following sections.

DI/DT TEST RESULTS

The second run of EPRI devices was undertaken on a reduced number of device options which, from Run 1 test results, showed the better device characteristics. Table 6-1 shows a catalogue of the devices that were started through processing.

What made the second run necessary was a premature breakdown in di/dt testing that was the result of surface arcing described in previous sections. The surface arcing was eliminated (but not the high channel voltage transient that caused them) by a simple round off etch prior to passivating the devices. This result was proved by elevated temperature turn-on tests with a .5μFd, 10 Ω snubber discharged from 1800 to 2000 volts. This test followed standard device blocking tests, static (open gate) dv/dt tests and forward drop testing. These later tests showed that the Run 2 devices were normal (compared to the standard 2600V electrically triggered HVDC cell) with the exception of a few devices being too light sensitive and consequently having a lower than normal dv/dt capability. What we now conclude is that the masked etch that is done to tailor device sensitivity should be 15 to 18 microns which would result in a 3 - 5 mA gate threshold current and a 2000V/μsecond dv/dt. With these preliminary tests completed most of the test effort was spent on di/dt testing.

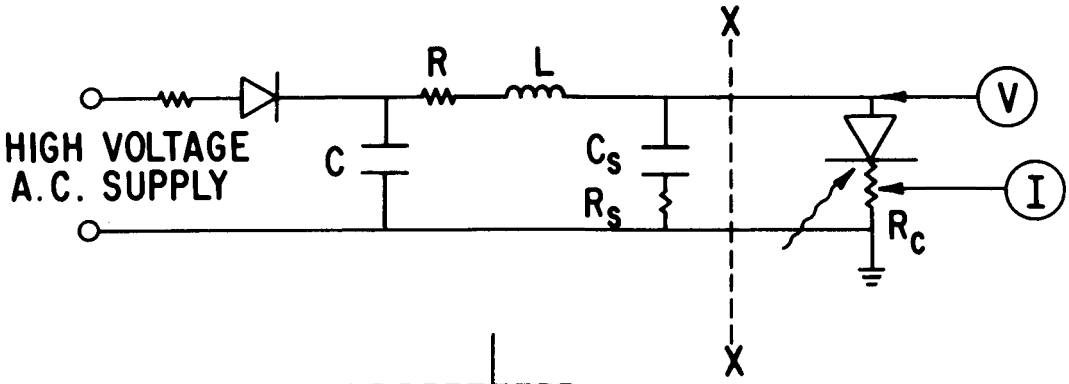
Two types of di/dt testing were performed on Run 2 devices. The normal di/dt tests in which the light fired amplifying stages are integral to the main device will be called "integral gate" or "integrated" di/dt tests. In the hybrid option, where the light fired stage and perhaps one or more additional amplifying stages are separated from the main device, the tests will be termed "separate gate" tests or "separate" di/dt tests. In this latter case the output of the separate light fired gate device is fed into the gate of a regular electrically fired device. In this option the electrical device will be the normal 2600V, HVDC thyristor.

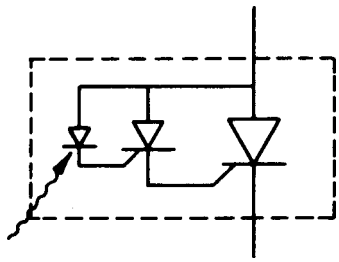
In all, 41 devices were tested as integral light fired devices and, of these, the inner stages of 29 were tested as the separate gate device in the hybrid or separate gate test. Results of both types of tests were positive, indicating that there are several light fired device types in Table 6-1 that will serve adequately in an HVDC application calling for 2600 volt devices.

Integral Gate di/dt Tests

Figure 6-1 shows both the integral test set up and the separate gate di/dt test network. For this section of the report we will concentrate on the integral gate di/dt tests. As can be seen from Figure 6-1(a), there are five major circuit components that could be varied. First there is the R_S, C_S snubber network whose presence is required to produce an initial current pulse to about 40A without any circuit inductive elements to limit di/dt. This serves to simulate stray capacitive discharge. Second is the R, L, C network which is selected to give a peak current at approximately the device rating and at a di/dt value which is adjusted in test. R_c, a small (.0025 Ω), inductance free resistor inserted to monitor device current, is held constant. In general our tests would start out with a small C_S (.1μFd) and a large R_S (100 Ω) and at a low di/dt (40A/μsec). As well as varying the circuit elements we used two ambient temperatures - the first giving a junction temperature of 30 to 40°C, and the second giving a junction temperature of between 100 and 110°C. Table 6-2 gives the initial test sequence that was followed. Note that the R, L, C network is not given. Instead the di/dt that it produced switching from 1750 volts is given. Note that the di/dt at an equivalent stress, but turning on at 1400 volts, would be about 25% larger. After several devices of each type had been tested the test matrix was considerably shortened by starting the test at one di/dt level below what we expected to be the 50% failure value. At this di/dt we would perform the tests at 25°C ambient (35° junction temperature) with perhaps an 85% pass rate.

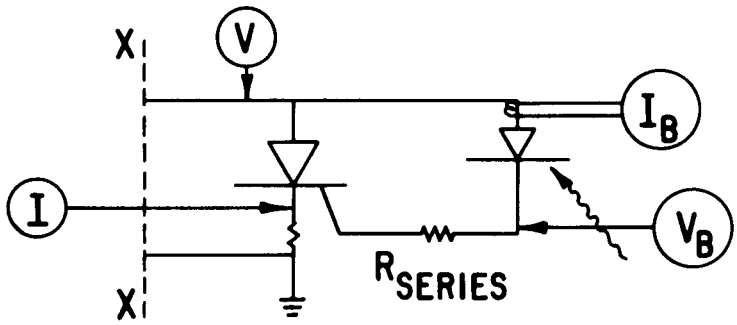
a.) INTEGRAL GATE TEST





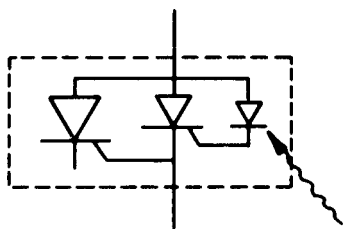
SCHEMATIC OF
2 AMPLIFYING STAGE
LIGHT FIRED DEVICE

b.) SEPARATE GATE TEST



MAIN ELEC.
FIRED DEVICE

SMALL LIGHT
FIRED DEVICE



SCHEMATIC SHOWING
HOW THE INNER STAGES
OF A TWO AMPLIFYING
STAGE DEVICE CAN BE
USED AS A SMALL
SEPARATE GATE DEVICE.

Figure 6-1: Circuit diagrams and device schematic for integral and separate gate di/dt tests.

TABLE 6-2: TEST SEQUENCE FOR INTEGRAL DEVICE di/dt

Test	R_S, C_S (ohms, μFd)	di/dt* (A/μsec)	Junction Temperature (1^oC)
1	(100, .1)	33	35
2	(100, .5)	33	35
3	(37.5, .1)	33	35
4	(37.5, .5)	33	35
5	(100, .1)	75	35
6	(100, .5)	75	35
7	(37.5, .1)	75	35
8	(37.5, .5)	75	35
9-16	Repeat of 1-8 but at $T_J \sim 105^oC$		
17	(100, .1)	110	105
18	(100, .5)	110	105
19	(37.5, .1)	110	105
20	(37.5, .5)	110	105
21	(100, .1)	150	105
22	(100, .5)	150	105
23	(37.5, .1)	150	105
24	(37.5, .5)	150	105

* At 1400 volts the same turn-on stress would be achieved with a 25% higher di/dt.

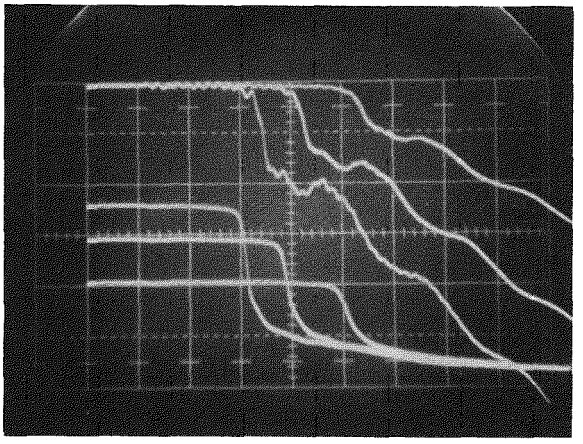
This would be followed by the high temperature tests at the next di/dt value after which the device would be released from the test and examined. Both passing and failing devices were examined for evidence of surface arcing and failed devices inspected carefully for physical evidence of failure mode.

Gate Drive Amplitude di/dt Failure Anomaly

In the previous description of the di/dt tests no mention was made of gate drive amplitude. In fact, we attempted to have all tests done at a minimum gate overdrive which would be the same for all devices tested. To remove the uncertainties of different gate sensitivities and different photocoupling efficiencies, the laser voltage, and thus the energy in the laser photo-pulse, would be adjusted so that at room temperature the device turn-on delay at 50 volts would be 2μseconds.

After having tested about one-third of all devices, we decided that before removing a passed device from test we would vary the photo-pulse energy both up and down from the test value. In general the laser supply voltage was lowered until the high voltage (1750 volts) turn-on delay time reached two microseconds. Normally, due to better turn-on speed and better photo efficiency at high voltage, delay time at the normal test gate energy would be about one microsecond. In general fewer failures were observed than might have been expected during the additional one minute under high turn-on stress conditions. Quite the opposite occurred on increasing the laser supply voltage, and thus its light pulse energy, to its maximum. Delay time shortened as expected but many more device failures occured than were expected. In fact, about half the passed devices now failed, indicating that increased local turn-on losses must be occurring. Figure 6-2 shows the turn-on traces of a device with different di/dt values while Figure 6-3 shows the same device at maximum di/dt stress being turned on with different levels of light energy. It appears that the signature of extra turn-on stress is exemplified by a voltage vs. time as shown in Figure 6-4. Here we have

a) Device 4A3, T_J = 105°C, Standard Gate Drive

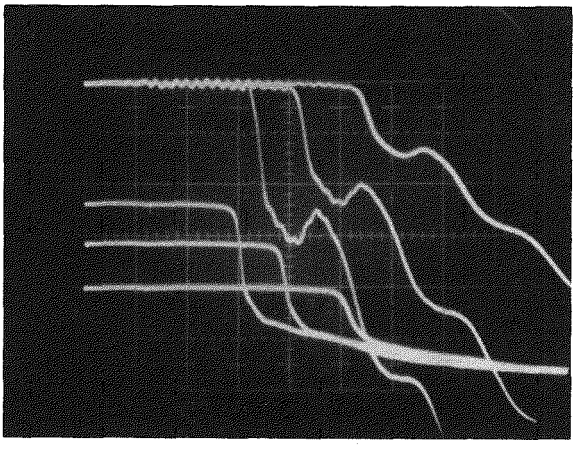


I_{SCR}, 40A/div (positive downward)

V_{SCR}, 500V/div

.5μsecond/div

b) Device 4A3, T_J = 105°C, Standard Gate Drive



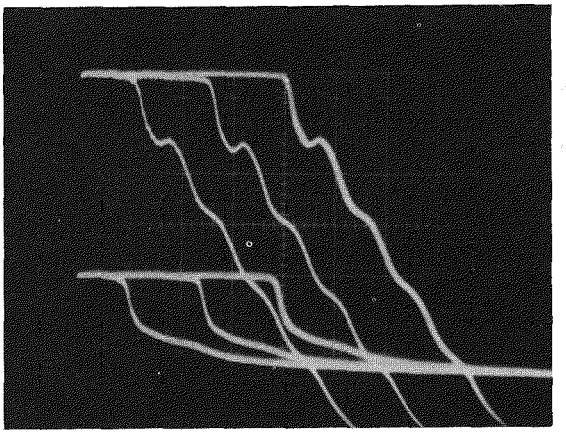
I_{SCR}, 40A/div (positive downward)

V_{SCR}, 500V/div

.5μsecond/div

Figure 6-2 (a) and (b): Typical current, voltage traces in di/dt test for turn-on from 1000, 1400 and 1750 volts. Device 4A3 passed the 75A/μsecond maximum at 1750 volts in (a) and the ∿160A/μsecond di/dt at 1750 volts in (b). Both (a) and (b) used the standard gate drive.

a) Device 4A3, T_J = 105°C, Gate Drive Varied

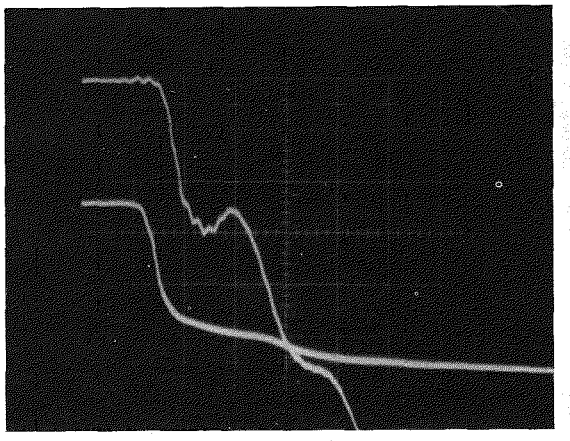


I_{SCR}, 40A/div (positive downward)

V_{SCR}, 500V/div

1μsec/div

b) Device 4A3, T_J = 105°C, at Maximum Gate Drive
Device fails after 50 seconds during this test.



I_{SCR}, 40A/div (positive downward)

V_{SCR}, 500V/div

.5μsec/div

Figure 6-3: di/dt turn-on test traces at different gate drive levels for the same R, L and C as 6-2(b). (a) Turn-on at 1000 volts with low, standard and high gate drive. (b) Turn-on from 1750 volts (~160A/μsec di/dt) at maximum gate drive.

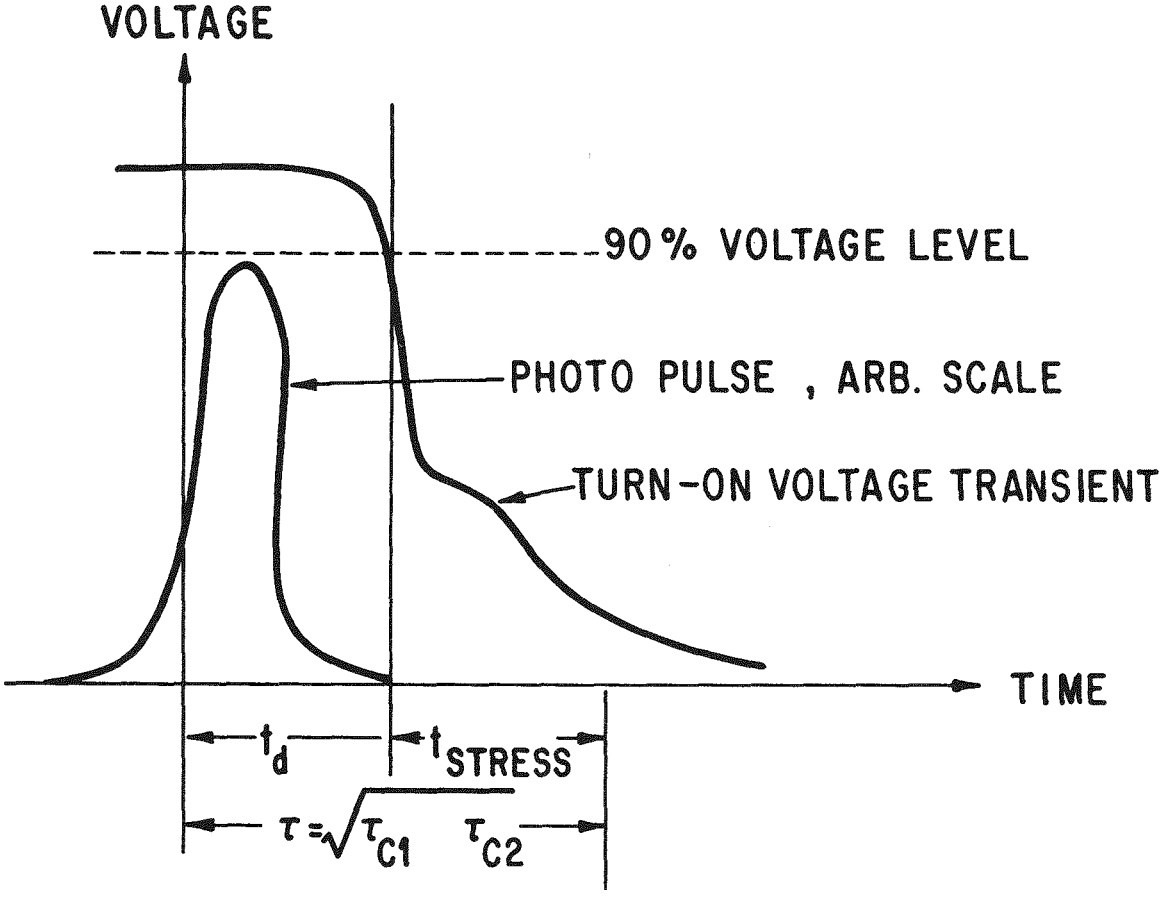


Figure 6-4: Illustration of gate and following stage(s) turn-on. Note that the electrical stage's fastest response is fixed by physical time constants while the light fired stage's minimum delay time is not limited. Thus t_{stress}, the period of high gate stage stress, can be longer at very high photo-gate drives.

defined a "high stress period" in which the gate stage is essentially on while the following electrically fired stages are only starting to build up base charge. The stress is not alleviated until the turn-on of the next stage is reasonably complete. What is responsible for the longer than normal high stress period is the near instantaneous turn-on of the gate stage which can occur at very high levels of incident gate photo energy. In fact, what is seen is a sudden acceleration of a trend which is seen at all gate energies, namely a greater percentage decrease in the photo gate amplifying stage delay time than in the next electrically fired stage when measured against device delay time. Consequently there is the possibility of increased turn-on power dissipation. For example, the charge control turn-on model described in the previous section predicts that the photo gate stage can be as much as a time constant ahead of an electrically fired stage of the same gate sensitivity and when gated at the same current level. It appears, at this time, that the devices in which the anomaly is best seen belong to the device types with one or more amplifying stages and which also have a minimum lateral p base impedance between the light fired gate stage and the main emitter metallization.

Test Results

Figure 6-5 shows in a relatively simple manner the di/dt capability of the devices measured in all of the integral gate di/dt tests. Percent of tested devices surviving is plotted against di/dt for the different designs comprising Run 2. In all of these the snubber RC network is .5μFd, 37 Ω and the junction temperature approximately 105°C. The size of the error bars is large because of the relatively small number of devices of each type. The number tested is shown in each graph. Disregard, for the present, the references to the "SG" (separate gate) tests.

The poorest device is clearly the GE2 type which appeared to have surface channel voltage problems leading to a degradation type of failure. This would generally be seen as a drop in blocking voltage to somewhere near 1000 volts.

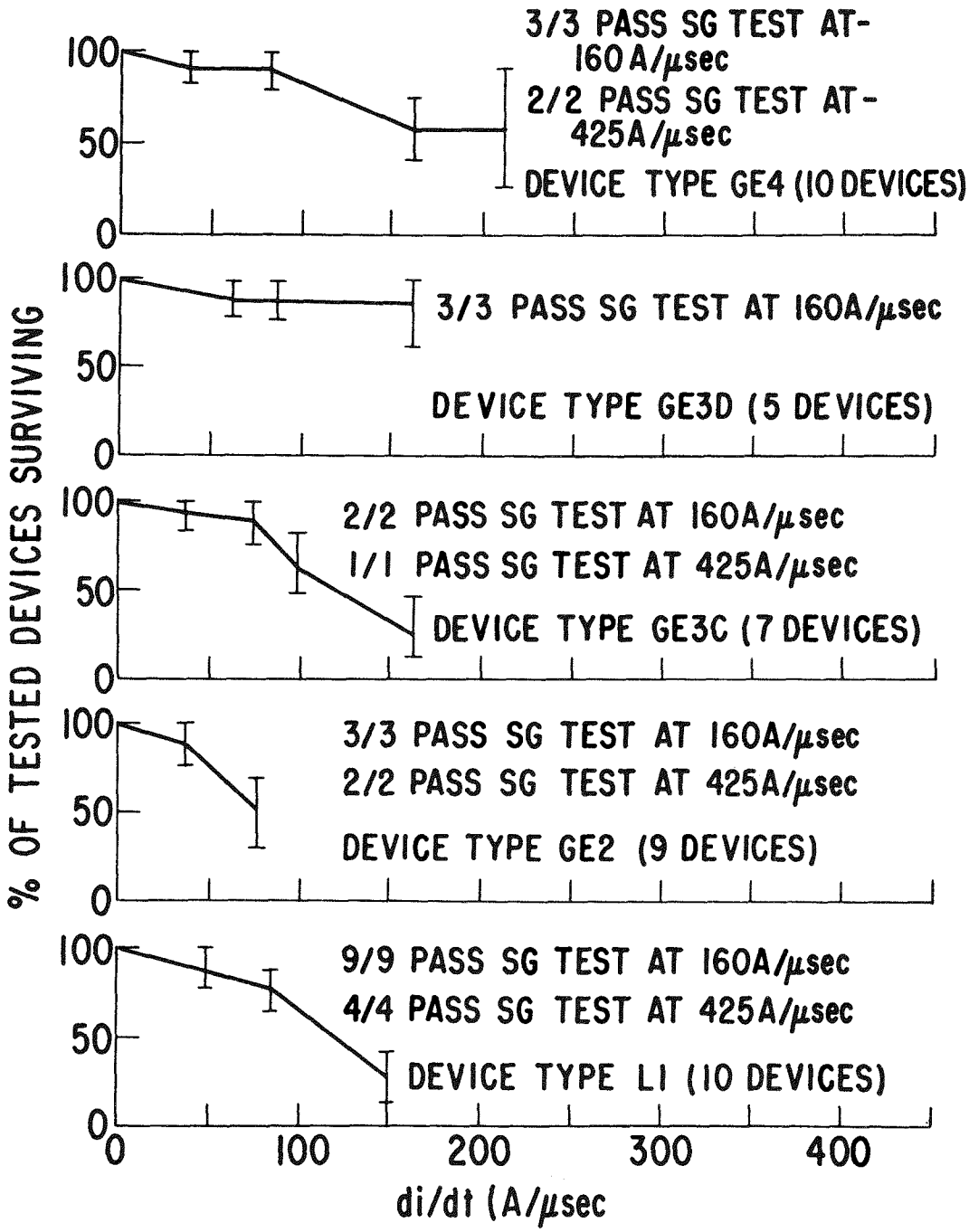


Figure 6-5: Integral gate and separate gate di/dt test summary. Results of the integral gate test are plotted vs di/dt. Results of the separate gate tests are noted for each device type.

With this surface related degradation failure there would not appear to be any loss in reverse blocking capability so that the failed device would still perform as needed under most HVDC operating conditions.

The L1 type test devices, first described and fabricated in Phase I, were the second worst with respect to di/dt capability. These devices, with only two amplifying stages, the first one smaller than we now feel optimum, degraded at the light fired stage turn-on line, a condition that leads to gradually worsened blocking voltage. Recall that these devices were included in Run 2 as being the least affected by channel voltage and current transients.

The failure mode of device type GE3C was similar to that of type GE2C with local surface degradation resulting in a loss in forward blocking voltage. Physically it was sometimes possible to see a surface crater and/or aluminum melt and reflow. This would generally occur under the outside edge of the n^+ alignment band between the second and third amplifying stages and has led us to consider and implement a minor design change to the n^+ alignment band. Narrower bands would result in smaller voltage drops across the bands and to a substantially lower device surface failure mode rate in both the GE2 and GE3 device series.

There is little to choose between the GE3D device and the GE4 type devices. Both series have a 50% failure point above 150A/μsecond with perhaps the GE3D device being the better. It is very interesting to compare the performance of the GE3D device with that of the GE3C, and the GE4 devices with the L1 devices. The superiority of the GE3D compared to the GE3C device seems to confirm the usefulness of the interrupted n^+ metallization concept and the improved performance of the GE4A devices over the L1 devices could be ascribed to the presence of the n^+ alignment band. Both concepts appear to be useful and applicable in electrically fired thyristor design as well.

As a final comment, it is relevant to point out that the results shown in Figure 6-5 are somewhat inferior to similar test results on the regular electrically fired device in which the 50% point is greater than 250A/μsecond. The reliability implications of this degree of di/dt stress test difference will be discussed further.

HYBRID TURN-ON TESTING OF RUN 2 DEVICES

Introduction

Hybrid turn-on testing of EPRI light fired devices was first done in Phase I after discovering that the EPRI-GE1 device was subject to thermal runaway in high temperature snubber dump tests. This type of testing led to the discovery and prediction of the critical turn-on line temperature excursion and ultimately to the GE2, 3 and 4 device series all of which were able to withstand the initial snubber dump that caused failure in the GE1 device. In testing the new device types the snubber dump was augmented by a follow-on di/dt waveform by doing the same experiment in the di/dt test fixture. The test circuit is shown schematically in Figure 6-1(b).

Although the hybrid light fired approach may appear, at first glance, to be more costly than the integral gate approach, by virtue of a further device and series impedance, R_{series}, there are a number of advantages to this approach. From the technical viewpoint, the insertion of a fixed, moderate wattage impedance in the initial turn-on current path virtually guarantees the survival of the light fired gate stage under extremely high circuit and stray capacitance di/dt stress. Also from a technical point of view, one now has the ability to remove the light fired stage from the higher temperatures which characterize the main device heat sink. Another possible advantage which our limited tests have shown is a net increase in the di/dt capability of the main electrically fired device resulting from the fact that part of the normal turn-on losses have been shunted to the gating device. From a system mechanical point of view

it will be easier to orient, couple to, and to maintain a small device than the main device in its heat sink. From a device fabrication view point, it is possible to separate the yield of the small (say 150 devices per 3 inch wafer) device from that of the main device. This would remove some of the present processing constraints imposed on the integral light fired device.

The data presented in this section illustrates two things. First it shows the tremendous di/dt capability of the light fired gate designs in the separate gate configuration. Second, because we can separately measure gate device and main device current and voltage, we are able to more easily see the interaction between a fast turn-on initial stage (device) and a slower turn-on following stage (device).

Some of the data presented relates to the single possible technical drawback of a hybrid gate system and that is the inter-relationships between gate pulse length, minimum firing voltage and the value chosen for the R_{series} protective impedance.

di/dt Capability

Approximately 20 devices were tested under the separate gate circuit conditions shown in Figure 6-1(b). In these tests the gate stage was tested at temperatures above and below that of the electrically fired device. The di/dt was varied from 35A/μsec to approximately 425A/μsec with the stiffest snubber dump (.5μFd, 37 Ω). At first the devices were tested only to 160A/μsecond. When all of these passed with R_{series} varied from 10 Ω to 500 Ω , we began to test to 425A/μsecond, the highest our circuit would allow. Still we observed no gate stage failures but would experience an occasional main device failure. This would often correlate to a weak photo gate signal and a subsequent slow rising (comparatively) gate device turn-on current. However, the gate stage itself was not affected by either high or low photo-gate energies. The

425A/μsecond failure observed for the main electrically fired devices were less frequent that one would expect which leads to the tentative conclusion that hybrid turn-on can also benefit the main stage, one reason, the sharing of turn-on losses, was mentioned earlier. A second reason may, in fact, be the availability of a normally stiff gate current from the gate stage device at high voltage.

Table 6-3 gives a list of the parameters independently varied and their ranges for the separate gate test. The results of the stiffest test (maximum voltage, maximum di/dt, minimum R_{series}, maximum gate drive) are given in Figure 6-5. The result was no gate stage failures at all.

Typical Turn-on Transients

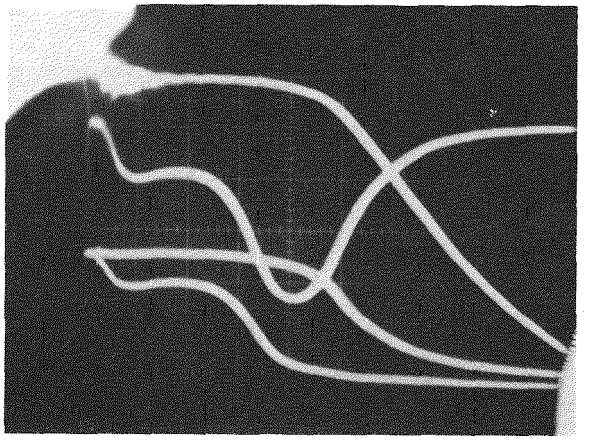
Figure 6-6(a)-(c) illustrates separate gate turn-on at 50 volts for device 4A3 using the standard gate drive. In each of the photos the top trace is I_A, the main device current, and the next lower trace, I_B, the gate device current. Both are positive downward to leave room for V_A, the main device voltage and V_{AB}, the gate device voltage. All of the curves are similar and demonstrate the always present turn-on stages of the hybrid (and integral) light fired thyristor. First one gets a current I_B (and a voltage drop in $V_{AB} \approx I_B R_{series}$) due to photo current. With this current plus internal feedback, the device builds up base charge. After a sufficient charge has built up the device turns on; I_B increases rapidly, and V_{AB} falls off. All this time I_B is trying to gate the main device which turns on when it attains a sufficient base charge level. I_A rises rapidly and V_A falls.

The difference between figures 6-6(a), (b) and (c) lie in a decreasing R_{series} which can be seen to result in a faster turn-on of the following stage. This is because I_B cannot be any larger than V_A (here 50 volts) divided by R_{series}. In fact, before the first stage turn-on the value of I_B is smaller than this - approximately V_A divided by the sum of R_{series} and $R_{GK}(0)$, the

TABLE 6-3: VARIABLES CONSIDERED IN THE SEPARATE GATE di/dt TEST

Variable	Range
di/dt	33 to 425A/μsec
Temperature of the gate device	25 to 105°C
Temperature of the main device	25 to 105°C
R_{series}	10 to 500 Ω
Gate Drive	Minimum - device barely fires at 1000 Volts Standard - 2μsecond delay at 50V High - maximum rated laser pulse

a) R_{series} = 200 Ω, 2μsec/div



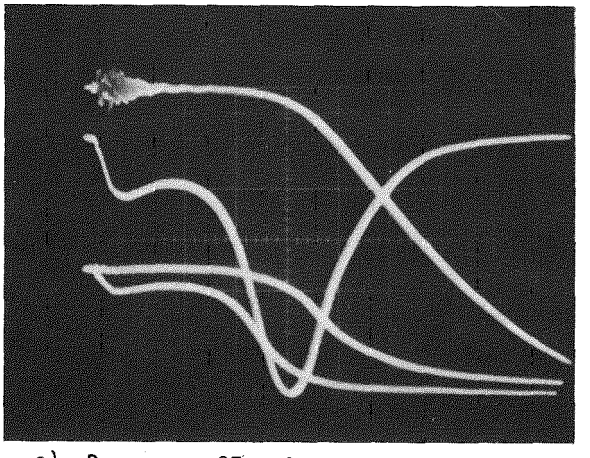
I_A(main device current) 4A/div

I_B(gate device current), 50mA/div

V_A(main device voltage), 20V/div

V_{AB}(gate device voltage), 20V/div

b) R_{series} = 100 Ω, 2μsec/div



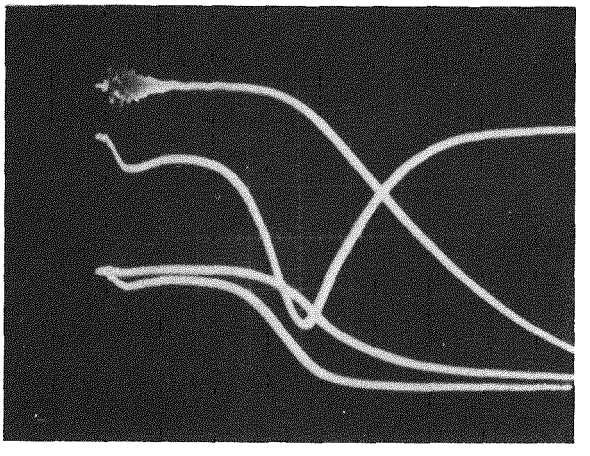
I_A, 4A/div

I_B, 50mA/div

V_A, 20V/div

V_{AB}, 20V/div

c) R_{series} = 37Ω, 2μsec/div



I_A, 4A/div

I_B, 100mA/div

V_A, 20V/div

V_{AB}, 20V/div

Figure 6-6: The effect on gate and main device turn-on of varying R_{series} at low anode voltage. Both the gate and main device are at ∿100°C. The snubber is .5μF, 37 Ω. The gate device is 4A3(2).

initial internal gate-cathode impedance of the main device. Further, the maximum initial photo current peak is smaller still - V_A divided by R_{series} plus $R_{GK}(0)$ plus the snubber resistor, R_S. This leads to the one technical difficulty of the hybrid approach and that is a relationship between gate pulse length, peak photo current amplitude, and the protective series impedance. First $V_A/(R_{series} + R_{G-K}(0) + R_S)$ times the pulse length τ_L must be able to deliver the required threshold gate charge of the gate stage. Once this stage is on it will feed current for at least one snubber circuit time constant into the main device whence $V_A/(R_{series} + R_{GK} + R_S)$ must be greater than the gate current threshold of the main device. For the main device to stay on it is sufficient for $V_A/(R_{series} + R_S)$ to be greater than the latching current. Figure 6-7 gives a simplified set of curves relating R_{series} to the minimum firing voltage for different pulse lengths. Note that our room temperature solid state laser source has just the value at which the gate stage and main stage device cross-over. This really implies that above a pulse width of .2μseconds it would be the main electrically fired device which would set the minimum firing voltage while below .2μseconds it would be the gate stage.

Figure 6-8(a) to (c) shows turn-on from 1750 volts with the same R_{series} as in Figure 6-6. Here the turn-on of the gate stage and the turn-on of the main stage are so nearly coincident that I_B is held down to 1A in (a) and 1.5A in (c), far less than V_A/R_{series}. This is because the rapid transfer of current to the main device occurs so soon that the gate device has barely started to turn-on. In fact, at one point the current in the gate stage actually reverses. For example, in (a) we can follow the normal reaction of the gate stage from .5μseconds to about 1.2μseconds where the main device turns on. During this time the gate device is building up charge and is in the process of turning on as is evidenced by a growing value of I_B. However at 1.2μseconds the main device turns on and, as the result of having a much larger initial turn-on line, catches and surpasses the gate stage. Being

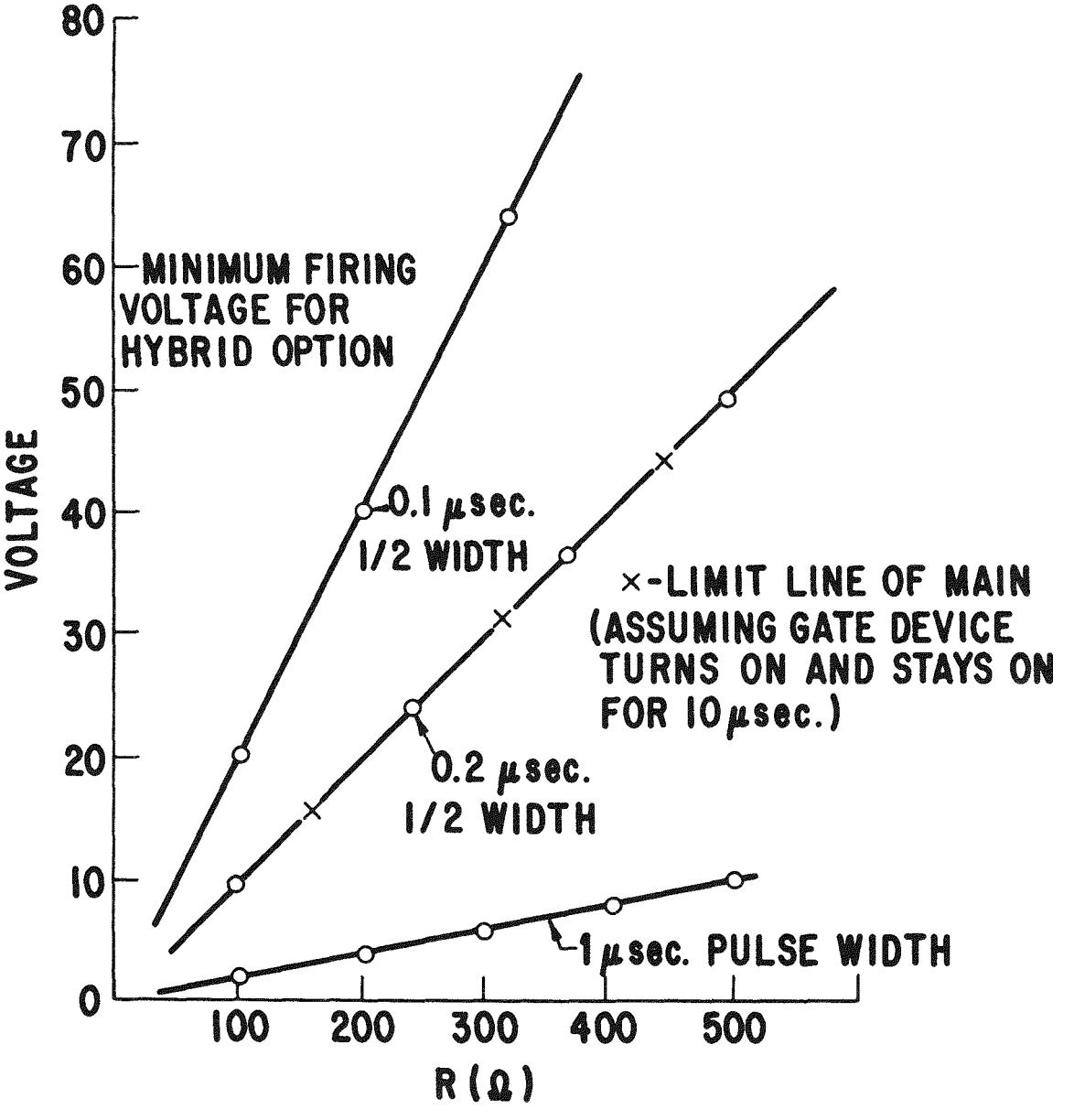
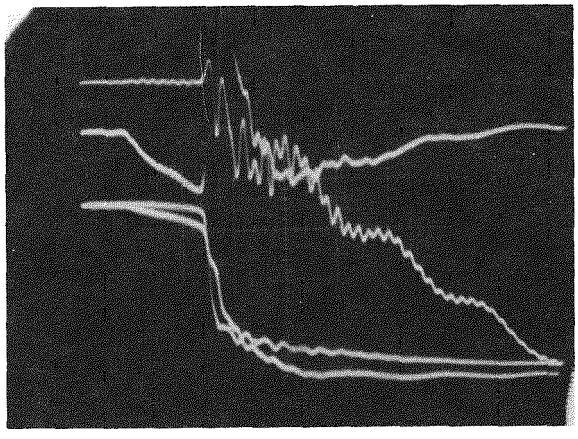


Figure 6-7: Maximum value of R_{series} which will allow separate gate stage turn-on for different gate pulse widths.

a) R_{series} = 200, .5μsec/div



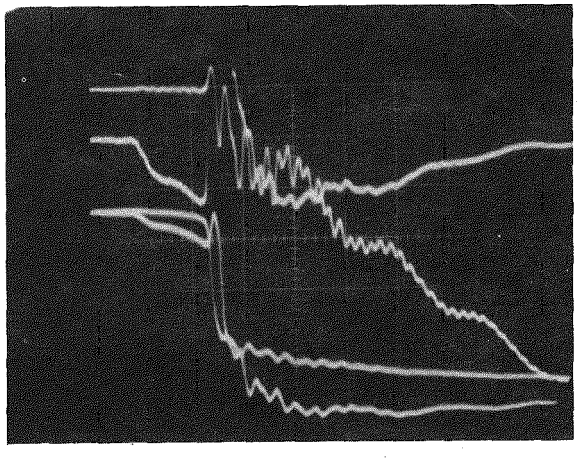
I_A, 80A/div

I_B, .5A/div

V_A, 500 V/div

V_{AB}, 500V/div

b) R_{series} = 100, .5μsec/div



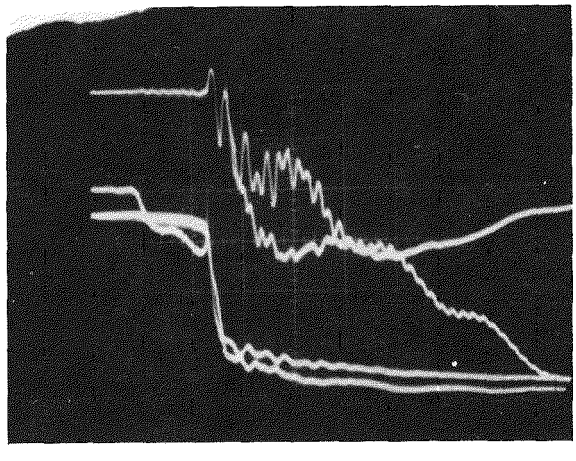
I_A, 80A/div

I_B, .5A/div

V_A, 500V/div

V_{AB}, 500V/div

c) R_{series} = 37, .5μsec/div



I_A, 80A/div

I_B, .5A/div

V_A, 500V/div

V_{AB}, 500 V/div

Figure 6-8: The effect on gate and main device turn-on varying R_{series} at high anode voltage. Both gate and main device are at ∿100°C. The snubber is .5μF, 37 Ω. The gate device is 4A3(2).

"more on" than the gate stage, charge flows from the main device into the gate device for a short period of time. This accounts for the I_B current reversal.

Gate Drive Anomaly in the Separate Gate Test

Figure 6-9 shows the effect of varying the photo gate amplitude. Here device 4A3 is used as the gate device and turned on at four different levels of gate photocurrent all at V_A = 1000 V. In Figure 6-9(a) the gate level is turned down so that the device is barely firing. Turn-on of the gate stage device is so slow that the main device is able to build up base charge at the same time. Note the I_B current reversal that marks this turn-on mode. In Figure 6-9(b) a higher gate drive has been used. Turn-on is speeded up but not so much that the main device turn-on cannot rapidly follow that of the gate device. In Figure 6-9(c) we see the beginning of a trend toward a finite separation in the gate stage and main stage turn-on. Gate stage turn-on has become so fast that the inherently slower electrically fired main stage is not able to respond in time to hold down I_B. The I_B value now has a sharp peak which starts to climb toward V_A/R_{series} rather than to a value representative of the gate drive requirements of the main stage. At the highest gate drive, as shown in Figure 6-9(d), the width of the I_B peak is even wider and the I_B value seems to be reaching a limit imposed by R_{series}, R_{GK}, and R_S. It is very likely that the high stress period, illustrated with the integral gate particularly in Figure 6-4, corresponds to the turn-on modes of Figures 6-9(c) and (d) but without the current limiting action of R_{series} to save the inner stages (and possibly channels) from degradation.

Delay Time Variation

One final consideration that an R_{series} element complicates is the delay time that is expected vs. anode voltage for different R_{series} values. Figure 6-10 shows, for a fixed value of photo energy, the sort of variation in turn-on delay time to be expected. Here device 3C1 was turned on at different anode (V_A) voltages with a 37 Ω R_{series} and a 500 Ω R_{series}. As can be seen, there

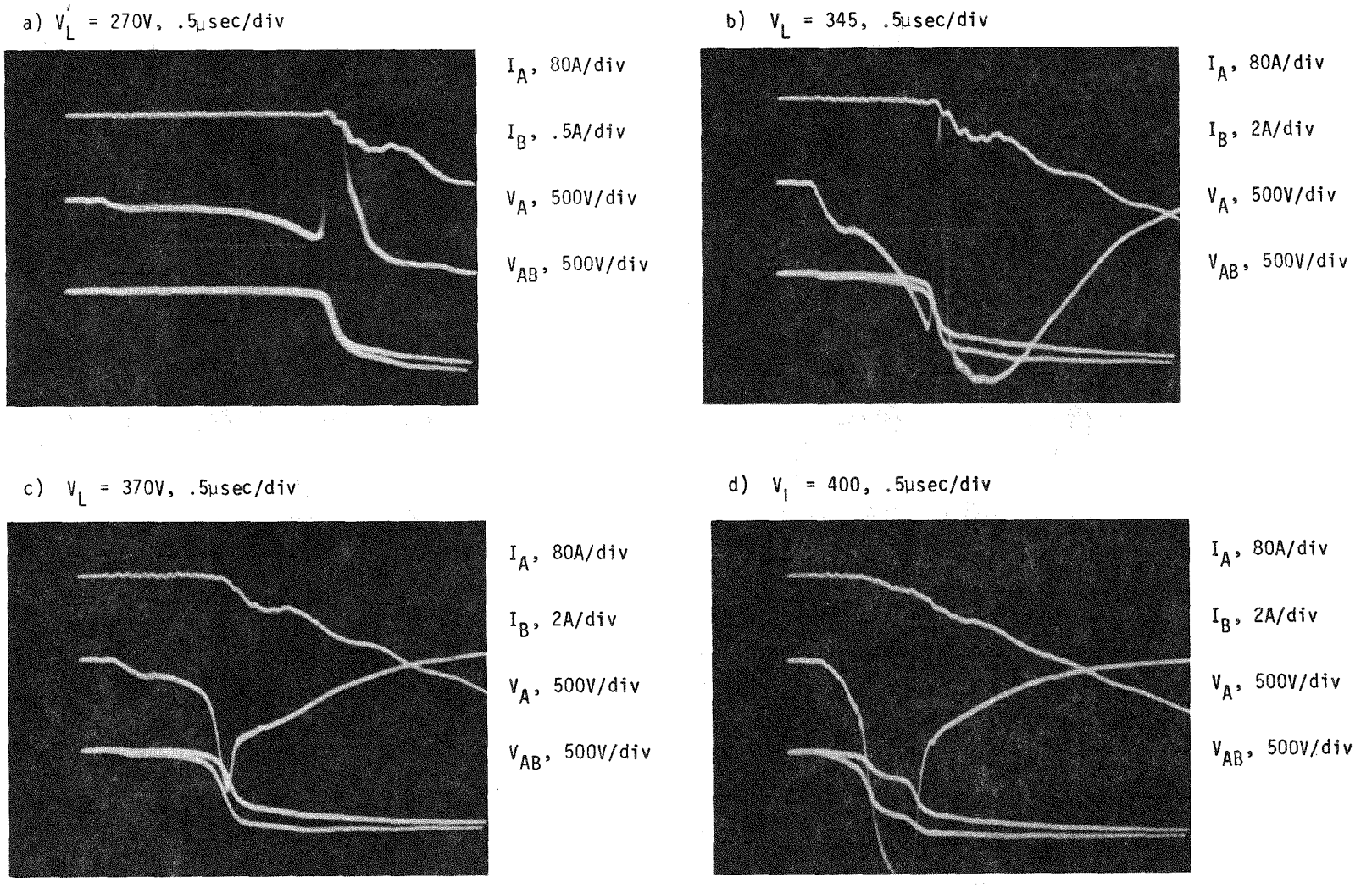


Figure 6-9: Effect of varying light pulse amplitude in separate gate turn-on tests for device 4A3(2). Both devices are at 100°C. The snubber is .5μF, 37 Ω. R_{series} was 37 Ω.

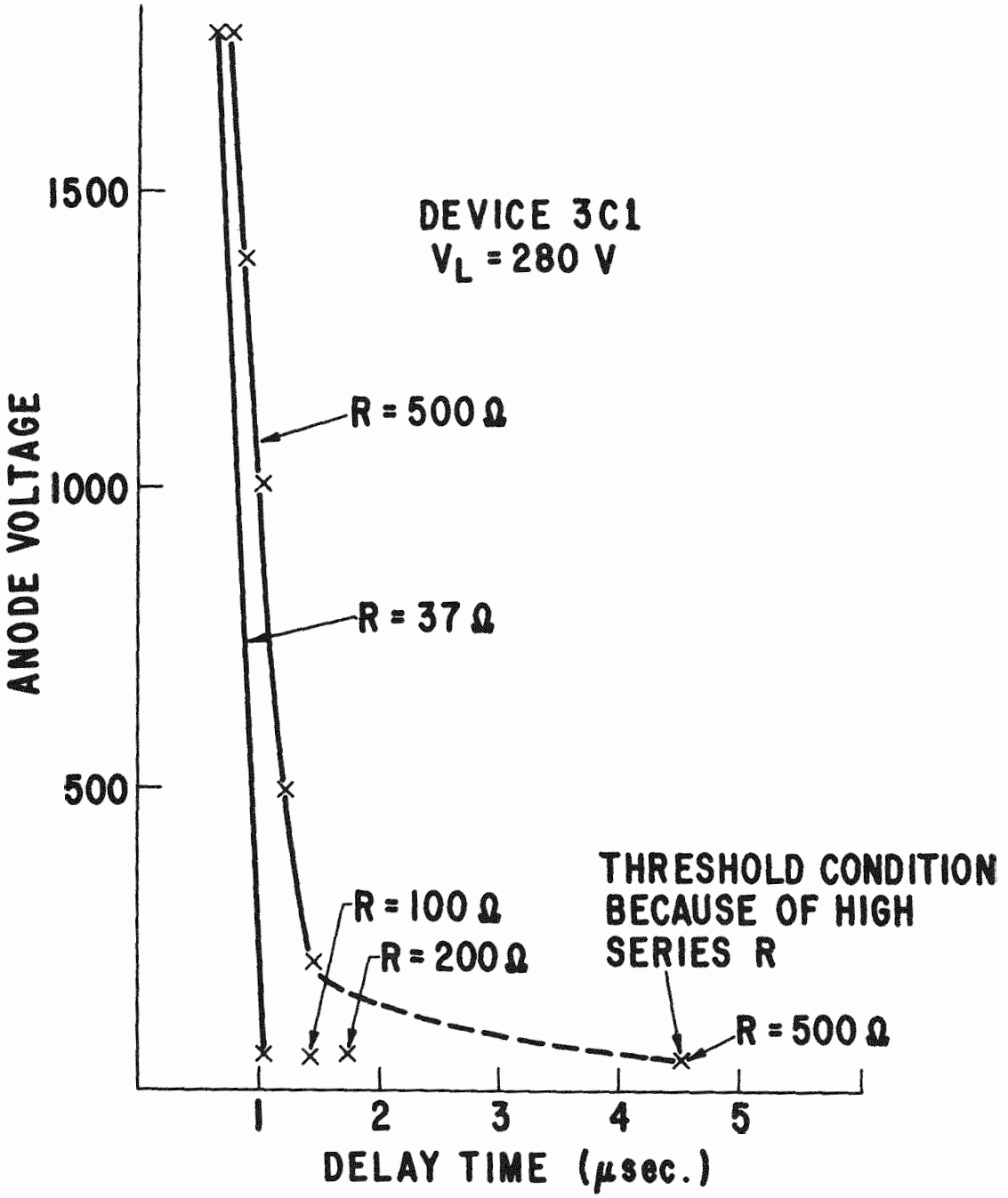


Figure 6-10: Measured turn-on delay time vs. anode voltage with device 3C1(2) as the separate gate device. R_{series} are as marked.

there is an insignificant different between the 37 Ω and 500 Ω delay times above 200 volts. There is also very little variation from 50 V to 1750 V for the 37 Ω case which indicates that for normal R_{series} values (say 10 to 100 Ω) there will be no delay time related problems. However at R_{series} = 500 Ω there is a large delay time difference in going from 50 to 200 volts, approximately 3μseconds. This is probably too large to be tolerated so that, with the gate drive condition in Figure 6-10 and with a minimum firing voltage lower than 200 volts, R_{series} = 500 Ω would not be suitable. However, $R_{series} \leq$ 200 Ω is apparently acceptable.

Summary

Separate gate di/dt tests have shown this firing method to be superior in di/dt capability to the integral gate device. It has also been shown that a wide variation in R_{series} is possible and that delay time and minimum firing voltages are well within the overall system requirements. We have also shown, in the variaiton of I_B with photo gate signal level, what is probably responsible for what we have termed the "anomalous integral" and "anomalous separate gate" turn-on.

CONCLUSION

In this section we have discussed the process changes which resulted in virtually eliminating surface arcing as a failure mode. Turn-on di/dt tests were carried out on a new run (Run 2) of devices of various types with several types giving di/dt capabilities greater than the 55A/μsecond (at 105°C) screen test for HVDC. Yields were reasonably good even at twice this di/dt considering this was the first run of devices with the modified process. It was also discovered that di/dt capability could be markedly increased in our so-called "separate gate" configuration. Whether this gate option is an economic one remains a question but its 2 to 3 times higher di/dt capability makes it too important to dismiss.

Section 7

RUN 3 (PRODUCTION RUN) DEVICE SUMMARY

INTRODUCTION

Approximately 50 devices were fabricated during the sixth quarter. Detailed testing of 10 of these devices at SPCO and CRD showed normal blocking voltage, forward drop and dv/dt capability. All ten devices passed di/dt tests at 105°C, 150A/μsecond. These results are reflected in an improvement change in forcasted di/dt failure rate. In addition tests on the remaining devices are partially completed at SPCO where 31 of 33 devices have passed 110A/μsecond di/dt tests. Even here, the two failures reported were not believed to be di/dt failures.

These 50 devices were of the EPRI-GE3 and EPRI-GE4 variety with minor mask modifications involving a slight narrowing of the n^+ alignment band to reduce channel voltage. This final run of devices has been referred to as the "production run" since most were to be eventually packaged as will be described in Section 8 of this report.

This section also describes results of a short series testing of devices to demonstrate that near simultaneous switching can be achieved. In this test the actual two level snubber used on the EPRI valve was used in conjunction with our di/dt tester to obtain the test waveforms.

Finally we describe our theoretical and experimental basis for projecting device life at normal HVDC stress levels from our 1 minute di/dt tests. This is done for the purpose of considering either HVDC systems at higher di/dt or at higher voltage per cell. Several projections are made considering 5kV per cell HVDC systems.

TEST RESULTS

di/dt Test Results

Like the Run 2 devices both separate gate and integral gate di/dt tests were made on the Run 3 devices. Not one of the seven tested devices failed the separate gate tests at our highest (425A/μsec) di/dt level when turned on from 1800 volts. In the integral gate test, where no separate series resistance is present to protect the small light sensitive gate stage, we tested to 160A/μsecond in 10 devices on di/dt test equipment at CRD, again with no failures. A further 31 of 33 devices passed di/dt tests at SPCO. Even the two failed devices, when subsequently inspected, were discovered to have been failed in a manner that could be traced to dv/dt test failure.

Since these devices were already qualified for blocking voltage, for dv/dt capability, for forward drop and for gate sensitivity, they were set aside for packaging and a series of re-tests after being packaged. The packaging activity is described in Section 8.

Results of di/dt testing on all of the EPRI-GE3 and EPRI-GE4 devices made in Runs 2 and 3 during Phase II are condensed to the di/dt yield type plot of Figure 7-1. Run 1 results, in which channel arcing failures gave low di/dt's, are not shown.

What one can conclude from such tests is, of course, that the typical device will survive turn-on from 1800 V for one minute at 105°C junction temperature (the test condition) with about a 150A/μsecond di/dt. The difficulty is to relate passing this test at 5 to 10 times the highest HVDC di/dt level to overall HVDC system reliability. This relationship is described later in this section.

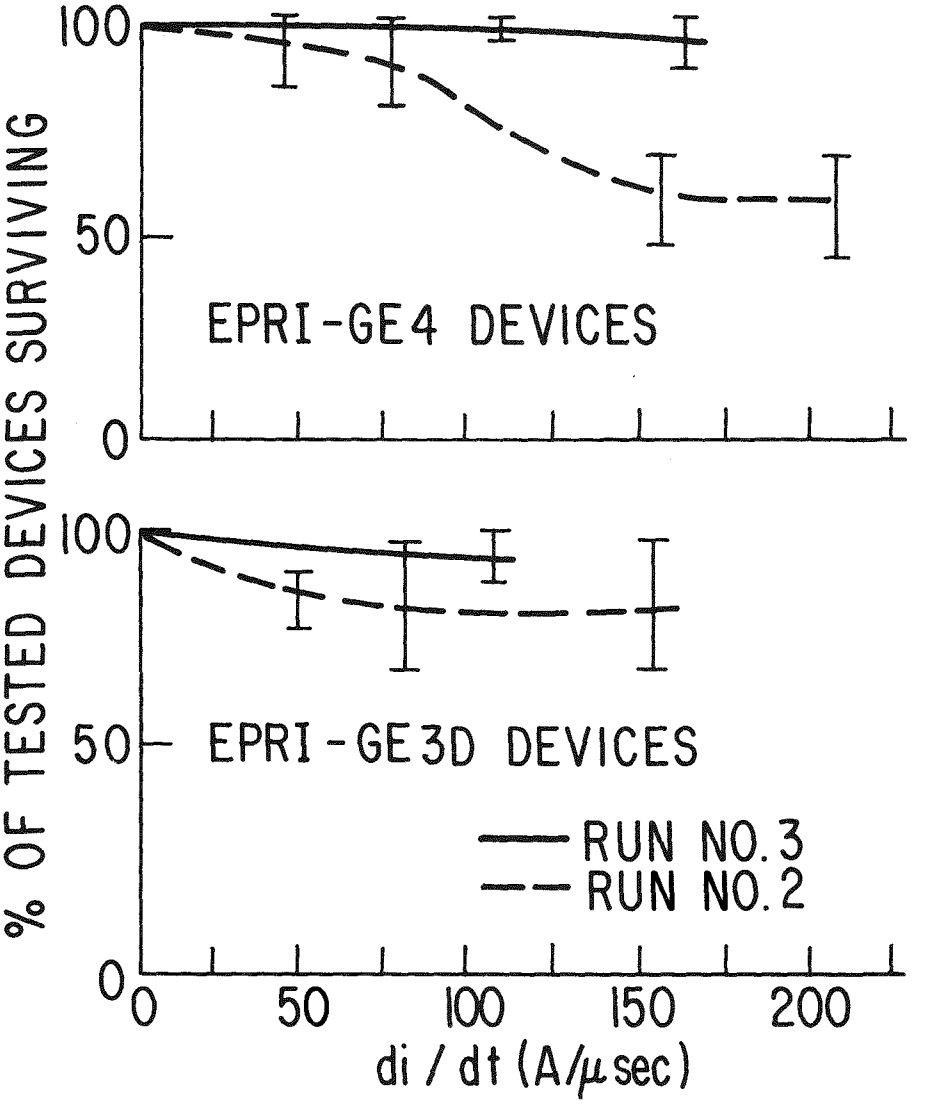


Figure 7-1: Integral gate and separate gate di/dt test summary. Results of the integral gate test are plotted vs. di/dt. Results of the separate gate tests are noted for each device type.

Series Test Results

To demonstrate the feasibility of smooth operation in HVDC valves, evidenced by uniform delay times and an absence of voltage spikes during switching, two light triggered thyristors (LTT) were operated in series. Both devices were gated from the same source, an LD166 Laser diode. Using a Velonex Model 350 High Power Pulse Generator, a 1μsecond wide, 12 ampere flat top pulse was generated at 60 Hz, to pulse the laser diode. Liquid nitrogen cooling was used to increase laser efficiency and to prolong the life of the laser. A single light pipe was connected to the output of the laser diode. This light pipe was then split into two smaller light pipes which were used for the simultaneous triggering of the series devices. The diameter of the smaller light pipes was 10 mils and, in its 63 mil diameter brass ferrule, fit snuggly into the device package.

The di/dt tester (Figure 7-2a) was used in conjunction with the EPRI snubber (Figure 7-2b) to perform the series testing. A very brief explanation of the circuit will now be given. To simplify matters, only current discharges through LTT_1 will be discussed. There is an initial current path through capacitors C_{11} and C_{21} through the R1 resistor, LTT_1 and the R2 resistor. This is followed by a current through the R3 resistor and saturable reactor L_1, through the diodes D_{11}, through C_{21}, the R1 resistor, and LTT_1 and the R2 resistor. The final path of current is from capacitor C_3 through the resistor R and then inductor L through LTT_1, L_{M} (saturable reactor) and LTT_2. The dotted lines in Figure 7-2b trace the current path throughout the EPRI snubber for LTT_1. A similar current path applies for LTT_2.

The function of the 25.9μH inductor is to limit the follow on di/dt which flows through the devices after the initial discharges from the EPRI snubber. A di/dt of 110A/μsec at 3200 volts is obtained with the present circuit.

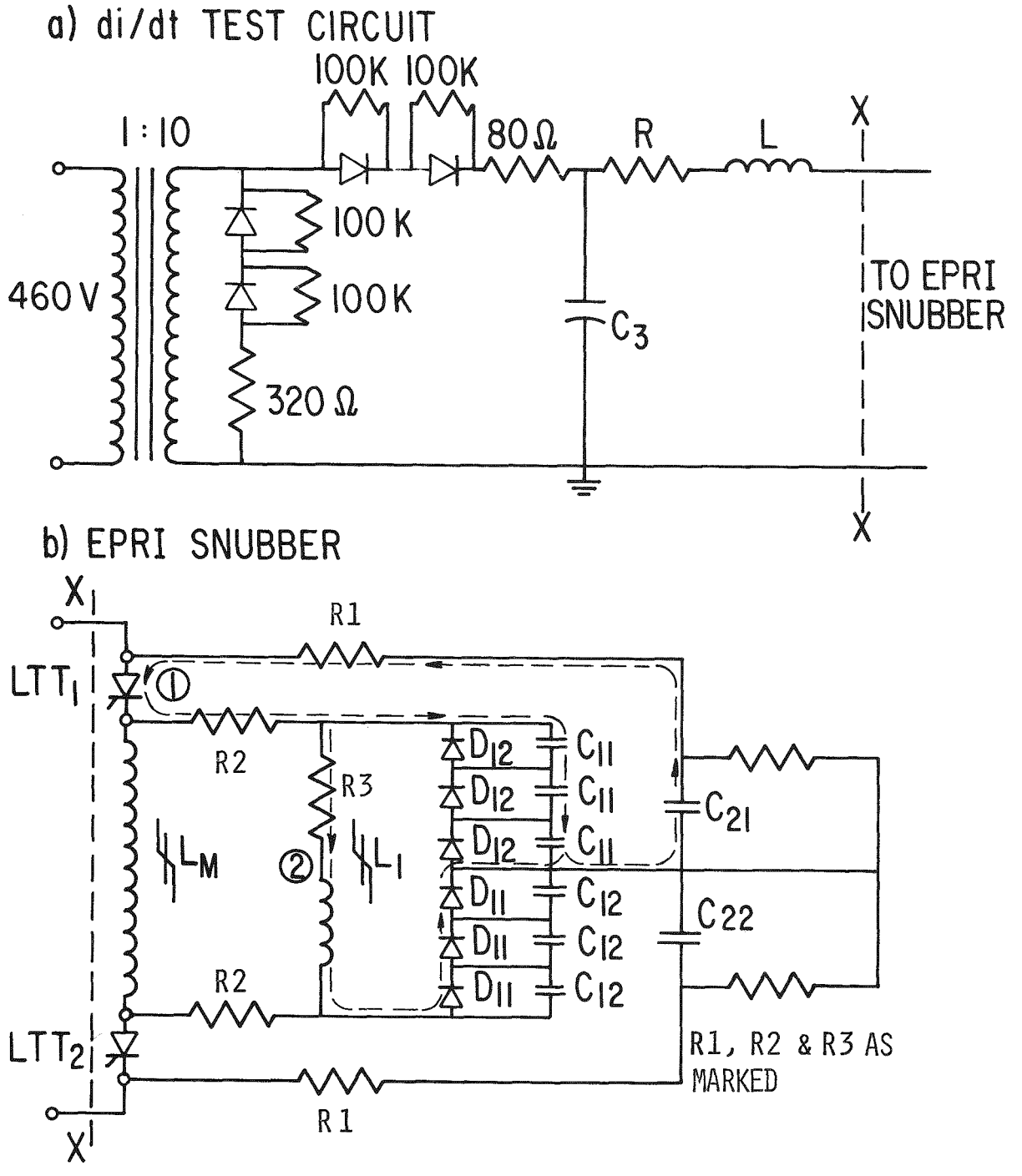


Figure 7-2: (a) External circuit for series tests. (b) EPRI snubber in which the two light triggered devices were tested.

Optimally coupling the light bundles into the device packages, results in uniform turn-on of both devices (see Figure 7-3). With 200 volts V_{AK} across each device, a very small (.4μsec) difference in delay times is observed between the two devices. Figure 7-4 shows turn-on at 1000 volts across each device. At this voltage, there is no appreciable difference in delay times. As a point of interest, the coupling of light to device #1 was misaligned somewhat to observe the effect. In addition, the large saturable reactor (L_M) was replaced by 2 henrys of inductance. As expected, device #2 turned on first, which resulted in the voltage across device #1 rising until the device was triggered into conduction (see Figure 7-5).

The light pipe coupling was then returned to normal, and both devices once again fired without any voltage spikes.

Finally, Figure (7-6) shows both devices turning on with a voltage from anode to cathode of 1600 volts. All tests were performed at 25°C.

PROJECTED RELIABILITY AT DIFFERENT STRESS LEVELS

In this section it is proposed that the results of the one minute di/dt stress test be related to system reliability, in particular, the expected number of cycles to failure. Two assumptions are generally made in this type of analysis. First the system turn-on temperature transient is related to the circuit and to the device. For example, Equation 7-1 below is an empirical one relating turn-on dissipation transient to the snubber through the first two terms and to the follow-on di/dt through the last term.

$$\Delta T \propto A\ C_S V^2 + B\ V^2/R_S + V\ di/dt \qquad (7\text{-}1)$$

Prefactors A and B (as compared to 1 for the di/dt term) are related to the relative effect of snubber energy and peak snubber current on the ΔT of a particular device. At this point the actual values of A and B are unknown beyond the fact that with C_S = .5μFd and R_S = 10 Ω , no devices failed until

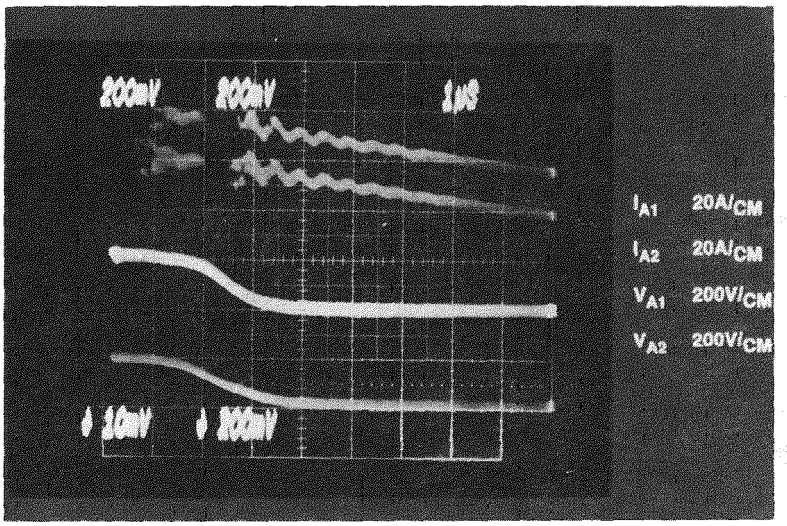


Figure 7-3: Series turn-on at 200 V across each device.

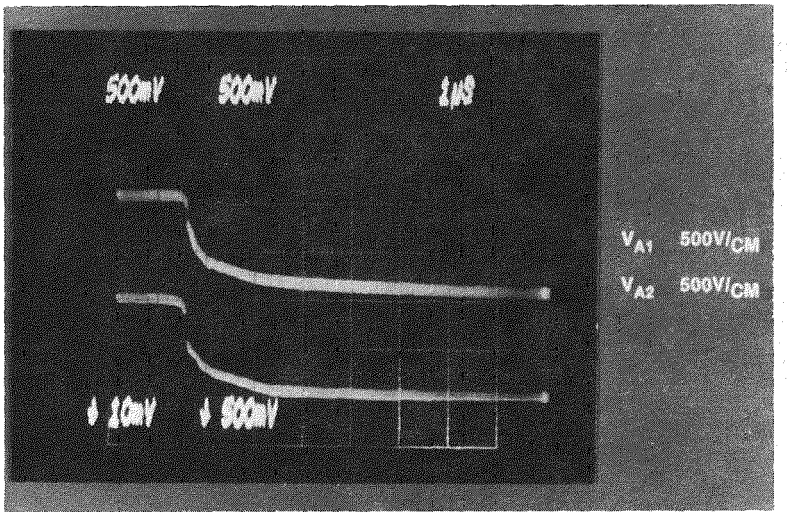


Figure 7-4: Series turn-on at 1000 volts across each device (good coupling).

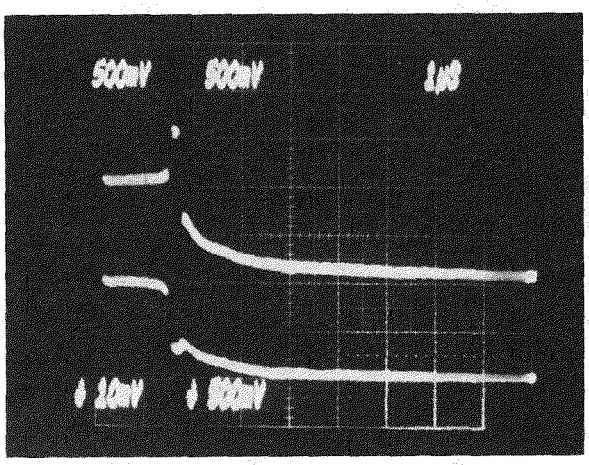


Figure 7-5: Series turn-on at 1000 volts across each device with misaligned coupling across each device and the line saturable reactor replaced by a fixed inductance of 2 microhenries.

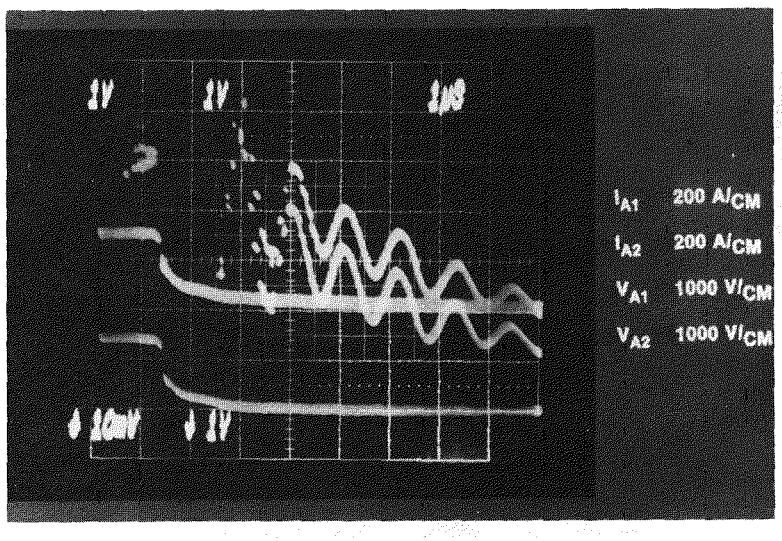


Figure 7-6: Series turn-on at 1600 volts across each device. (Good coupling and line saturable reactor restored.)

the di/dt was raised. In the integral gate tests R_S was even larger so that we can expect the results plotted in Figure 7-1 to chiefly represent the thermal stress from the V di/dt term. Since the actual di/dt value goes like V/L it is clear that the turn-on stress is proportional to V^2 if C_S, R_S and L are held fixed. It is immediately apparent that the higher voltage devices anticipated in the next generation of HVDC valves will have di/dt problems going up as V^2, unless, of course, A C_S, B/R_S and $1/L$ are scaled like $1/V^2$. Even this will result in higher turn-on stresses owing to the naturally slower and more lossy turn-off of the thicker, higher voltage cell.

The second assumption that is to be made is that the number of cycles to failure goes as shown in Equation 7-2.

$$N = \left[\frac{T^*}{\Delta T}\right]^n \qquad (7\text{-}2)$$

In thyristors manufactured with closed tube diffusion processes T* can lie anywhere between 250 and 400°C depending on the short term thermal properties of the packaged devices. Usually n is a large number which, for this report, will be taken to be 10.

Reliability of the 2600 Volt Device

In this section we compute the life at 60Hz of a device which passes a one minute stress test at a given level. The most convenient form to look at this data is in a log-log plot where number of cycles to failure is plotted against the di/dt x V product. As can be seen in Figure 7-7, each device passing a one minute stress test at a given level will result in a minimum expected cycles to failure curve. The appropriate curves for several integral light fired device types are given along with one for the electrically gated device and one for the hybrid light fired approach.

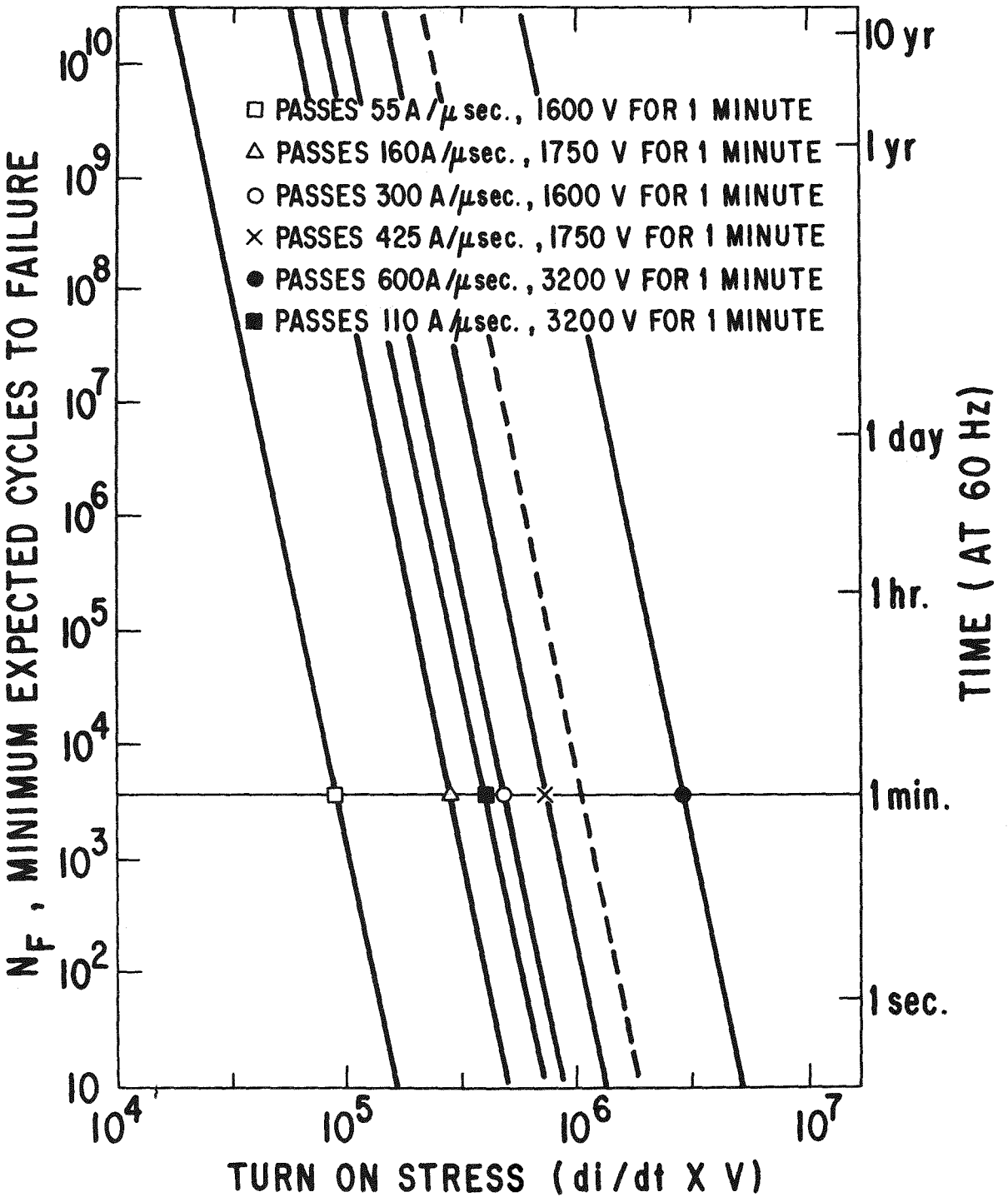


Figure 7-7: Estimated minimum cycles to failure for different light fired devices.

The lowest lying curve relates to a typical HVDC di/dt screening test. The curve marked by the solid square is one that is scaled up by V^2 for a 5200 Volt device. The approximate curve on which the typical 2600 V electrically fired device falls is the open circle while the closed circle gives the corresponding requirements for a 5200 V device with the same di/dt margin. The open triangle shows approximately where the EPRI-GE3D and GE4 type devices fall while the "X" represents the hybrid test results.

In actual device operation where one can predict the probability of switching at a certain voltage, and thus at a certain V x di/dt, it is possible to estimate device life as t_{Life} below.

$$t_{Life} = \sum_i t(V_i) \tag{7-3}$$

where $t(V_i)$ is the amount of time the system spent turning on in a small voltage range centered about V_i and $t(V_i)$ is defined below.

$$\sum_i 60 \frac{P(V_i)\ t(V_i)}{N_F\ (V_i)} = 1 \tag{7-4}$$

Here $P(V_i)$ is the probability that the device will be in the i^{th} voltage range and $60/N_F(V_i)$, the probability that it will fail in 1 second at that voltage.

Suitability of the Present Designs for 5000 V Devices

From Equations 7-1 to 7-4 and from the data plotted in Figure 7-7, it is possible to conclude that the present light fired designs in an integral gate device would not even pass the minimum screen test at 5000 volts, let alone have any margin for safety. On the other hand the same designs in a hybrid system would be limited only by the electrically fired main device which itself would be more rugged if fired by a separate gate stage.

The 2600 volt light fired device at its present typical di/dt of 160A/μsecond (1750 volts), is sufficiently reliable to serve in an HVDC valve. In fact, firing 100% of the time at 1200 volt, 12A/μsec stress, typical of gating at 90° phase angle, the 2600 V device would be projected to last more than 100 years. Note, however, that the margin of safety that the typical electrically fired device has over the typical EPRI-GE3D or GE4 is over a factor of 100 in terms of life at all stress levels. A light fired 5kV device with the same operation margin as the present light fired 2600 V device would need to lie on the dashed curve in Figure 7-7. This would need a further light fired device design breakthrough to accomplish in an integral device whereas in the hybrid device the gate stage has already proved sufficiently robust. The electrically fired main stage can be modified in a predictable fashion (i.e., longer initial turn-on line and higher gate current) for the 5kV application.

POSSIBLE FUTURE EFFORTS

The comparison of the integral and separate gate tests implies that if a proper series resistance can be built into the initial turn-on current path that the turn-on thermal transients can be controlled. This area is being pursued but, at present, results are negative. This is chiefly for two reasons. First the actual current densities which occur in the "built-in" R_{series} are anywhere from 1000 to 100,000A/cm^2. This burns up the part of the P base region allocated for the series resistance. And second, this resistance is modulated by the presence of a high density of holes and electrons so that the R_{series} resistance that we are trying to build in is going down as a function of turn-on current level. It is possible that these difficulties may be overcome. Barring that, the only alternative is that of running with a reduced system reliability combined with a lower circuit system di/dt (high L value).

In all of the above we are assuming that the integral 5kV light fired device will be able to survive the stress caused by the stray capacitance and initial snubber dump. These, too, normally increase as V^2 and, if L is increased to lower di/dt stress, may become dominant.

Actually the marked di/dt capability improvement with the separate gate stage approach points the way to what is necessary in improved amplifying gate thyristor design, and that is most clearly some degree of control of interstage current. Whether or not this conrol can be accomplished within an integral gate design (on the same wafer) will require extensive investigation and suitable innovation.

Section 8

PACKAGE DEVELOPMENT

INTRODUCTION

Concurrent with the design of the light fired thyristor we developed a package to house the device. One constraint was that the packaging be compatible with existing cell systems (stacks). Therefore it was decided to adapt production packages to the light-fired thyristor requirements. Based on this decision, there were two philosophies of introducing light to the central gate region of the cell, (1) radial entry through a port in the side wall of the lower ceramic housing, or (2) axial entry through the top of the housing. One technique of the former will be shown and two of the latter. Light pipe-heat sink design is also discussed.

RADIAL ENTRY PACKAGE

The principal benefit of this design, shown in Figure 8-1, is that series assemblies can be made, which would aid the equipment designers. The cell would have a light fiber rod inside the housing, extending from the existing gate pin position to the gate region. The light fiber would be positioned and sealed in place before the top housing is welded in place. External connections are made using a modified coaxicon type threaded connector.

A radial entry design was made and feasibility demonstrated. However, the internal fiber optic rod was fragile and it was shown that handling could be a problem. One vendor was approached to produce a fiber rod completely sheathed and hermetically sealed in metal tubing. The vendor's quote showed technical capability, but economically impractical for volume manufacturing ($\sim$\$35.00/unit).

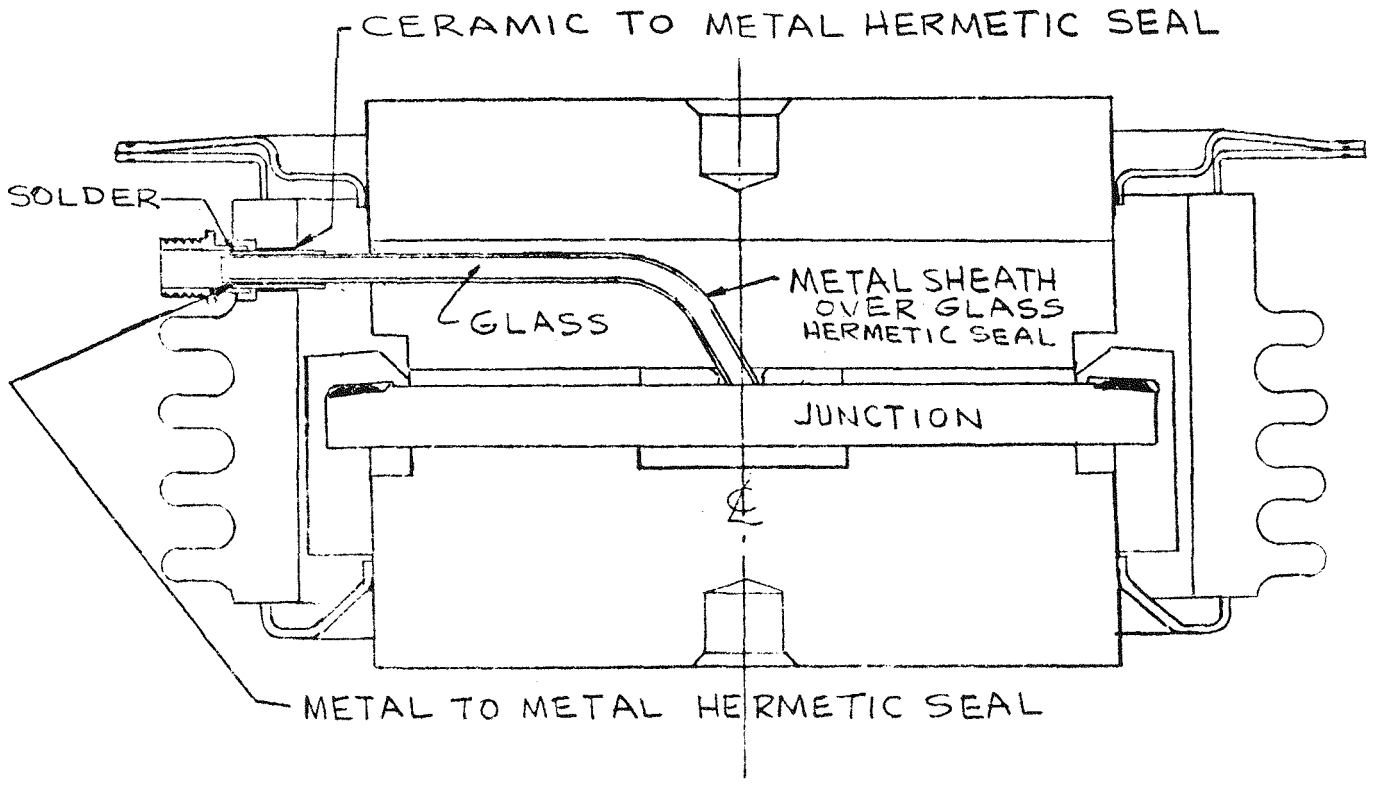


Figure 8-1: Schematic drawing of the radial entry package.

A second attempt was made to produce a similar design. Fiber rods, bent to final dimension, were coated with a layer of metal. This was to give the strength needed to protect the glass rod and achieve the same result as the fiber rod sealed in a tube. This approach was abandoned when system designers approved an axial entry system which proved simpler, less costly, and did not have the factor of two reflection and transmission losses of the light fiber rod.

FIRST AXIAL ENTRY SYSTEM

Our first axial entry system was devised to allow for a high degree of flexibility. A bellows, shown in Figure 8-2, was used to guide the light pipe termination through the cathode pole plate. One end of the bellows is covered by a 12 mil thick glass window. In the finished package one end of the bellows is soldered into the cathode pole plate while the window end is either mounted on the device or held in position by the locator fixture. Figure 8-3 shows the cathode pole plate with the bellows on the right and the thyristor with the locator fixture on the left. The packages would be assembled like the normal package for the electrically fired device.

Figure 8-4 shows the pieces required for the case where the bellows is mounted on the device. In this case the pole plate is placed in position and soldered together. Then the package is sealed in the normal manner.

Figure 8-5 shows an assembled but unwelded package of the first axial entry design along with the key parts of the modified heat sink. In the foreground is a tube press fit into a coaxial coupler drilled out to the appropriate diameter. The tube is partially sawed through .4" from the end to allow the tube to be crimped. The coaxial coupling is a standard part which would be obtained without the teflon sleeve and central conductor normally present. In the background the coax receptor is shown soldered to one of the spring clamps of the thyristor assembly. Finally, Figure 8-6 shows the pieces put together. Note that the light pipe can easily be inserted to correct depth and locked into place under compression. The shoulder of the light pipe

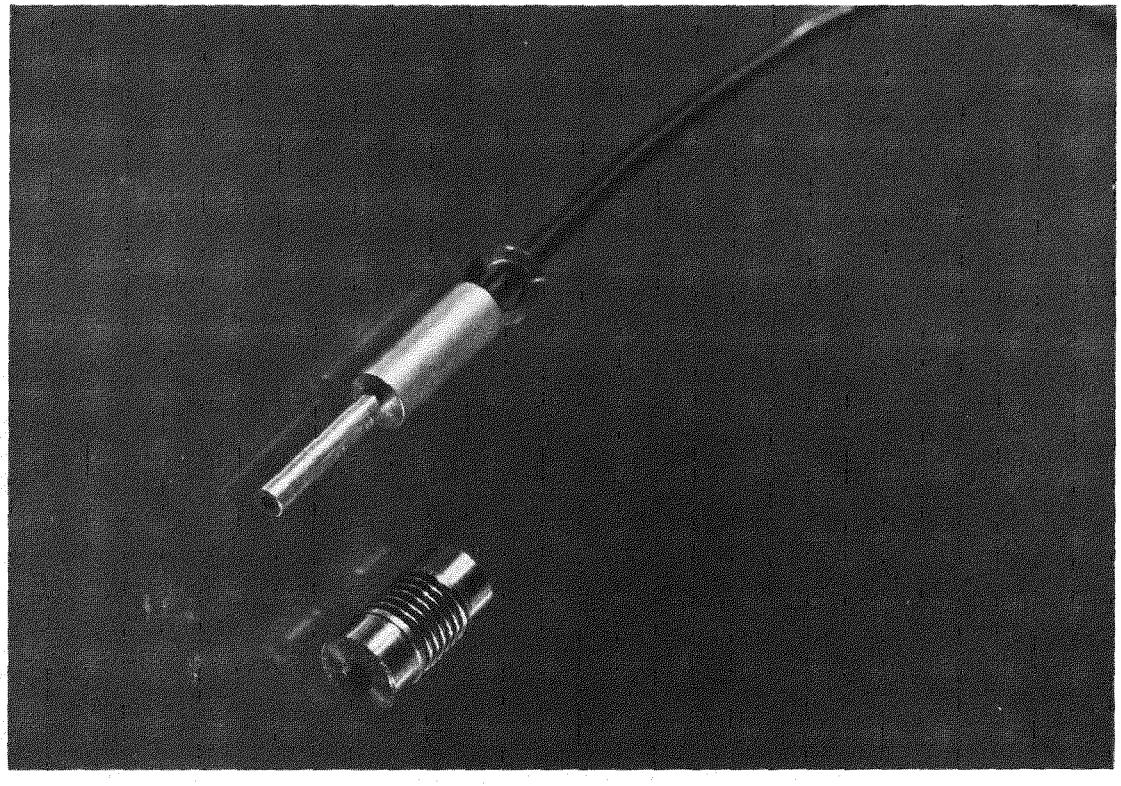


Figure 8-2: Bellows fixture for guiding light pipe termination through the cathode pole piece.

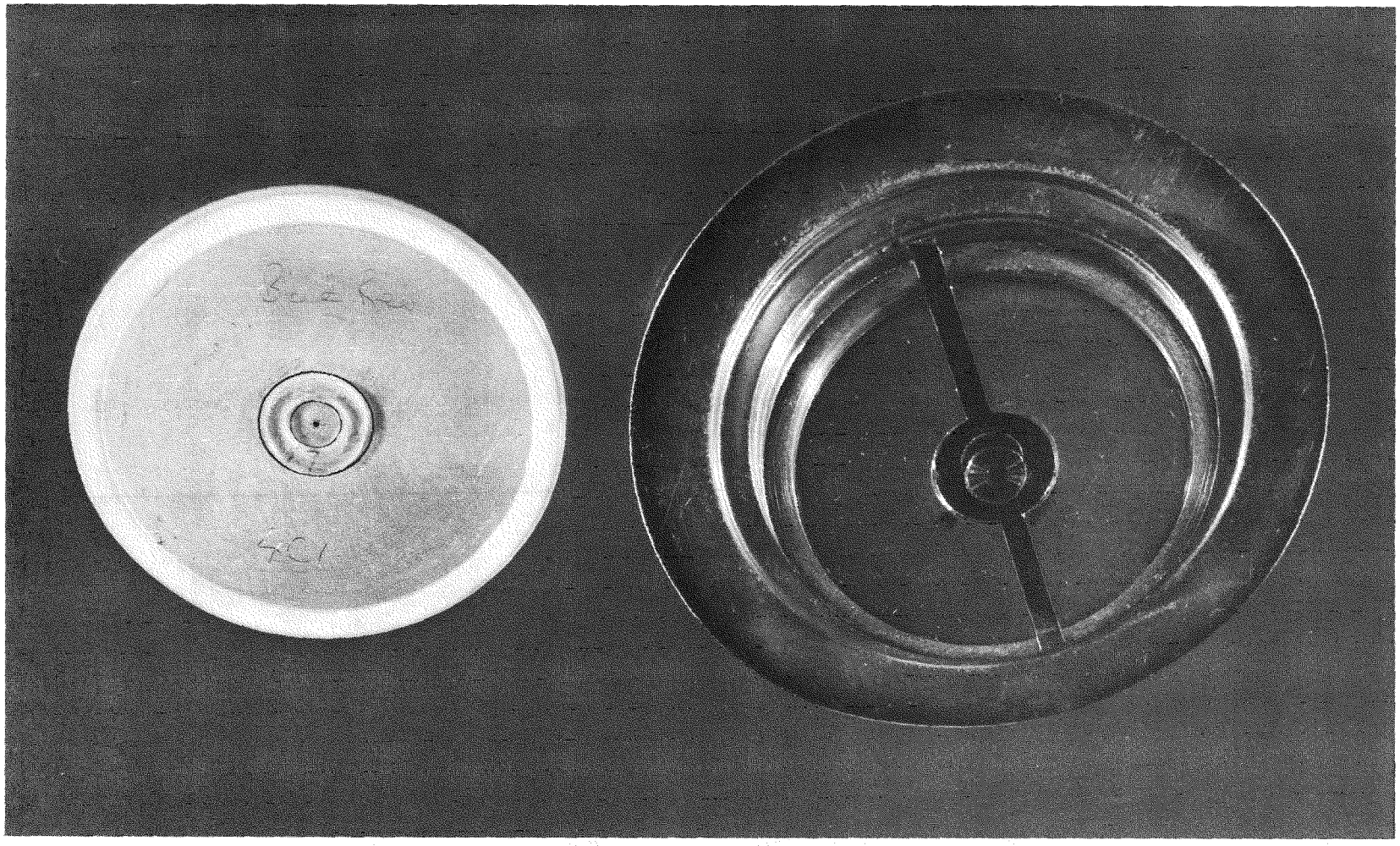


Figure 8-3: Cathode pole piece with bellows on the right and thyristor with locator fixture on the left. The bellows has a glass window and is hermetically sealed to the cathode pole piece.

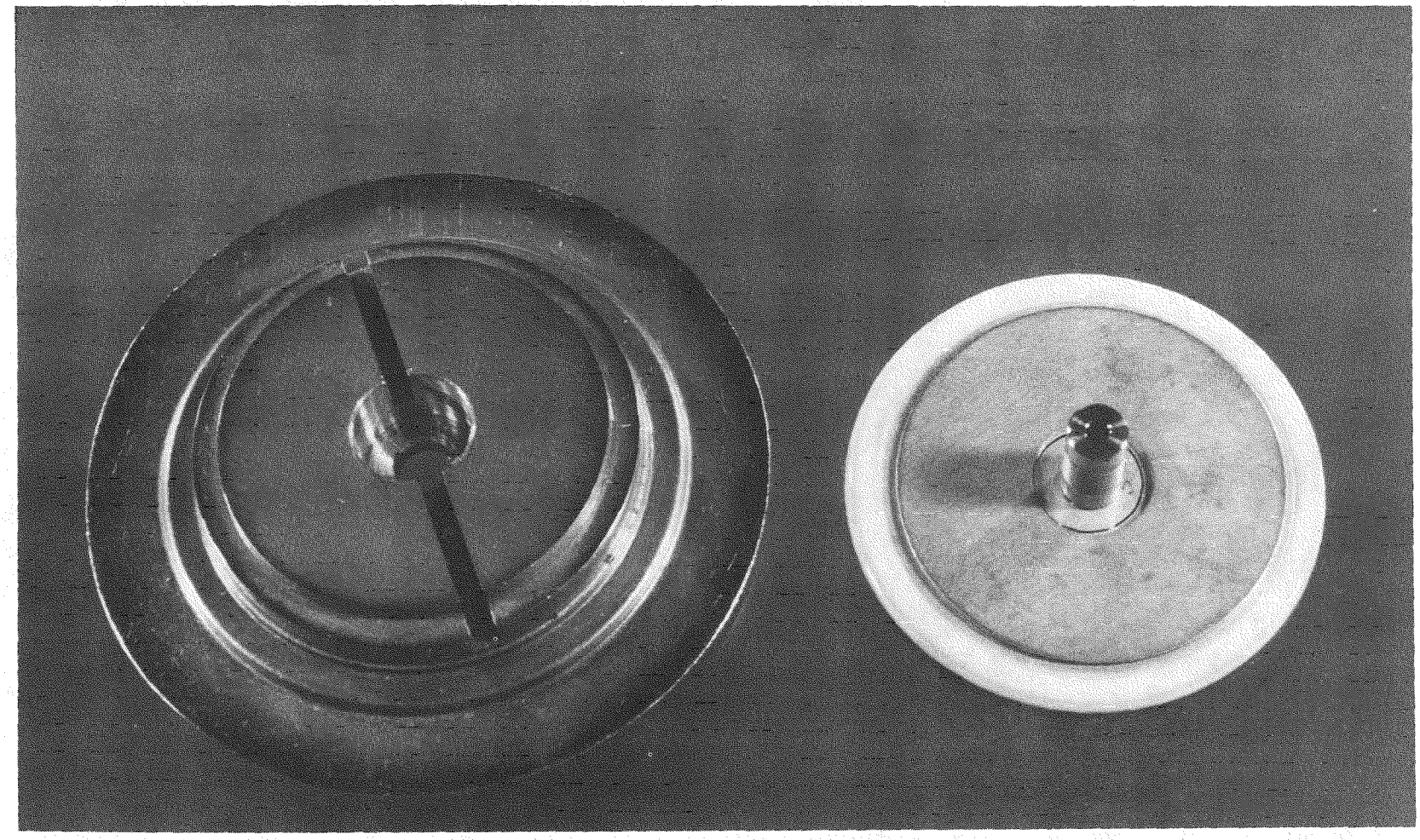


Figure 8-4: Same parts as shown in Figure 8-3 except the bellows is first fixed to the device.

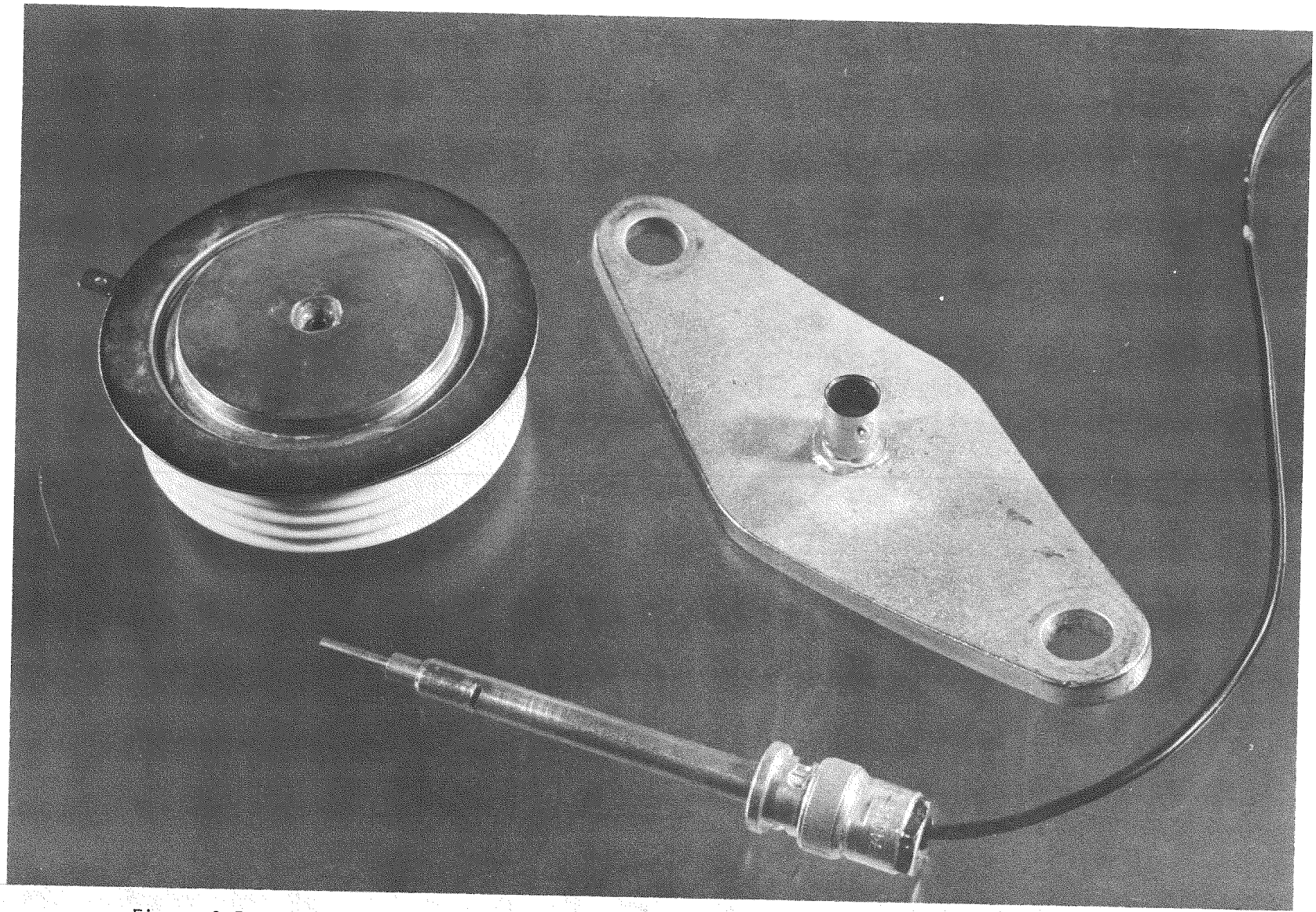


Figure 8-5: Assembled package along with a specially prepared light pipe entry fixture which locks onto the outer clamp of the heat sink assembly.

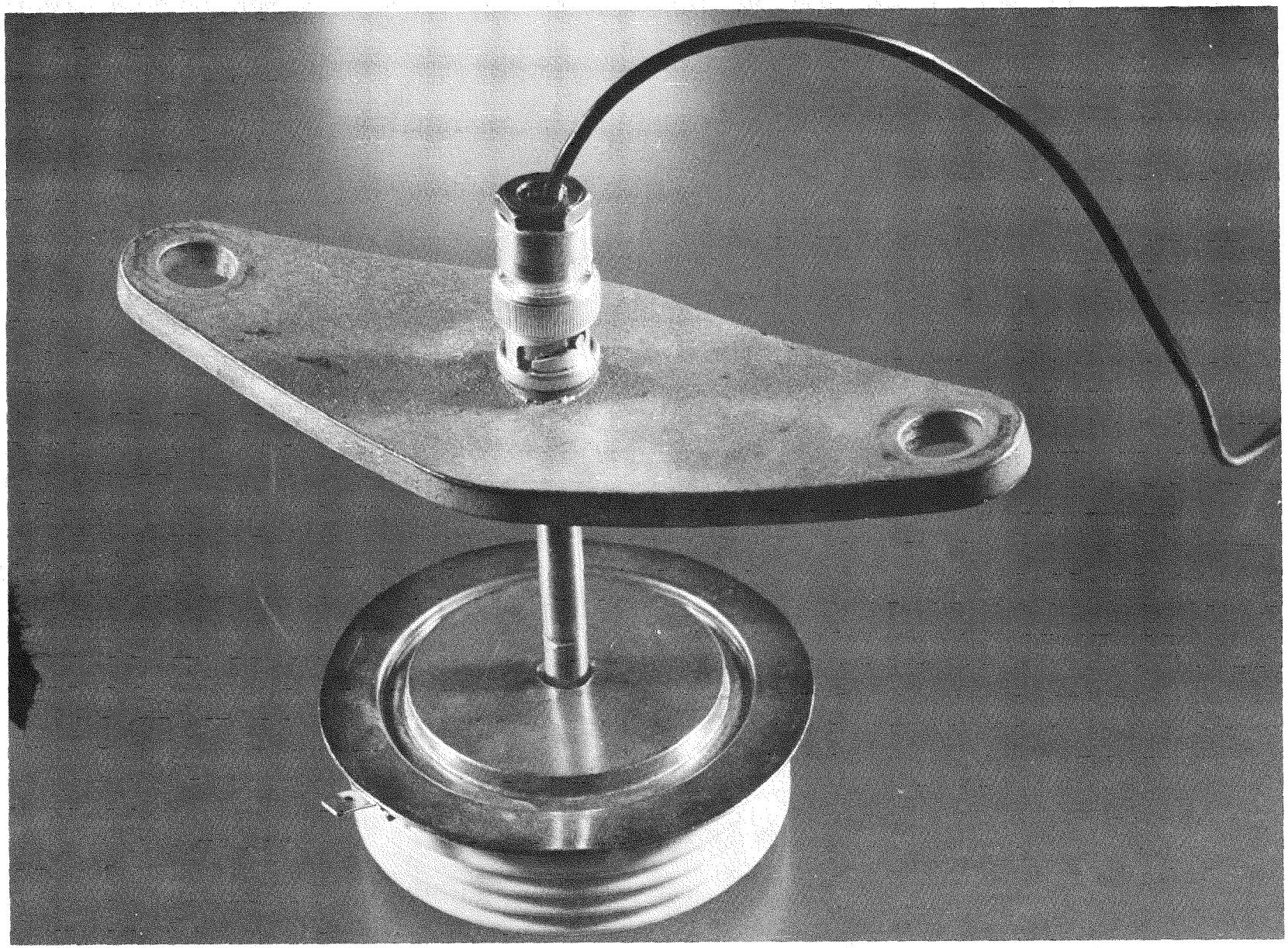


Figure 8-6: Same parts as in Figure 8-5 but assembled to illustrate how the light pipe passes through the clamped heat sink.

termination is pressed against the top end of the bellow fixture. The end of the light pipe is purposely kept to 10 mils above the glass window at the bottom end of the bellows. Again, it is believed that a little optical grease should be used to eliminate the air transmission and to keep the optical path free of foreign particles.

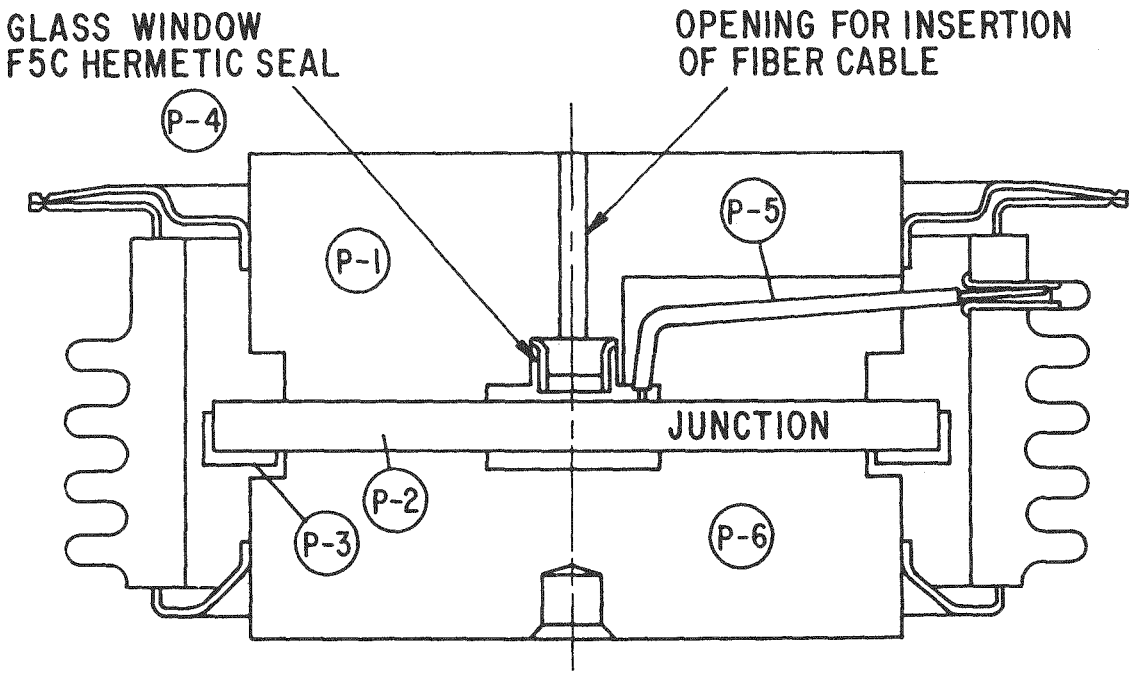
SECOND AXIAL ENTRY SYSTEM

This system allows the external light cable to be brought directly to the gate region of the cell. A hermetically sealed window is situated in the center of the top post directly over the gate of the cell, as shown in Figure 8-7. With this method, the lateral positioning of the top housing to attain maximum light transmission is critical. Similarly, the cell itself must be held securely in the lower housing to prevent any shifting once the top post is aligned.

Top posts with hermetically sealed glass windows have been made. An F5C housing having .032 inch thick glass was selected. Tests with a laser diode source showed a 2 db loss in transmission through the glass. The glass housing is sealed in the top such that is is approximately 2 to 5 mils off the gate structure. It is possible to add a small amount of optical grease betweeen the gate and the window to eliminate this small air path. The hole in the top housing is toleranced to be a slip fit with the fiber optic cable termination.

The design allows one to easily assemble the cell system, then insert the fiber optic cable through the clamping system and heat sink into the hole of the top housing. Once in place, the optic cable is to be secured in place with a clamp.

One of the problems is the possibility of a movement of the thyristor with respect to the top of the package which holds the light pipe. This problem may be alleviated by using a simple locator fixture similar to that in the



PT.NO.	DESCRIPTION	PT.NO.	DESCRIPTION
1	TOP POST ASM.	4	GLASS WINDOW
2	JUNCTION	5	V_{BO} GATE CONTACT
3	CENTERING RING	6	BOTTOM POST ASM.

Figure 8-7: Schematic drawing of light fired thyristor package identifying the six parts required.

device in Figure 8-3. A high temperature epoxy, EPOTEK H-54, was used to bond the fixture to the thyristor. The inner diameter of the locating fixture can be chosen to be a sliding fit with the external diameter of the F5C housing. The top of the package, the cathode pole plate, is machined to reflect the outer diameter of the locator fixture. If it is deemed necessary to have an electrical gate contact for the VBO protection board or other device protective circuitry, then the locating fixture would be slotted on one side. Note that the locating fixture is not part of the hermetic seal and could probably be made of a high temperature plastic.

During the last part of Phase II 24 ceramic housing assemblies were fabricated to package production run (Run 3) GE3 and GE4 junction designs. The design of the top housing included a provision for an alternative V_{BO} triggering contact. An attempt was made to use a very small window lens (.077" diameter shell, .053" diameter lens, ∿.30" focal length). However,there was sufficient difficulty in visual alignment of the top housing and the central triggering region to preclude its use at least for the present. As a result the overall package design with the F5C flat window was retained.

In an early package design, centering of the junction assembly was accomplished using a standard production silicone rubber ring. With the use of a smaller gate area, smaller fibers, and a narrower entrance opening, any accuracy in alignment of the top package housing and the enclosed cell could be lost in an unclamped condition. Therefore, a close tolerance metallic centering ring for the cell has been adopted.

The first technique to align the top housing consisted of using a microscope to visually sight the central gate through the glass window. When aligned, two small crimps are made on the outer periphery of the weld flange which hold the assembly in alignment through final assembly and welding steps. A second technique, consisting of optimizing dc photoresponse using a microscope light with the device at a moderate reverse voltage, proved considerably superior.

The light is directed vertically into the package through the cathode pole piece and when, through moving the anode section, optimum photocurrent is detected the package is welded.

Parts of the present package are shown in Figure 8-8. Figure 8-9 shows the cell assembly as it would appear in its heat sink with a light pipe inserted through the heat sink directly into the package.

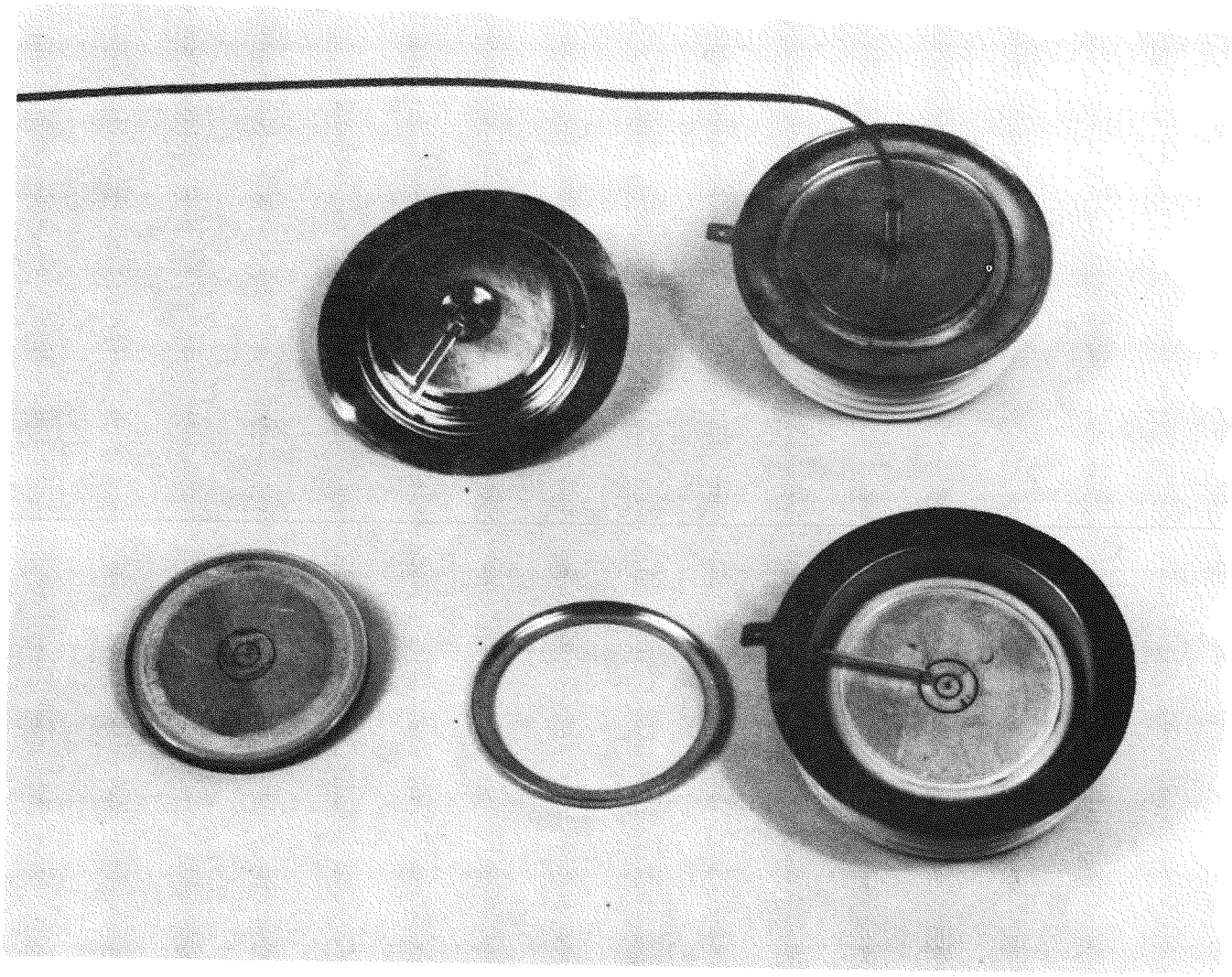


Figure 8-8: Photograph of the device package parts shown in the schematic in Figure 8-7.

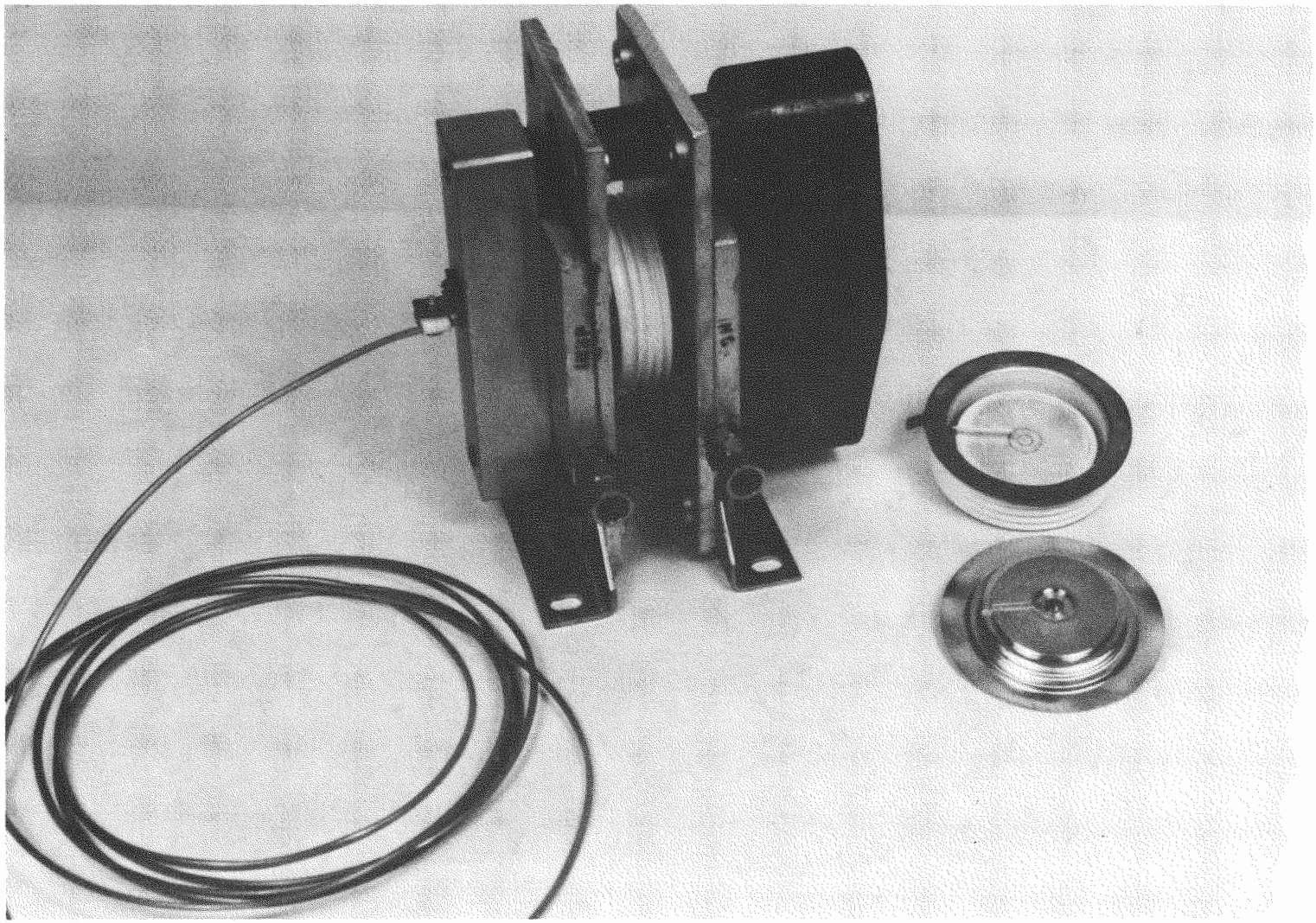


Figure 8-9: Light fired device assembled in its heat sink with a light pipe inserted and clamped into position.

Section 9

LIGHT SOURCE AND LIGHT PIPE ASSESSMENT

LIGHT SOURCES

Virtually all of the light source study undertaken as part of the light triggered thyristor program was undertaken and reported in Phase I and is, thus, available in the Phase I Final Report. What will be described here is a possible alternative to the room temperature laser which was the light source designated in Phase I. In Phase I the LED and arc flash sources were discarded principally because low pulse intensity made it impossible to design devices with high dv/dt capability. In addition, arc sources were perceived to be too short lived for HVDC station use.

During Phase I and now through Phase II, solid state GaAs lasers were often used at low temperatures. Cooled in a liquid nitrogen bath to 77°K, their characteristics are much better suited to high energy pulsed output than at room temperature. Measured input requirements are lower, 180 compared to 900 W seconds, and light output, as measured at 50 volts on a thyristor detector, is higher, 355 compared to 72 mAμseconds. Basically the laser is about 7 times more efficient at liquid nitrogen temperature and, in addition, has a 10 times longer maximum pulse length. The advantage of going to a 2μsecond, 10A pulse compared to a .2μsecond, 100A pulse pays off in other ways,notably in driver costs. Now an inexpensive transistor driver is sufficient. This can mean savings of hundreds of dollars per driver.

The information that is most needed and which we are obtaining at this time on an internal G.E. program is related to laser reliability at such temperatures. Our ongoing experiment pulses seven lasers at 1.25kHz with 4μsecond long pulses at the maximum current rating for 77°K operation. Data accumulated to date shows little problem with the laser but indicate that light

pipe coupling may be a problem. Our conclusion is that liquid nitrogen cooled lasers may be the prime source in commercial HVDC systems despite their need of liquid nitrogen.

Before leaving this topic we present Figure 9-1 showing the photo response of our light triggered thyristor as a function of light wavelength and device voltage. This figure shows that as the laser temperature is reduced the photoresponse falls about 10% for equal incident energy. The small inset table also shows that light pipe absorption losses are also somewhat greater at 8500Å - about .1 dB over 60 feet. Both of these disadvantages are relatively minor, however.

LIGHT DELIVERY SYSTEM

In Phase I the light pipe and coupling system alternatives were described in some detail. In this section we are merely going to assert that our light pipe material choice is unchanged and to comment on the impact of our choice of final package on the overall light pipe system.

The glass fiber we suggest is Gallite 3000 or its equivalent. The light pipe cross-section arriving at each device should be from 10 to 40 mils in diameter; 10 being a minimum required to safely gate the device at 3 to 5 times threshold and 40 being the useful diameter of the photo-gate stage of the thyristor. If several sources are used to gate the 10 or 12 thyristors in a panel, then a multifiber cable is desirable. In our test we have used a 400 fiber bundle separated into two 200 fiber terminations at the laser end and into 13, 31 fiber terminations at the panel. When driven by room temperature lasers, photo outputs of 30 to 50njoules per pulse were easily obtained. With the liquid nitrogen source in the same coupling apparatus, more than 10 times this pulse output was achieved.

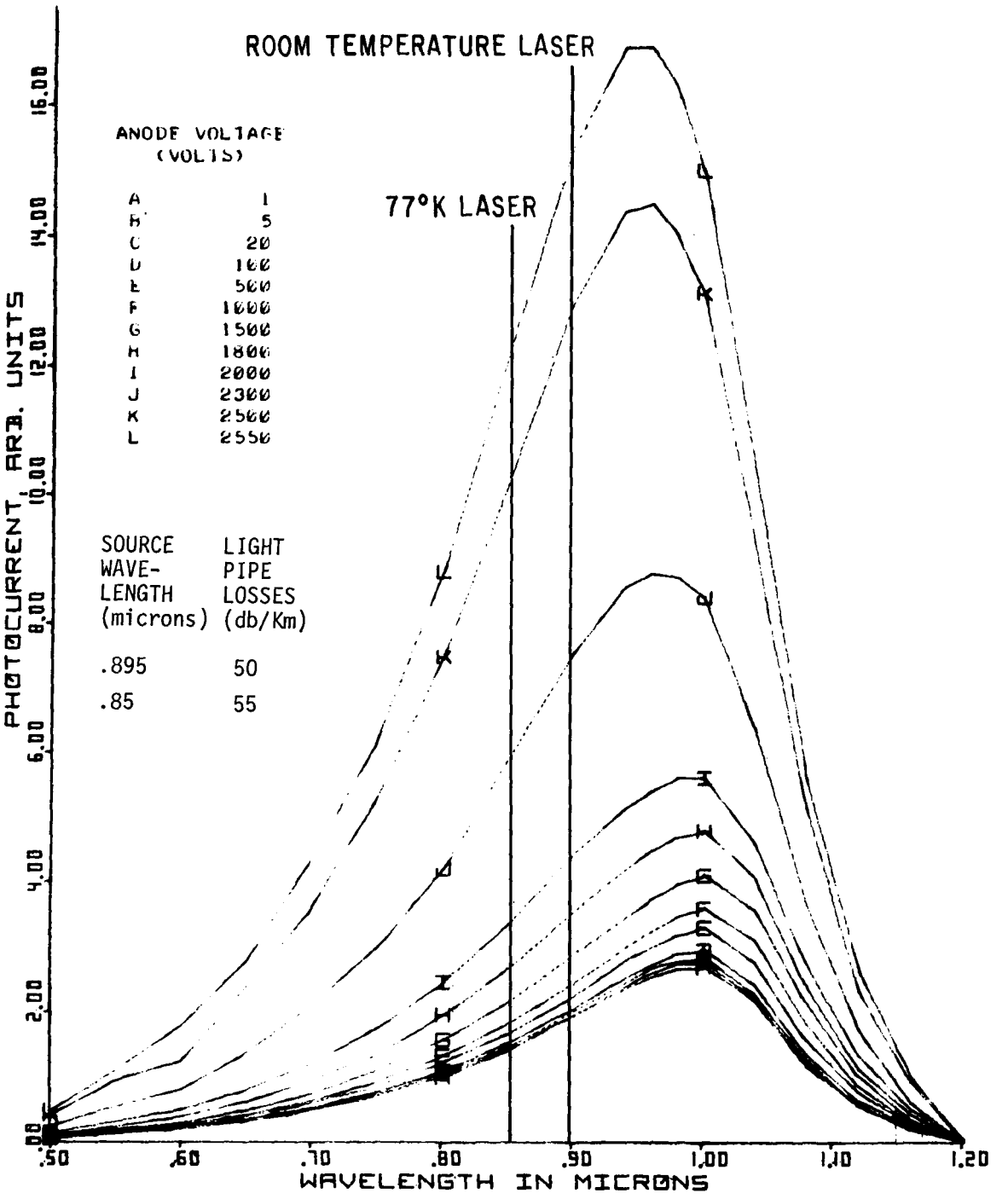


Figure 9-1: Photo-response of device 3. The photo-sensitive area was bare silicon, etched down 28 microns. (Original junction depth approximately 75 microns). The vertical lines mark the RT laser and 77°K laser wavelengths. Note that the light pipe losses are about 5 db/km larger at 77°K for Gallite 3000 light pipes.

With the present axial entry package there are no lossy couplings except for the FC-5 window in the package with its net 2 dB loss so that, with the typical 20njoule thyristor sensitivity at low voltage (sensitivty is better at high voltage), either of the two liquid nitrogen cooled laser sources could effectively have fired the entire panel with nanojoules to spare. After examining the available data,quotes on the 2 to 13 branched fiber optic cables were obtained.

Section 10

CONCLUSION

This report marks a milestone in the development of light triggered thyristors suitable for HVDC applications. Both the EPRI-GE3D and GE4 device types have a di/dt capability suitable for "reliable" operation in an HVDC valve using 2600 volt devices. To build up a sufficient supply of devices for possible applications, a run of GE3D and GE4 type devices was fabricated and is presently being packaged. This run incorporated two minor mask changes that moderately improved resistance to local channel (surface) type device degradation. These devices also proved the usefulness of the n^+ alignment band, a feature designed to ensure even turn-on, and the interrupted n^+ metal contact, a further feature improved to enhance spreading of the on area away from the initial turn-on line.

Important device characteristics other than a typical 160A/μsec or better di/dt at 105°C and 1800 volts include the following: (1) typical forward breakdown voltage of 2900 volts; (2) typical reverse breakdown voltage of 3100 volts; (3) dv/dt capability of 2000V/μsecond to 2200 volts; (4) forward drop at 105°C, 1000 amperes of 1.3 volts and, finally, (5) a typical photo threshold of 10 to 20 nanojoules of incident photo energy. Surge capability and other device ratings are similar to the original electrically fired device.

It is also significant that both the fabrication and packaging of these devices took place in a production facility and that the light triggered thyristor could be fabricated with the same process, apart from the extra sensitivity etch, as the regular electrically triggered device. Further, the package is a relatively simple one which requires only a few cents worth of extra parts.

Having an identical final stage, the surge, forward drop, etc., characteristics of the light fired device were guaranteed. This certainly simplified device testing.

Future device development is indicated for upgrading to higher light triggered device voltage chiefly because of much higher (better than V^2) di/dt stresses. Future work should also consider the possibility of building in more protective features, such as overvoltage turn-on protection (VBO protection) into the device itself as an important cost savings. In Phase II we have laid the ground for both these endeavors.

Section 11

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APPENDIX A

Figure A-1 is a repeat of Figure 3-6 from Section 3. The 13 tables given following the figure show some of the data required for the 13 cases described in Section 3 and summarized in Table 3-5.

FIGURE A-1: APPROXIMATE TURN-ON MODEL

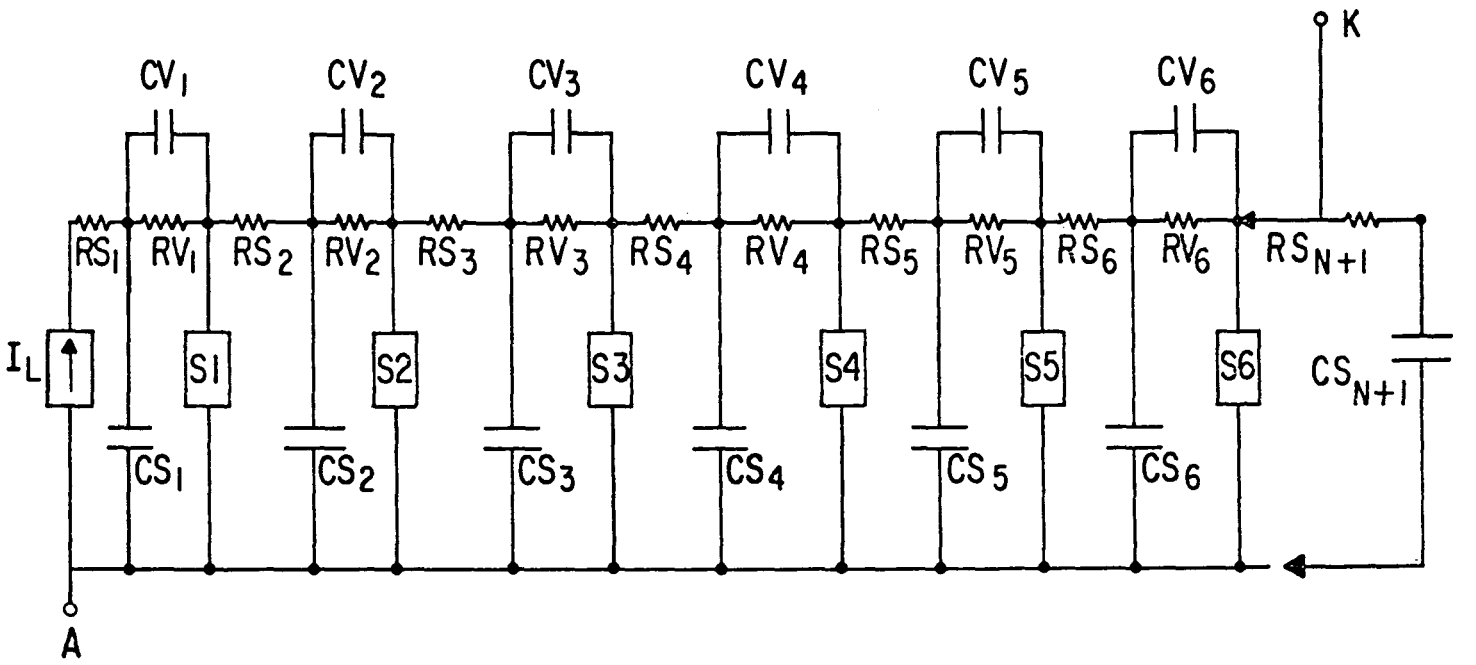

TABLE A-1: DATA FOR CASE 1 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=6)	RV (Ω)	236	68	49	30	17	6.5	
	CV (μF)	.0286	.0743	.1057	.1371	.1914	.4257	
	RS (Ω)	10	70	37	28	24	22	10
	CS (μF)	1.6PF	1.8PF	.3PF(?)	5.3PF	44PF	929PF	
	SI (μH)	20	7.69	5.41	4.17	2.98	1.34	

TABLE A-2: DATA FOR CASE 2 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=6)	RV (Ω)	236	68	49	30	17	6.5	
	CV (μF)	.0286	.0743	.1057	.1371	.1914	.4257	
	RS (Ω)	10	70	37	28	24	11	10
	CS (μF)	1.6PF	1.8PF	.3PF(?)	5.3PF	44PF	929PF	.5
	SI (μH)	20	7.69	5.41	4.17	2.98	1.34	

TABLE A-3: DATA FOR CASE 3 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=6)	RV (Ω)	236	68	49	30	17	6.5	
	CV (μF)	.0286	.0743	.106	.137	.191	.426	
	RS (Ω)	10	70	37	28	24	11	10
	CS (μF)	1.6PF	1.8PF	.3PF(?)	5.3PF	44PF	929PF	.5
	SI (μH)	20	7.69	5.41	4.17	2.98	1.34	

TABLE A-4: DATA FOR CASE 4 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=5)	RV (Ω)	218	80	30	17	6.5		
	CV (μF)	.0400	.0914	.1371	.1914	.4257		
	RS (Ω)	10	53	31	24	11	10	
	CS (μF)	2.1PF	0(?)	5.3PF	44PF	929PF	.5	
	SI (μH)	15	7.5	4.17	2.98	1.34		

TABLE A-5: DATA FOR CASE 5 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=3)	RV (Ω)	300	17	6.5				
	CV (μF)	.0357	.1914	.4257				
	RS (Ω)	10	12	11	10			
	CS (μF)	15PF	0(?)	929PF	.5			
	SI (μH)	16	2.98	1.34				

TABLE A-6: DATA FOR CASE 6 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=3)	RV (Ω)	300	17	6.5				
	CV (μF)	.0357	.1914	.4257				
	RS (Ω)	10	34	11	10			
	CS (μF)	15PF	0(?)	929PF	.5			
	SI (μH)	16	2.98	1.34				

TABLE A-7: DATA FOR CASE 7 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=3)	RV (Ω)	236	30	3.25				
	CV (μF)	.0286	.137	.851				
	RS (Ω)	10	28	11	10			
	CS (μF)	12PF	0(?)	929PF	.5			
	SI (μH)	20	4.17	.67				

TABLE A-8: DATA FOR CASE 8 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=1)	RV (Ω)	236						
	CV (μF)	.0286						
	RS (Ω)	10	10					
	CS (μF)	980PF	.5μF					
	SI (μH)	20						

TABLE A-9: DATA FOR CASE 9 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=1)	RV (Ω)	236						
	CV (μF)	.0286						
	RS (Ω)	10	10					
	CS (μF)	980PF	.5μF					
	SI (μH)	20						

TABLE A-10: DATA FOR CASE 10 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=2)	RV (Ω)	17	6.5					
	CV (μF)	.191	.426					
	RS (Ω)	24	11	10				
	CS (μF)	44PF	929PF	.5				
	SI (μH)	2.98	1.34					

TABLE A-11: DATA FOR CASE 11 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=2)	RV (Ω)	17	6.5					
	CV (μF)	.1914	.4257					
	RS (Ω)	24	11	10				
	CS (μF)	44PF	929PF	.5				
	SI (μH)	2.98	1.34					

TABLE A-12: DATA FOR CASE 12 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=2)	RV (Ω)	236	6.5					
	CV (μF)	.0286	.426					
	RS (Ω)	10	11	10				
	CS (μF)	40PF	9(?)	.5μF				
	SI (μH)	20	1.34					

TABLE A-13: DATA FOR CASE 13 OF SECTION 3

		1	2	3	4	5	6	7
DATA TABLE (N=3)	RV (Ω)	236	30	6.5				
	CV (μF)	.0286	.1371	.4257				
	RS (Ω)	10	28	11	10			
	CS (μF)	12PF	0(?)	929PF	.5			
	SI (μH)	20	4.17	1.34				