

# MASTER

## NSLS DIPOLE POWER SOURCE\*

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### ABSTRACT

An SCR DC to DC converter is described which will operate at an output of 275 kW and will supply current to electron storage ring magnets requiring 5 hr. stability of 50 ppm. The operation of this modified chopper is described and design equations are presented, along with the system control loop description.

### INTRODUCTION

The National Synchrotron Light Source (NSLS) under construction at Brookhaven Laboratory will be a uniquely copious source of x-ray and ultraviolet photons with a wide spectrum. Selected frequencies of this radiation with wavelengths of the order of atomic and molecular dimensions will be an important tool in the study of matter. Some of the potential uses of this light include studies of absorption spectra, photo emission of electrons, x-ray scattering, biochemical studies and other areas of basic research. It can also be used for micro-lithography of integrated circuits for ultra-dense semiconductor devices.

This light is generated by electrons which are made to follow a closed orbit in an electron storage ring at nearly the speed of light in vacuum thus undergoing centripetal acceleration due to the magnetic guide field. This acceleration causes the electron beam to radiate energy with a wide spectrum with a peak dependent on the electron energy and the radius of curvature. The NSLS will include two electron storage rings; one operating at an energy of 0.7 GeV with a peak or characteristic wavelength in the vacuum ultraviolet (VUV) region, the other at 2.5 GeV with a characteristic wavelength in the soft x-ray region. The beam storage duration is dependent on the mutual repulsion of the electronic charges, collisions with the residual gas in the vacuum and the stability of the magnetic field of the storage ring dipoles, among other things<sup>1,2</sup>.

### DESIGN REQUIREMENTS

The power source required for the storage ring dipoles of the National Synchrotron Light

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Source must meet a number of stringent requirements. It must generate a nominal 1500A at 65Vdc for the VUV ring (or 185Vdc for the x-ray ring) with a relatively slow rise and decay and with a short term (5 hr.) current stability of  $\pm 50$  ppm, max in order to maintain the beam orbit within desired limits. The required long term stability is  $\pm 100$  ppm, max, over one month. The peak to peak magnetic field ripple must be less than 50 ppm. Thus the power source must be virtually independent of the 480V, 30, 60 Hz line voltage variations, phase imbalances and transformer/rectifier tolerances. Also a  $\pm 10^\circ$  temperature variation at the power supply must be anticipated.

#### Design Alternates

Phase controlled SCR approaches with various correction circuits to minimize the effects of line voltage perturbations and line frequency variations as well as the transistor bank regulator approach were considered. The problem of sensing the line voltage zero crossing of the SCR phase controlled regulator in the presence of frequency variations can be solved with a phase locked loop but line voltage perturbations can only be corrected by shifting of the subsequent SCR trigger. The resulting wobble in the regulator output is attenuated but not eliminated by the filtering of the inductive magnet load.

The transistor bank regulator can produce relatively fast responses to disturbances. The inefficiency of the transistor bank regulator can be minimized by different preregulator approaches which add to its complexity and cost. It is an expensive approach but it is capable of wideband, effective control.

A cheaper, more energy efficient alternate is an SCR switching regulator or chopper. When used in a type 1, 100 Hz bandwidth loop with feedforward control to correct for input voltage variations, the chopper loop has adequate control agility for the storage ring application while eliminating virtually all the variations and imperfections of the input a.c. power source. The chopper approach which was chosen is based on a voltage commutated chopper described by Dewan and Jackson because it permits more rapid turnoff of the series switch at the instant required by the loop control. It results in a straight forward single input-single output control system which meets the design goals

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without significant complications or cost.

#### Chopper Operation (See Figure 1)

Basically the chopper operates as follows:

The load switch turn-on occurs as a direct result of the clock pulse, connecting the input voltage source to the output filter and load. Turn-off occurs as a result of the comparison of the integral of the load switch output  $v_s$ , and the amplified error voltage. The OFF switch (Q2) is then triggered connecting the load switch anode (Q1) to the negatively charged commutating capacitor, C, forcing the load switch off. This is followed by a flyback and recovery sequence which ends with the C again charged negatively to ground.

After the contactor closes, the sequence must begin with the inhibit of triggers by the triggering logic until the input filter capacitor, C1, is charged. A series of OFF triggers is then generated each of which starts a flyback and recovery sequence which proceeds as follows:

Q2 is triggered causing C to charge to 2v thru L1. The gate of Q3 is held off by the current in the diode, D2, although Q3 is forward biased. After that first 1/2 sine of current thru Q2 and D2 ceases, Q3 conducts, resulting in a second 1/2 sine of current thru C and L4 and a reversal of the voltage on C.

Assuming no losses and  $L1 = L2$ , on subsequent triggers, C, initially charged to -2v, will tend to charge to + 4v. However, D1 begins conducting when the voltage induced in L2, which is tightly coupled to L1, equals +v, thus tending to clamp the voltage on C to + 2v. The current in Q2 then decreases to zero, disconnecting C and L1. The current thru D1 then decreases to zero, while returning energy to C1 and discharging the L1/L2 transformer while the C voltage again returns to - 2v as a result of recovery current thru Q3 and L4.

The triggering logic then permits the load switch, Q1, to be triggered by the ON pulse, charging L1. The loop generated trigger pulse to Q2 later turns off Q1 by forcing the anode of Q1 negative long enough to allow charge recombination in Q1 so that Q1 will remain off (up to 25 sec for the presently used units). During the OFF period, load current continues to flow thru D3. The flyback proceeds as before except that the initial current in L1 adds to the initial energy in L1 and results in the minimum time for Q1 charge recombination.

The output filter with a resonant frequency of 400 Hz attenuates the high frequency components of the resulting square at the junction of Q1 and D3. The VUV dipole load magnet, with a time constant of 2.07 sec (x-ray, 2.6 sec), further reduces the ripple component of the current to acceptable levels.

#### CIRCUIT EQUATIONS SUMMARY

As the equivalent circuit and waveforms of figure 2 indicate, the steady state current thru L5

changes linearly in the two regions,  $\tau_1$  and  $\tau_2$ . The change in current in L5 is given by

$$I_2 - I_1 = \frac{v - v_o}{L_1 + L_5} \tau_1 \text{ and } I_2 - I_1 = \frac{v_o}{L_5} \tau_2$$

The average output current,  $I_o$ , is then

$$I_o = \frac{I_1 + I_2}{2}$$

With  $\tau_1 + \tau_2 = T$ , it follows that the peak current in Q2,  $I_2$ , is

$$I_2 = I_o + \frac{T/2}{\frac{L_1 + L_5}{v - v_o} + \frac{L_5}{v_o}} \quad (1)$$

At  $t_2$  the OFF SCR is triggered with a rapid turnoff of Q1. Then the current thru L1, i, is found from

$$v = L_1 \frac{di}{dt} + \frac{1}{C} \int i \, dt : i(0) = I_2, v_c(0) = v_{co}, t = 0 \text{ at } t_2$$

or

$$\frac{v}{s} = L_1 \left( sI(s) - I_2 \right) + \frac{1}{C} \left( \frac{I(s)}{s} + \frac{Cv_{co}}{s} \right). \text{ Then}$$

$$I(s) = \frac{(v - v_{co})/L_1 + sI_2}{s^2 + \frac{1}{L_1 C}},$$

or

$$i(t) = I_2 \cos \omega_o t + (v - v_{co}) \sqrt{\frac{C}{L_1}} \sin \omega_o t$$

$$\text{where } \omega_o = 1/\sqrt{L_1 C}. \quad (2)$$

Now

$$v_c(t) = v - L_1 \frac{di}{dt} = v + \sqrt{\frac{L_1}{C}} I_2 \sin \omega_o t - (v - v_{co}) \cos \omega_o t \quad (3)$$

Q1 is reverse biased for the period,  $t_q$ , which is found when  $v_c(t_q) = 0$ .

Then

$$t_q = \frac{1}{\omega_o} \left[ \cos^{-1} \left( \frac{v}{\sqrt{\frac{L_1}{C}} I_2 + (v - v_{co})} \right)^{\frac{1}{2}} \right. \\ \left. - \tan^{-1} \left( \frac{I_2 \sqrt{\frac{L_1}{C}}}{v - v_{co}} \right) \right].$$

Given  $I_2$  and  $v$ ,  $L_1$  and  $C$  are chosen such that  $t_q$  is always greater than the turn off time of Q1. See Dewan<sup>3</sup>.

$I_3$ , the peak value of  $i$ , occurs at  $t_3$  when  $v_c(t_3 - t_2) = v$ . From (3)

$$t_3 - t_2 = \frac{1}{\omega_0} \tan^{-1} \left( \frac{v - v_{co}}{\frac{v}{L_2} - \frac{L_1}{C}} \right),$$

and from (2)

$$I_3 = \left[ \frac{v^2}{L_2} + \frac{C}{L_1} (v - v_{co})^2 \right]^{\frac{1}{2}}.$$

The increasing voltage of  $v_A$  ( $= v_c$ ) induces a decreasing voltage across  $D1$  via  $M$  until  $D1$  is forward biased. That point is reached when  $v = -M \frac{di}{dt}$  or  $\frac{di}{dt} = -\frac{v}{M}$ . Then from (3)

$$v_c(t_4 - t_2) = v - L_1 \frac{di}{dt} = v \left( 1 + \frac{L_1}{M} \right)$$

or

$$v \left( 1 + \frac{L_1}{M} \right) = v + I_2 \sqrt{\frac{L_1}{C}} \sin \omega_0 (t_4 - t_2) - (v - v_{co}) \cos \omega_0 (t_4 - t_2).$$

Thus

$$t_4 - t_2 = \frac{1}{\omega_0} \left[ \cos^{-1} \left( \frac{-\frac{L_1}{M} v}{\left[ \frac{L_1}{C} I_2^2 + (v - v_{co})^2 \right]^{\frac{1}{2}}} \right) \right. \\ \left. - \tan^{-1} \left( \frac{I_2 \sqrt{\frac{L_1}{C}}}{v - v_{co}} \right) \right]$$

and

$$I_4 = i(t_4 - t_2) = I_2 \cos \omega_0 (t_4 - t_2) \\ - (v - v_{co}) \sqrt{\frac{C}{L_1}} \sin \omega_0 (t_4 - t_2).$$

When  $D1$  conducts, returning energy to  $V$ , the following equations apply where  $i_1$  is the current thru  $L_1$  and  $C$ ,  $i_2$  is the forward current in  $D1$  and  $L_2$ . The lead inductance,  $l$ , must also be included:

$$v = l \frac{di}{dt} (i_1 - i_2) + L_1 \frac{di_1}{dt} + \frac{1}{C} \int i_1 dt + M \frac{di_2}{dt}$$

$$-v = l \frac{di}{dt} (i_2 - i_1) + L_2 \frac{di_2}{dt} + M \frac{di_1}{dt}$$

where  $t = 0$  @  $t_4$ ,  $i_1(0) = I_4$  and  $v_c(0) = v \left( 1 + \frac{L_1}{M} \right)$ . In the  $s$  plane,

$$(2+L_1) I_4 - \frac{v}{s} \frac{L_1}{M} = I_1(s) \left[ s(2+L_1) + \frac{1}{sC} \right] \\ + I_2(s) \left[ s(M-l) \right]$$

$$(M-l) I_4 - \frac{v}{s} = I_1(s) \left[ s(M-l) \right] + I_2(s) \left[ s(L_2+l) \right]$$

from which

$$I_1(s) = \frac{sI_4 - \frac{v}{s} \left( \frac{L_1}{M} + \frac{l-M}{l+L_2} \right)}{s^2 + \omega_1^2}$$

and  $I_2(s) =$

$$-\frac{s^2 \frac{v}{s} \left( \frac{L_1}{M} + l \right)}{L_e (l+L_2)} + \frac{sI_4 \frac{M-l}{s(L_2+l)}}{s^2 \left[ s^2 + \omega_1^2 \right]} - \frac{v}{CL_e (l+L_2)}$$

where

$$\omega_1 = \frac{1}{\sqrt{CL_e}} \text{ and } L_e = \frac{l(L_1+L_2+2M) + L_1 L_2 - M^2}{l+L_2}$$

Then

$$i_1(t) = I_4 \cos \omega_1 t - v \sqrt{\frac{C}{L_e}} \left( \frac{L_1}{M} + \frac{l-M}{l+L_2} \right) \sin \omega_1 t \text{ and}$$

$$i_2(t) = v \sqrt{\frac{C}{L_e}} \left( \frac{l - \frac{1}{2} \left( 1 + \frac{L_1}{M} \right)}{L_2 + l} \right) \sin \omega_1 t - \frac{v}{L_2 + l} t \\ + \frac{I_4(M-l)}{L_2 + l} (1 - \cos \omega_1 t).$$

At Q2 turn-off,

$$i_1(t_5 - t_4) = 0 \text{ or } t_5 - t_4 = \frac{1}{\omega_1} \tan^{-1} \left[ \frac{I_4 \sqrt{\frac{L_1}{C}}}{\frac{L_1}{M} + \frac{l-M}{l+L_2}} \right]$$

and  $i_2(t_5 - t_4) = I_5$

The final capacitor voltage is then

$$v_c(t_5 - t_4) = v \left( 1 + \frac{L_1}{M} \right) + \frac{i}{C} \int_0^{t_5 - t_4} i_1 dt$$

$$v_c(t_5-t_4) = I_4 \sqrt{\frac{L_a}{C}} \sin \omega_1 (t_5-t_4) + v \left[ 1 + \frac{M-2}{L_2+2} + \left( \frac{L_1}{M} - \frac{M-2}{L_2+2} \right) \cos \omega_1 (t_5-t_4) \right].$$

After Q2 stops conducting  $i_1 = 0$ ,  $i_2 = I_3$ , the simple first order equation in  $i_2$  yields

$$t_6 = t_5 + \frac{I_5}{L_2 + 2}$$

The preceding analysis does not include core loss and copper loss in the coils or losses in the capacitors. These losses will result in lower peaks in the maximum  $v_c$  and  $i_{Q2}$ . However, in the case of the circuit of figure 1 which shows one of two chopper switches which are switched on alternately,  $L_1 = L_2 = 20\text{uh}$ ,  $C = 100\text{uf}$ ,  $L_5 = 75\text{uh}$ ,  $V = 200\text{Vdc}$ ,  $v_{co} = 500\text{v}$ ,  $M = 19\text{uh}$ ,  $i = 1\text{uh}$ ,  $v_o = 70\text{v}$  and  $I_o = 750\text{A}$ .

Then

I	$v_c$ , $v_A$
$I_1 = 556\text{A}$	$v_{A1} = 173\text{v}$
$I_2 = 945\text{A}$	$v_{A2} = 173\text{v}$
$I_3 = 1830\text{A}$	
$I_4 = 1780\text{A}$	$v_{c4} = v_{A4} = 400\text{v}$
$I_5 = 1190\text{A}$	$v_{c5} = v_{A5} = 793\text{v}$

t	$\Delta t$
$t_1 = 55\text{usec}$	$t_1 = t_2 - t_1 = 280\text{usec}$
$t_2 = 385\text{usec}$	$t_q = 35\text{ usec}$
$t_3 = 431\text{usec}$	$t_3 - t_2 = 46\text{usec}$
$t_4 = 442\text{usec}$	$t_4 - t_2 = 57\text{usec}$
$t_5 = 477\text{usec}$	$t_5 - t_4 = 35\text{usec}$
$t_6 = 602\text{usec}$	$t_6 - t_5 = 120\text{usec}$
$T = 714\text{usec}$	$t_2 = t_7 - t_2 = 416\text{usec}$

#### Feedforward Circuit

The system operates to keep the average value of switch output voltage,  $v_s$ , directly proportional to a control voltage on a pulse to pulse basis, virtually eliminating line variations. This is accomplished by applying a voltage proportional to the instantaneous value of the switch output voltage to an integrator. The output of the integrator is compared with the control voltage to generate the OFF pulse. See Figure 1. Variations in the line voltage,  $v$ , whether due to phase imbalance,

ripple or line perturbations are integrated to advance or retard the OFF pulse giving a feedforward correction to hold the average value of the switch output voltage proportional to the control voltage,  $v_2$ .

After being reset at  $t_0 = 0$  the integrator output is

$$v_1(t) = \frac{1}{R'C'} \int_0^t v_s(t) dt = \frac{a}{R'C'} \int_0^t v_s(t) dt$$

The OFF trigger occurs at  $t_2$  when  $v_1(t_2) = -\frac{R_1}{R_2} v_2(t_2)$ , after which  $v_s = 0$  until the next ON pulse occurs. The average value of  $v_s$ ,  $\bar{v}_s$ , is then  $\bar{v}_s = \frac{1}{T} \int_0^T v_s(t) dt$ . Thus  $v_1(t_2) = \frac{a}{R'C'} T \bar{v}_s = -\frac{R_1}{R_2} v_2(t_2)$  from which  $\bar{v}_s$  is a linear function of  $v_2(t_2)$ :

$$\bar{v}_s = -\frac{R_1 R'C'}{a T R_2} v_2(t_2)$$

#### Control Loop

The block diagram of Figure 3 includes the approximate low frequency transfer function of the load magnets and the linearization of the switch transfer discussed above. The current to be regulated is sensed by a precision Hazemeyer D.C. current transformer which is rated at  $\pm 1\text{ ppm}/^\circ\text{C}$  gain-temperature coefficient with an absolute accuracy of  $\pm 10\text{ ppm}$  of full scale. The output of the DCCT is compared with the output of a selected 16 bit D/A converter which has negligible offset variation and a gain T.C. of  $2\text{ ppm}/^\circ\text{C}$  max in a chopper stabilized precision error amplifier. The A2 integrator minimizes static loop gain errors and provides lead-lag compensation for loop stability. The resulting static errors should be within the time and temperature stability requirements.

The switch output filter will reduce the  $1.4\text{K}$  &  $2.8\text{K}$  Hz basic ripple and eliminate the higher harmonics of the chopper output. The inductance of the load magnets and the attenuation due to eddy currents in the magnet laminations and the aluminum vacuum chamber will further reduce the field ripple seen by the beam to acceptable levels.

The frequency response of the components of the system as well as the overall open loop gain and phase frequency response are given in Figure 4. Analytically,

$$GH = \left[ \left( R_D \right) \left( \frac{R_1 \left( 1 + \frac{s}{\omega_1} \right)}{s R_c C_1 \left( 1 + \frac{s}{\omega_1} \right)} \right) \left( - \frac{R_1 R' C'}{R_2 \alpha T} \right) \right]$$

$$\left( \frac{1 + b \frac{s}{\omega_0}}{\left( 1 + c \frac{s}{\omega_0} \right) \left( 1 + 2 \gamma a \frac{s}{\omega_0} + \left( \frac{as}{\omega_0} \right)^2 \right)} \right) \frac{1}{R \left( s \frac{L}{R} + 1 \right)} \left[ \frac{\epsilon}{R_A} \right]$$

for which in the case of the 7UV dipoles,

$$\begin{aligned} R_D &= 500K & R_1 &= 2K \\ R_1 &= 16K & R_2 &= 5.6K \\ R_c &= 2.4K & R' &= 51K \\ C_1 &= 1\mu F & C' &= 0.01\mu F \\ C_2 &= 0.01\mu F & \alpha &= 0.05 \end{aligned}$$

$$\begin{aligned} T &= .7 \text{ msec} & R &= .044\Omega \\ \omega_0 &= 628 \text{ rps} & L &= 91.5 \text{ mH} \\ a &= .605 & r &= 10V/2000A \\ b &= 1.6 & R_A &= 5K \\ c &= .875 & \gamma &= 0.6 \end{aligned}$$

The phase margin at the gain crossover at 100 Hz is then 68° which results in optimum system speed of response and settling time.

#### CONCLUSION

The design described meets the requirements for the system with an approach that reduces to a straight forward control loop. It avoids the complication of multiple correction loops required for an SCR phase control loop to achieve this level of stability or the cost and power loss of a transistor bank regulator.

It presents some practical problems, however. The leakage inductance and lead inductance at L1/L2 must be minimized in order to minimize the capacitor voltage and the resulting capacitor losses due to two voltage reversals per cycle. Operation at audio frequencies at this power level can produce objectional mechanical effects which must be dealt with. Also, the electrical interference generated causes difficulties, not the least of which is interference in the sensing of the current by the DCCT. Nevertheless, these are problems which can be solved, making this SCR chopper regulator a very interesting and useful alternate to more classical accelerator magnet power supply approaches.

#### ACKNOWLEDGMENTS

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**CAPTIONS**

**Figure 1. Chopper Control Loop  
NSLS Dipole Magnet Power**

**Figure 2a. Chopper Switch Equivalent**

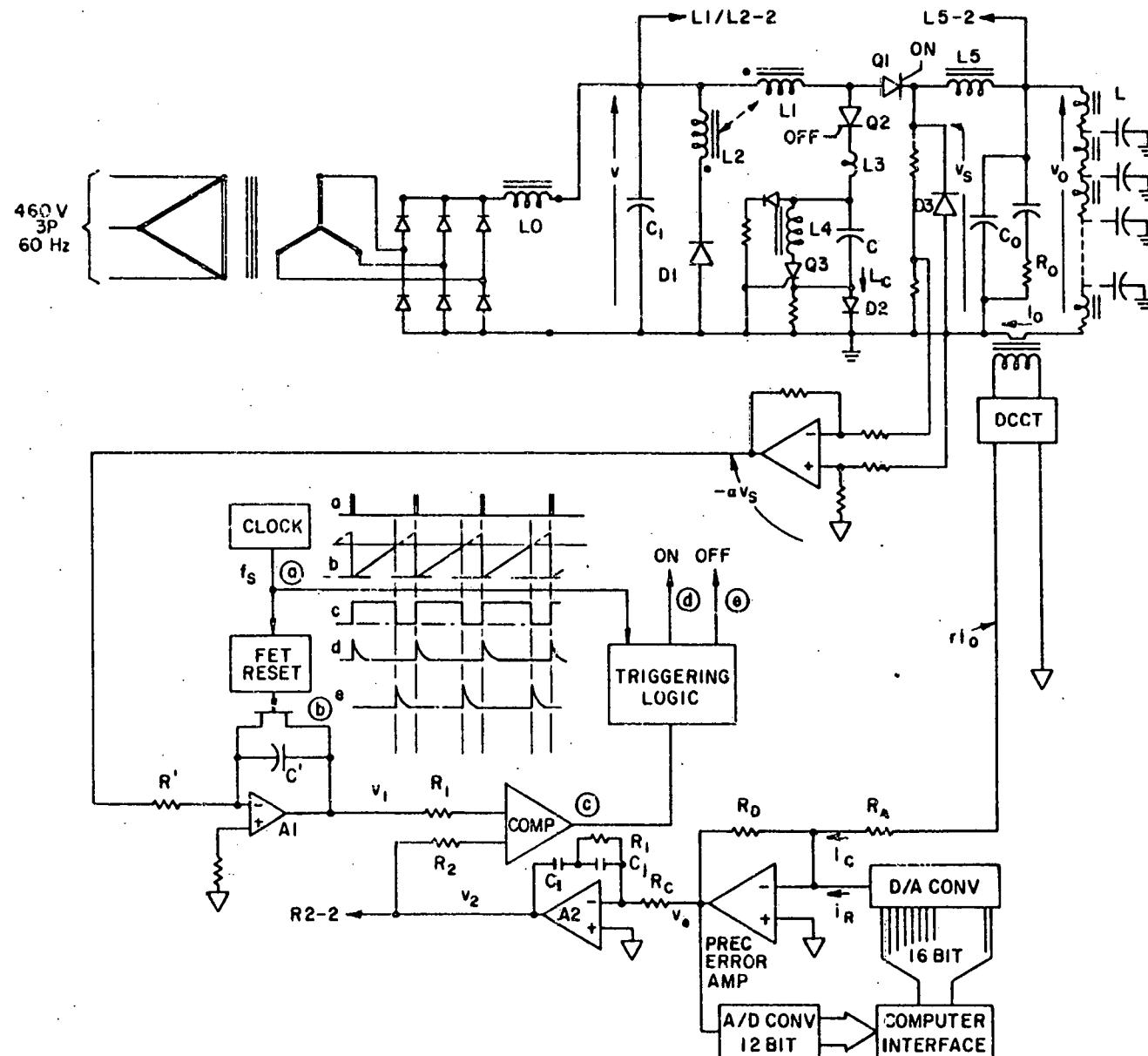
**Figure 2b. Typical Waveforms  $L_1=L_2$  M**

**Figure 3. Chopper Power Supply  
Block Diagram**

**Figure 4. Frequency Response  
NSLS Dipole Power Source**

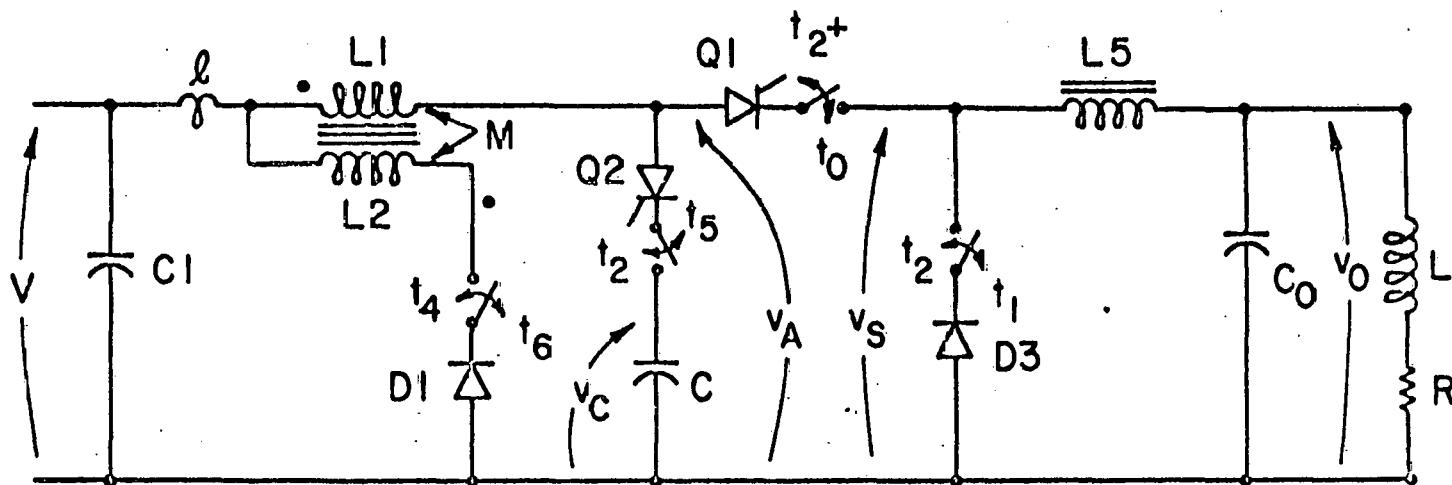
**Figure 5. Switch Assembly  
NSLS UV Dipole Power Source**

**Figure 6. Switch Assembly Semiconductor  
Components  
NSLS UV Dipole Power Source**



CHOPPER CONTROL LOOP  
NSLS DIPOLE MAGNET PWR  
FIGURE 1

FIGURE 2a



CHOPPER SWITCH EQUIVALENT

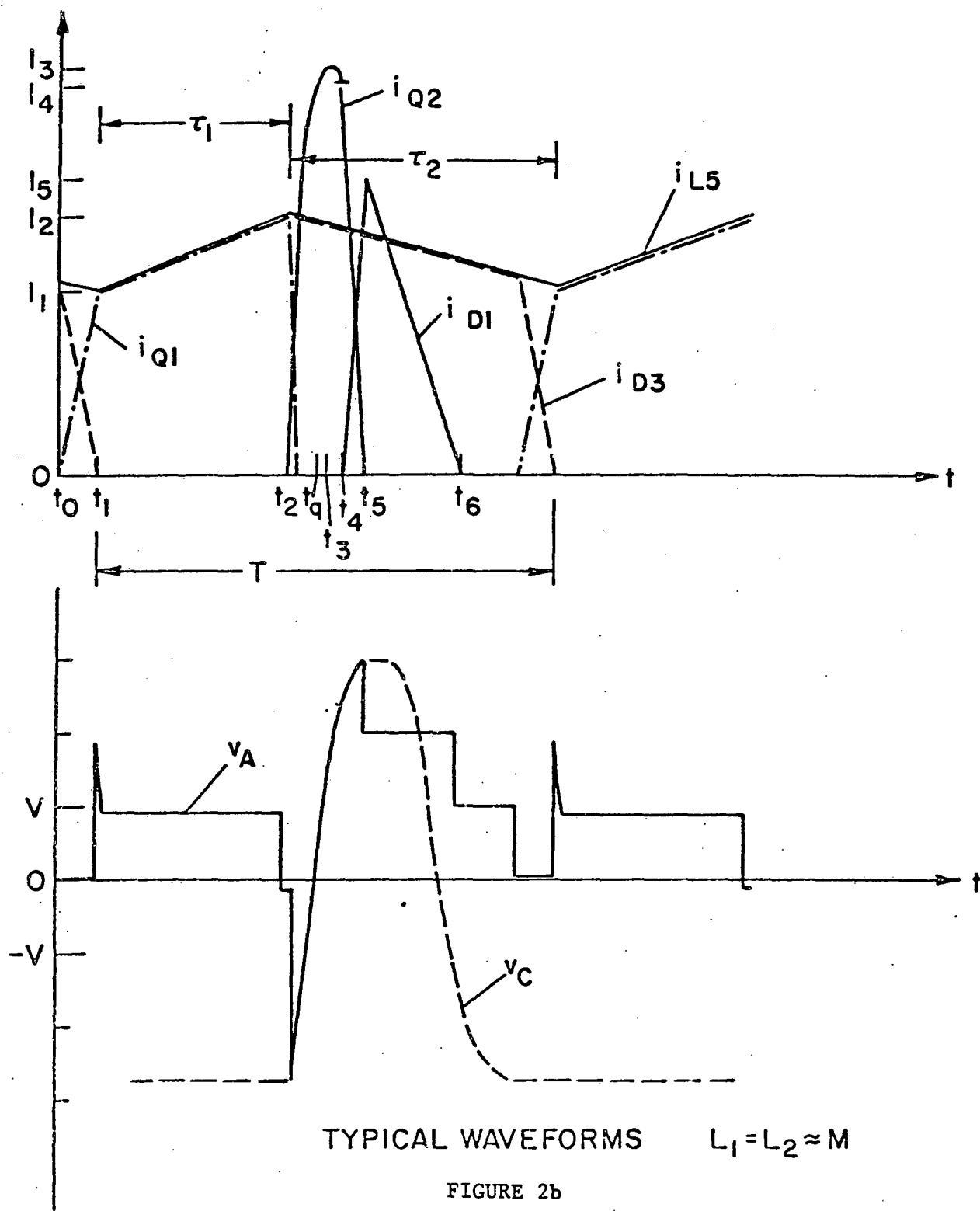
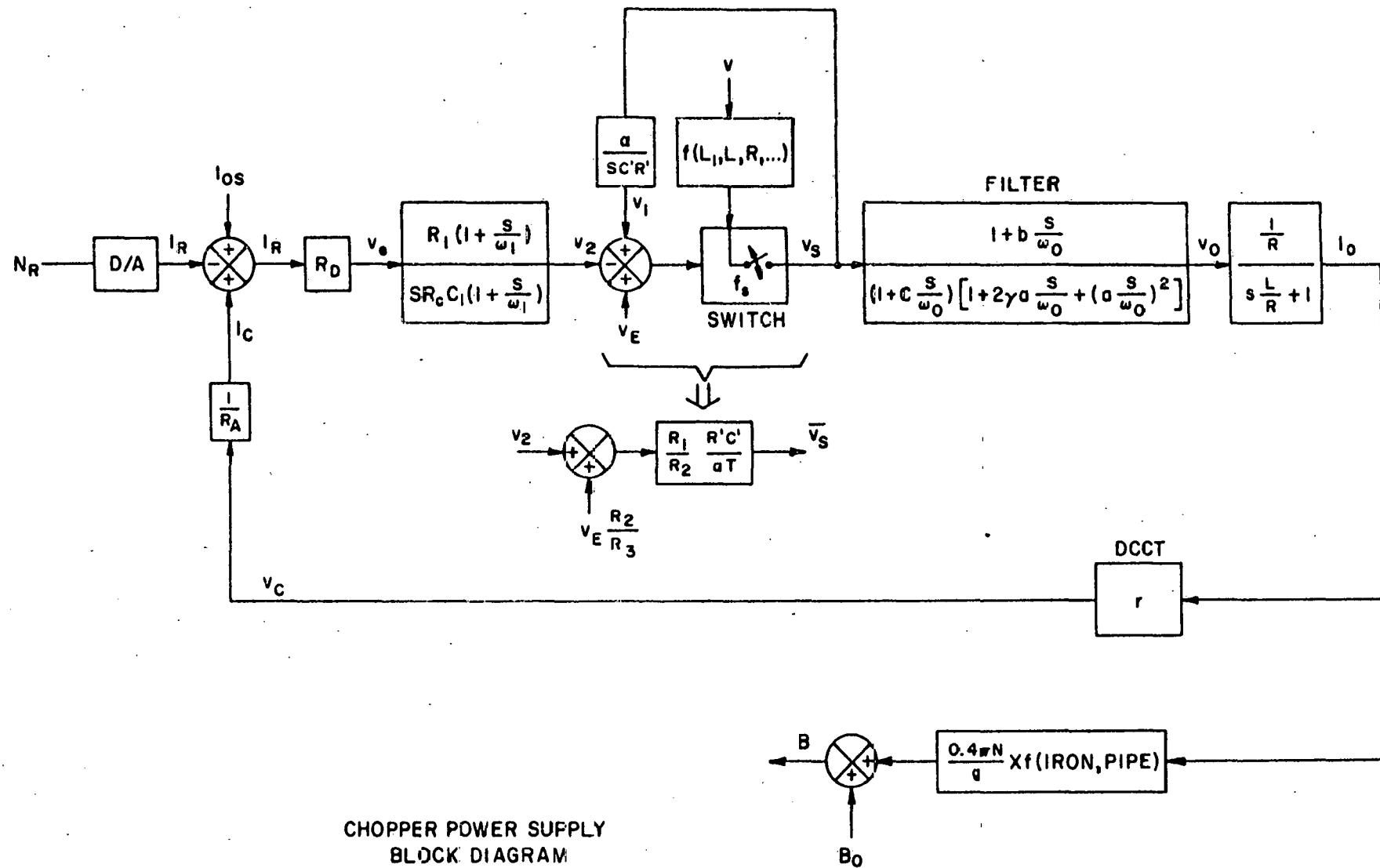
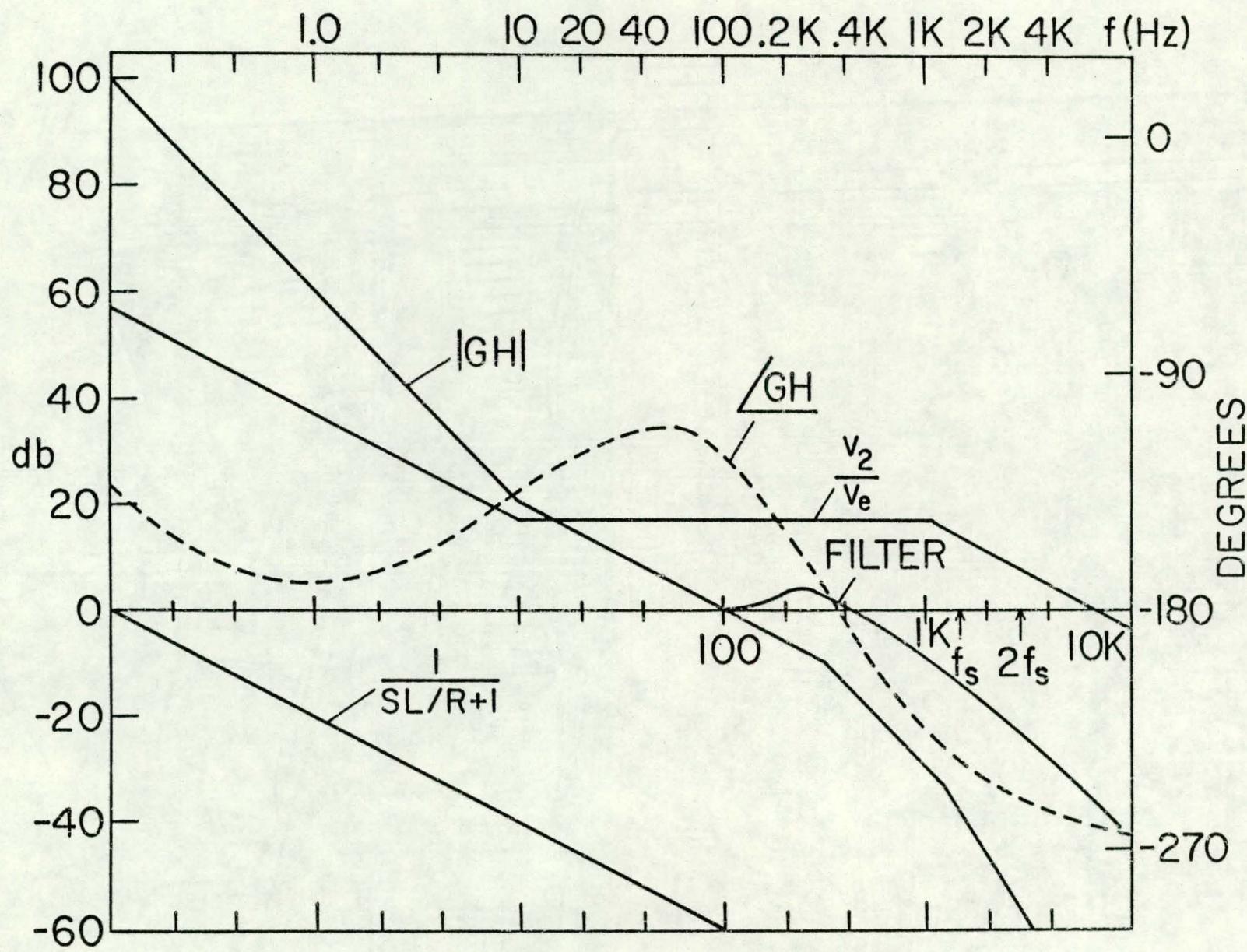


FIGURE 2b

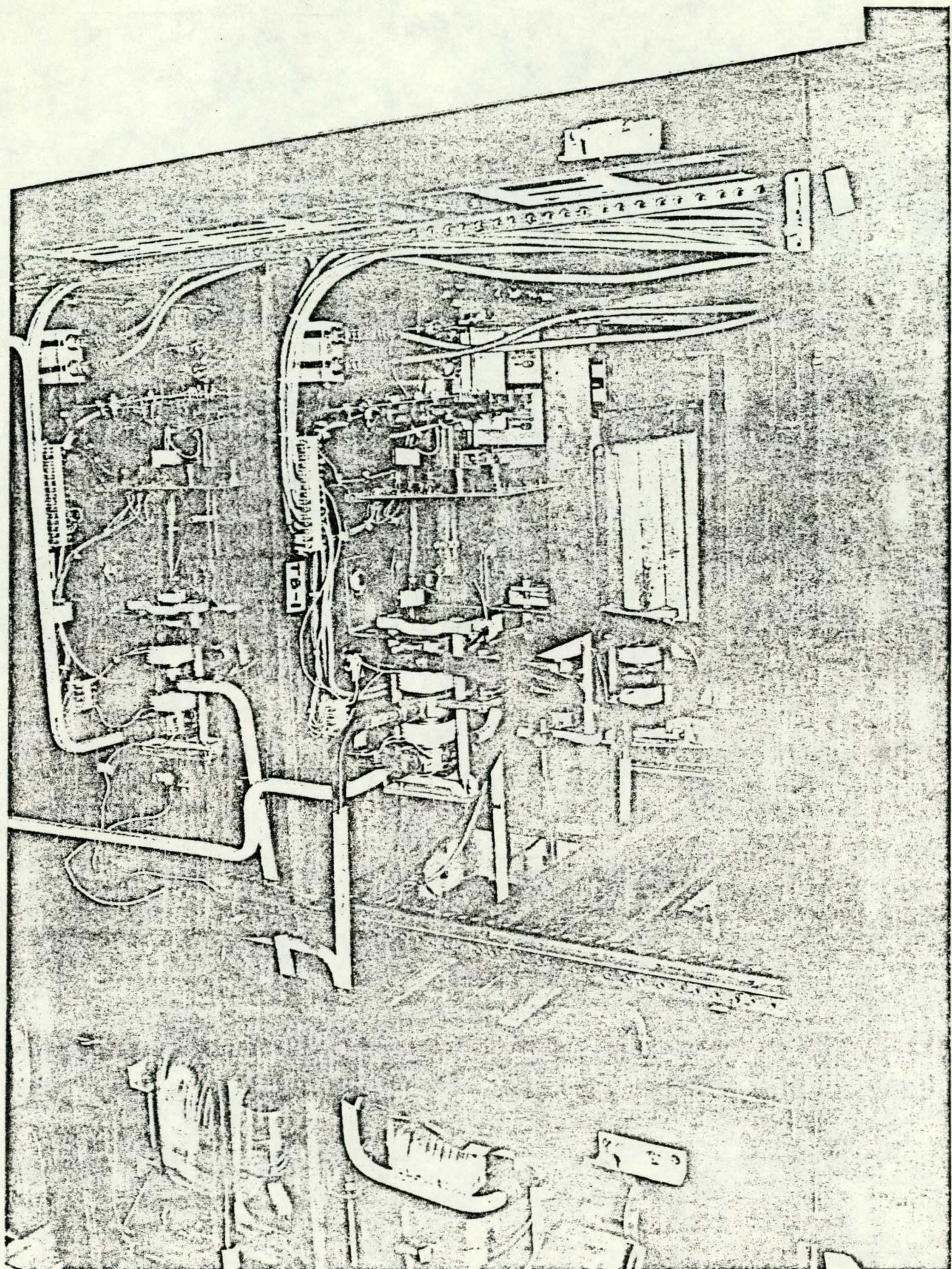




FREQUENCY RESPONSE  
NSLS DIPOLE POWER SOURCE  
FIGURE 4



SWITCH ASSEMBLY  
NSLS UV DIPOLE POWER SOURCE  
FIGURE 5



SWITCH ASSEMBLY SEMICONDUCTOR COMPONENTS

NSLS UV DIPOLE POWER SOURCE

FIGURE 6