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Title: **Multichip Module Technology Development**

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Abstract

This is the final report of a one-year, Laboratory Directed Research and Development (LDRD) project at Los Alamos National Labortory (LANL). A Multichip Module (MCM) was designed and submitted for fabrication to the Lockheed Martin foundry using a licensed process called High Density Interconnect (HDI). The HDI process uses thin film techniques to create circuit interconnect patterns on multiple layers of dielectric film which are deposited directly on top of unpackaged electronic die. This results in an optimally small package that approaches the area of the bare die themselves. This project tested the capability of the Lockheed Martin foundry to produce, in an HDI process, a complex mixed-mode (analog and digital) circuit on a single MCM substrate.

Background and Research Objectives

The trend in electronics chip design has been toward a higher degree of complexity on smaller and smaller substrates, made possible by the capability of semiconductor foundries to achieve feature sizes of one micron or less. For the most part, the packaging of these electronics die has not kept pace with the die miniaturization, and therefore the potential benefit of creating a complex device with a minimum package size has not been fully exploited. This is especially true when the device uses both analog and digital circuitry. To date, the most extensive developments in package and circuit miniaturization have been confined to digital-only applications such as computer memories and processors.

The vast majority of circuits that populate electronics instrumentation are made from packaged integrated circuits. The packages are usually plastic or ceramic, they completely encapsulate the die inside, and have pins or pads to connect them to a circuit substrate. The package is usually several times larger than the die itself. Unpackaged die can be directly attached to a circuit substrate by gluing them in place with a conductive epoxy or attaching them via bump or ultrasonic wire bonding. When a circuit is created using unpackaged die,

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it is referred to as a Multichip Module, or MCM. There are several types of MCMs which are differentiated by the die-attach and trace patterning method they employ. In this project, we have designed in the HDI process. The process exploits the fine line capability and precise patterning of thin film technology. The bare die are epoxied into wells that are machined into the surface of an alumina substrate. The depth of the wells is precisely controlled so that when the die are placed into them, the top surface of each die is coplanar with the unmilled surface of the substrate. A polyimide film is then glued onto the entire surface. Holes are laser-drilled through the polyimide, over the contact pads of the die, and subsequently metallized to make very low inductance electrical connection. The trace circuitry is patterned onto the polyimide layer according to the design layout. Multiple layers are built up in like fashion.

When a circuit is built from packaged parts, it is relatively straightforward to test the part before it gets soldered into place on the circuit board. It is not easy to do this when bare die are used. The die are small, typically a few millimeters on a side. They are fragile, typically made on 1/2 millimeter-thick substrates. And their input/output pads (I/O) can be patterned on an extremely small pitch, 50-100 microns pad-to-pad. Sophisticated probing equipment is required to make electrical contact with the die I/O. It is also much more difficult to replace a defective die than it is to replace a packaged IC on a conventional circuit board. It is, therefore, crucial to ensure the functional integrity of each bare die before it is attached to a substrate. A die that has been qualified for die-attach by a complete functional test is referred to as a *known good die* (KGD).

In the case of a commercially developed die, it is possible to purchase the die as KGD. This is typically expensive, mostly due to the fact that the packaged IC market dwarfs the demand for unpackaged die.

Importance to LANL's Science and Technology Base and National R&D Needs

In the Physics (P) Division at Los Alamos, research in particle and nuclear physics experiments has led to developing position-sensitive instruments that are comprised of tens of thousands of individual readout channels. These instruments perform in colliding- and fixed-target accelerator environments where both mechanical and electronic constraints require that readout electronics boards be as small as possible. The efficient dissipation of the heat generated by this dense circuitry is also a very important issue. The HDI process addresses the packaging constraints and provides excellent thermal contact between the electronics die and the alumina substrate because the die are housed in wells in the

substrate. The alumina efficiently spreads the heat over the entire substrate, therefore facilitating the removal of the heat. This performance was confirmed in thermal simulations that were run by B. Wong-Swanson.

In the Nonproliferation and International Security (NIS) Division, the development of space-based and hand-held discreet surveillance detectors share similar requirements. Board shrink of existing designs through an HDI layout can take a conventional printed circuit design that is the size of an attaché case, and reduce it to the size of a pocket pager.

Scientific Approach and Accomplishments

The first step in the development of an MCM is to get the appropriate die in unpackaged form. This MCM is comprised of both commercial and custom integrated circuits. The custom circuits are a three-die set that has been designed by engineers at Oak Ridge National Laboratory (ORNL). The first die is an amplifier/discriminator, the second is an analog memory, and the third is an analog to digital converter. The die perform these functions in a serial manner, the output of the first feeding the input to the second, etc. The first two die are essentially analog devices, while the third is a digital circuit. Procurement authority to have these die manufactured was given to our group by ORNL. We submitted a fabrication run to the ORBIT semiconductor foundry. We purchased sixteen of each die in unpackaged form. The die I/O pad layout and interconnect pattern was transferred electronically to the design team in NIS, and subsequently translated from the ORNL ORCAD format into the NIS Mentor system.

Each MCM also has two commercial die. These are field programmable gate arrays (FPGAs) manufactured and distributed by Xilinx. The FPGAs are used for the control logic for the synchronized operation of the MCM. Xilinx does not sell their product in bare die form direct to the customer. Instead we purchased the die from a broker called Chip Supply. Chip Supply buys and stocks integrated circuit wafers from a number of manufacturers. They archive the manufacturer documentation and perform various levels of bare die test upon request. Because of the cost, the FPGAs that we bought for the MCM were visually inspected parts only, with no functional testing.

The layout (Fig. 1) of the MCM was done by Rick Muck. The design layout was made for an MCM substrate measuring 48mm x 40mm and 1.5mm thick. The substrate material is fired, white alumina (Al_2O_3, 96%). It has 14 wells milled into it to house the 12 custom application-specific integrated circuits (ASICs) and 2 FPGAs.

The circuit layout comprises four metal layers plus a base metal layer for the die attach. The first layer is the analog trace layer. The second is the power plane. The third layer is the digital signal layer. As much as possible, the analog and digital traces are routed perpendicular to each other to minimize crosstalk. The fourth layer is the ground plane. There are 29 surface mount chip capacitors on the top layer to provide decoupling on sensitive signal lines and critical voltage lines. In total, there are nearly 1000 connections, and 3600 vias. The via drill size is 0.045mm, and the via pad size is 0.072mm. The minimum trace width is 0.048mm with a minimum trace-to-trace spacing of 0.048mm.

The input connector is 34 contact pads for 32 inputs and 2 detector bias connections. The pads are 1.5mm x 0.45mm on a 0.7mm pitch. The output connector is 208 contacts. These pads are 1.5mm x 0.1mm on a 0.2mm pitch. Connections to the connector pads will be made by ultrasonic wire bonding. The pads are metallized on the base metal layer.

The design was submitted for fabrication early in 1997. We share the foundry production line with another LANL project in order to reduce the one-time cost of using that line. Unfortunately, the other project had several documentation errors relating to the commercial bare die that they supplied to the foundry. Much time was lost because of this. The foundry released the design to their production facility on April 10, 1997. The projected date of delivery of the completed MCM was the first week of July, 1997. Foundry problems have caused this date to slip as well.

Four MCMs will eventually be delivered to LANL. When they arrive, they will be wire-bonded to a silicon strip detector at the input, and to an existing data acquisition system on the output. The MCM functionality and performance will be tested and documented.

Although the project has experienced several significant delays, and the final performance of the mixed-mode MCM is not yet available, there have been several important accomplishments and lessons learned in the project.

The HDI process is a very sophisticated one, which requires an unusually precise knowledge of the physical parameters of the electronic die to be used. Because the present market is driven by packaged devices, commercial manufacturers are very slow to update their documentation on changes that affect the physical aspect of a die, when it leaves the packaged part unchanged. There is much better documentation control when the die being used for the HDI-MCM are custom designed by, or for, the user.

The market for production quantity HDI-MCMs is still developing. Lockheed Martin demonstrated, by their performance, that although they have had success in

processing relatively simple MCMs, they still have a learning curve to climb to be able to function in an entrepreneurial mode to deliver complex devices to customers on schedule. The experience that they have gained through this project may have helped them toward achieving that goal.

The design group at NIS successfully demonstrated the capability to lay out a complex, mixed-mode circuit in the HDI process. To achieve that end, they dealt with technical communication issues across internal and external group boundaries.

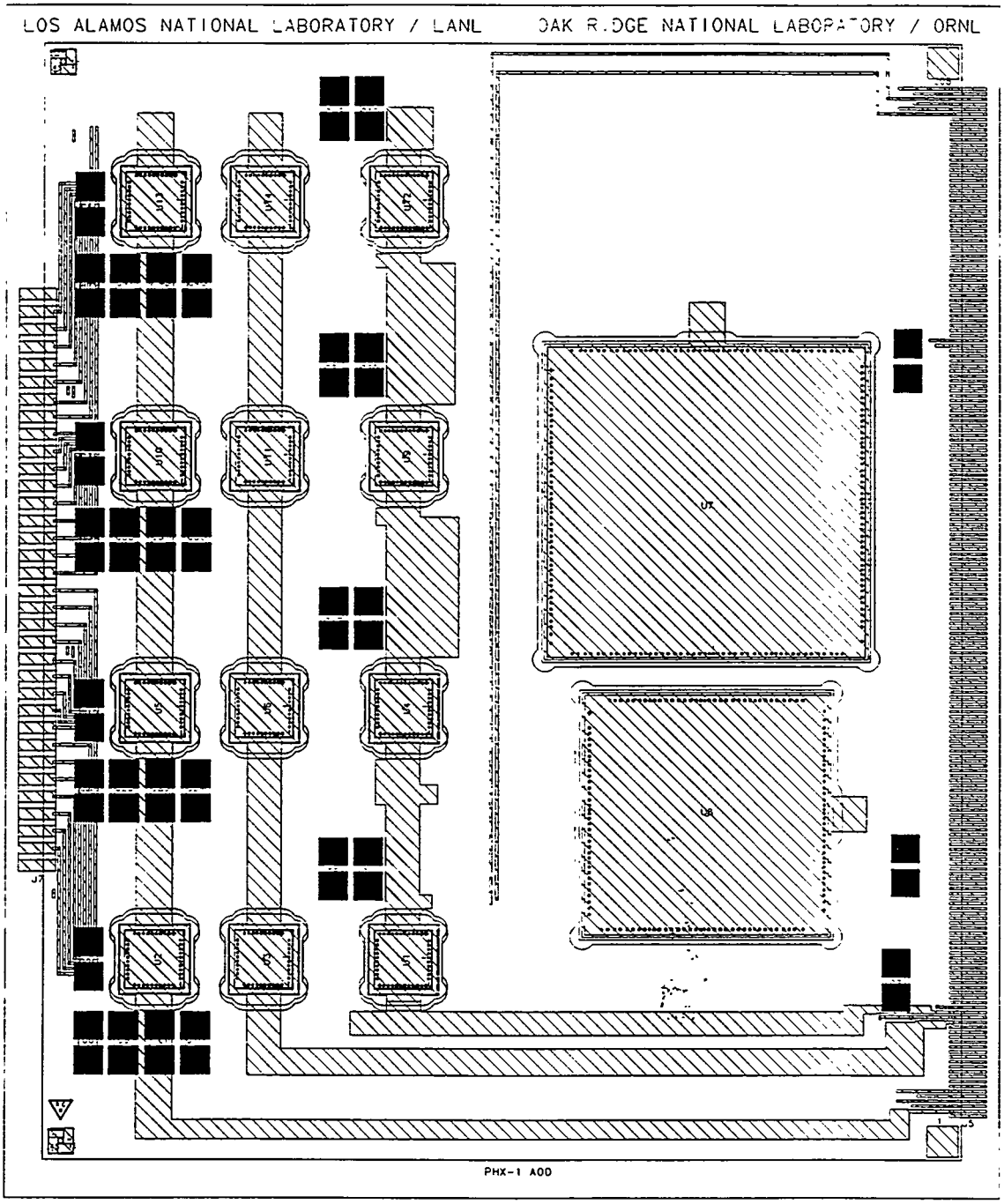

Figure 1. Multichip Module (MCM) layout.