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LANSCE ACCELERATOR TIMING SYSTEM UPGRADE

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Abstract

The Los Alamos Neutron Science Center (LANSCE) 800 MeV proton linear accelerator (linac) operates at a maximum repetition rate of twice the AC power line frequency, i.e. 120 Hz. The start of each machine cycle occurs a fixed delay after each zero-crossing of the AC line voltage. Fluctuations in the AC line frequency and phase are therefore present on all linac timing signals. Proper beam acceleration along the linac requires that the timing signals remain well synchronized to the AC line. For neutron chopper spectrometers, e.g., PHAROS at the Manuel Lujan Jr. Neutron Scattering Center, accurate neutron energy selection requires that precise synchronization be maintained between the beam-on-target arrival time and the neutron chopper rotor position. This is most easily accomplished when the chopper is synchronized to a stable, fixed frequency signal. A new zero-crossing circuit which employs a Phase-Locked Loop (PLL) has been developed to increase the phase and frequency stability of the linac timing signals and thereby improve neutron chopper performance while simultaneously maintaining proper linac operation. Results of timing signal data analysis and modeling and a description of the PLL circuit are presented.

1 INTRODUCTION

The Los Alamos Neutron Science Center (LANSCE) 800 MeV proton linear accelerator (linac) provides pulsed beams of protons for direct use and for production of spallation neutrons. Employing Time-of-Flight (TOF) techniques and an assortment of instruments, experimenters at the Manuel Lujan Jr. Neutron Scattering Center (Lujan) use the pulsed neutron beams in a variety of research areas. One of those instruments, the PHAROS high-resolution chopper spectrometer [1], employs two rotating mechanical choppers. A "T0" chopper is used for background suppression of prompt gamma rays and high energy neutrons while a fast monochromating Fermi chopper is used for neutron energy selection. For the Fermi chopper to be effective, its rotor position must remain precisely synchronized to the proton beam arrival time on the spallation target. Lack of synchronization results in lower "good data" rates and wasted beam time. The finite bandwidth of the combined chopper rotor and drive system implies that precise synchronization is most easily achieved when the linac reference clock frequency is fixed and stable. However, this is not the optimal timing scenario for linac operation.

The linac is a pulsed machine which operates at a maximum repetition rate of 120 Hz, i.e., twice the AC power line frequency. Presently, the accelerator RF systems operate at a duty factor of about 10%. Each machine cycle occurs a fixed delay after each zero-crossing (ZX) of the AC line voltage. This was done to maximize performance of the linac. The gains of certain klystrons used in the Side Coupled Linac (SCL) are sensitive to their operating point relative to the AC line phase. These sensitivities are due to defects in the AC powered filaments and result in gain variations of ±15% over one full 60 Hz cycle. This constrains linac operations to remain well synchronized to the AC line.

Using the ZX reference signal the Master Timing System (MTS) generates all the logic timing signals used in triggering the ion sources, beam deflectors, linac RF amplifiers and other accelerator pulsed-power systems. Therefore, these timing signals contain phase and frequency fluctuations present in the line. This results in optimal linac operation but inefficient chopper operation.[1]

Recent measurements on the linac revealed that a several hundred microsecond window is available in which machine cycles could occur relative to the actual AC line ZX and not impact accelerator performance. This led to the possibility of operating the accelerator on a version of the ZX signal which had been filtered to reduce unwanted phase and frequency jitter, thereby resulting in a more stable reference signal for the choppers to follow. The bandwidth of the filter was selected to prevent the cumulative phase error between the raw and filtered signals from exceeding this available window. A simple Phase-Locked Loop (PLL) circuit consisting of a Phase Detector (PD), Loop Filter (LF), Voltage Controlled Oscillator (VCO) and frequency divider was chosen to provide the narrow-band filtering of the raw ZX signal.

2 DATA ACQUISITION, MODELING AND ANALYSIS

The AC power grid which supplies electrical energy to the accelerator is fed by variable output generators which respond to continuously fluctuating loads. This results in

[1] A provision does exist for starting each cycle on a trigger which occurs within a 75 μs window after the ZX. The PHAROS neutron spectrometer uses this feature along with an option to define the Proton Storage Ring extraction time to achieve proper synchronization of the beam-on-target arrival time and the Fermi chopper rotor position. However, the chopper uses the ZX signal as a reference and will therefore attempt to follow all the variations present in this signal.

a frequency modulated 60 Hz AC waveform [2]. Both the magnitude and rate of change of the frequency variations are important. To determine the correct amount of filtering to be applied to the raw ZX signal, a simple data acquisition system was employed to collect pulse-to-pulse time variations and a simple PLL model was developed for analysis of these data.

The ZX signal is a nominal 120 Hz pulse train. However, the existing ZX circuit did not contain any prefiltering to remove unwanted higher harmonics present in the AC line and also at times introduced unwanted 60 Hz modulation of the output pulse train. A new circuit incorporating a band-pass filter and precision comparator was therefore assembled to provide an accurate ZX signal for this analysis. A CAMAC module (single input, dual scalar with an internal 2 MHz clock) was available which allowed the time difference between adjacent pulses (~8333 μs) to be measured without dead time. These data were recorded and stored in event files for off-line analysis. A typical spectrum of the time difference between adjacent ZX pulses is shown in Figure 1.

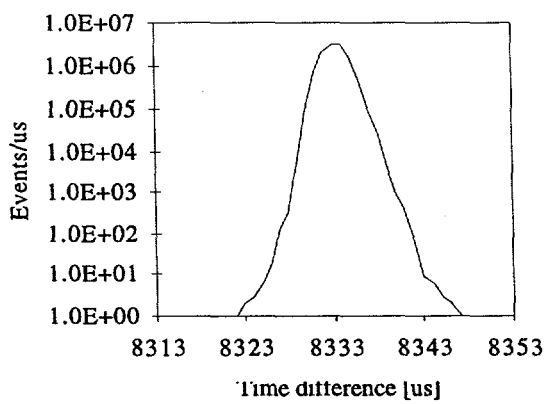

Figure: 1 Typical distribution of time differences between adjacent zero crossings for a 24 hour period.

A simple PLL model was developed for the analysis. The basic information available was a sampled data set of the time difference between adjacent zero-crossings. Although these time differences, i.e., sampling intervals, are not constant, the variations are small enough that to a good approximation the sampling frequency is 120 Hz. Each measurement was reduced to the time (phase) error between the actual and ideal waveforms by subtracting off the time interval of the 120 Hz sampling frequency. These data were then used as input to the PD in the PLL model. Because the data were sampled, a discrete-time PLL model [3] was used. This is shown schematically in Figure 2. This is a linear model of a 2nd-order PLL which is initially locked, i.e. no loop error, at the desired frequency of 120 Hz. In the actual PLL phase detector, the input and clock signals are combined to produce a pulse-width modulated error signal. In this model the phase detector is represented by a summing junction which produces

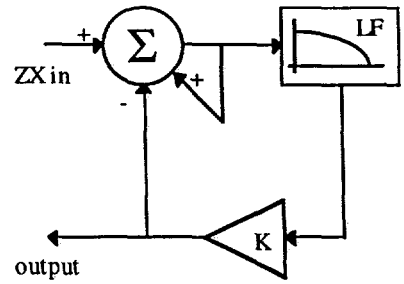

Figure: 2 Block diagram of discrete-time PLL model used in analysis of ZX data.

weighted impulses at the sampling frequency. To properly account for the accumulated phase difference between the actual loop input and VCO output signals, the error signal is summed back into the junction. The LF is a discrete time representation of a passive lag filter. Using the weighted impulse approximation, the phase error in the VCO output signal is then simply proportional to the output of the LF. This loop output served as the other PD input signal. Finally, the overall loop gain, K, is represented by a single gain block.

The PLL model was used in combination with the ZX data to evaluate the impact of different loop parameters on the cumulative phase (loop) error distributions. A FORTRAN program was written to simulate the PLL using the aforementioned model. Approximately twenty-four hours of contiguous zero-crossings were analyzed in order to get a representative picture of the phase error distribution that might be accumulated in a typical day. Results of the analysis suggested a 3 dB cutoff frequency (f_{3dB}) of 0.3 Hz and a damping factor (ζ) of 0.7 would produce a cumulative phase error distribution within the several hundred microsecond window.

3 NEW ZERO-CROSSING HARDWARE

A block diagram of the new Zero-Crossing Detector is shown in Figure 3. The detector consists of three major components: the pre-filter, the PLL, and the fault detection circuit. The pre-filter section performs the functions of reducing the AC line voltage to a manageable level and curtailing the line voltage sine-wave impurities. To accomplish these functions the pre-filter employs a transformer circuit, two 2-pole low-pass filters [4], and a 8-pole Butterworth switched capacitor band-pass filter [5]. All components and filter cutoff frequencies were selected to obtain a minimum phase shift at 60 Hz. Once the pre-filter has conditioned the input, the zero-crossing is detected in the PLL section using a precision comparator. This section also contains two PLL's [6] as well as the detection and pulse-shaping circuit. One PLL is used to generate the clock needed for the band-pass filter implementation to track the ZX center frequency. The

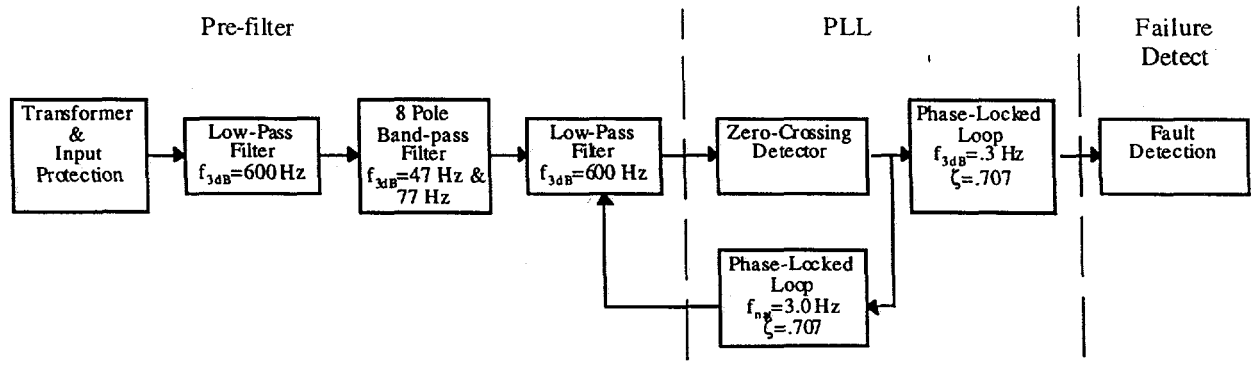

Figure: 3 New Zero-Crossing Hardware Diagram.

other PLL performs the narrow-band filtering of the zero-crossing pulse train. The type of phase detectors used in both PLL circuits are Phase Frequency Detectors (PFD). The PFD has several advantages over other phase detectors [6]. However, the PFD will cause the VCO output to go to its maximum value if one of the phase detector inputs is missing. Provisions to handle this failure mode were made in the fault detection circuitry. Loop filters for the two PLL's differ in filter order and implementation. The PLL which provides the clock for the band-pass filter was implemented using a fifth-order low-pass filter as described in Reference [7]. Using the method found in Reference [6], a natural frequency (f_{nat}) of 3.0 Hz and a ζ of 0.707 were measured for this PLL. A ζ of 0.707 and a much lower f_{3dB} of 0.3 Hz were achieved for the other PLL using a traditional passive lag filter with an additional pole to reduce jitter. The jitter was seen as power in the side bands when looking at the output using a spectrum analyzer [6]. Following the filtering action of the PLL, the pulse train enters the fault detection circuit where the time delay from pulse to pulse is checked for instantaneous frequency shifts. When a fault is detected, an oscillator, which was synchronized to the last known good zero-crossing pulse, is switched into operation. Provisions were made for the circuitry to automatically switch back to the detected zero-crossing once the fault is cleared.

4 SUMMARY

A new ZX circuit employing a PLL has been implemented at the LANSCE facility. This new circuit produces a more stable reference signal for the neutron choppers to follow without impacting linac performance. It also affords the option of improving the stability of the ZX signal even further by reducing the bandwidth of the filter through simple component replacement. This option will be pursued as the sources of the linac's AC line phase sensitivities are better understood and mitigated.

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