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Performance Characterization and Validation of ASCI Applications: A Memory Centric View

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Extended Abstract

Performance and scalability of high performance scientific applications on large scale parallel machines are more dependent on the hierarchical memory subsystems of these machines than the peak instruction rate of the processors employed. The dependence is likely to increase in the future [1,4]. While single-processor performance may double every eighteen months, memory bandwidth increases by only 15% during the same period.

In addition, distributed shared memory (DSM) architectures are now being implemented which extend the concept of single-processor cache hierarchies across an entire physically-distributed multi-processor machine. Machines which will be available to the Department of Energy's Accelerated Strategic Computing Initiative (ASCI) can have as many as 128 processors in a single DSM. Scalability of these machines to large numbers of processors is ultimately tied to issues of memory hierarchy performance, which includes data migration policies and distributed cache coherence protocols. Investigations of the performance improvements of applications over time and across new generations of machines must explicitly account for the effects of memory performance.

In this paper, we characterize application performance with a "memory-centric" view. The applications are a representative part of the ASCI workload. Using a simple Mean Value Analysis (MVA) strategy and observed performance data, we infer the contribution of each level in the memory system to the application's overall performance in cycles per instruction (CPI). Our empirical model accounts for the overlap of processor execution with memory accesses.

Measurements of ASCI codes were obtained on the latest Origin 2000 and Power Challenge machines from Silicon Graphics, Inc. (SGI). These machines provide a very interesting perspective since they use the identical MIPS R10000 processor but differ significantly in the design of the memory subsystems [2,3].

The full paper describes the parts of the machine architecture relevant to this work, codes from the ASCI workload, the model and empirical methodology, validation of the model using a combination of measurement and simulation, results, analysis and major conclusions.

In this abstract, we will provide an abbreviated discussion of the model and present one characterization of the ASCI codes that was obtained using the model.

The application analysis in the paper uses a typical mean value parameterization [5] to separate CPU execution time from stall time due to memory loads/stores. The key issue in

the analysis is to determine the amount of memory access time that is overlapped by computation.

The model projects the overall CPI of an application as a function of CPU execution time and average memory access times:

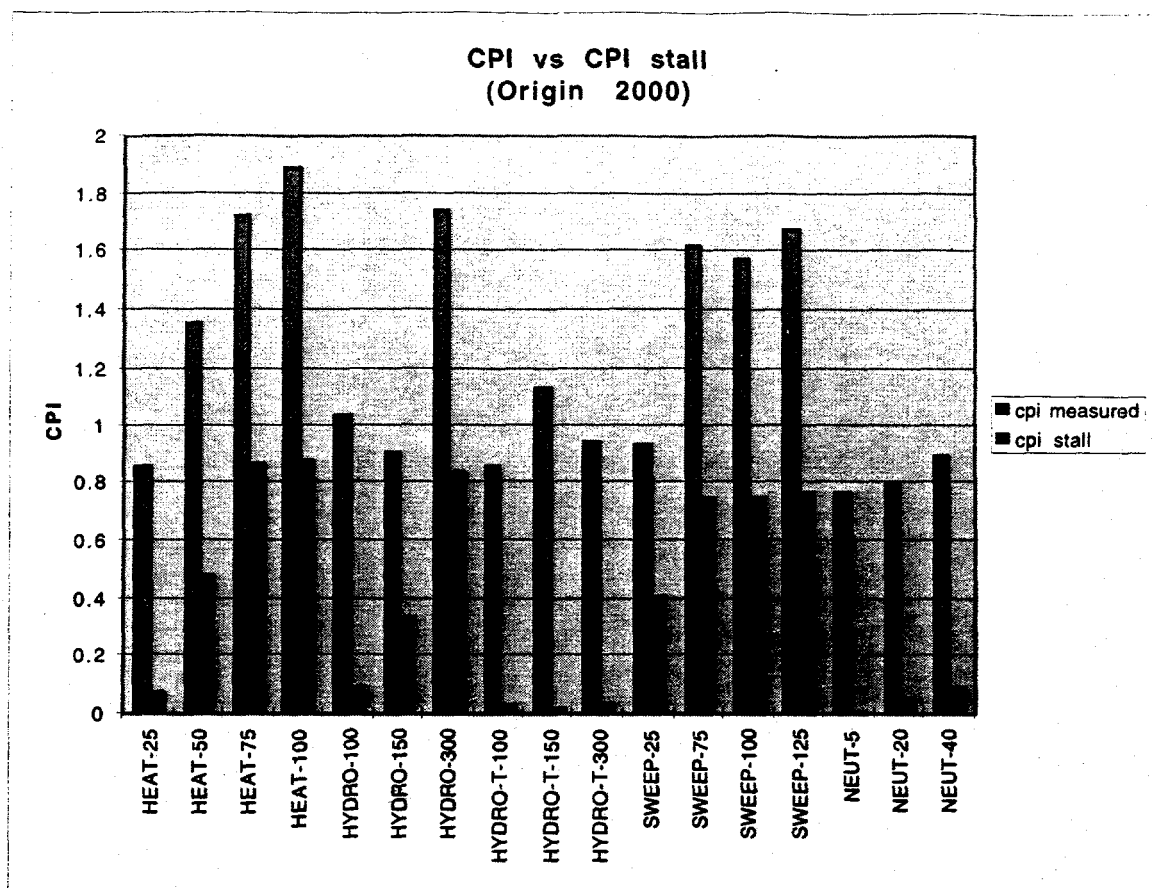$$CPI = CPI_0 + \sum_{i=1}^{nlevels} h_i * t_i \qquad (1)$$

where CPI_0 is the CPI of the application assuming that all memory accesses take 1 clock period (CP), and h_i and t_i are, correspondingly, the hits per instruction and average non-overlapped access times for the ith level cache.

If no overlap of CPU execution and memory access occurs, every memory access to the ith level incurs the full round-trip latency, which we denote as T_i. We define a measure of the overlap of memory accesses with computation as m_o, where

$$CPI = CPI_0 + (1-m_o) \sum_{i=1}^{nlevels} h_i * T_i . \qquad (2)$$

Although this overlap is not directly measurable, using the relationship in Eq. 1, we can infer the overlap for an individual application by performing a least-squares fit of the model parameters to observed execution data (CPI, h_i) for that code. CPI and hits are obtained from the MIPS R10000 hardware performance counters [6]. Validation of the inferred model parameters is accomplished by using the model to predict performance on a different machine configuration. In addition, confidence in the methodology is further established with an independent measurement of CPI_0 using an R10000 simulator made available from SGI [7] and from direct measurement of the overall CPI of a small problem that fits in the L1 cache.

The figures below show the results in terms of overall CPI and non-overlapped memory access stall cycles. The results suggest that the ASCI applications on the Power Challenge are indeed dominated by memory access time with two exceptions (HYDRO-T and NEUT). The Origin data suggest a significant improvement in the memory sub-system over the Power Challenge. Overall CPIs have decreased by more than a factor of two and stall time is proportionately less.

CPI vs CPI stall
(Origin 2000)

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2. MIPS Technologies, Inc., "R10000 Microprocessor Product Overview."

3. Yeager, K. C., "The MIPS R10000 Superscalar Microprocessor," IEEE Micro, April, 1996, pp 28-40.

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5. Vernon, M.V, Lazowska, E. D., and Zahorjan, J., "An Accurate and Efficient Performance Analysis Technique for Multiprocessor Snooping Cache-consistency Protocols," in Proc. 15th Annu. Symp. Comput. Architecture, Honolulu, HI, June, 1988, pp 308-315.

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7. Private communication, Steve Turner, Silicon Graphics, Inc., January, 1997.

CPI vs CPI stall
(Power Challenge)