

LOW-COST EPITAXIAL TECHNIQUES
FOR SOLAR-CELL FABRICATION

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R. V. D'Aiello
P. H. Robinson

RCA Laboratories
Princeton, New Jersey

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Solar Energy Research Institute
A Division of Midwest Research Institute
1536 Cole Boulevard
Golden, Colorado 80401

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PREFACE

The objective of this work is to extend epitaxial techniques for the growth of silicon films on the lowest cost silicon substrates consistent with the material and device requirements for the fabrication of high-efficiency solar cells. The specific approaches toward this goal are:

- The characterization of several candidate silicon substrate materials to determine impurity level, doping distribution, grain boundary morphology, and defect state;
- Optimization of epitaxial growth parameters in relation to the substrates; and
- Solar-cell and device fabrication and evaluation to provide feedback relating to the epitaxial growth and the substrate quality.

SUMMARY

During the second quarter, experiments were continued on the material characterization and epitaxial growth of solar-cell structures on three grades of a candidate low-cost upgraded metallurgical grade (UMG) silicon substrate. Enough epitaxial solar cells to characterize the baseline performance of cells on these three substrate grades were fabricated and tested. With a 15- μm -thick epitaxial structure grown on the purest form of UMG substrate, an average cell AM-1 efficiency of 12.5% was obtained. Similar structures grown on the less pure multicrystalline substrate grades result in efficiencies of 9 to 10.3%. A novel way of slicing these substrates which exposes larger grain areas and results in higher cell efficiencies is described.

The application of slow-cooling and gettering to the growth of thicker ($\geq 50 \mu\text{m}$) epitaxial solar-cell structures was found ineffective. The use of alternate silicon gas sources was explored by using silane for the growth of cell structures. The initial results are encouraging and will be further pursued.

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SECTION 1.0

INTRODUCTION

1.1 BACKGROUND

Previous work [1,2] has demonstrated the feasibility and technical advantages of using chemically vapor deposited (CVD) epitaxy for the growth of silicon solar-cell structures. Silicon solar cells having nearly ideal electrical characteristics and very high open-circuit voltage were fabricated in epitaxial layers grown on high-quality silicon substrates [1]. This technique was also explored for potential application in the low-cost manufacturing of solar cells by the use of epitaxial growth in conjunction with substrates such as edge-defined film-fed growth (EFG) ribbon [3] and several forms of simply purified metallurgical grade silicon [4,5]. This latter work identified the need for a full technical qualification and the establishment of supply for the lowest cost silicon substrate consistent with high efficiency, good yield, and reproducibility of epitaxial solar-cell fabrication. The integration of low-cost epitaxial solar-cell processes with a defined low-cost silicon substrate forms the basis of this contract work.

1.2 OBJECTIVE AND APPROACH

The major objective of this contract work is to refine and apply epitaxial growth techniques to several candidate low-cost silicon substrates in order to define the growth technique and substrate combination which will allow the fabrication of low-cost and efficient solar cells. The planned approach is:

- Define and characterize several potentially low-cost silicon substrates in terms of physical, chemical, and electronic properties.
- Refine and explore suitable epitaxial growth methods in conformance with the substrate characteristics so that the resultant epitaxial layers can be used in the fabrication of high-efficiency solar cells. The efficiency goal for such cells is 14%, AM-1.
- To fabricate solar cells and diagnostic devices and to perform electronic characterizations so that the influence of the epitaxial growth and structure, as well as the substrate, can be evaluated.

Section 2.1 below describes the specific material characterization applied to the substrates selected for study. This material consists of three forms of upgraded metallurgical grade (UMG) silicon which was purchased from the Hemlock Semiconductor Corporation.* The characterization consists of physical and chemical impurity analysis involving mass spectroscopy applied to the substrates and to epitaxial layers grown on them.

*Hemlock Semiconductor Corporation, Hemlock, Michigan, a subsidiary of the Dow Corning Corporation.

The grain geometry for the multicrystalline substrate grades and a novel method of slicing these substrates which maximizes the grain area is described in Section 2.2.

Section 2.3 describes the epitaxial techniques applied to date in the growth of diagnostic and solar-cell structures.

In Section 2.3.1, the electrical characteristics of epitaxial solar cells fabricated on the three grades of UMG silicon are given and compared.

A discussion and summary of the results obtained to date are presented in Section 3.0 and plans for the next quarter of work are given in Section 4.0.

SECTION 2.0

PROGRESS

2.1 SUBSTRATES UNDER STUDY

The primary substrates which have been used in this program to date are formed from upgraded metallurgical grade (UMG) silicon obtained from Hemlock Semiconductor Corporation. This material was produced by remelting and applying chemical purification techniques to metallurgical grade silicon as obtained from an arc furnace. Three grades of such material have been studied. These grades differ in the amount of purification or upgrading applied to each, and as a result they differ both in their impurity content and crystallinity. Table 2-1 summarizes the nomenclature associated with each silicon grade, and lists the range of concentration of impurities as obtained from spark source mass spectrographic analysis.

TABLE 2-1. PROPERTIES OF UMG SILICON

UMG Grade	Crystallinity	Type	Impurities ^a (ppm)					
			<u>Al</u>	<u>B</u>	<u>P</u>	<u>O</u>	<u>C</u>	<u>Cr</u>
1S	Single Crystal <100> Orientation	p	1-4	36-71	1-5	58-170	3-47	13
2P	Large Grain Polycrystalline	p	3-40	48-150	3-11	200-240	10-36	~1
1P	Large Grain Polycrystalline	p	0.6-1	46-53	1-4	44-192	4-50	6

^aFrom spark-source mass spectroscopy.

Several spark-source analyses were conducted on the UMG substrates. Because of the variation in the precision of this method and because of the suspected spatial inhomogeneity of impurities these values are valid only in a qualitative sense.

Similar measurements were made on thick (100 μm) epitaxial layers grown on UMG and control substrates. The results show lower levels of most impurities detected; however, the sensitivity of this measurement is only of the order of 1 ppm. The data shown in Fig. 2-1, taken from reference 6, illustrates the concentration dependence of solar-cell performance for various metallic impurities in p-type silicon. It is noted that these impurities adversely affect cell performance at levels well below 1 ppm.

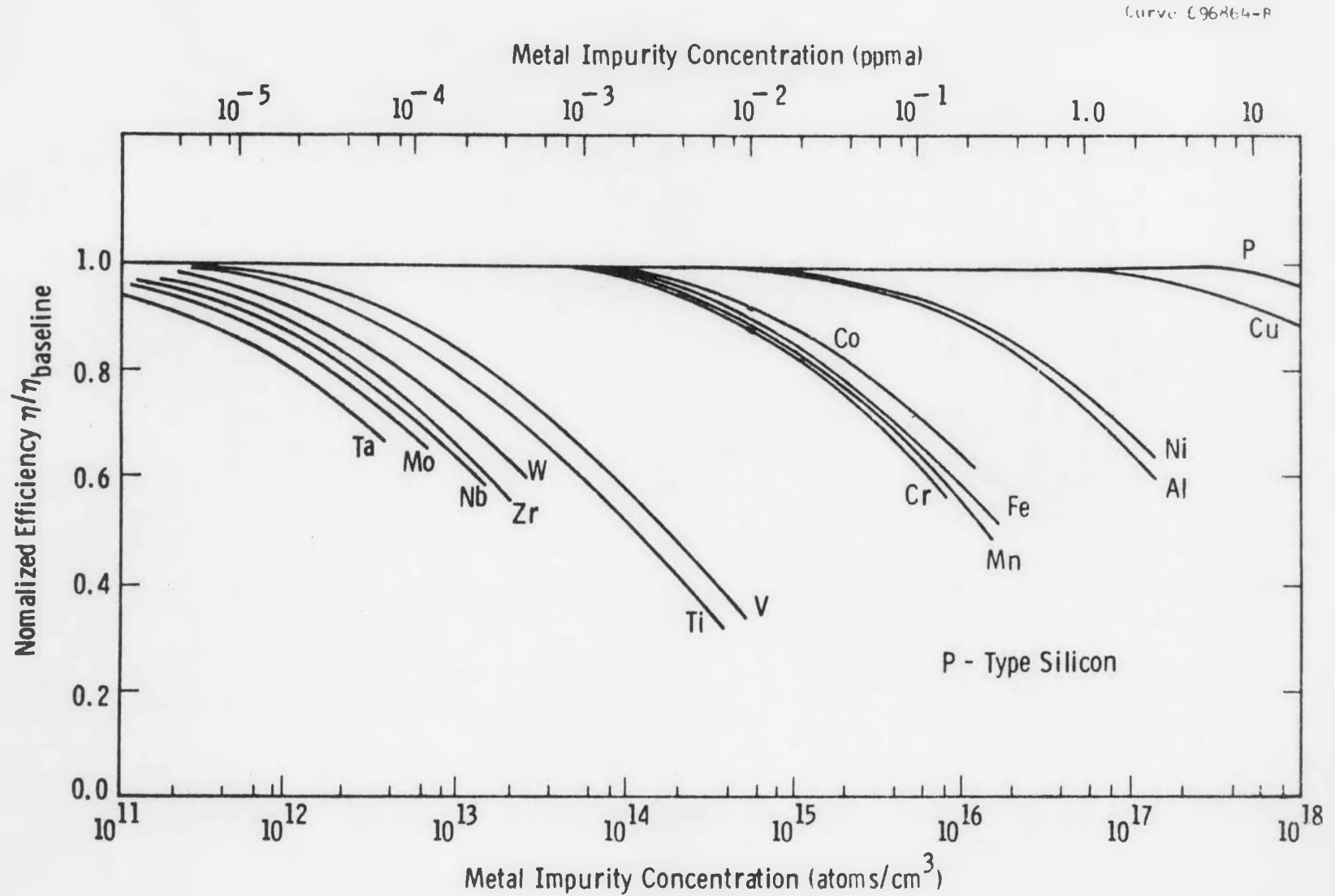


Figure 2-1. MODEL-DERIVED IMPURITY-PERFORMANCE CURVES FOR SINGLE-METAL CONTAMINANTS IN P-TYPE Si. THE CURVES FOR Mo, Ta, W, AND Co ARE CALCULATED FROM RECENT CELL EFFICIENCY AND IMPURITY CONCENTRATION DATA [6].

2.2 GRAIN BOUNDARY CONSIDERATIONS

Since grades 1P and 2P have a multigrained structure, the size, distribution, and geometry of the grains can be important in the epitaxial growth and in the final solar-cell performance. Photographs of typical sections of the grade 1P material cut both longitudinally (\parallel) and transversely (\perp) to the direction of solidification are shown in Figs. 2-2 and 2-3. For the transverse cut, the grain sizes vary from about 1 mm to 5 or 6 mm in maximum length. In contrast, the longitudinal cut exposes grains of greater length (several cm) because of the columnar nature of the grain formation in the ingot. This can be utilized to advantage in the case of epitaxial cells since the growth of the active film will replicate the surface grain geometry resulting in columnar grains which are then transverse to the original direction, but of considerably larger area. We have explored this condition by the growth and fabrication of solar cells on both transverse and longitudinally cut sections of grade 2P material. The results tend to support the advantages described above. The details of these results are given in Section 2.3.2.

2.3 EPITAXIAL GROWTH AND SOLAR CELLS

2.3.1 Baseline Experiments with UMG Substrates

We have continued growth experiments using the epitaxial procedures outlined in Quarterly Technical Progress Report No. 1 [7]. The purpose of this work was twofold: first, to generate a sufficient number of samples grown on the three UMG silicon grades to assess the range of cell efficiencies obtainable and to provide solar-cell samples for diagnostic measurement; second, to explore the effect of growth and cell performance for grade 2P material cut transversely and longitudinally to the direction of solidification.

Solar-cell structures 15 and 50 μm thick were grown on the three substrate grades and solar cells were fabricated for evaluation.

2.3.2 Solar-Cell Performance

We have fabricated a sufficient number of solar cells to evaluate performance as a function of substrate grade. A summary of this type of data is given in Table 2-2 for 15- μm -thick epitaxial structures. For comparison, the results for cells prepared on grade 2P substrates cut longitudinally or parallel to the direction of solidification are also included.

These data, exclusive of the results for the parallel cut material, lead to conclusions very similar to those given earlier based on a smaller set of samples. These conclusions are

- Aside from the slightly ($\sim -5\%$) reduced short-circuit current, the performance of the epitaxial cells made on the single-crystal grade 1S substrates is comparable to that of the control cells made on high-quality Czochralski (CZ) silicon. The average cell efficiency is 12.5% with very reproducible current-voltage characteristics. Peak efficiencies as high as 12.9% have been measured.

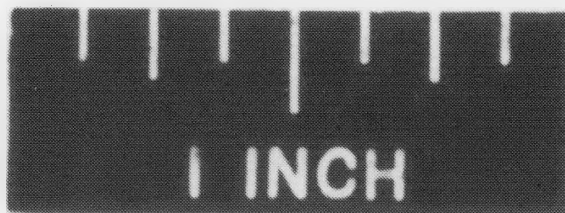


Figure 2-2. UMG SUBSTRATE SLICED PERPENDICULAR TO THE DIRECTION OF SOLIDIFICATION

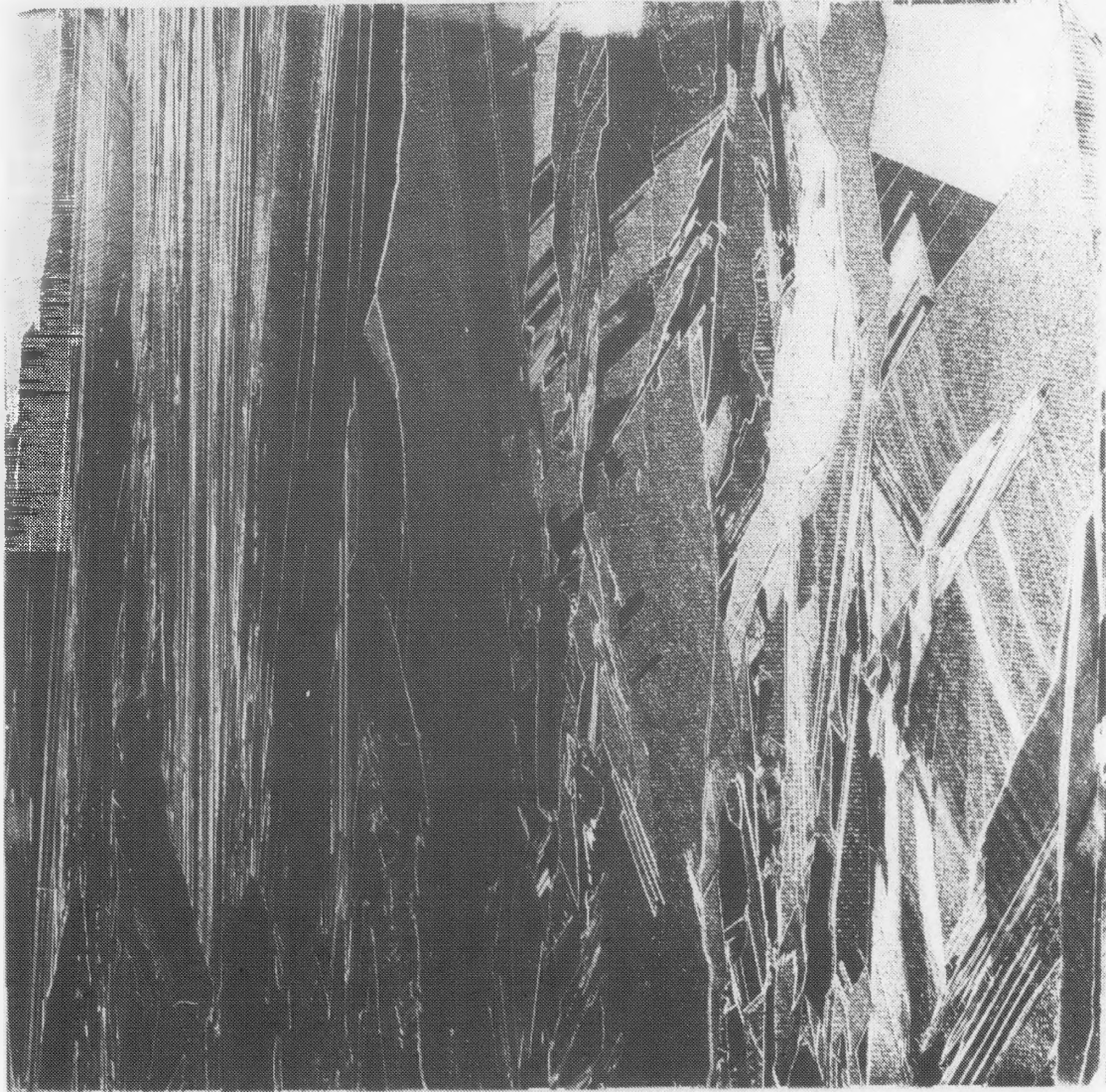


Figure 2-3. UMG SUBSTRATE SLICED PARALLEL TO THE DIRECTION OF SOLIDIFICATION

TABLE 2-2. SUMMARY OF SOLAR-CELL DATA FOR 15- μ m-THICK EPITAXIAL STRUCTURES

Substrate	Cell Area (cm ²)	J _{sc} (mA/cm ²)	V _{oc} (mV)	FF -	η (%)	Comment	
P ⁺ CZ Control	MAX	4.45	28.2	605	0.810	13.2	
	TYP	4.45	27.0	580	0.779	12.4	
	MIN	4.45	25.8	575	0.784	11.6	
Dow Grade 1S	MAX	4.45	26.5	600	0.792	12.6	
	TYP	4.45	25.9	604	0.797	12.3	
	MIN	4.45	25.7	570	0.776	11.4	
Dow Grade 1P	MAX	4.45	24.7	550	0.713	9.7	
	TYP	4.45	23.6	550	0.720	9.5	
	MIN	4.45	22.2	549	0.718	8.8	
Dow Grade 1P	MAX	0.40	23.4	560	0.801	10.1	Large grained area Many grain boundaries
	TYP	0.40	22.4	545	0.767	9.3	
Dow Grade 2P	MAX	4.45	24.8	570	0.734	10.3	\perp ^a
	TYP	4.45	23.1	545	0.729	9.2	
	MAX	0.40	23.2	570	0.730	9.6	
	TYP	0.40	23.1	545	0.729	9.2	
Dow Grade 2P	MAX	4.45	24.4	578	0.750	10.6	\parallel ^b
	TYP	4.45	23.7	552	0.760	9.9	
	MAX	0.40	25.5	565	0.791	11.4	
	TYP	0.40	23.5	570	0.745	9.9	

^a \perp = Ingot cut transverse

^b \parallel = Ingot cut longitudinally

- Performance of epitaxial cells grown on the two multicrystalline substrate grades (1P and 2P) are similar, with slightly higher peak efficiencies observed for the 2P material. The presence of grain boundaries, impurities, and defects lowers the short-circuit current and causes variations from sample to sample in the open-circuit voltage and fill-factor. However, with no special processing, an average efficiency of 9.5% was obtained, and values as high as 10.3% have been achieved.

The data for the small-area (0.40 cm^2) cells form an interesting comparison in that their linear dimensions are of the order of the maximum grain size, so that some of these cells are located in areas containing only one or two grain boundaries. In these cases, the short-circuit current, open-circuit voltage, and fill-factor tend to be higher than for cells of the same area but encompassing few grain boundaries. However, it should be noted that the typical values of efficiency for the small-area cells do not differ greatly from those of the 4.45-cm^2 cells. Scaling up to larger areas is thus not expected to result in efficiencies much lower than that already achieved for the 4.45-cm^2 area cases. Experiments to verify this for 10- to 20-cm^2 cells are planned for the next quarter.

The data in Table 2-3 for the cells fabricated on longitudinally cut substrates show higher efficiencies than the cells made on the same grade material cut transversely to the direction of solidification. This is true for both the large- and small-area cells with the highest values being associated with the small-area cells. We believe this is primarily due to the increased grain area exposed by this cut. This difference is illustrated for finished cells in Figs. 2-4, 2-5, and 2-6, where it is seen that considerably larger grain areas are obtained in the parallel cut case.

TABLE 2-3. COMPARISON OF SMALL AND LARGE AREA CELLS ON PARALLEL CUT UMG SUBSTRATES

Sample	Cell Area (cm^2)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF	η (%)	Substrate	Cut
C-1L	0.40	23.7	568	0.780	10.5	Grade 2P	Parallel
C-1R	0.40	23.2	570	0.738	9.7	Grade 2P	Parallel
C-1	4.45	23.4	540	0.725	9.2	Grade 2P	Parallel
C-2R	0.41	25.5	565	0.791	11.4	Grade 2P	Parallel
C-2L	0.40	23.0	570	0.752	9.9	Grade 2P	Parallel
C-2	4.45	23.7	552	0.760	9.9	Grade 2P	Parallel

In this case, some small-area cells are located almost entirely within a grain, while others intersect a few grain boundaries. A comparison of the cell parameters for two such cases is given in Table 2-3, with the corresponding cell samples indicated on Figs. 2-5 and 2-6.

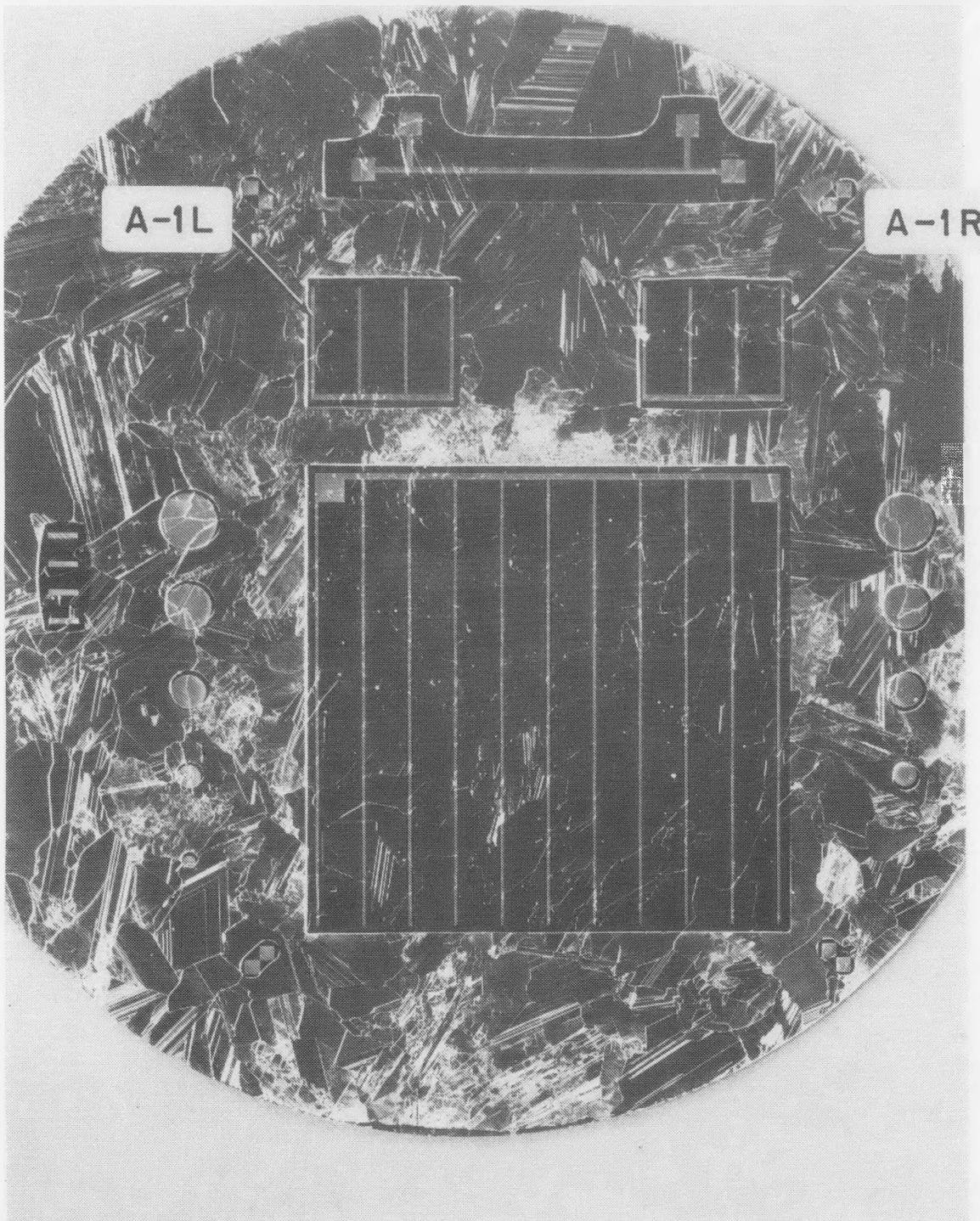


Figure 2-4. EPITAXIAL SOLAR CELL FABRICATED ON 1 CUT GRADE 2P.
(Sample A-1)

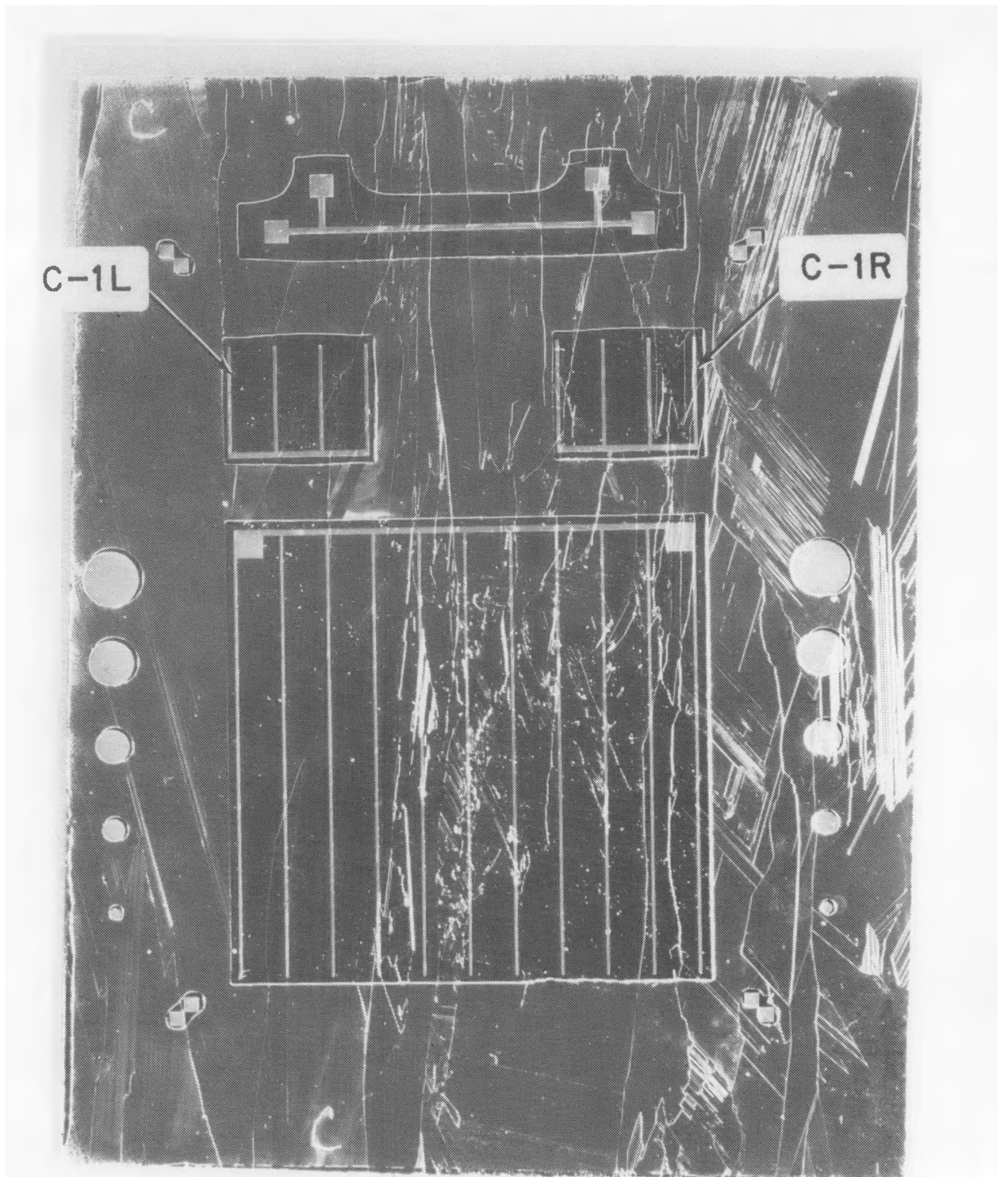


Figure 2-5. EPITAXIAL SOLAR CELL FABRICATED ON \parallel CUT GRADE 2P.
(Sample C-1)

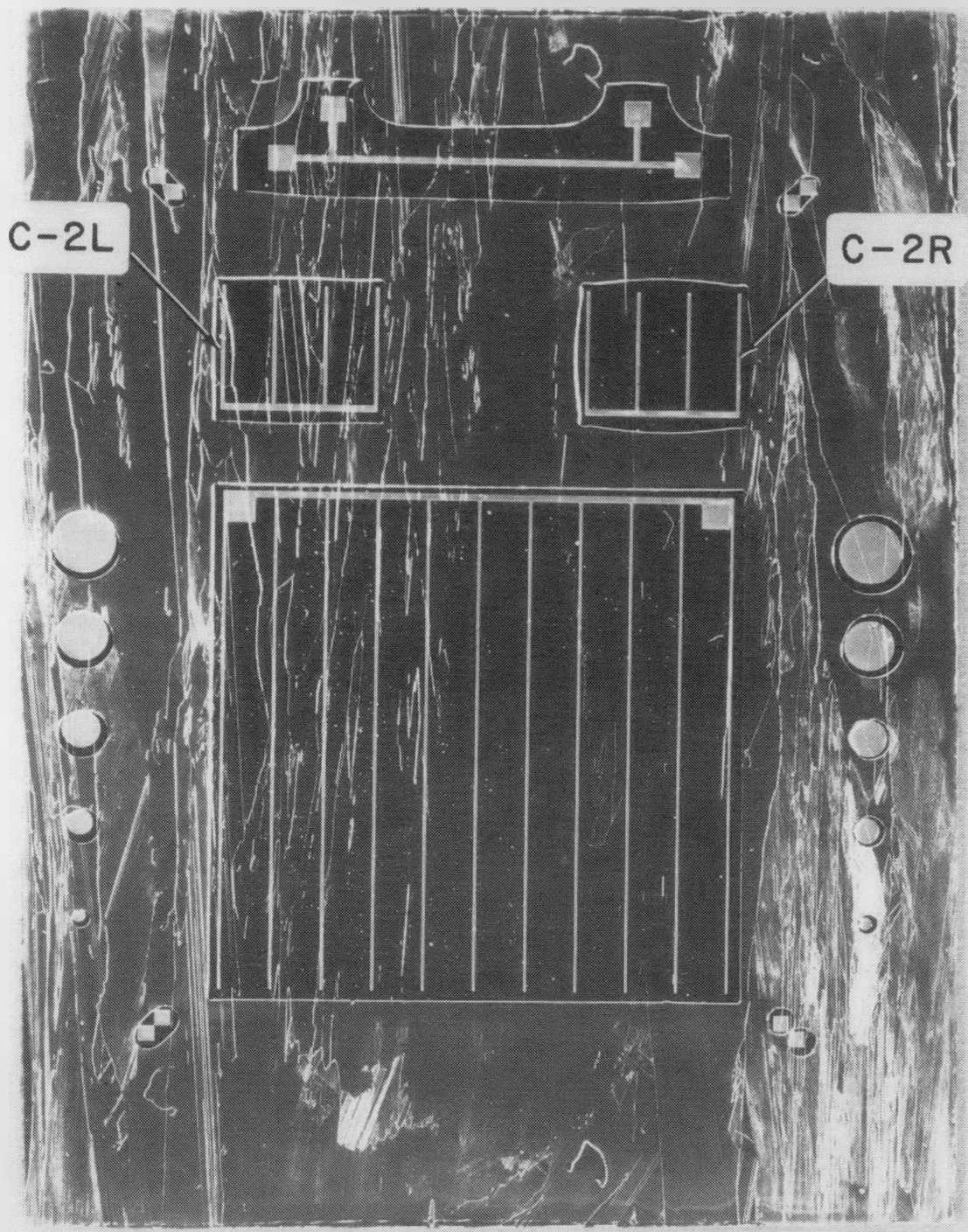


Figure 2-6. EPITAXIAL SOLAR CELL FABRICATED ON \parallel CUT GRADE 2P.
(Sample C-2)

2.3.3 Slow Cooling and Gettering

Two techniques were applied to the epitaxial process in an attempt to improve the electronic properties of the grown layer. Slow cooling from the growth temperature is a method often used to maintain or improve diffusion length in high-temperature processing of silicon minority-carrier devices. Gettering with a high concentration phosphorus source on the back of the wafers is also often employed to reduce the concentration of unwanted impurities in the active region of silicon devices.

Slow-cooling capability was added to our epitaxial reactor system by providing a voltage ramp on the power supply output to the rf generator. This allows the wafers to be cooled at a rate of 3°C/min from the growth temperature (1100°C) down to 800°C.

In separate experiments, a heavily doped n^+ layer was incorporated on the back of the substrate wafers prior to epitaxial growth. The substrate preparation consisted of a $POCl_3$ deposition on the backside of a standard p epitaxial wafer. A 10- μ m polycrystalline silicon layer was then grown over the $POCl_3$ deposition to seal the back surface and reduce autodoping effects. The front surface was then re-polished. Several n p p epitaxial structures were then grown using these substrates in order to provide some gettering during growth. The n^+ region on the back of the cell was removed by etching prior to completing the solar cells.

Both of these techniques were applied to the growth of thick (50 to 100 μ m) epitaxial solar-cell structures because these structures are more sensitive to increased diffusion length than thin (15 to 20 μ m) structures.

The results of these experiments along with the characteristics of two representative baseline cells are summarized in Table 2-4. The data for the case of slow cooling show that little or no improvement in solar-cell performance was obtained. In the cases where a $POCl_3$ diffusion-gettering was used, the resulting diffusion lengths and short-circuit currents are lower than even the baseline cases where no slow cooling or gettering was applied. A likely explanation is that the 10- μ m-thick polycrystalline layer used as a cap over the diffused region did not effectively seal the back of the wafers during the epitaxial growth. Under these conditions the diffused layer becomes a source of phosphorus which is then incorporated in the growing boron-doped layer, resulting in compensated doping in the active layer.

Since the slow-cooling resulted in no measurable improvement in the performance of cells made on UMG substrates, and because this procedure would add considerable time and cost to the epitaxial process, it will not be pursued further. $POCl_3$ or other similar gettering techniques should in principle remove unwanted impurities, and be especially desirable in the case of substrates derived from metallurgical grade silicon. The $POCl_3$ gettering experiment described above failed because of the particular method selected to seal the phosphorus-doped layer during the subsequent epitaxial cycle. More effective methods, such as the use of Si_3N_4 films, will be attempted in order to unambiguously test the effectiveness of this gettering technique. We will also concentrate efforts on simplification and improvement of the thin (15 to 20 μ m) structures since these structures are more economical to fabricate and the data (see Table 2-2) show that their performance is equal to or better than that of the thick epitaxial structures.

TABLE 2-4. SUMMARY OF DATA ON SLOW COOLING AND GETTERING

Sample	Epi Thickness (μm)	Process	QE $\lambda = \mu\text{m}$				L^a (μm)	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF -	η (%)	Substrate
			0.4	0.6	0.8	0.9						
III	50	Baseline	32	88	79	58		26.2	570	0.785	11.7	Single-crystal CZ
V	100	Baseline	-	-	-	-		25.8	560	0.785	11.0	Single-crystal CZ
E ³	50	Slow Cool	28	94	86	61	55	27.9	564	0.774	12.2	Single-crystal CZ
F ²	100	Slow Cool	31	92	74	53	48	26.2	553	0.750	10.9	Single-crystal CZ
O	50	POCl ₃	29	91	51	26	15	21.6	540	0.790	9.2	Single-crystal CZ
P	50	POCl ₃	35	97	72	45	35	24.4	550	0.784	10.5	Single-crystal CZ
MC	50	Slow Cool	42	92	76	53	50	26.3	562	0.766	11.3	Single-crystal CZ
M	50	Slow Cool	36	90	72	48	40	25.8	564	0.784	11.4	Dow grade 1S
L	50	Slow Cool	45	92	68	46	35	23.9	530	0.712	9.0	Dow grade 2P
K	50	Slow Cool	49	80	54	31	20	22.3	526	0.743	8.7	Dow grade 1P.

^aDiffusion length obtained from curve fit to spectral response data.

2.3.4 Epitaxial Growth with Silane

We have begun to explore the use of silane as the silicon source in the epitaxial growth of solar-cell structures. Silane is chemically simpler and can be lower in cost than other commonly used silicon gas sources. Also, growth with silane can be conducted at temperatures 100 to 200°C lower than presently possible with higher order chlorosilanes. This could be important in reducing the diffusion of impurities from low-cost substrates into the grown layer.

In the first experiments, baseline solar-cell structures 20 and 50 μm thick were grown on single-crystal, CZ, p^+ substrates at a temperature of 1000°C. After growth, the wafers were examined and a considerable degree of surface imperfections in the form of slip and haze was noted especially for the thicker structures. However, the solar-cell characteristics were quite good for three of the four epitaxial runs made. These data are summarized in Table 2-5. Except for run T-154, the efficiencies and cell parameters are comparable to those obtained in typical runs using dichlorsilane for the baseline cases.

TABLE 2-5. SOLAR-CELL PARAMETERS FOR SILANE-GROWN STRUCTURES

<u>Epi-Run</u>	<u>Epi Thickness</u> (μm)	<u>I_{sc}</u> (mA)	<u>J_{sc}</u> (mA/cm ²)	<u>V_{oc}</u> (mV)	<u>FF</u> -	<u>η</u> (%)	<u>Comment</u> (Surface Condition)
T-114	20.4	123	27.6	598	0.767	12.7	Slip and haze
T-115	20.1	124	27.8	584	0.776	12.6	Slip, slight haze
T-115	20.1	124	27.8	582	0.770	12.5	Slip, slight haze
T-153	50	121	27.1	570	0.761	11.8	Slip, haze and small Surface pits
T-153	50	122	27.4	575	0.777	12.3	Slip, haze and small Surface pits
T-154	50	96	21.6	520	0.690	7.7	Surface very rough and pitted
T-154	50	87	19.6	375	0.490	3.6	Surface very rough and pitted

In the next experiments, silane will be used to grow 15- to 20- μm -thick cell structures on UMG substrates.

SECTION 3.0

DISCUSSION AND SUMMARY OF RESULTS

During the second quarter, characterization of silicon substrate material and epitaxial layers was continued with emphasis placed on the lower grades of UMG silicon. Spark source mass spectrographic (SSMS) analyses were conducted on the UMG substrates and on epitaxial layers grown on them. Qualitatively, the results of these analyses show that the detectable impurities of interest for solar-cell performance are reduced in the epitaxial layer. However, the reported levels at which some of these impurities can adversely affect solar-cell performance are below the detection limit of SSMS. More sensitive methods of analyses such as neutron activation analysis or deep-level transient spectroscopy (DLTS) would have to be applied in order to obtain quantitative comparisons. Such experiments are planned for the next quarter.

In examining the geometric grain structure for the grade 2P UMG substrate, it was found that if the ingot is sliced parallel to the direction of solidification, considerably larger grain areas are exposed at the surface than if the cut is perpendicular to that direction. The epitaxial layer grown on such a surface replicates this grain structure and provides columnar grains transverse to those in the original ingot. The epitaxial solar cells made in this way exhibited the highest efficiency that we have obtained to date with this material, 11.4% for a 0.4-cm² cell and 10.6% for a 4.45-cm² cell.

Baseline experiments in the growth and fabrication of 15- μ m-thick epitaxial cells on the three UMG substrate grades were conducted on a sufficient number of samples so that a comparison of the efficiencies obtainable with our standard epitaxial process was obtained. The results show that for the single-crystal, purest grade (1S) substrates the average cell efficiency is 12.5%. This value is ~95% of that obtained when high-quality CZ substrates are used, with the 5% reduction due almost entirely to a lower short-circuit current. The results show little difference between the multicrystalline grades 1P and 2P, with a typical value of cell efficiency of 9.5%. Peak values in excess of 10% were observed for several cells on the 2P material, and as described above, when 2P ingots are cut parallel to the columnar growth direction, cell efficiencies of over 10% seem readily attainable.

Slow-cooling and gettering techniques were applied in the epitaxial growth cycle in attempts to improve the performance of the thicker (>50 μ m) epitaxial solar-cell structures. Slow cooling was found to be ineffective and will not be pursued further. Gettering techniques need further experimentation before any firm conclusion can be made.

Initial experiments were conducted in the use of alternate gas sources for the epitaxial growth. Silane was used to grow 20- and 50- μ m-thick solar cells on standard single-crystal substrates. Although more surface defects were noted with silane than with our standard process using dichlorosilane, the performance of the 20- μ m-thick solar cells was very similar to that normally obtained with dichlorosilane. The lower growth temperature (1000°C vs 1100°C) may be beneficial in the case of the low-cost substrates. Experiments are in progress to apply this silane growth technique to the UMG substrates.

SECTION 4.0

PLANS FOR NEXT QUARTER

The work planned for next quarter includes:

Task I Substrate and Materials Characterization

- Deep-level transient spectroscopy (DLTS) experiments will be conducted on diagnostic diodes which have been fabricated along with the bulk and epitaxial solar cells on the UMG substrates. The first experiments will compare the response from the devices on the UMG material with similar devices prepared in epitaxial layers on single-crystal CZ wafers.

Task II Epitaxial Growth

- Evaluate surface preparation techniques, i.e., chemical etching and/or in situ HCl etching.
- Use of silane to grow solar-cell structures on UMG substrates.
- Test the results of varying growth parameters for dichlorosilane system. Specifically, the effect of lower growth temperature from 1100 to 950°C and higher growth rate $>5 \mu\text{m}/\text{min}$ will be assessed.
- Prepare epitaxial solar-cell structures on large-area UMG and control substrates (12 to 25 cm^2).

Task III Solar-Cell Fabrication and Evaluation

- Fabricate and evaluate larger area (10 to 20 cm^2) solar cells.
- Perform detailed evaluation by laser scanning and light-spot spectral response on selected solar cells. Attention will be focused on cells in grade 2P material of both transverse and parallel cuts.
- Study the electrical (dark and illuminated) I-V characteristics of cells and diodes on grades 1P and 2P epitaxial layers.

SECTION 5.0

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