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FABRICATION AND CHARACTERIZATION OF ITO/SILICON SIS SOLAR CELLS

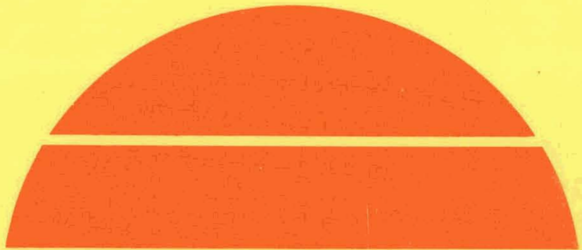
Final Report for Period October 1, 1978—April 30, 1980

By
Joel DuBow
Rajeshwar Krishnan
Rajendra Singh
Carl Wilmsen

June 1980

Work Performed Under Contract No. AC02-77CH00178

Colorado State University
Electrical Engineering Department
Fort Collins, Colorado



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FINAL REPORT

Oct. 1, 1978 → April 30, 1980

Joel B. DuBow - Principal Investigator

June 1980

Colorado State University
Electrical Engineering Dept.
Fort Collins, Colorado 80523

Written By: Joel DuBow, Rajeshwar Krishnan
Rajendra Singh, and Carl Wilmsen

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ABSTRACT

The objectives of this research were to optimize the performance of ITO/polycrystalline silicon solar cells, identify performance limitations, identify major stability problems which would inhibit terrestrial application of these devices, evaluate the impact of indium supply and price on terrestrial applications, and evaluate the economic viability of ITO sputter deposited solar cells. These goals were successfully achieved during the course of this multipronged effort.

Both area scaling with efficiency maintenance were achieved by process modifications including surface preparation and in-situ passivation techniques. Indium tin oxide on Wacker polycrystalline silicon solar cells were fabricated which achieved 13.7% efficiency for 11 sq. cm. devices. Typical open circuit voltages were 0.525 volts, short circuit currents, 34 mA/cm^2, and fill factors of 0.75.

In the course of this project, three device measurement techniques which assisted in improving cell efficiency and which have broad applicability to all photovoltaic devices were introduced. These were automated admittance and surface state analysis, noise spectral density analysis, and automated I-V and C-V analysis. These measurements were combined with Auger/ESCA, EBIC and flying spot scanner, and other measurement techniques to identify grain boundaries, intragrain defects, edge leakage, and interface losses which were subsequently alleviated through process improvements.

A study of accelerated aging did not reveal any degradation mechanisms which would inhibit large scale terrestrial applications of these cells. However, further study is required to firmly establish long term device stability. Indium availability is such that production could be increased many fold from existing mine tailings and the price increased many fold before a significant impact on solar cell price would be obtained. There is some economic advantage for the sputter deposited fabrication technology used here, primarily arising from reduced antireflection coating and metalization requirements, over p-n junction technology. However, evidence exists which indicates that sputter deposited ITO/SIS cells could attain improved performance and stability on highly defected silicon substrates and on advanced materials. It is concluded from this work that prototype production of cells and modules based on this technology would be warranted in the near term.

1. INTRODUCTION

This report describes the research done under SERI subcontract #XS-9-8232-1. This project was a systematic investigation of indium tin oxide (ITO) on silicon solar cells with a view towards optimizing their performance and evaluating efficiency loss mechanisms and performance limitations. The focus was on polycyrstalline silicon substrates. Since indium tin oxide based solar cells have demonstrated considerable promise as an alternative to p-n junctions for large scale terrestrial photovoltaic applications, a secondary goal of this research program was to evaluate the stability of these cells, their economic viability using the LSA methodology, and the impact of indium price and supply on the viability of ITO based solar cells for terrestrial applications.

During the course of this research program all of the above questions were successfully addressed in detail. None of the performance limitations examined appeared fundamental. Indeed, efficiencies of ITO/silicon devices fabricated using neutralized ion beam sputtering technology proved competitive with p-n junctions fabricated on comparable material. In the course of this investigation, efficiency limitations on presently fabricated devices were uncovered and processing steps modified to overcome these limitations. The nature of the ITO/silicon interface was studied in detail compositionally, structurally, and electronically. It was found that a thin interfacial layer of SiO_2, with a small grading layer, did exist and was critical to the functioning of the device.

Degradation studies showed that ITO based cells degraded approximately as p-n junction cells do in the dark. While no fundamental degradation mechanisms were discovered for illuminated cells, the question of lifetime in the field under illumination and temperature cycling has not yet been answered.

The supply of indium is such that it is a biproduct of zinc and

copper refining and, for the amount of indium required for large scale terrestrial applications, supply nor price did not prove a limitation under a wide range of possible scenarios. Indeed, the supply of indium can be increased by over an order of magnitude without mining additional ores. Also, an analysis of the economic viability of sputter deposited ITO/silicon solar cells indicates that, assuming DOE LSA goals are met for materials and substrates, they will be competitive with p-n junction cells using technology presently envisioned.

The following report is divided into sections analyzing substrate quality, device fabrication, analysis of the ITO/silicon interface, device performance, device analysis, device stability studies, and process economics. The results of each of these sub-investigations provided insight into the modifications required for the fabrication process which ultimately led to the high efficiencies reported.

The first section summarizes a study of the localized response of the solar cells Flying spot scanner and EBIC study of the substrates indicated that the two techniques gave essentially identical information, with different features highlighted in each technique. A key conclusion derived from this study was that a grain boundary reduces the output of a solar cell only in a small region surrounding the boundary. This proved consistant with a double depletion layer model of a grain boundary proposed by recent authors. It also indicated that intragrain properties, as exemplified by etch pits and dislocations intersecting the interface, occupied more geometric area in medium to large grain size material than did grain boundaries. Therfore, passivation of surface defects would be just as significant in improving junction quality as grain boundary passivation. These results guided us in our choice of surface preparation and hydrogen annealing techniques.

The fabrication sequence attempted to integrate the results of substrate and finished device measurements, along with interfacial analyses derived from cells and specially fabricated devices. Optimization of the process involved a careful study of sources of contamination within the system and proper substrate preparation along with the use of reactive gas annealing during substrate milling. Using these modifications, along with multilayer metalizations, 17.6 sq. cm active area devices were fabricated with typical open circuit voltages of .525 V, short circuit currents of 32.5 mA/cm^2 and fill factors of .77. Devices were routinely fabricated with active area efficiencies of 12.5 to 13.7%. Metalization proved more complicated than originally envisioned. Conventional metalizations had series resistance, adherence, and heat cycling problems. Finally, appropriate front and back surface metalization were achieved and, near the conclusion of the contract period, grid pattern and area optimizations were being developed.

A detailed study of the ITO/SiO_2 interface established that iron, aluminium, or tantalum impurities severely degraded device performance. The existance of an SiO_2 layer was clearly established. Also, the structure of that layer, which consisted of a thin transitional region (4 or 5 angstroms) followed by a layer almost entirely SiO_2 was established. Silicon monoxide was not detected in the interface. The oxygen depth profile detected the existence of a transition layer. The kinetics of oxidation at reduced pressure and on sputtered surfaces was investigated, and it was found that the sputtered surface does indeed oxidize more readily than a chemically etched surface. The rate of oxidation was measured as a function of oxygen exposure, and the results used to guide the growth of the interfacial oxide region in our fabrication.

The next chapter describes the development of three novel techniques for evaluating solar cell performance which supplemented conventional electrical and optical sutdies of the device. These techniques were: automated solar cell analysis; an automated admittance analysis; and measurement of noise spectral density versus temperature. The automated analysis system digitally recorded the I-V and C-V curve and extracted the primary solar cell performance characteristics along with barrier heights and saturation current densities. The capacitance-voltage analysis also extracts barrier heights and doping profile around the junction.
The network analysis system provides a measurement of the capacitance and conductance as a function of bias, frequency, and temperature. From these measurements, plots of surface state density versus energy may be obtained. These in turn, are used to evaluate the effect of processing variations on interfacial properties at the ITO-silicon interface. The speed and accuracy of the system permitted it to be used as an integral part of the fabrication and analysis process. Previously used techniques were so slow as to preclude measurement of any significant number of devcies. The temperature dependent noise spectral density test proved a useful reliability estimator for p-n junction devices in a previous investigation in the Principal Investigator's laboratory. This test was applied to various solar cells. While temperature dependent noise spectral density does not correlate with device efficiency, it did correlate with irregularities in the reverse current voltage curve and with variable failure rates under accelerated thermal aging. While promising, the test still required statistical validation.

The next chapter describes the results obtained from the solar cell

fabrication phase of the program and outlines the alterations and improvements in cell performance as a result of various process changes and improvements. During this contract period, cell performance improved substantially, particularly on polycrystalline substrates. Defect passivation with hydrogen and improved fabrication procedures reduced the edge leakage problem seen in earlier devices. Scaling to large areas, with attendent decreased peripherey-to-area ratios, further reduced edge effects. Large area devices showed virtually no evidence of these effects, which had plagued the earlier, smaller area devices. Surface preparation and hydrogen annealing techniques significantly improved the performance of the cells on polycrystalline silicon. Since ITO has different surface morphological properties than diffused silicon layers, obtaining optimized grid patterns and adherent grids took some effort. By the end of our research program, progress was being made in grid optimization, but the grids still occupied 15 to 20% of the cell area. However, despite the fact that ITO forms an antireflection coating on silicon, it is estimated that another antireflection coating layer would improve efficiency by a further 10%. Also, the pefection of solder dipping technology and the development of optimized grids with bounding pads which facilitate device-to-device interconnections would move the technology even closer to commercialization.

A critical question that needed to be answered was whether th ITO/SIS cells degraded similiarly to tin oxide/silicon solar cells. Our study of thermally accelerated aging indicated that the shelf life in the dark would be quite long and that there did not seem to be any significant reliability problems arising from thermal aging in the dark. Preliminary measurements on life evaluation under illumination did not reveal any major degradation mechanisms, but were inconclusive as to whether there were any open circuit voltage reductions similar to, but smaller

than, those observed in tin oxide cells. While long term stability has not been conclusively established, rapid degradation and major instabilities either in the dark or under illumination have not been observed either.

The final chapter discusses the economics of ITO/SIS cell fabrication in the context of MIS and Conductor-Insulator-Semiconductor (CIS) cell structures based upon polycrystalline and amorphous silicon. It is found that performance on polycrystalline, amorphous, and highly defected structures will be more of a factor in determining the utility of SIS structures for terrestrial applications than will fabrication economics and indium supply. Economically, the ITO/SIS structure, even using vacuum fabrication, appears competitive with and slightly less expensive than p-n junction structures. Indium is available in enough supply to provide the raw material for the small amount of ITO required.

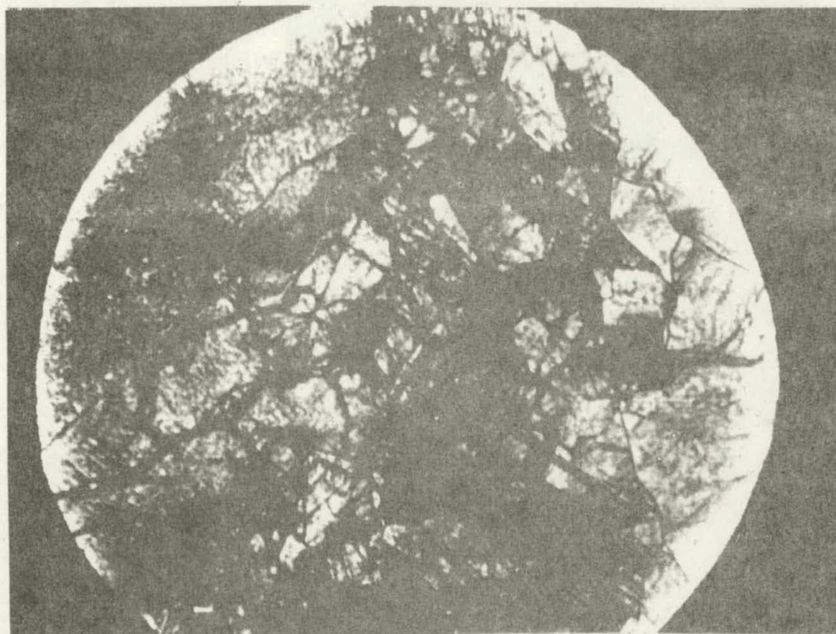
The major conclusions derived from this work are enumerated in the final section. A list of publications that originated from this program and students who worked on this project conclude the report.

2. POLYCRSTALLINE SILICON CHARACTERIZATION

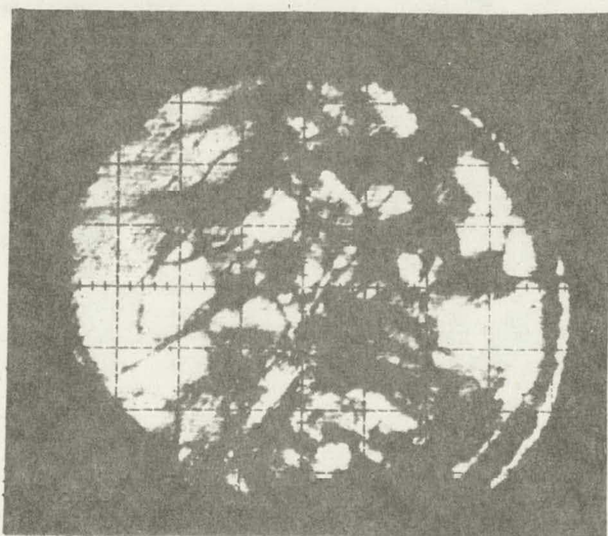
The quality of the bulk polycrystalline material plays an important part in the efficiency of solar cells. This quality can be measured in many ways, many of which yield information which averages the results over the entire cell. We have chosen to investigate the local response of the solar cells and relate these measurements to the properties of the substrate.

2.1. EBIC and SLS Techniques

For this research, the electron beam induced current (EBIC) and scanning light spot (SIS) techniques were employed. EBIC utilizes a scanning electron beam while the SLS scans a light spot. Both of these techniques have their advantages and disadvantages. EBIC yields a response which is approximately the same as the photoresponse since the minority carriers are generated near the cell surface for both techniques. This is demonstrated in Fig.2.1which illustrates the EBIC and scanning light spot (SLS) (using 6328Å) response maps for the same ITO/Monsanto cell. Note that the major features are the same in both but that the resolutions and detail of the EBIC map is much greater. The SLS resolution can be improved to that of the EBIC but the field of view is greatly reduced. In order to use the EBIC and SLS techniques requires a junction to collect the generated minority carriers. A junction was obtained by depositing a 3000Å layer of the transparent conductor indium tin oxide. For EBIC a thick metal, such as Al can be used but the SLS requires a material transparent to light. Figure 2.2illustrates other modes of displaying the SLS response maps. The intensity modulated mode of Fig. 2.2b allows easy location of surface features with some quantitative information.

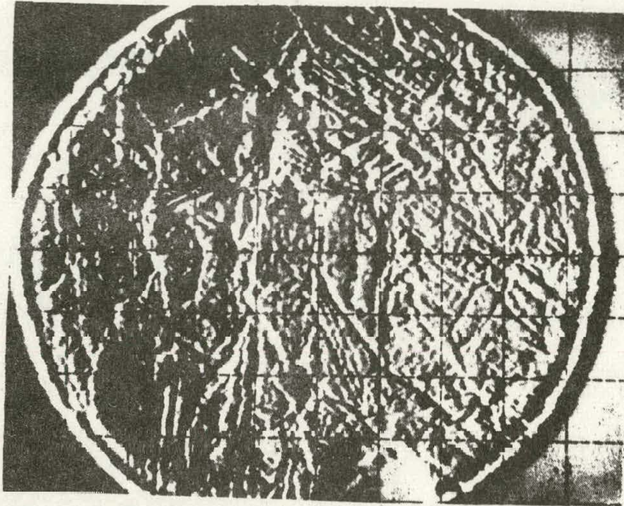


(a)

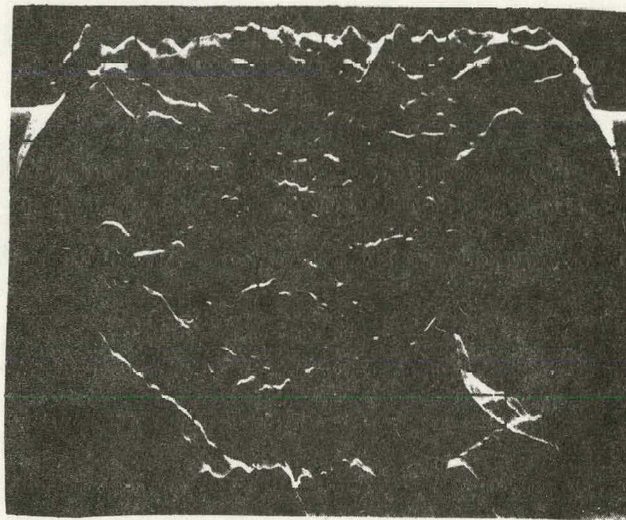


(b)

Figure 2.1.: Comparison of a) EBIC and b) SLS response, ≈25X



(a)



(b)

Figure 2.2: SLS maps of polysilicon solar cells a) capacitance coupling, z modulating; b) Y modulation with a very low frequency ramp voltage for the vertical mirror drive.

The map of Fig.2.2a utilizes capacitive coupling which differentiates the signal and hence intensifies the local changes in response. The y modulated mode map shown in Fig.2.2b yields the best quantitative measure. Similar types of displays are available with EBIC.

The resolution of SLS is determined primarily by the size of the light spot. The resolution and depth of beam penetration of EBIC are determined by the energy of the beam and the density of the material. This is usually discussed in terms of the electron range or the interaction volume. Fig. 2.3 plots the electron range vs. beam energy for a silicon substrate. Note that at 30 keV, $R \approx 8$ μm and at 5 keV $R \approx 0.3$ μm. Thus the lower the energy, the greater the spacial resolution and it would appear that lower beam energy is the more desirable. However, there are two other effects to be considered. First, the EBIC signal decreases drastically with beam voltage. Therefore the signal to noise ratio becomes poor below 15 keV. Second, the depth of sampling changes with beam energy. This has both good and bad features. Fig. 2.4 shows grain boundaries observed with beam energies from 15 to 30 keV. Note that the width of the grain boundary appears to increase greatly as the beam energy is increased. Also in Fig.2.4 note the gray grain boundary marked A and the single EBIC trace. Grain boundary A has a smaller dip in the EBIC signal and therefore gray. This is explained in terms of the location of the grain boundary with respect to the substrate surface. Fig. 2.5 shows both an EBIC and secondary electron (SE) mode photomicrographs of the area shown in Fig.2.4. In the SE photo, the "dark" grain boundary is clearly seen. However, the gray grain boundary is not observed. Fig. 2.6.shows a SE photo of the same area after etching away

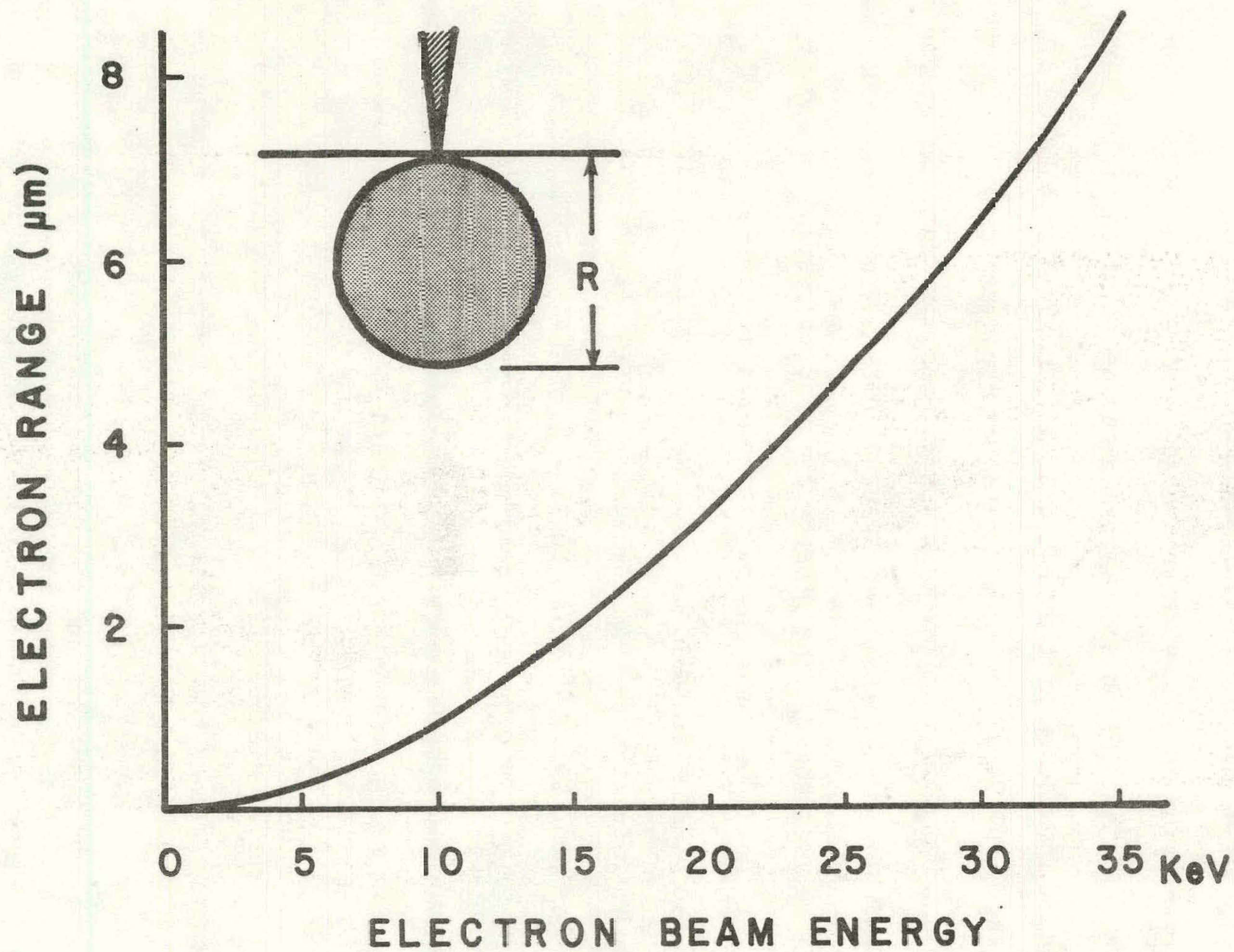


Fig. 2.3. Electron range in silicon vs. beam energy

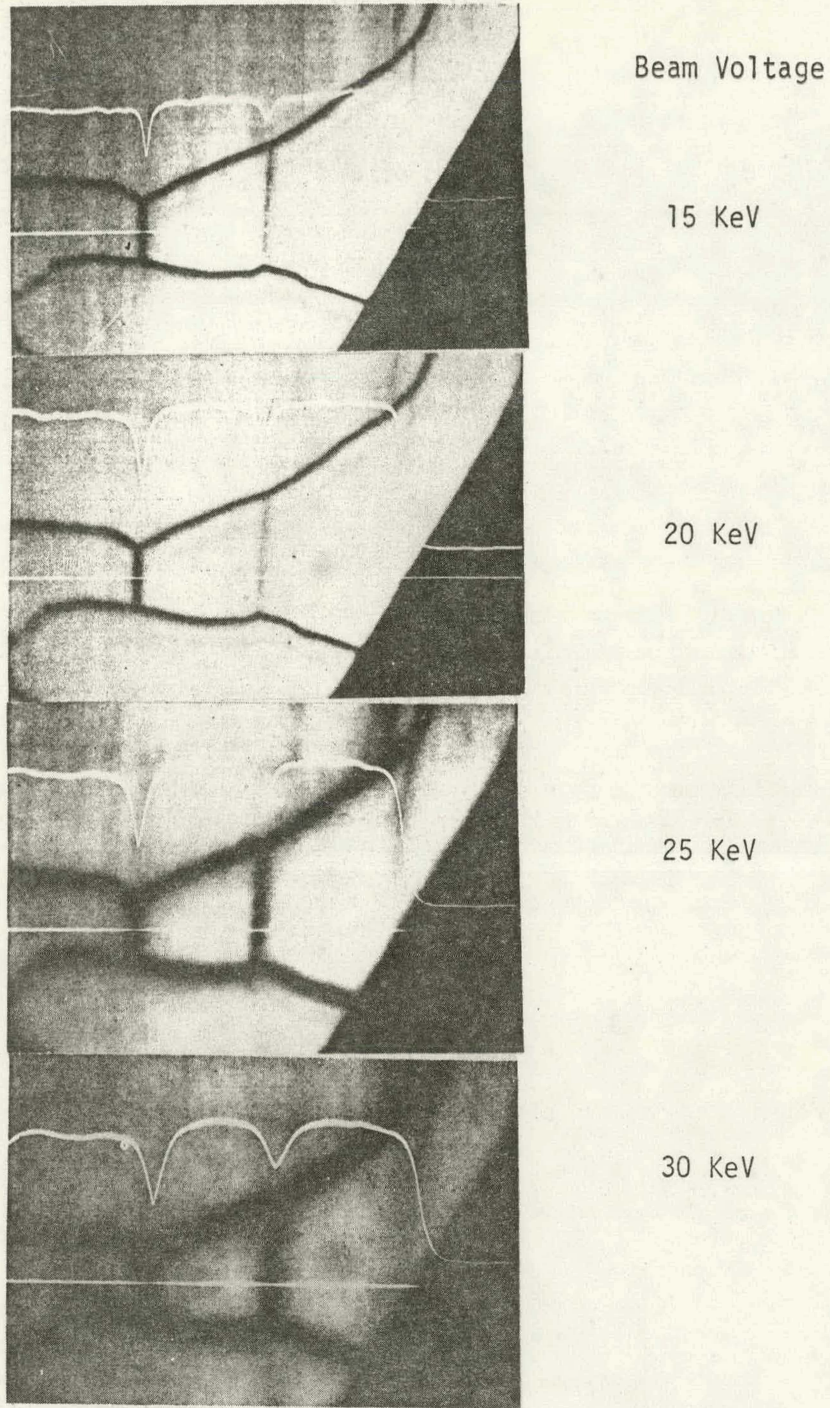
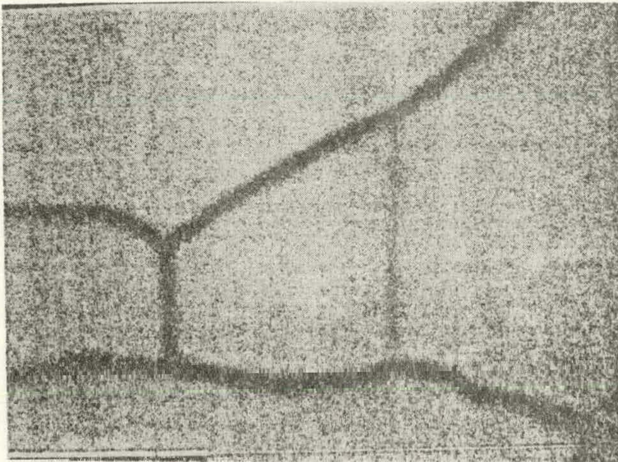
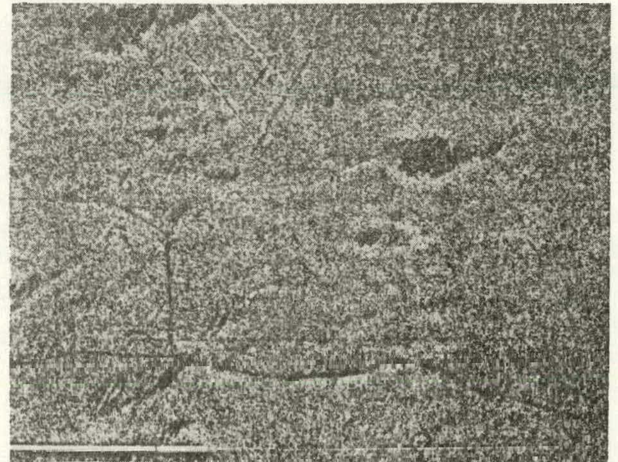


Figure 2.4. EBIC micrographs using different primary beam energies, 300X.



EBIC Mode

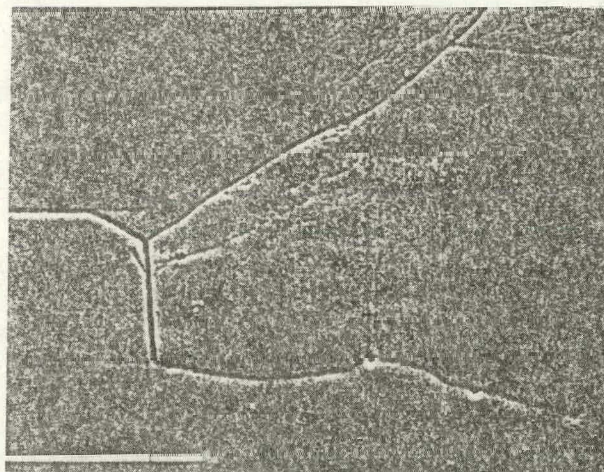
15 KeV, 300X



Secondary Mode

15 KeV, 300X

Figure 2.5 Comparison of EBIC response and surface topography. Note the absence of a surface feature corresponding to the gray grain.



Secondary Mode

15 KeV, 300X

Figure 2.6. Surface topograph of the cell area of Fig. 4 after etching the silicon surface 1.7 μm.

1.7 μm of the surface. Note that the gray grain boundary is now visible, indicating that the grain boundary starts below the surface. This is illustrated more dramatically in Fig. 2.7. (a-e).

B. Grain Boundaries

Much of the previous research on polycrystalline materials assumed that the intragrain region is of reasonable quality. In this section we show that this assumption is not always justified. In this section we use the EBIC technique and calculations to show that grain boundaries do not reduce the current significantly beyond a few microns from the grain boundary. Figs. 2.8-2.10 illustrate this experimentally.

An EBIC map of a part of a Monsanto polysilicon solar cell is illustrated in Fig. 2.8. The dark region in the left hand corner is due to the shadow of the electrode contact. The high magnification EBIC map of the "V" shape region from the center of the map is given in Fig. 2.10 which indicates that the region outside the "V" has no noticeable grain boundaries although a few small defects are present. It is also obvious that there are no significant defects inside the "V". The EBIC response from the indicated scans 1 through 6 is given in Fig. 2.10 which shows the electron beam position vs. current response along the lines of Fig. 2.9. It is seen that the response near a grain boundary is reduced for only a short distance. However, when grain boundaries are close to each other the response between them is greatly reduced. Later it is shown that grain size may not be the dominant mechanism which reduces the overall photoresponse of a cell if the grain size is larger than 10 μm. However, regions containing a high density of grain boundaries and other defects showed a reduced response.

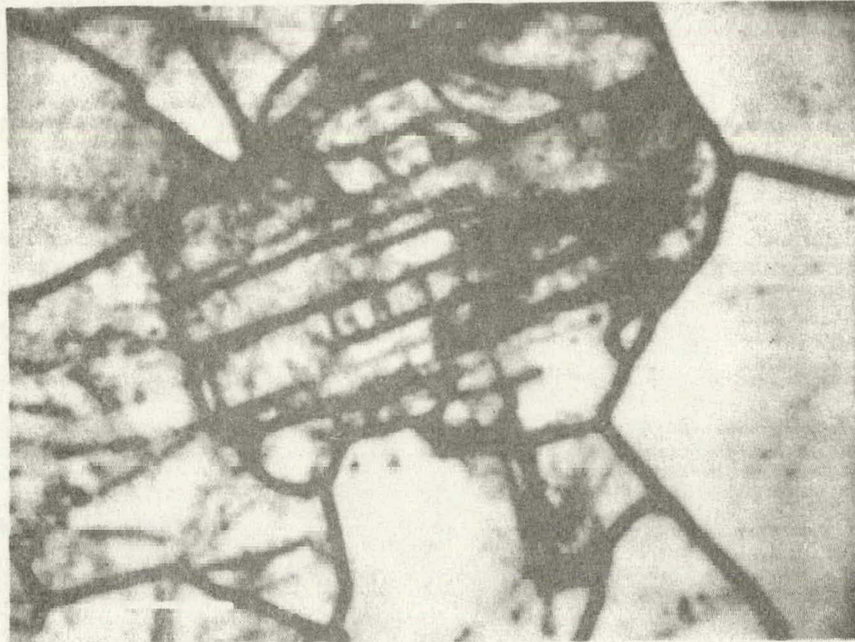
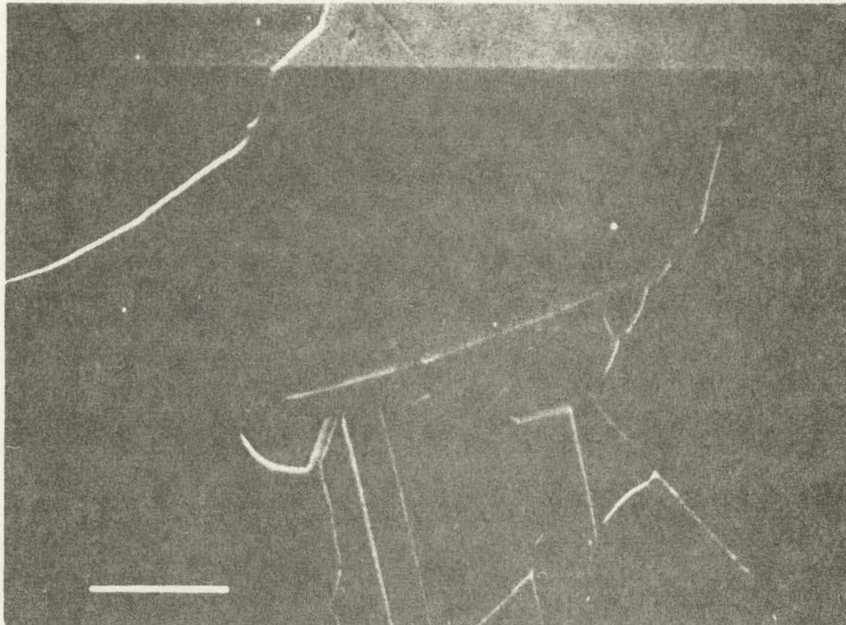


Fig. 2.7a EBIC micrograph (25 KeV, 165X) of a polysilicon solar cell. The grain boundaries appear to be dark or gray lines.



↑ (b) 15 sec

↓ (c) 45 sec

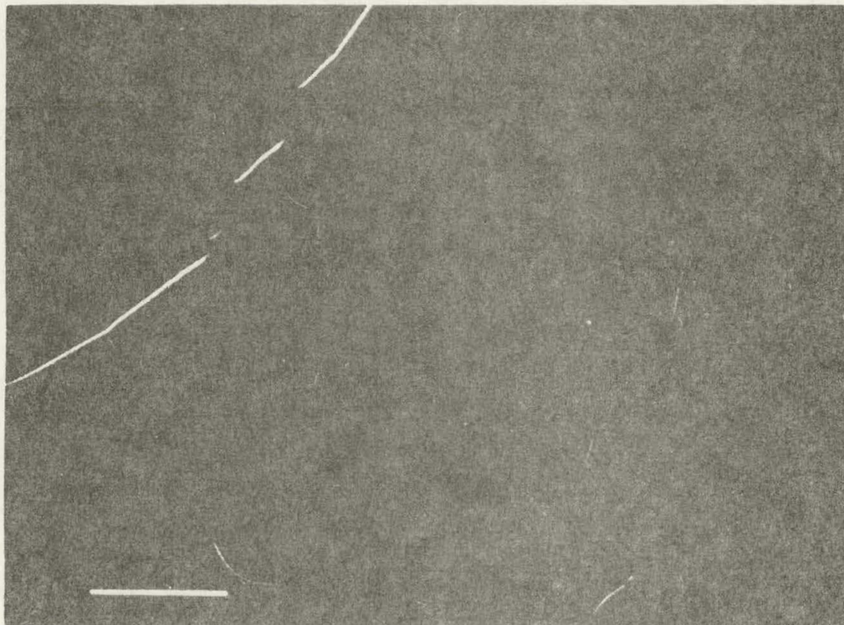
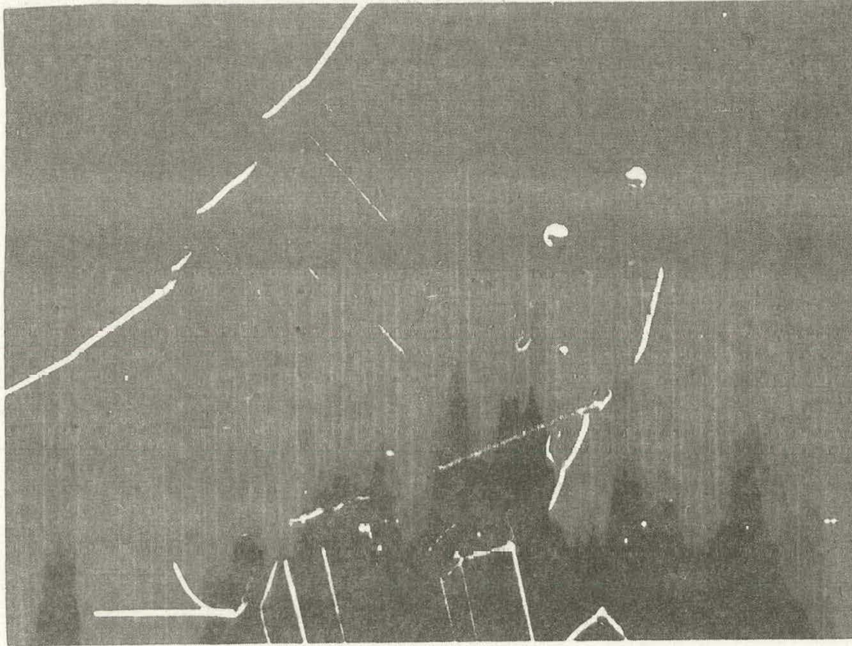


Fig. 2.7b The secondary mode micrographs of the same region of Fig. 4-1 obtained after the etching for (a) 15 sec, (b) 45 sec, (c) 90 sec, and (d) 150 sec.



↑ (*d*) 90 sec

↓ (*e*) 150 sec

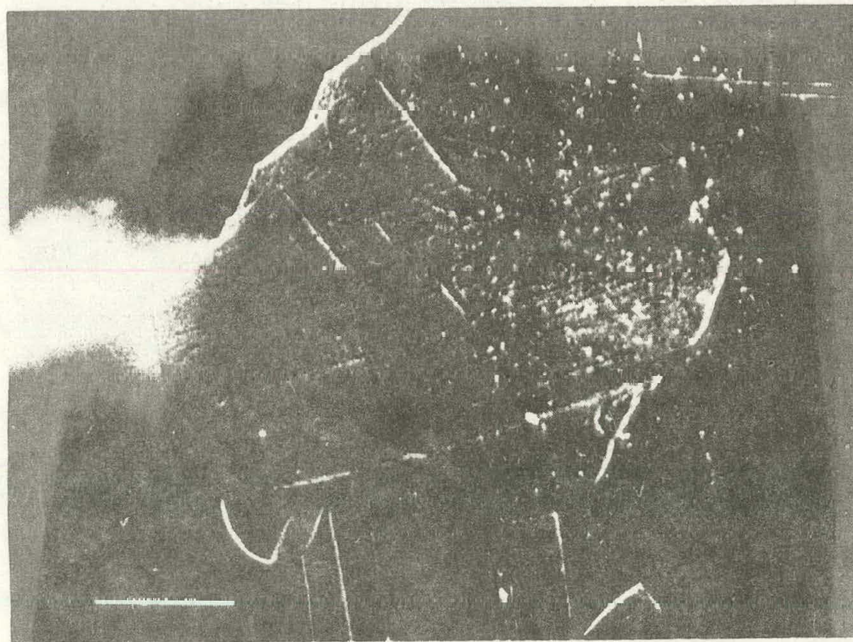


Fig. 2.7.

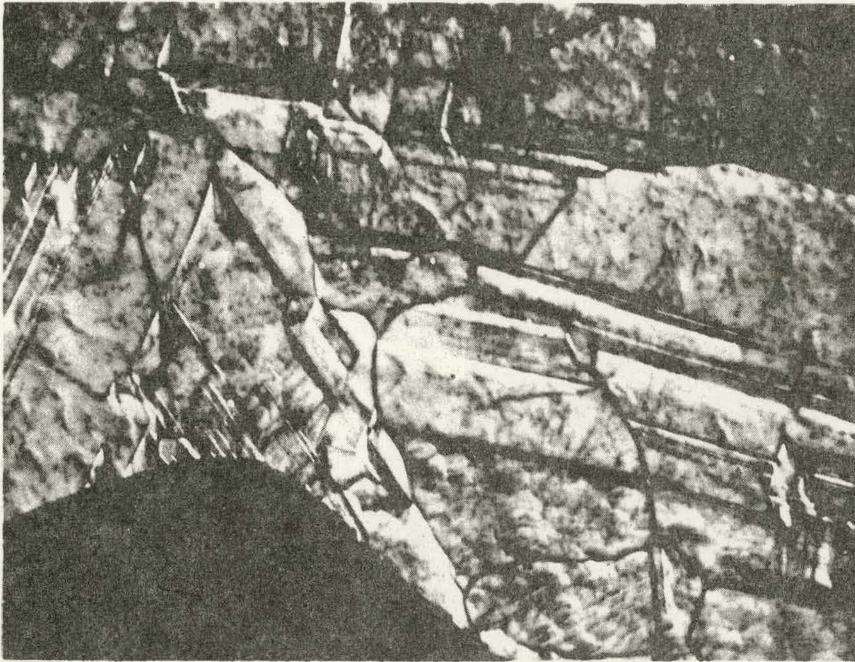


Fig. 2.8. "V-shape" grain boundary intersection is seen in the middle of the EBIC map.

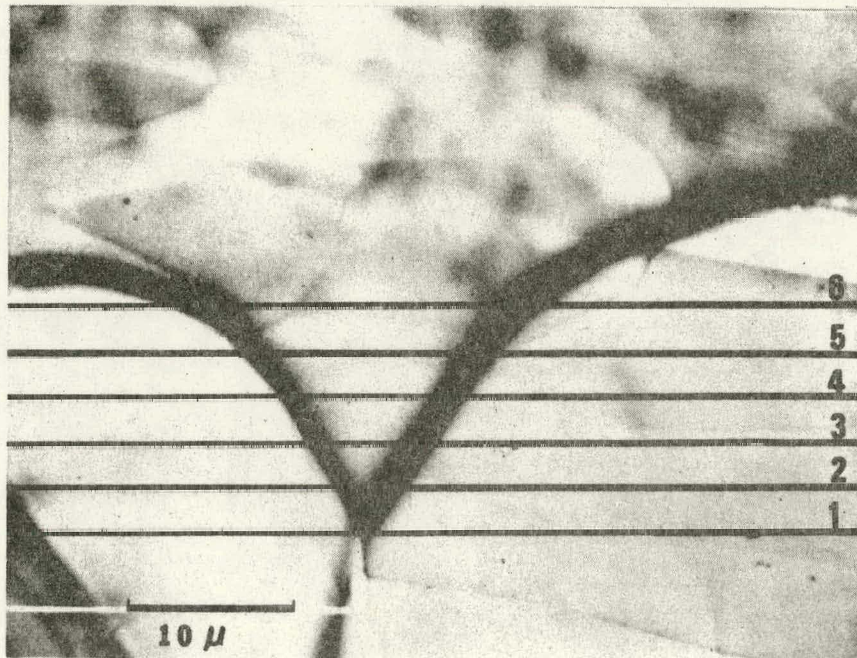


Fig.2.9. The high magnification EBIC map of the "V-shape".

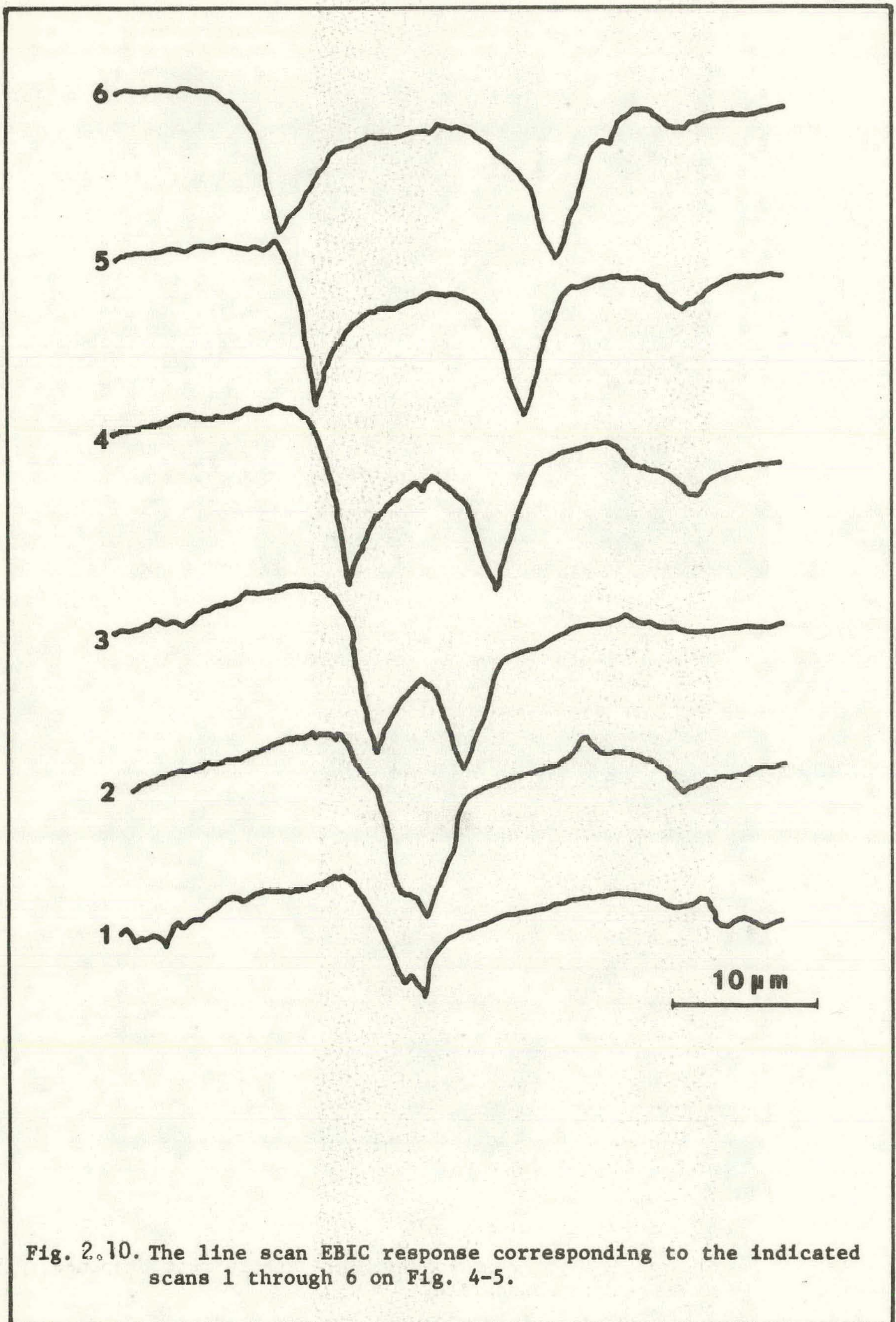


Fig. 2.10. The line scan EBIC response corresponding to the indicated scans 1 through 6 on Fig. 4-5.

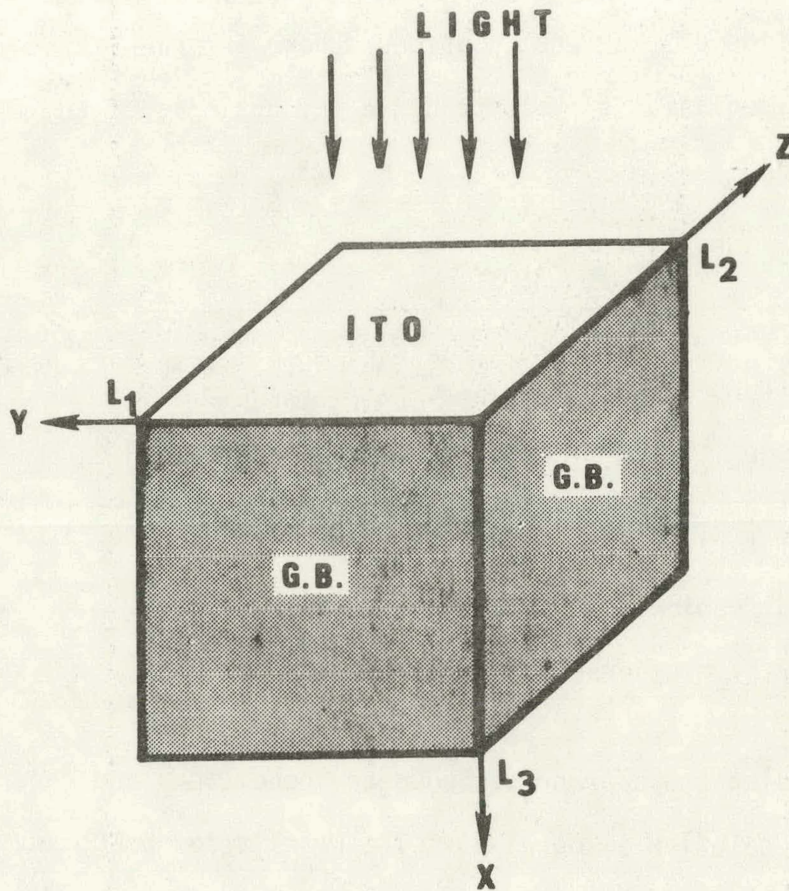


Fig. 2.11. The grain model used to calculate the current response around grain boundaries.

In order to better interpret these EBIC results, a theoretical calculation was performed. For simplicity, the carrier generation due to the electron beam in the bulk is assumed to be that of a uniform monochromatic light illumination. Though this assumption may produce a quantitative difference, the analysis should be accurate enough to explain the qualitative behavior of the grain boundaries. The grain configuration of the model considered here is shown in Fig.2.11. The continuity equation for electrons in the grain is of the form:

$$D_n \nabla^2 n - \frac{n - n_o}{\tau_n} = - G_L(x,y,z)$$

where

n = minority carrier concentration (electron for the case of ITO/p-Si)

n_o = equilibrium minority carrier concentration

τ_n = lifetime of minority carrier in the equivalent single crystal material

D_n = diffusion coefficient

$G_L(x,y,z)$ = generation rate

By using the appropriate boundary conditions and generating function, a numeral solution is obtained. The results for a 10μ and 30μ grain size and a diffusion length of 35μ are shown in Fig.2.12. These calculations show that for a diffusion length of 35μ, the photoresponse is ≈90% of its maximum at 10μ from the grain boundary. Thus, most of the generated carriers are collected by the surface junction before they can diffuse to the grain boundary. At a given point, for planar boundary, one-half the carriers are moving towards the grain, and one-half are moving away from it. Of the one-half moving towards the boundary, the transport equation solution indicates that the majority of them reach the function due to geometric generation depth profiles and velocity profiles.

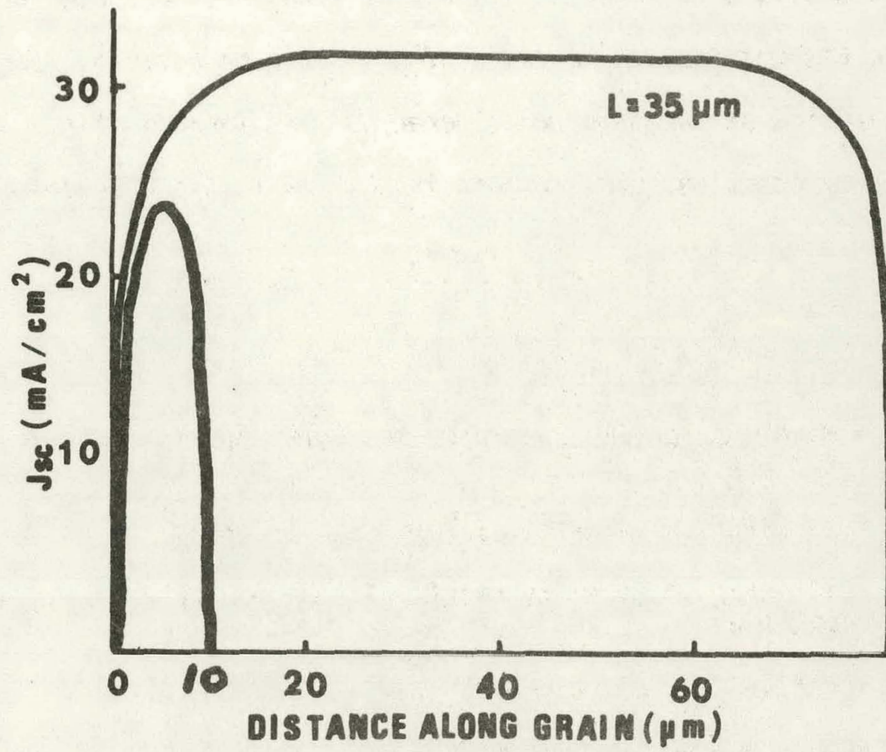


Fig. 2.12. Theoretical curves for current density vs. distance for two grain boundary separations. (a) 10 µm. (b) 80 µm.

C. Intragrain Affects

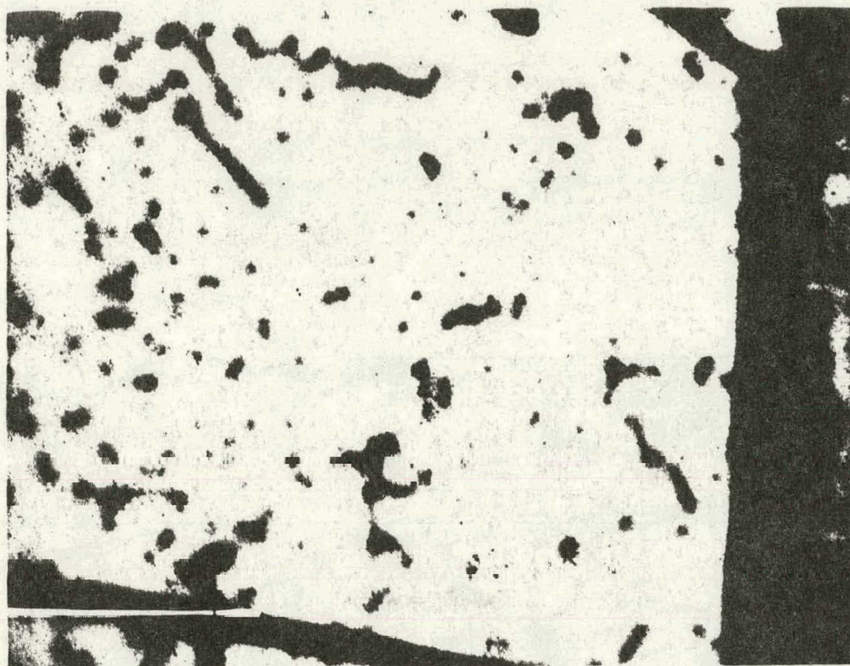
The intragrain quality of Monsanto float zone refined and Wacker cast polysilicon materials were examined with EBIC.

Fig. 2.13. illustrates the EBIC response from a portion of a cell made with a Monsanto polycrystalline substrate. The grain boundaries are clearly seen as dark lines which indicate low response. The grain size appears small in some regions but large in others. In addition to the grain boundaries, the EBIC map shows small dark spots whose density varies across the cell. In some large grain regions, the dark spots are dense and these appear to dominate the local photoresponse. Two regions of the cell of Fig 2.13were examined more closely as shown in the higher magnification EBIC maps of Fig.2.14. Few grain boundaries are seen in these EBIC maps but there is a high density of dark spots. Region B has a much higher density of dark spots than does Region A.

Etching away the ITO and then etching the silicon surface with a Dash etch for 30 min. reveals many triangular etch pits as shown in Fig. 2.15. The triangular etch pits indicate the presence of edge dislocations which intersect a <111> surface at near normal incidence. X-ray diffraction studies indicate that the crystallites are indeed oriented <111>, Fig. 2.16. Using a transparent overlay, it was determined that there is a one-to-one correspondence between the EBIC dark spots of Fig2.14.and the etch pits of Fig. 2.15 thus indicating that dark spots of the EBIC map are caused by recombination at active dislocations in the intragrain regions of the Monsanto polysilicon.

A similar study was carried out on Wacker polysilicon cells as illustrated by the EBIC map of Fig.2.17. It is observed that the grain size is much larger than that of Monsanto polysilicon. The magnified EBIC

Fig. 2.13. The EBIC map of a cell made from a Monsanto polysilicon substrate. Two regions (A,B) were selected for etch pits studies.



↑ (a) Region A

↓ (b) Region B

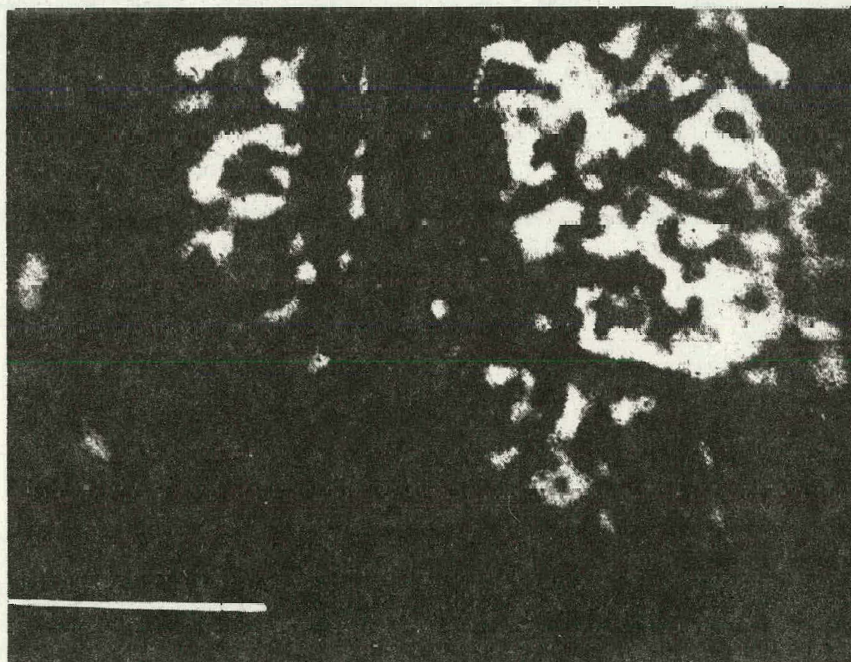
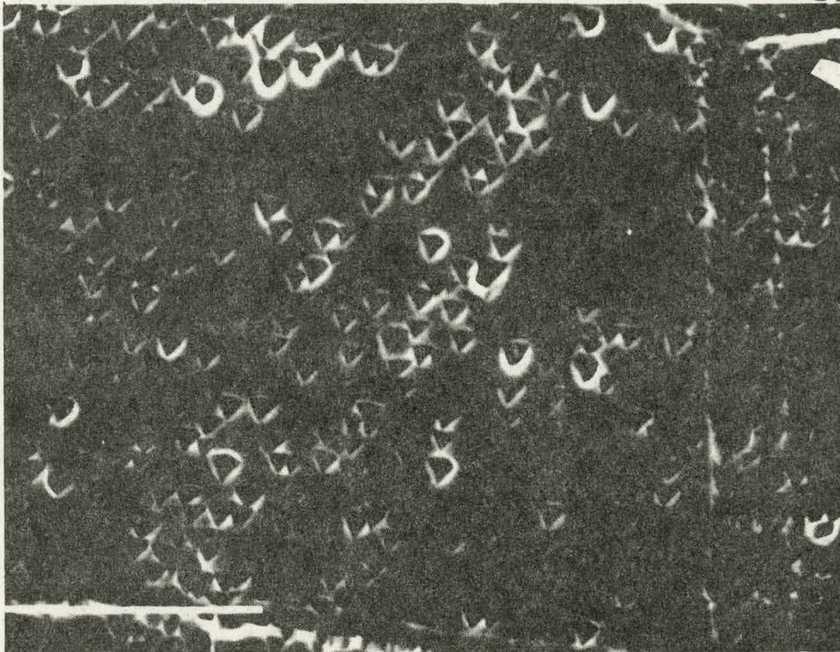


Fig. 2.14. The high magnification EBIC map (690X) of the (a) region A and (b) region B.



↑ (a) Region A

↓ (b) Region B

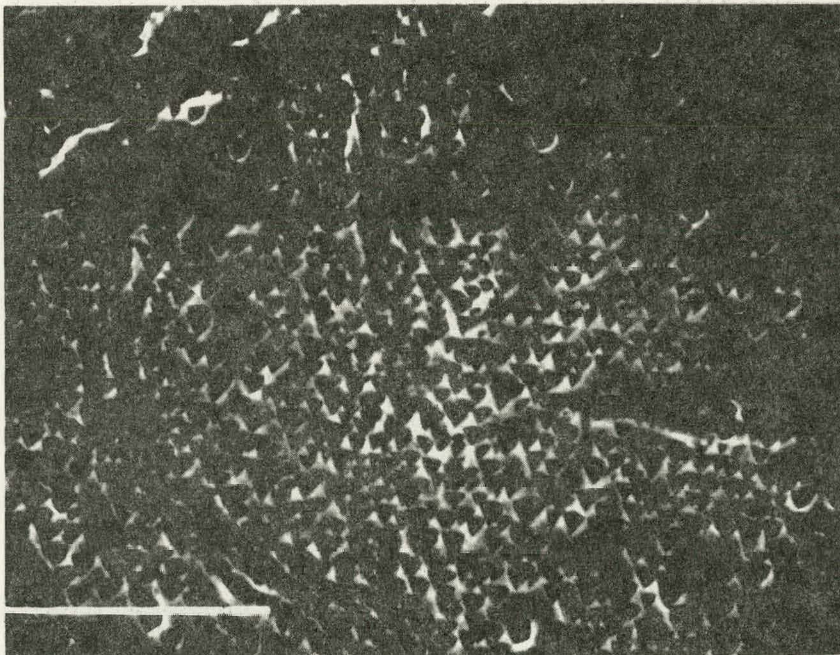


Fig. 2.15. The SE mode micrographs of the (a) region A and (b) region B taken after etching the surface.

Monsanto

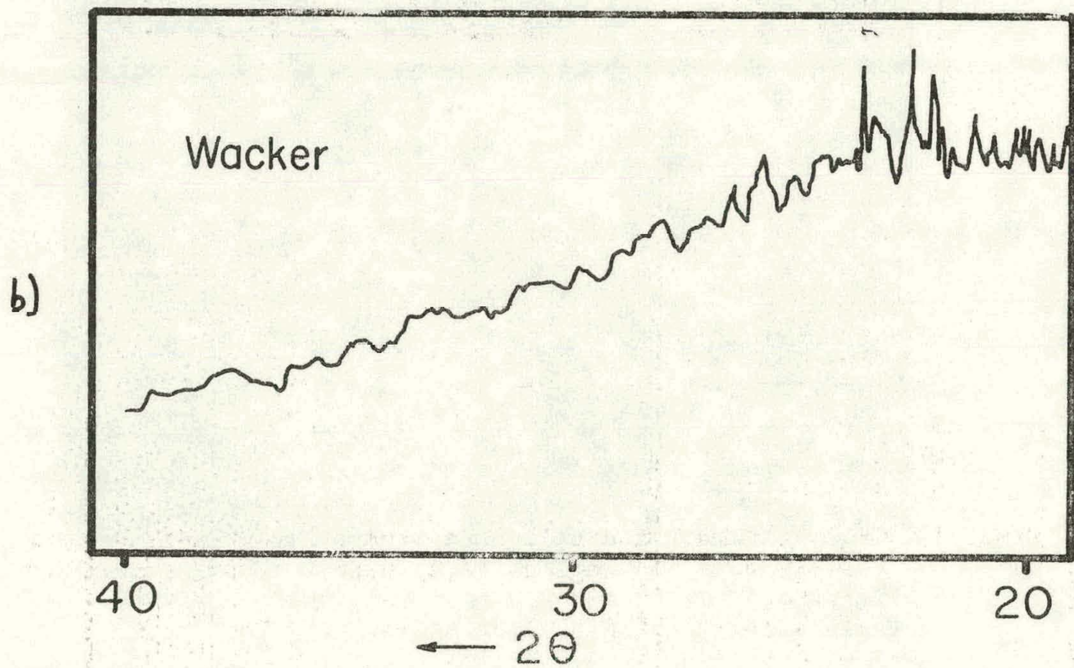
←(III) Orientation

a)

X-Ray Signal

40 30 20

Figure 2.16.: X-ray diffraction patterns for (a) Monsanto and (b) Wacker polysilicon.



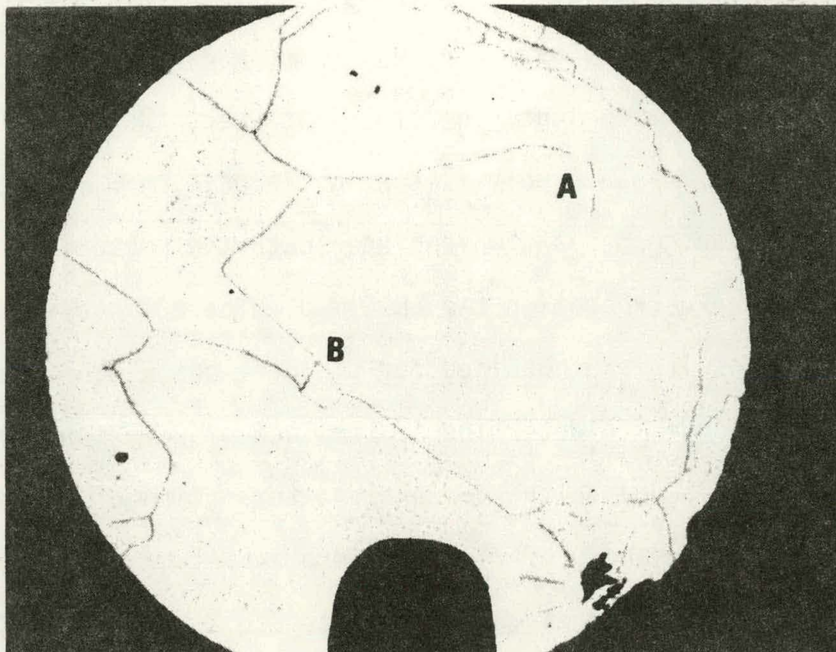


Fig. 2.17. The EBIC map of a cell made from a Wacker polysilicon substrate. Two regions (A,B) were selected for etch pits studies.

map of region A (Fig.2.18)shows that, in contrast to the Monsanto polysilicon, very few dark dots appear in the map of the Wacker cell. Etching the surface with Dash etch causes the appearance of many defect etch pits of irregular shape (Fig.2.19)but there is very little correspondence between the EBIC spots and the etch pit locations. In fact, there are many more etch pits than EBIC spots. The irregular shape of the etch pits on the Wacker materials is in keeping with the random orientation of the crystallite surface, as shown by the x-ray diffraction pattern of Fig.2.16b The dislocation lines therefore intersect the surface at odd angles. As seen in Monsanto polysilicon, a dislocation which is an active recombination center and which intersects the surface at normal incidences yields a dark spot on the EBIC map. There is some question whether similar results are obtained for dislocations which intersect at an odd angle. In order to determine if the lack of EBIC spots in the Wacker polysilicon is due to the odd angle intersection of the dislocation, two etch pits, p and q of Fig.2.18 were investigated. High magnification micrographs of these two etch pits Fig 2.20 shows that etch pit q intersects the surface at normal incidence while p is inclined 30 to 50°. In the EBIC map of Fig. 2.18, an etch pit p, although an inclined dislocation, appears to be a dark spot but the pit q has no corresponding dark spot. Thus, active odd angle dislocation can be observed with EBIC and the lack of EBIC spots can not be attributed to the angle of intersection. These results lead to the conclusion that most of the dislocations in the Wacker polysilicon are passivated. Note also that some grain boundaries that do not appear in the EBIC map, appear in the secondary mode micrographs after etching. This implies that some of the grain boundaries are also passivated or lie sufficiently below the surface so as not to be detected by EBIC.

Fig. 2.18. Magnified EBIC map of region A of figure 16.

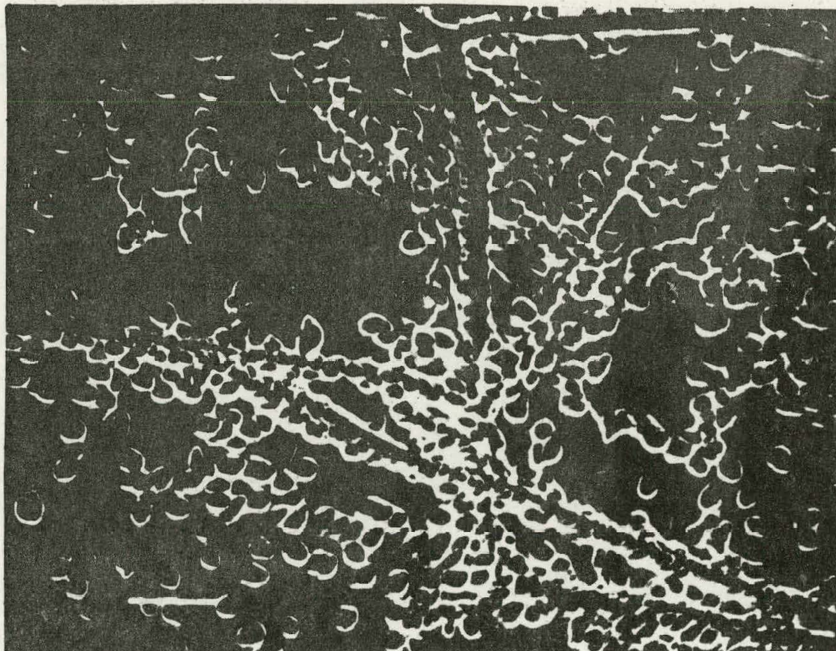
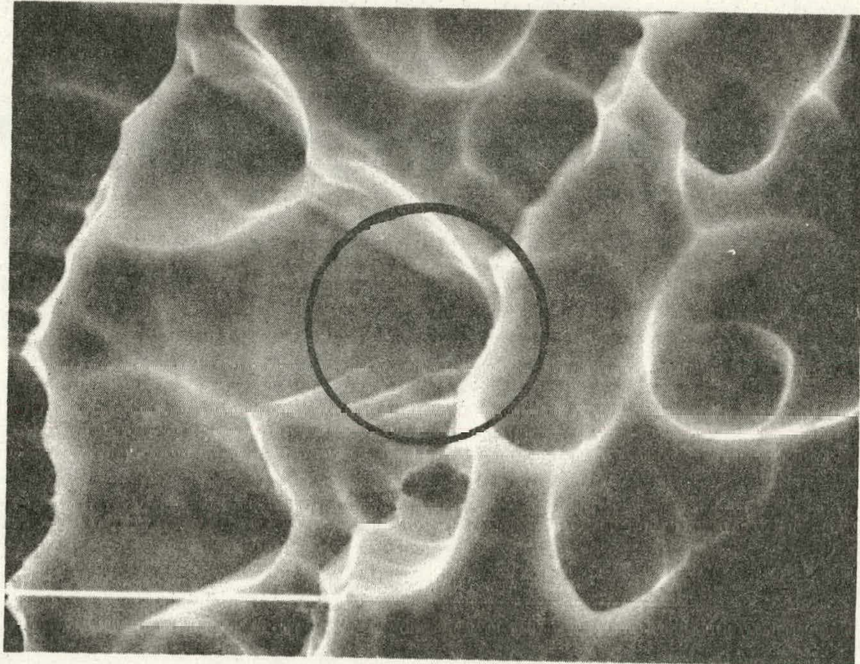


Fig. 2.19. The surface of figure 17 after etching.



(a) Inclined dislocation

(b) Normal dislocation

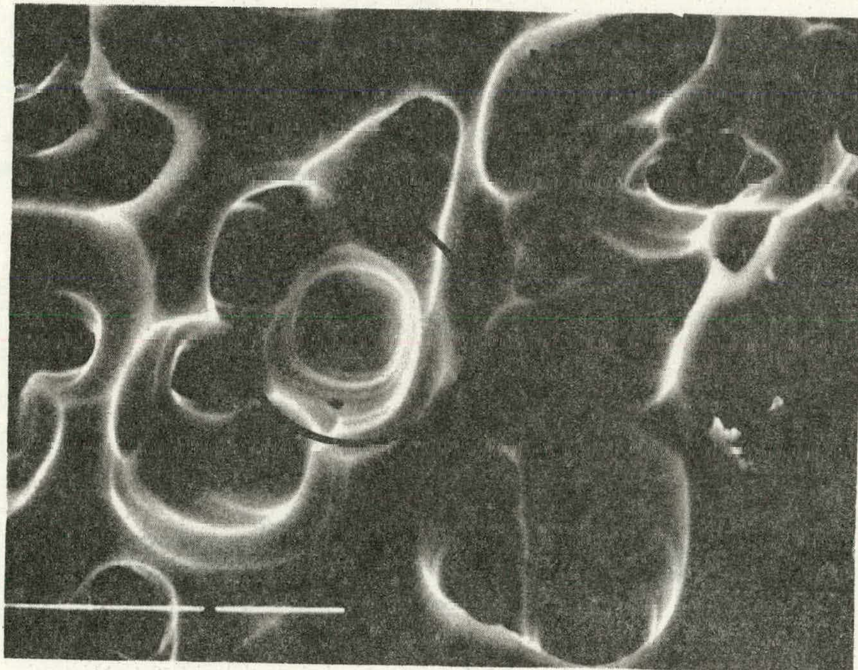
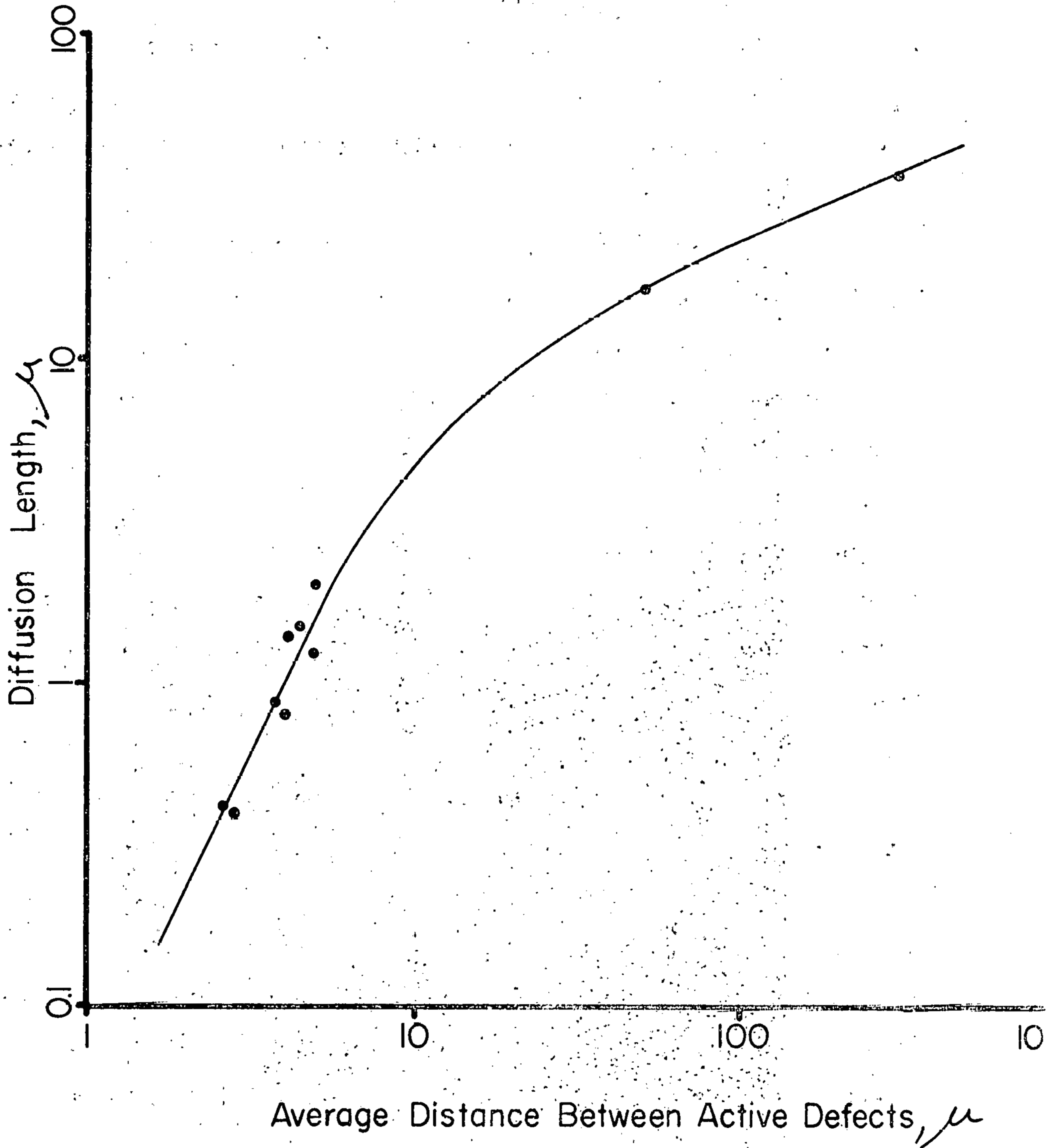


Fig. 2.20 Etch pits terminating (a) inclined dislocation, P, and (b) normal dislocation, q.

To quantify the effects of the defects, the local current response and diffusion length were measured in several regions of a Monsanto polysilicon cell with a focused light spot. Two wavelengths of light (7000 and 8000Å) were used to measure the diffusion length. The concentration of dislocations in each of the regions was estimated by counting the dark spots of an EBIC map of the regions. The results of these measurements are given in Fig.2.21 which plots the local diffusion length as a function of the average distance between dislocations, i.e. (concentration of defects)$^{-1/2}$. There are a number of factors which add to the uncertainty of the measurements for Fig.2.21. These are the uncertainty in the local adsorption coefficient of the polysilicon and uncertainty in correlating the position of the EBIC and local diffusion measurements. Thus, the values of the diffusion length shown in the Figure should be taken as relative values and not absolute. There is, however, surprisingly little scatter in the data which would indicate that the measurements are reasonable and that there is a correlation between defect density and diffusion length. As the defect density is reduced, the diffusion length becomes dominated by impurities and generation-recombination centers etc., and hence the curve shown in Fig 2.21 will begin to flatten out.

Fig. 2.21 Experimental relationship between diffusion length and defect density.



3. FABRICATION OF ITO/Si SOLAR CELLS

The fabrication of ITO/Si SIS photovoltaic devices utilizing neutralized ion beam sputter deposition technology has yielded reproducible high efficiency large area solar cells on both single and polycrystalline substrates. This chapter is concerned with the fabrication of the devices.

3.1. FABRICATION SYSTEM

The vacuum system used in the fabrication process was a modified NRC 3117. The schematic diagram of the system is shown in Figure 3.1. The vacuum is achieved by means of a six inch diameter, three-stage, liquid nitrogen trapped oil diffusion pump. The pump has a pumping capacity of 2000 ℓ/s and can achieve a vacuum of 1×10^{-7} Torr in the chamber.

The high purity gases (argon, hydrogen and oxygen) needed in fabrication processes are introduced directly into the ion source. The gases were controlled by Brooks 5810 leak valves which allow repeatable setting of flow rates. The gas flow rate was monitored by Brooks model 5810--1 CZDYA thermal mass flow sensors with their analog outputs fed into Brooks model 5820-1-YA meters calibrated in 0-5 sccm. This permits reproducible flow rates accurate to within ± .05 sccm.

The ion source used in the fabrication process was a model 10-1000-200 manufactured by Ion Tech, of Ft. Collins, CO. A schematic diagram of the ion source is shown in Figure 3.2. The gases are introduced into the ion source behind the anode pole piece assembly. Both the anode and cathode assemblies are electrically isolated from the source body. Electrons thermionically emitted from the tantalum cathode experience increased path length due to the magnetic field produced by the anode assembly. This increased path length increases the probability of the electron striking an atom to produce an ion. The ion source is capable of generating ions with energies from 50 to 1500 eV. Depending on the mode of operation, the

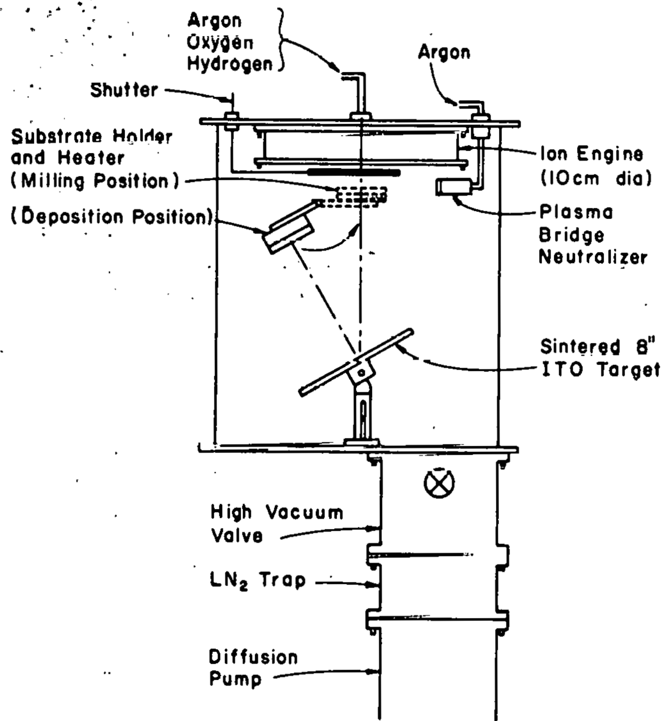


Figure 3.1. Schematic diagram of ITO sputtering system.

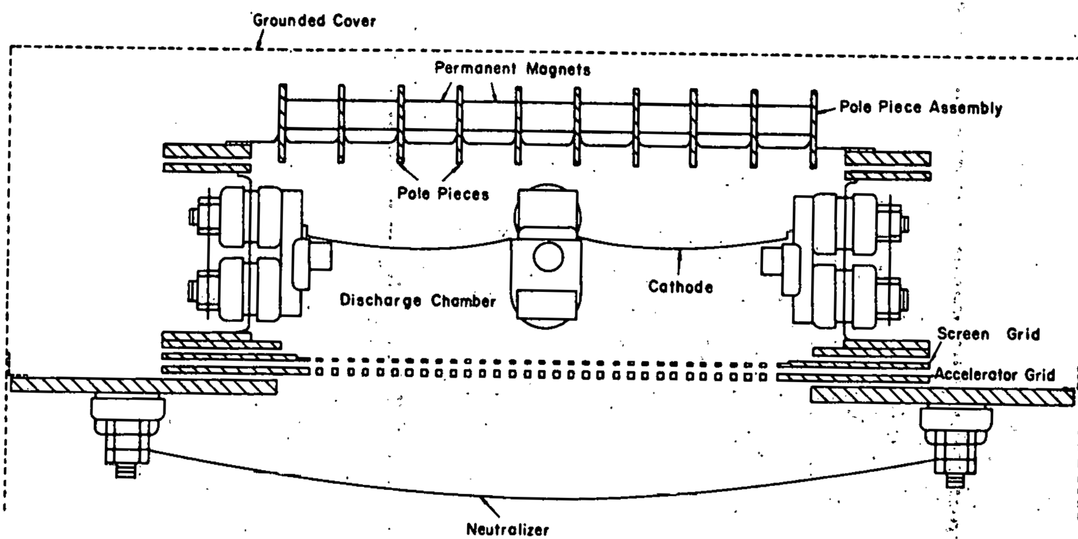


Figure 3.2. An Ion Tech. Engine used for Ion-Beam Sputtering.

beam density can attain values in excess of 2.5 mA/cm^2, with a divergence half angle of less than 7°.

The operation of an ion source can lead to the generation of a space charge region in the path of the beam. The creation of such a region can influence the density, profile and divergence of the ion beam. The field due to the space charge region can become sufficiently intense as to cause the ions to be repelled back toward the source. This could result in termination of the ion beam. To prevent this process, a neutralizing wire is placed across the accelerator grid structure. When a current is passed through the neutralizer, electrons are released by thermonic emission. The current can be controlled to effect a net volume neutralization of the beam, even though electron-ion recombination may not take place.

A major disadvantage of the use of neutralizer wire is that material from the wire is milled off by the ion beam. This material contaminates both sputtering target and substrates. Tantalum from the neutralizer wire has been detected in the solar cells using Auger/ESCA profiling techniques. For this reason, a plasma bridge neturalizer has been constructed. This system of neutralization injects a beam of electrons into the ion beam by means of argon propellant and electrostatic acceleration. In this manner reduced contamination and more complete neutralization are achieved. Better neutralization results in lower beam divergence and further reduced contamination by reducing sputtering of the fixturing.

The substrate heater was comprised of a commercially available heating element bonded to a stainless steel plate which was milled to accomodate the silicon substrate. The heater maintains less than a 2°C gradient across the silicon wafer at 400°C. The stainless steel plate is protected from the milling process by a carbon mask. Carbon was chosen because of its low milling rate and its low coefficient of thermal expansion. The mask is used to define the cell areas on the substrate.

The sputtering target was composed of 90% indium oxide and 10% tin oxide, this is the optimum ratio of the oxides for conductivity/transparency tradeoffs [1].

The ITO target utilized in the system was pressed commerically by Metals Mart, Great Neck, New York. The target material was hot pressed and sintered, yielding a structurally sound electrically conducting, dense disc. It may be worth noting that the target is nominally 99% pure, and that efficent cells do not require stringent purity in the target. The target material was a nominal thickness of 3/8 inch and a diameter of 8 inches. This ITO disc was indium soldered to a chrome plated water cooled copper backing plate.

The mechanical stability offered by this target allowed for complete control of the target angle. This permitted placement of the substrate heater in the central lobe of the sputter beam. To this date the sintered target has survived 775 runs with no visible degradation.

3.2. FABRICATION SEQUENCE OF ITO/Si SIS CELLS

The fabrication of ITO/silicon solar cells is basically a five step process. First, a substrate is selected and placed on the heater surface, and a carbon mask is selected, depending on the number and size of the cells desired, and is placed over the wafer. The system is evacuated and the substrate heater is activated. During the time required for the substrate heater to reach the desired temperature, argon, hydrogen and oxygen flow rates are adjusted and allowed to stabilize.

The argon, hydrogen, and oxygen gases were adjusted to a partial pressure of 4×10^{-5}, 2×10^{-5}, and 2×10^{-5} Torr respectively, for a total system pressure of 9×10^{-5} Torr. Secondly, the ion beam source was adjusted to a beam energy of 800 eV, current density of 2 mA/cm^2, and allowed to mill the silicon substrate for approximately five minutes. Studies have shown that ion milled silicon oxidizes much more rapidly than a chemically etched surface,

thus facilitating the needed oxide growth. Third, after the required milling time, a shutter was rotated between the ion source and substrate heater to allow the interfacial oxide to form. The substrate heater was rotated into deposition position and, after the oxide growth time, the shutter was removed and the ion beam allowed to impinge on the sputtering target, thus sputtering ITO onto the thermally grown oxide. It has been shown that the ITO layer forms an antireflection coating on silicon with a thickness of 750 Å [2]. At this thickness, ITO forms a 1/4 wavelength coating for the peak in the visible spectrum of 6000 Å wavelength.

When the ITO film has reached the desired thickness of 750 Å, the sputtering process is stopped and the ITO/silicon solar cells removed from the system.

To complete the fabrication process, a front grid contact is evaporated through a shadow mask. Considerable effort was expended in obtaining reliable front contact grids to ITO/Si SIS solar cells. Experimental results show that silver forms an excellent ohmic contact to the ITO, but exhibit poor adhesion to the ITO. Due to high current associated with large area devices ($\sim$ 315 mA for 11.46 cm^2 devices), the front contact must exhibit low series resistance. Measurement of a typical 11.46 cm^2 device shos as much as 187 mV drop across the main bus bar for a 3.5 μm silver grid, at the maximum power point, which yields poor fill factor (FF < 0.60). Attempts to solve this problem by increasing the grid thickness did not prove satisfactory due to adhesion problems possibly caused by differential thermal expansion problems.

One possible solution was to develop multilayer metallization consisting of a "bonding" layer, a low resistivity layer and protecting third layer, suitable for solder coating. The following metallization system have been attempted with ranging results as shown in Table 3.1.

Table 3.1.

1st Layer		2nd Layer		3rd Layer		Adhesion	Solderability	Remark
Material	Thickness	Mat	Thick	Mat	Thick			
Ti	100 Å	Al	10μm	none		Excel.	-----	a
Ti	50 Å	Ag	5μm	none		Fair	Poor	b
Ti	100 Å	Ag	5μm	none		Fair	Poor	b
Ti	250 Å	Ag	5μm	none		Excel.	Good	c
Ti	250 Å	Ag	10μm	none		Excel.	Good	c
Ti	250 Å	Ag	5μm	Ni	200 Å	Excel.	Good	d
Ti	250 Å	Ag	10μm	Ni	400 Å	Excel.	Excel.	e
Cr	400 Å	Ag	1μm	none		Excel.	Good	f
Cr	400 Å	Ag	10μm	none		Poor	Poor	f
Cr	250 Å	Ag	10μm	none		Good	Good	f
Cr	100 Å	Ag	10μm	none		Good	Good	f
Cr	100 Å	Ag	10μm	Ni	400 Å	Good	Good	f
Cr	100 Å	Ni	400 Å	none		Excel.	Excel.	g

a Titanium - Aluminum shows excellent adhesion to ITO, but due to thickness of Aluminum, grids showed stress in film as indicated by distortion at shadow mask. Process should prove excellent if used with a photolithography process as opossed to evaporation thru a shadow mask.

b Adhesion was not good after attempts to solder dip the contact. This was probably due to insufficient Ti thickness.

c Adhesion was excellent, but noticed some problems with solderability of fine lines. (i.e. incomplete soldering of lines.)

d Adhesion of all layer seemed to be excellent, but solderability of fine lines was not uniform.

e Adhersion of layer was excellent, also displayed excellent solderability.

f Showed problems at Cr - Ag interface, silver sometimes peeled off.

g Shows excellent properties, excellent adherence, excellent solderability.

As seen from Table 3.1, there are three systems that show good potential for ohmic contacts to ITO. The first is titanium-aluminum. This process demonstrates excellent adhesion and low resistivity grids, as evidence by FF greater than 0.75 with this system. However, due to the thickness of the Aℓ, it does not seem compatible with evaporation through this shadow mask.

The second system titanium-silver-nickel, also proved to have excellent adhesion properties and solderability. However, this system is less desirable due to the need for three evaporations resulting in a longer fabrication time and also due to the high cost of silver. The third system, chromium-nickel seems the most desirable of all systems investigated to this date. Both materials are relatively inexpensive and require the least amount of time within the vacuum system.

3.3. FABRICATION OF MoO_3/SINGLE CRYSTAL SILICON SOLAR CELLS

As an alternative to indium tin oxide (ITO), we have investigated MoO_3 as the top contact for SIS solar cells. The starting substrate was p-type single crystal silicon with resistivities of 0.1, 1.0, and 10 Ωcm. The silicon material was processed by standard industrial techniques. The wafers were oxidized and metallized by the Hewlett-Packard, Inc. of Loveland, Colorado. Approximately 1 μm of an aluminum-copper-silicon eutectic was deposited onto the back side for ohmic contact. In order to facilitate the isolation of many small diodes on a single wafer, there was 1000 Å of thermally grown silicon dioxide on the front side. The oxide layer was used merely to delineate the many diodes on a wafer and is not an essential fabrication feature.

The sputtering target used was prepared by applying a paste of MoO_3 to the front side of a water cooled stainless steel backing plate. A subsequent backout of 90° C for 30 hours was used to prepare the target

for vacuum conditions. An argon ion beam source was used to sputter the MoO_3 film. This technique is similar to that we have used in the fabrication of efficient ITO/single and polycrystalline silicon solar cells. The ion beam was used to sputter clean both the MoO_3 target and the exposed silicon surface through a carbon mask prior to deposition. Carbon was used to mask the wafer because of its low coefficient of thermal expansion and its low sputter rate. The MoO_3 was reactively sputttered onto the clean silicon surface in oxygen partial pressures of 5×10^{-6} Torr and 2×10^{-5} Torr. The oxygen introduced into the system helps form the oxide interfacial layer as well as effecting the reactive sputtering process.

The primary argon ion energy was 1000 eV and the MoO_3 has an impingement energy of $\sim$ 30 eV. The wafers were maintained at a temperature of 376°C during deposition. The deposition required 26 minutes to obtain the desired thickness of $\sim$ 3000 Å. These conditions indicate a sputter deposition rate of about 120 Å/minute. Contact was made to the MoO_3 surface by use of a mercury tipped gold probe. The cell diameters were 1/8 inch.

A glass slide monitor was included in each run and this slide was used to obtain film transmittivity and film resistivity information. These data are given below:

Oxygen Partial Pressure	2×10^{-5} Torr	5×10^{-6} Torr
Film Thickness	3400 Å	3150 Å
Film Transmittivity	76 percent	64 percent
Film Resistivity	160 Ωcm	63 Ωcm
Index of Refraction	2.06	2.68
Deposition Rate	110 Å/min.	120 Å/min.

The integrated white light film transmission was measured with a NASA calibrated solar cell at AM1 illumination. The index of refraction and film thickness were measured with an ellipsometer. The above results shows a dependence on oxygen partial pressure of the measured film properties.

The devices fabricated with partial pressure of 2×10^{-5} Torr of oxygen, resulted in linear resistors corresponding to a resistance of ≈ 160kΩ. The devices fabricated with partial pressure of 5×10^{-6} Torr of oxygen, exhibited photodiode behavior.

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2. G. Cheek, A. Genis, J. DuBow and V. R. Pai Verneker, Appl. Phys. Lett. 35, 495 (1979).

4. PERFORMANCE OF ITO/Si SIS SOLAR CELLS:

In this section the performance of ITO/SI SIS (single and poly) solar cells evaluated by current-voltage (I-V), capacitance-voltage (C-V) and conductance-voltage (G-V) characteristics are described. In addition, the photovoltaic characteristics of MoO_2/single crystal Si solar cells are also discussed:

4.1. Effect of interfacial layer on device performance:

The thickness, composition and electronic properties of the interfacial layer are critical determinants of the device conversion efficiency. The existance of the interfacial layer (SiO_2) was detected by Auger analysis [1]. The properties of the interfacial layers depend critically on the system temperature and oxygen partial pressure during the growth of the layer.

Cell performance is highly dependent on deposition parameters used in a fabrication sequence. Through systematic depositions we have observed functional dependence of various cell characteristics on substrate temperature, O_2 partial pressure in the ambient, and interfacial oxide growth times. These cell characteristics include open circuit voltage, short circuit current, fill factor and efficiency. We have observed that the fill factor is the parameter most affected by small changes in oxide thickness, induced by variation in oxygen partial pressure, substrate temperature, temperature gradients across the wafer, and film uniformity. The data obtianed from previous experiments have indicated that an optimum substrate temperature range exists for our system, virtually independent of other parameters. This temperature is in the range $373 \pm 10^{o}C$. The optimized value for oxygen pressure is $1 - 3 \times 10^{-5}$.

One potential problem with in-situ oxide growth employed in the present study is that of "pinhole" formation. Dry oxides seem to have a higher pinhole density than oxides grown in moist ambients (Huibrigtse, private communication). These pinholes have not appeared on the flying spot scanner results, but they may have a net integrated effect upon the overall cell performance. In the case of SiO_2, which is not a "nucleation" type of film, pinholes may represent oxide sections less than 10 Å thick.

4.2. Current Conduction Mechanism in ITO/single crystals Si Solar Cells:

The effect of temperature on the dark I-V characteristic is a sensitive probe whereby the current conduction mechanism of a solar cell may be understood. Fig. 4.1. shows the calculated dark I-V characteristics as a function of temperature for an ITO-SiO_2-(p-Si) Si diode [3]. The temperature was varied from 200° K-400°K. The depletion layer lifetime was taken to be one order of magnitude less than the bulk semiconductor lifetime. The calculated curve shows two distinct regions of slope 1 and 2 in the voltage range of interest for solar cells. At lower temperatures, the recombination-generation current in the depletion region dominates, while at the higher temperatures the diffusion current dominates.

The experimentally observe dark I-V characteristics as a function of temperature for a typical ITO-p-Si diode (12-G) are shown in Fig. 4.2. A careful inspection of this data shows that the dark I-V consists of two regions, one with slope $n_1 = 1.3$ and the other with slope $n_2 = 2.0$. The following parameters were measured for this device under AM1 (100 mW/cm^2) illumination:

$$V_{oc} = 0.52 \text{ V}$$
$$I_{sc} = 3.6 \text{ mA}$$
$$A = 0.2 \text{ cm}^2$$
$$FF = 0.78$$
$$\eta = 7.3\%$$

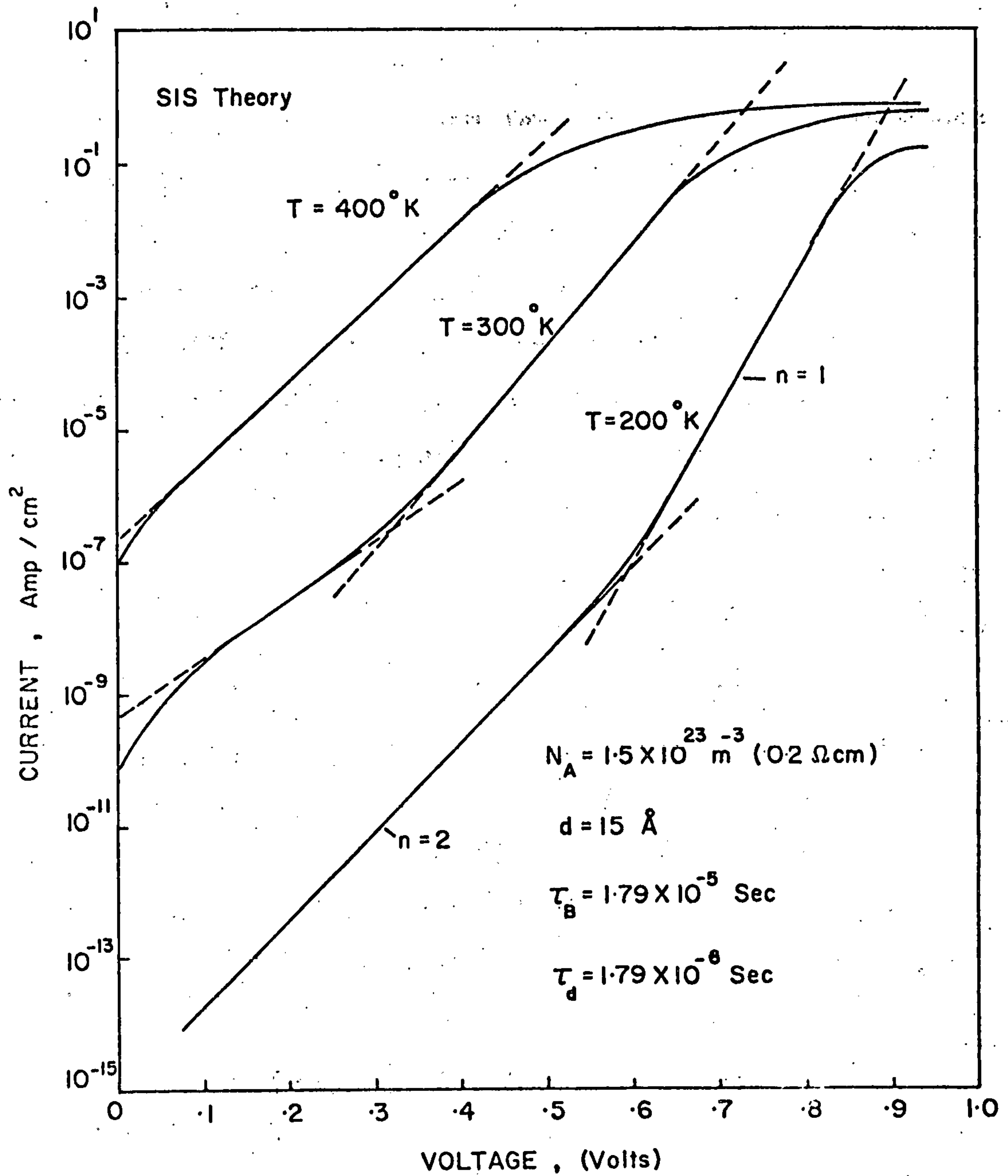


Figure 4.1.

Calculated effect of temperature upon the forward dark I-V characteristics of ITO-SiO_x-(p-type)Si tunnel diode. The substrate resistivity is 0.2 Ω-cm and the insulator thickness is 15 Å.

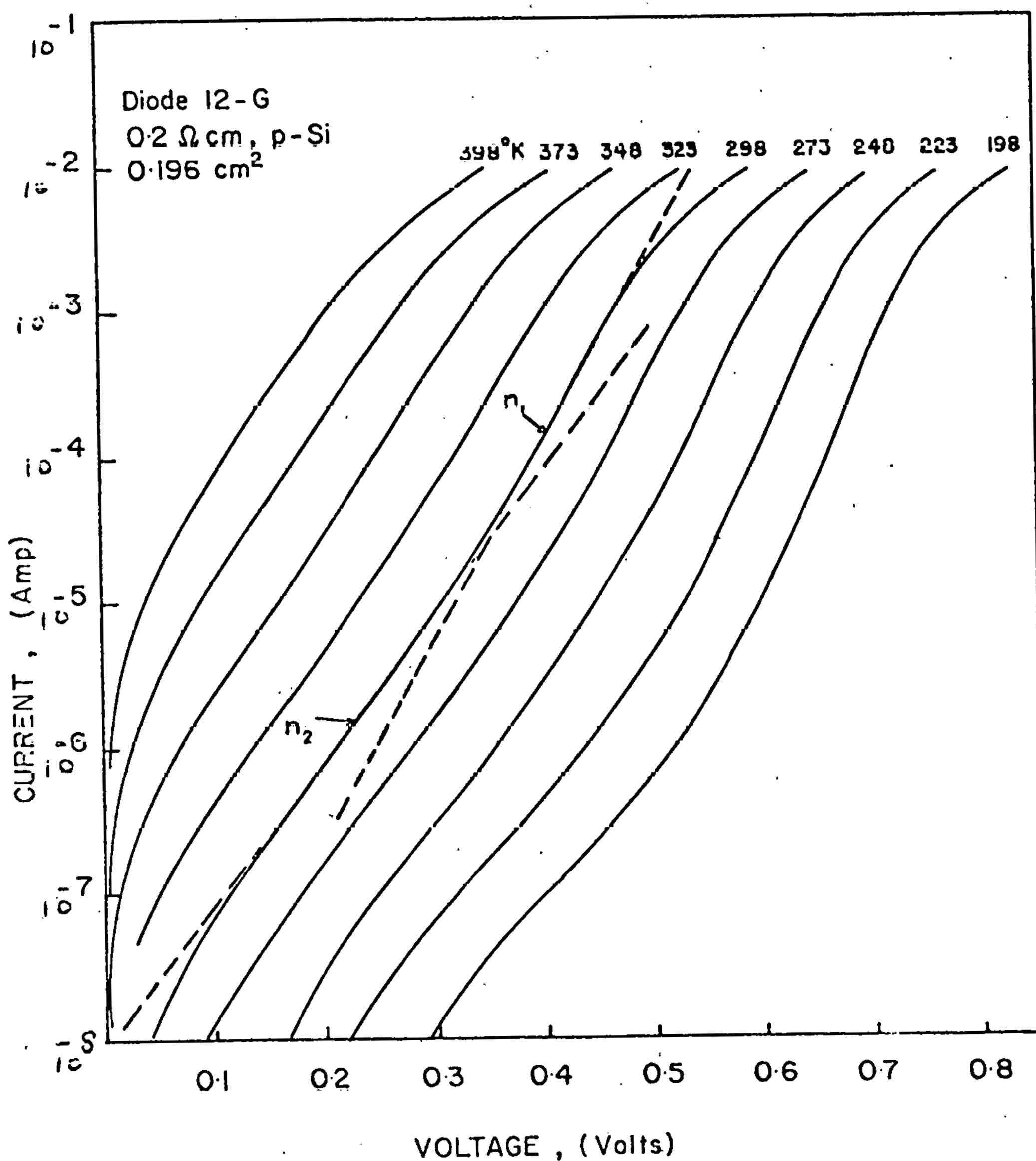


Figure 4.2.

Experimentally measured forward dark forward I-V characteristics of ITO-(p-Si) solar Cells No. 12-G as a function of temperature.

The series resistance of this device was measured by following the method of reference 17.

$$R_s = \frac{V' - V_{oc}}{I_{sc}}$$

where V' is the voltage from the dark I-V at the point where $I = I_{sc}$

Figure 4.2. were curve fitted by using the following equations:

$$I - \frac{V - IR_s}{R_{sh}} = I_{01}\left[\exp\left(\frac{V - IR_s}{n_1 kT}\right) - 1\right] + I_{02}\left[\exp\left(\frac{V - IR_s}{n_2 kT}\right) - 1\right] \quad (4.1)$$

where

$$I_{01} \propto T^3 \exp\left(\frac{-Eg}{n_1 kT}\right) \text{ (diffusion) } (4.2.)$$

and

$$I_{02} \propto T^{5/2} \exp\left(\frac{-Eg}{n_2 kT}\right) \text{ (recombination) } 4.3.$$

The reverse saturation current given by equation 4.2. is the diffusion current and equation 4.3. represents the recombination-generation current in the depletion layer. The values of $n_1 = 1.3$, $n_2 = 2$, $R_s = 5\ \Omega$ and $R_{sh} = 5 \times 10^7\ \Omega$ were used to fit the experimental curve. It is observed that a fairly reasonable fit is obtained, as shown in Fig. 4.5.

We have calculated Fig. 4 1. by taking $\phi_{osi} = 3.3$ eV, based on the best information available from the literature. If we generate another set of curves with a higher value of ϕ_{osi}, majority carriers will provide additional current, and shift the characteristics closer to the experimental ones. Such an exercise, along with other parameter variations would facilitate an exact fit but would not impact the case for the SIS model.

4.3. Optimum Thickness of Indium Tin Oxide

We have studied the short circuit current density of ITO/Si solar cells as a function of ITO thickness. The details of this work are reported in reference 10. Based on both the simple calculation of the optical reflection and also on comparison with the small area experimental devices it was concluded that the optimum thickness of ITO is about 750 Å. However, reflectivity/resistivity and grid coverage tradeoffs for large area devices indicate that best results may be obtained with ITO thickness of about 2250 Å.

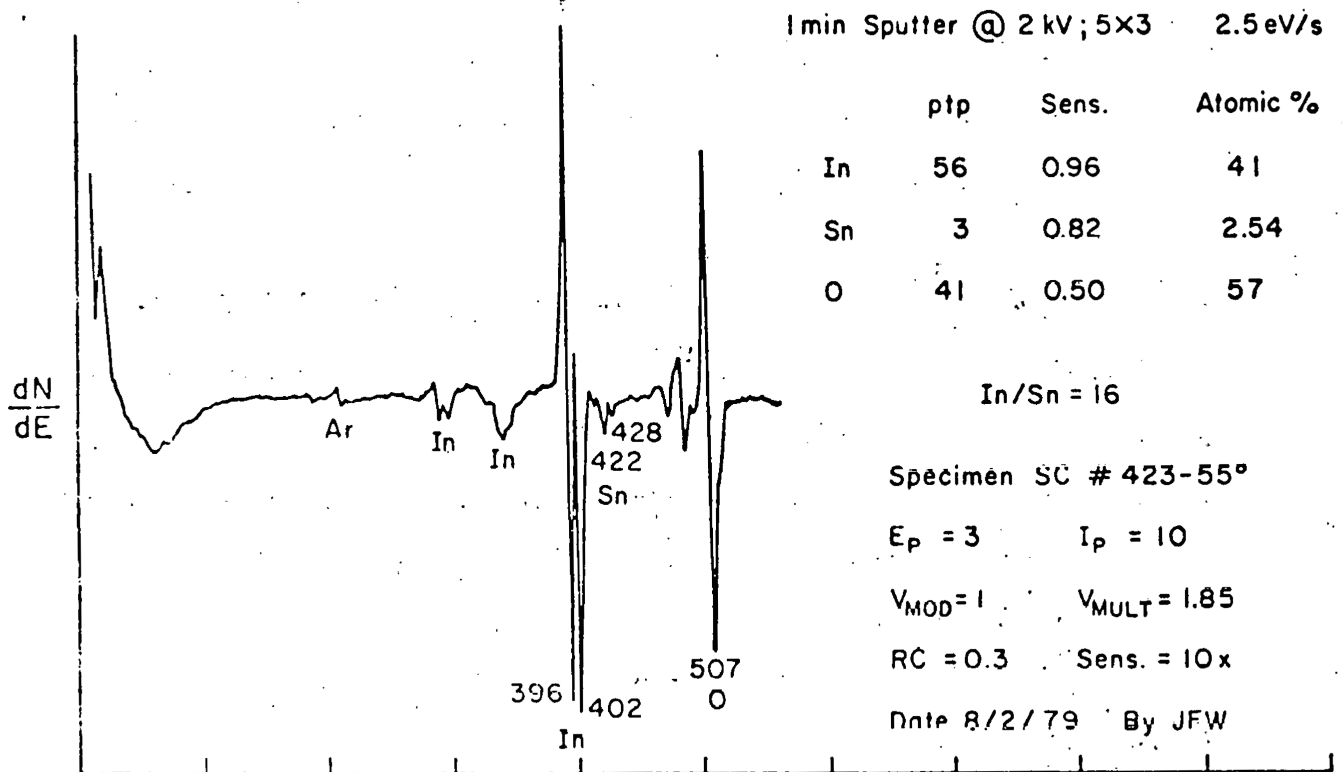
4.4. Angle of Incidence Effects in ITO/Single crystal Si Solar Cells:

We have performed experiments to determine if the angle of incidence between the sputtering target and the substrate has an effect on the conversion efficiency and, if so, what ITO film parameters are primarily responsible for this effect. A series of films were sputtered at different target-substrate angles. The thickness of the films were approximately 750 Å, and the color of the films appeared deep blue. The angle between the sputtered material and the substrate was varied from

50° to 120°. Three replicate experiments were performed while varying the angle of the target with respect to the substrate. All fabrication parameters were held constant as described above. After sputter deposition of the ITO, 10,000 Å of silver was resistively evaporated through a shadow mask to form a front contact. The cells had an active area of approximately 2 cm^2 after subtracting for coverage of the grids. The solar cells parameters were measured under AM1 illumination.

It was noted that, as the angle of incidence was increased from normal, the appearance of the cells became non-uniform in color, thus suggesting variation in the thickness of the ITO film. This was confirmed by ellipsometry measurements. It is believed that this variation is due to rotating the substrate out of the central sputter lobe of the target. However, the thickness variation of the ITO film, when reflected back through J_{sc} losses cannot explain the observed variation in open circuit voltage of 12 percent. It was thought that if the substrate was rotated out of the central sputter lobe, possible variations in stoichiometry could be present in the ITO film. Sincey varying indium oxide to tin oxide ratios vary open circuit voltage [6], Auger and ESCA analysis were utilized to determine if any compositional change can be seen in the bulk of the ITO films. As shown in Fig. 4.3. within the resolution of Auger and ESCA analysis there was no detectable compositional changes in the films.

The angle of incidence of the sputtered partial beam of the substrate may cause variations in the crystallite size within the ITO film. By depositing ITO on glass substrates with different angle of incidence, and maintaining all other deposition parameters constant, we have observed conductivity changes in ITO by an order of magnitude. The highest conductivities also crrespond to the highest open circuit voltages, In this regard, conductivities usually are associated with a more degenerate film,



1min Sputter @ 2 kV, 5×3 2.5 eV/s

	ptp	Sens.	Atomic %
In	52.5	0.96	41
Sn	2.5	0.82	2.28
O	38.0	0.50	57

In/Sn = 18

Specimen SC # 429-110°

E_P = 3 I_P = 10

V_{MOD} = 1 V_{MULT} = 1.85

RC = 0.3 Sens. = 10x

Date 8/2/79 By JFW

dN/dE

Ar In In 428 422 Sn 396 402 In 507 O

0 100 200 300 400 500 600 700 800 900 1000

Electron Energy, eV

Figure 4.3. Auger Depth profile for two ITO films deposited at the Angle of Incidence at 55° and 110°

a reduced work function and hence a higher barrier height. This may be the origin of observed increased open circuit voltages.

4.5. Reverse I-V Characteristics of ITO/Single Crystal Si SIS Solar Cells:

We have used reverse I-V characteristics under illumination to examine whether leakage current orginating from edge effects is present in our present devices. The following parameters were measured for the device R-339 at one sun (AM1, 100 mW/cm^2): -temperature -25° C, V_{oc} = 508 mW, J_{sc} = 28.39 mA/cm^2, FF = 0.74, active area = 3.28 cm^2 and efficiency = 10.67%. The reverse I-V characteristics under illumination are shown in Fig. 4.4. The reverse bias was varied from 0 to voltas and the intensity was varied from 18 mW/cm^2 to 144 mW/cm^2. As can be seen from Fig. 4.4., the photo-current remains practically constant as the reverse bias is increased. At the lower intentsities the photocurrent increases very slowly with reverse bias, which indicates that recombination current is contributing slightly to the photocurrent. In recent devices such as these the edge leakage problem observed earlier has been significantly reduced.

In order to determine the area dependence of the reverse I-V characteristics we tested a small area device R-507B with the following parameters: temperature - 25°C, V_{oc} = 493 mV, J_{sc} = 27.35 mA/cm^2, FF = 0.645, Area = 0.079 cm^2, and Efficiency = .70%. The reverse I-V characteristics under illumination are shown in Fig. 4.5. The intensity was increased from 7.1 mW/cm^2 to 144 mW/cm^2 and the reverse bias varied from 0 to 7 volt.

In this case the photocurrent was not quite constant, but increased slightly with bias even at higher intensity. This increase in reverse current is due to leakage current and could be due to the following two contributions: (1) the surface generation of minority carriers, occuring in the region where the junction intersects the surface of the silicon; and (2) the generation of minority carriers inside the depletion layer.

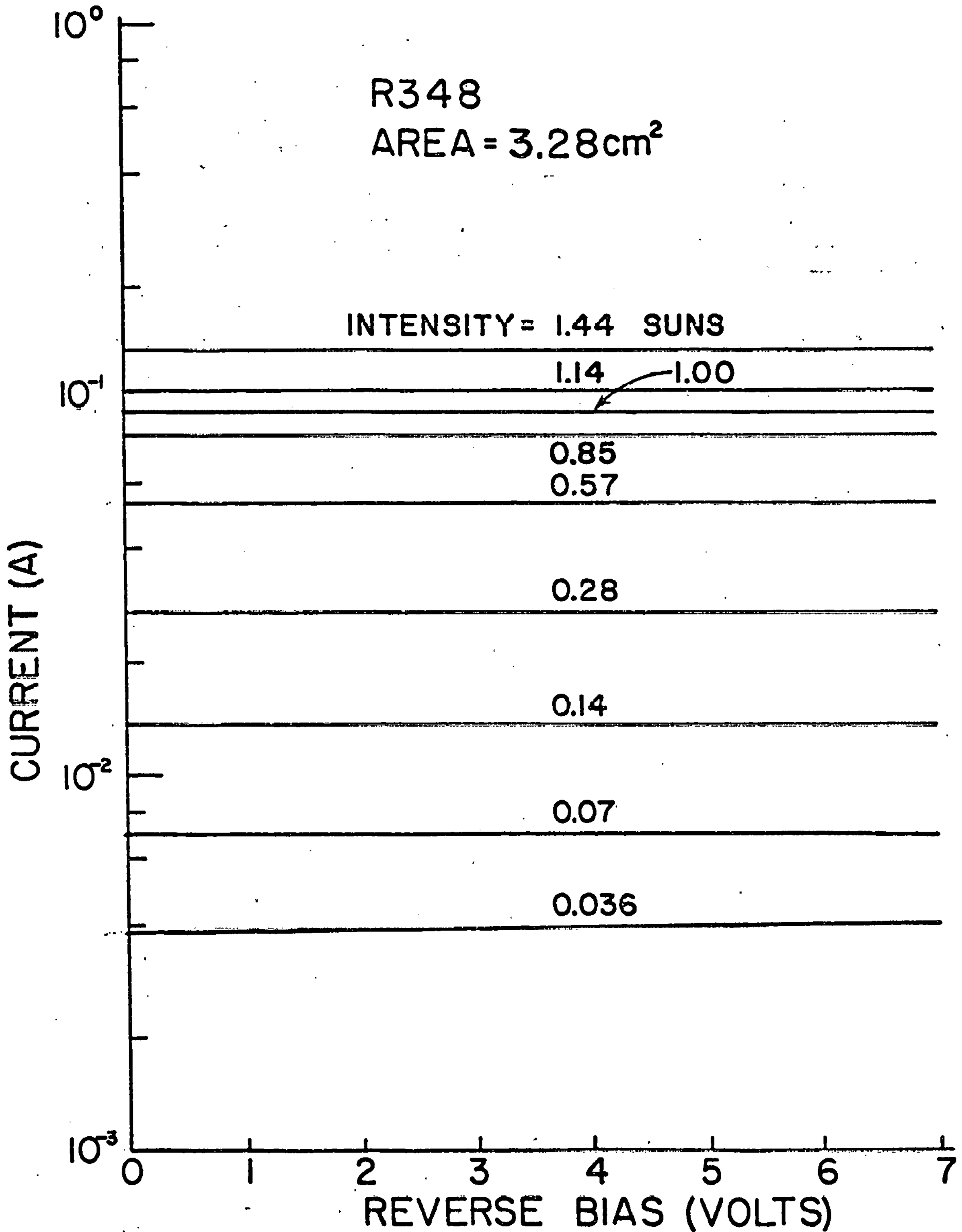


Figure 4.4. Reverse I-V characteristics of ITO/Si SIS solar cell (R-339) under illumination with intensity as the variable parameter.

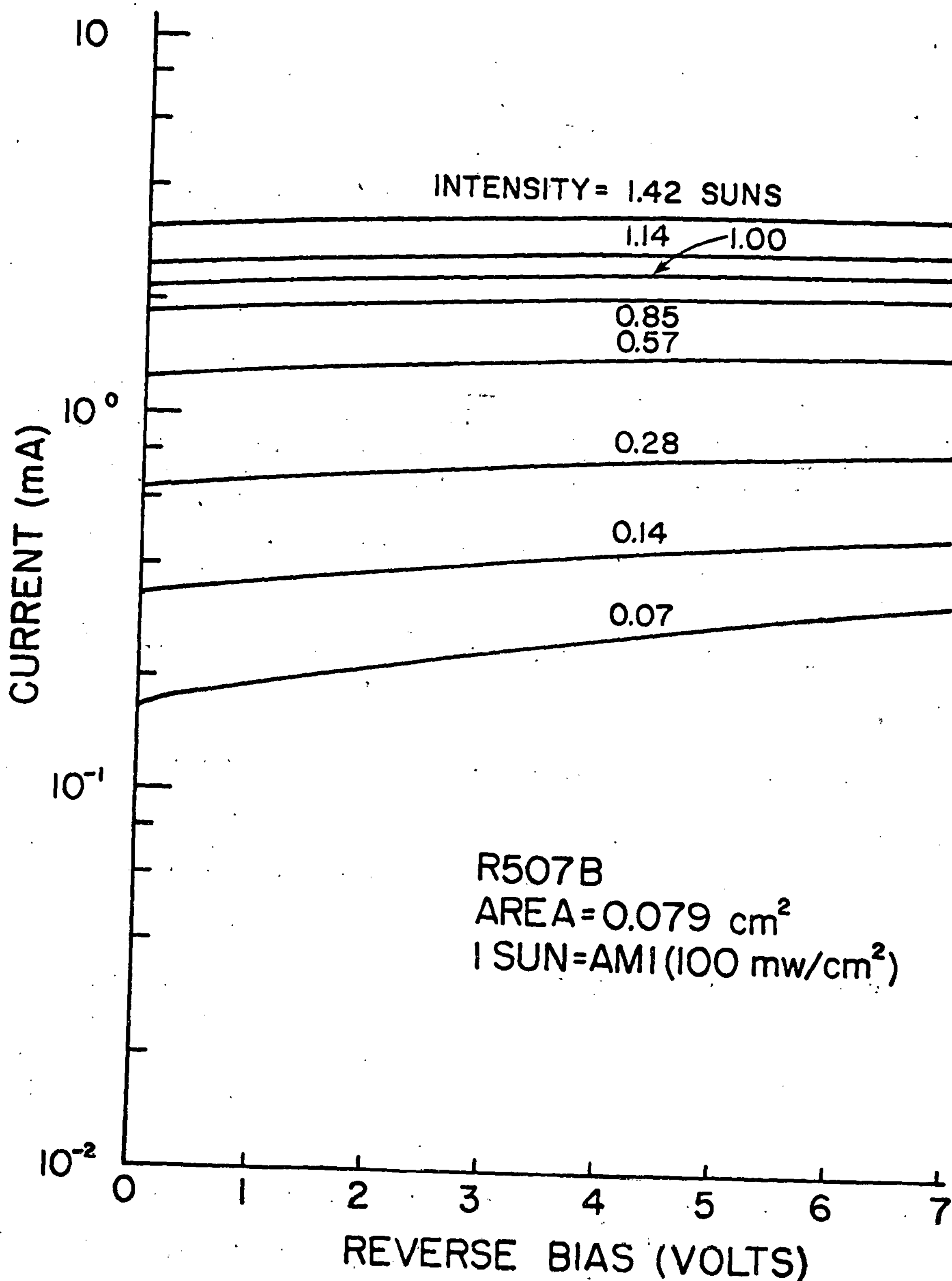


Figure 4.5. Reverse I-V characteristics of ITO/Si SIS solar cell (R-507B) under illumination with intensity as the variable parameter.

Since for large area devices almost no leakage current is observed, the surface and edge generation of minority carriers is likely to be responsible for the leakage current in small area diodes. Moreover, the diode reverse current is likely to be reduced if the surface is moved deeper into inversion by a combination of lower work function of the oxide and/or reduced interface state density.

4.6. Effect of Substrate Surface Preparation and Hydrogen Passivation on the Performance of ITO/Wacker Polysilicon SIS Solar Cells:

Prior to fabrication, some of the polycrystalline substrates were etched in a mixture of hydrofluoric and nitric acids for approximately 2 minutes to remove surface contamination and saw damage The etched wafers appeared smooth but some evidence of saw damage was still visible.

The light and dark I-V characteristics of three ITO/polysilicon SIS solar cells are shown in Fig. 4.6. and 4.7. Sample 661 is a diode that was fabricated with Wacker polysilicon as it was obtained from the supplier. The surface of sample 664 was prepared by chemical etching as described earlier to reduce the surface damages. During the fabrication of diode 660B, hydrogen was incorporated during milling and oxidation to pssivate the surface defects. As can be seen from Fig. 4.11 and 4.12 the diode characteristics were improved by chemical treatment of the surface. Since no grids were applied to these diodes, the fill factor is low. The hydrogen passivation further reduces the static and dynamic role of surface states. Since the open

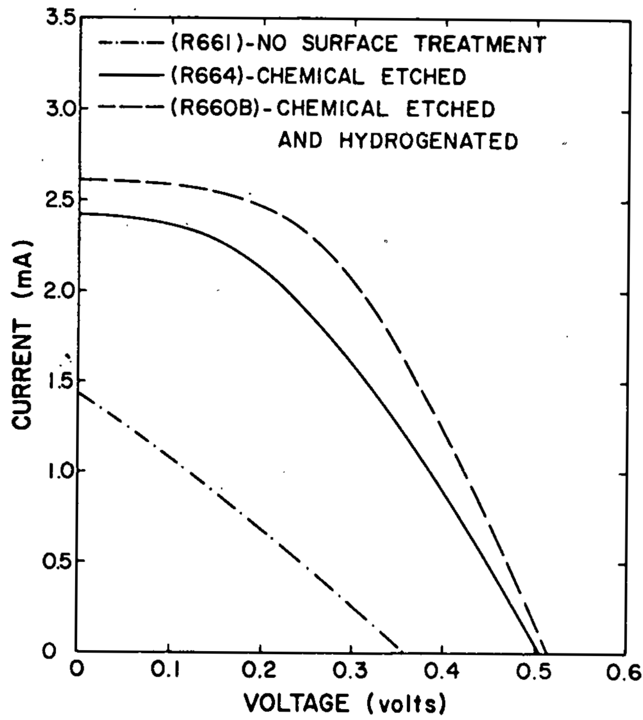


Figure 4.6.: Current-Voltage Illuminated (AM1) characteristics of ITO/Wacker polysilicon SIS solar cells for various surface treatments.

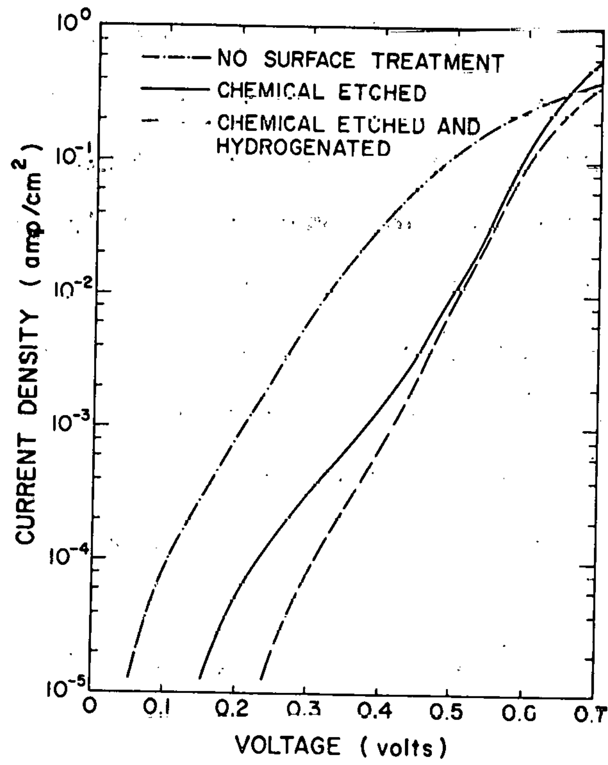


Figure 4.7.: Dark I-V characteristics of solar cells shown in Figure 4.11.

circuit voltage, V_{oc} of hydrogenated cells is better than the other two diodes, hydrogen at the interface must reduce the electrostatic effect of surface states and thereby enhance the open circuit voltage. This is supported by the barrier height measured by C-V method. These results are shown in Table 4.1; the hydrogenated cell has the highest barrier height. The increase in short circuit density J_{sc} with surface etching and hydrogen incorporation indicates that the deleterious effect of surface states is minimized. This is further compared by spectral response measurements which are shown in Fig. 4.8. For the diodes with untreated surfaces the spectral response is reduced at all wavelengths. A low barrier height enhances the effect of a high density of surface states and hence decreases the spectral response [7]. The reduced barrier also leads to a higher concentration of majority carriers at the insulator-semiconductor interface which increases recombination at surface states and also caused degradation in the spectral response at all wavelengths [7]. With hydrogen treatment, the spectral response at lower wavelengths increases slightly, indicating due to passivation of grain boundaries near the surface.

4.7. C-V and G-V Characteristics of ITO/polysilicon SIS Solar Cells:

Three samples were selected in this work. Sample #661 is a diode that was fabricated with Wacker polysilicon as it was obtained from the supplier. The back surface of sample R710 was prepared by chemical etching as described earlier to ensure good ohmic contact, but the front surface was untreated.

TABLE 4.1.

Effect of Various Surface Treatment on the Characteristics of ITO/Wacker Polysilicon SIS Solar Cells

Device No.	Surface Treatment	Total Area (cm^2)	Illumination and Temperature	Barrier Height (mV)	V_{oc} (mV)	J_{sc} mA/cm^2	FF	Efficiency %
R661	No Surface Treatment	0.079	100 mW/cm^2 28°C	798	335	18.1	0.273	1.75
R664	Chemical Etched	0.079	100 mW/cm^2 28°C	932	509	30.7	0.388	6.03
R660B	Chemical Etched and Hydrogenated	0.079	100 mW/cm^2 28°C	956	512	33.2	0.456	7.73

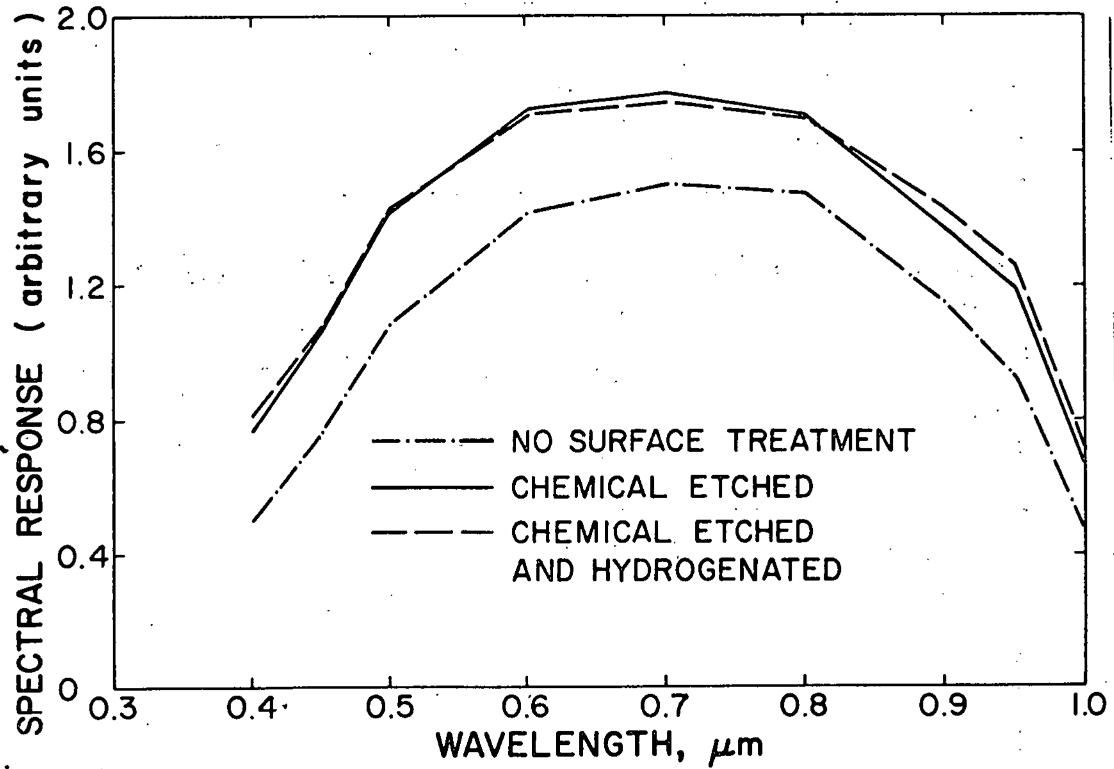


Figure 4.8. Relative Spectral response of solar cells shown in Figure 4.11

During the fabrication of diode R710 hydrogen was incorporated during the milling and oxidation to passivate the surface defects. Both front and back surfaces were chemically etched for sample R660B and hydrogen was incorporated during the milling and oxidation as in diode R710. Table 4.2. shows the photovoltaic output and barrier height data measured from 1MHz C-V characteristics. The admittance measurements were carried out by the automated technqiue described in Seciton 5.2.

The C-V and G-V characteristics of three samples measured at 30 KHz and 3 KHz respectively are shown in Fig. 4.9. and 4.10. In far forward bias the sample becomes highly conductive and the phase of the admittance $[\Theta = \tan^{-1} (-\frac{\omega C}{G})]$ tends to zero as G becomes much larger than ωC. The minimum phase that can be measured by the network analyzer system is 0.01 degree. This corresponds to a minimum $\frac{\omega C}{G}$ ratio of 1.75×10^{-4}. On comparing admittance measurements of different samples (Fig. 4.9. and 4.10), the lower efficiency samples (R 661, R 710) and C-V characteristics had lower turn on voltages than the higher sample (R 660B) as seen in Fig. 4.9. Therefore, for the poorer devices the phase becomes too small to measure at lower voltages than for R 660B, and the capacitance cannot be measured, as seen in Fig. 4.10. As shown in Fig. 4.9. at zero bias, the 30 KHz value of the capacitance is virtually independent for device R710 and R660B. Under reverse bias, the semiconductor cannot generate minority carriers sufficiently rapidly to maintain an inversion layer. Hence, the depletion region at the oxide-polysilicon interface expands to absorb the reverse bias and the capacitance decreases. The large value of capacitance at zero bias for devcice R661 indicates that the surface is either not inverted or even possibly depleted and the width of the depletion layer is smaller than in device R661 and R710. Strongly depleted or weakly inverted surfaces remain up to small forward

TABLE 4.2

Photovoltaic Output and Barrier Height
Calculated from C-V data Measured at 1 MHz

Device No.	Total Area (cm^2)	Illumination and Temperature	Barrier Height (mV)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF	Efficiency %
R661	0.079	AM1 100mW/cm^2 28°C	798	335	26.7	0.59	7.98
R710	0.079	AM1 100mW/cm^2 28°C	850	430	32.4	0.67	8.50
R660B	0.079	AM1 100mW/cm^2 28°C	956	512	33.2	0.73	9.56

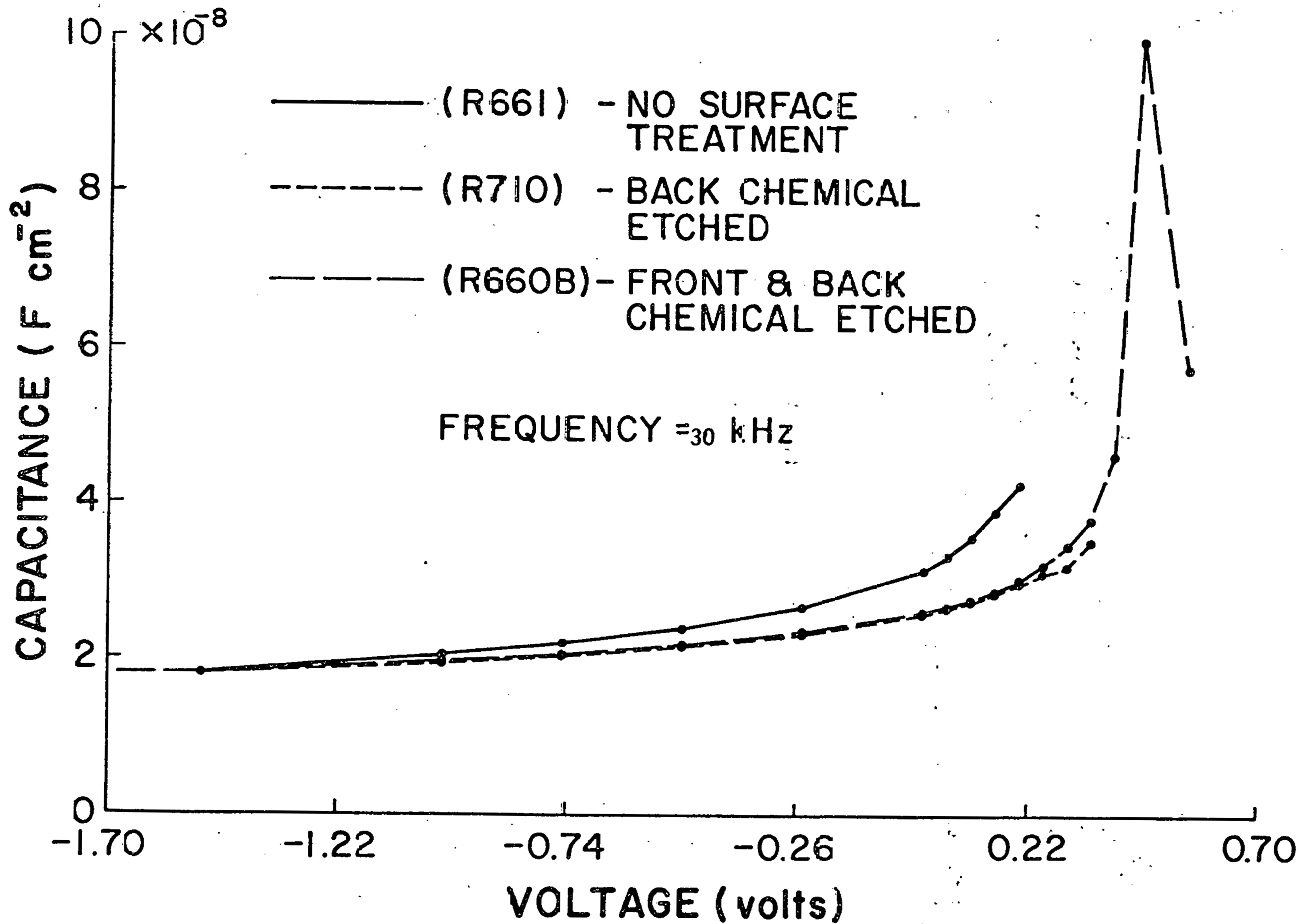


Figure 4.9. C-V characteristics measured at 30 KHz for devices R661, R710

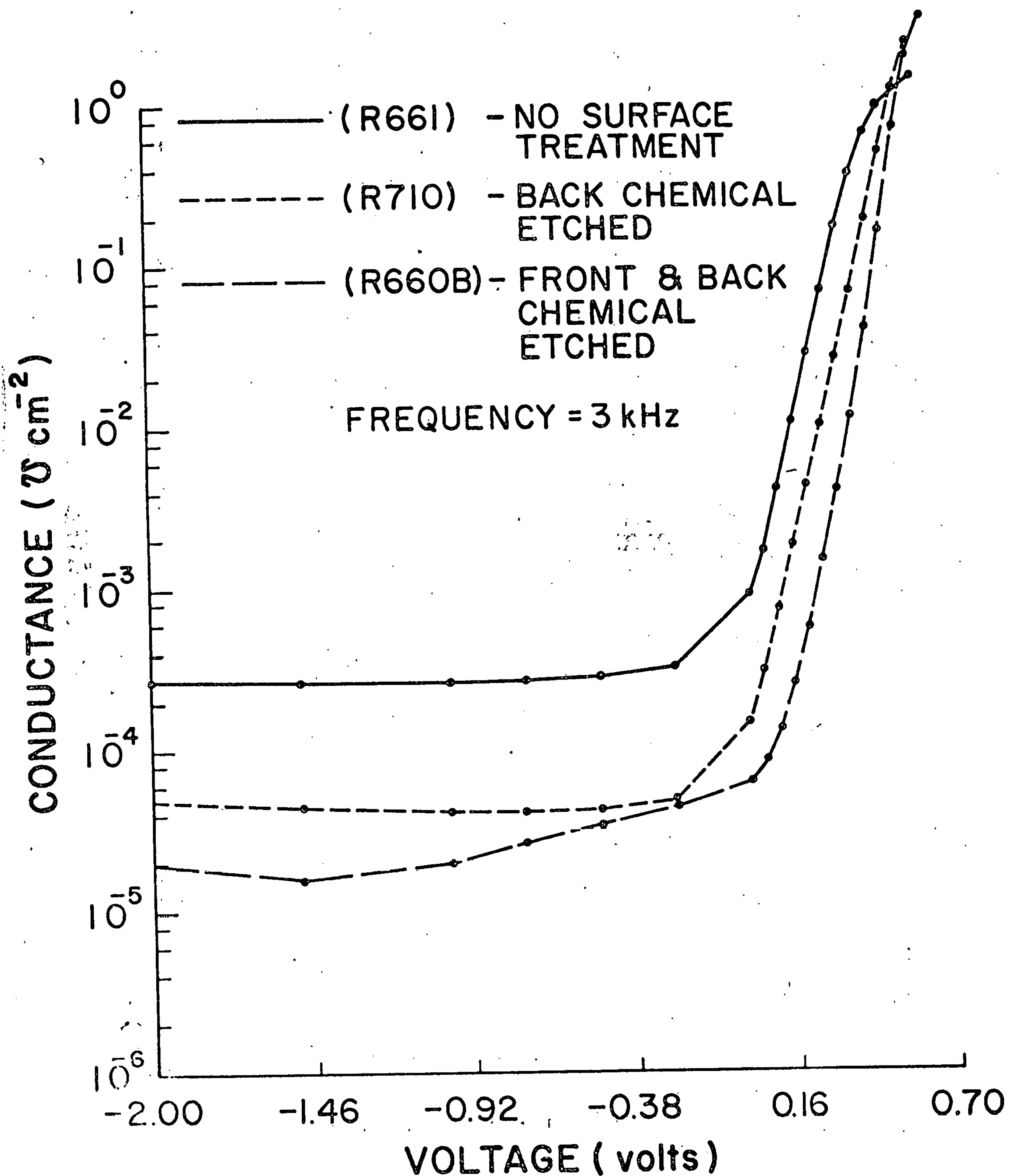


Figure 4.10.: G-V characteristics measured at 3 KHz for devices R661, R 710 and R660B.

bias ($\sim$ 0.2V) so that the depletion mode of behavior continues into this direction. At out 0.4V, the capacitance breaks off from this mode behavior and, reverts to the normal MIS behavior by about 0.6 V. It is within the region of bias, about 0.4 to 0.6 volt, that a large hump appears in the C-V characteristics. The hump is due to the unclamping of the inversion region as the diode becomes more positive. In terms of the interface characteristics, device R661 appears to be weakly depleted with smaller barrier height. The barrier height of device R660B should be greater than device R710. This is indeed the case, as can be seen from Fig. 4.11 and Table 4.2. Fig. 4.11 shows the light I-V characteristics of three samples, and the high V_{oc} device R660B further indicates high barrier height. As expected, the barrier height of device R660B is higher than either devices R661 or R710.

The G-V characteristics of the three samples are shown in Fig. 4.10 In reverse bias and small forward bias the minority carrier concentration does not change appreciably and the conductance varies slowly with the bias. At about 0.2 volts, the current flow increases rapidly with applied bias. In this region the device conductance at a given bias is high for device R661 and low for device R660B. This implies that the dark current in forward bias will be low for device R660B and high for device RR661. The values of conductances for device R710 lie in between that of R661 and R660B. This is supported by the measured forward dark I-V characteristics shown in Fig. 4.12 for the three samples.

The C-V and G-V characteristics of device R660B as a function of frequency are shown in Fig. 4.13 and 4.14. At high frequencies the capacitance can be measured up to 0.65 volts. However, for low frequencies (100Hz) the $\frac{\omega C}{G}$ ratio becomes too small and the capacitance cannot be measured past 0.2 volts forward bias. For comparison, in Figs. 4.15 and 4.16 we have also shown the theoretical C-V and G-V characteristics of ITO-SiO_x-

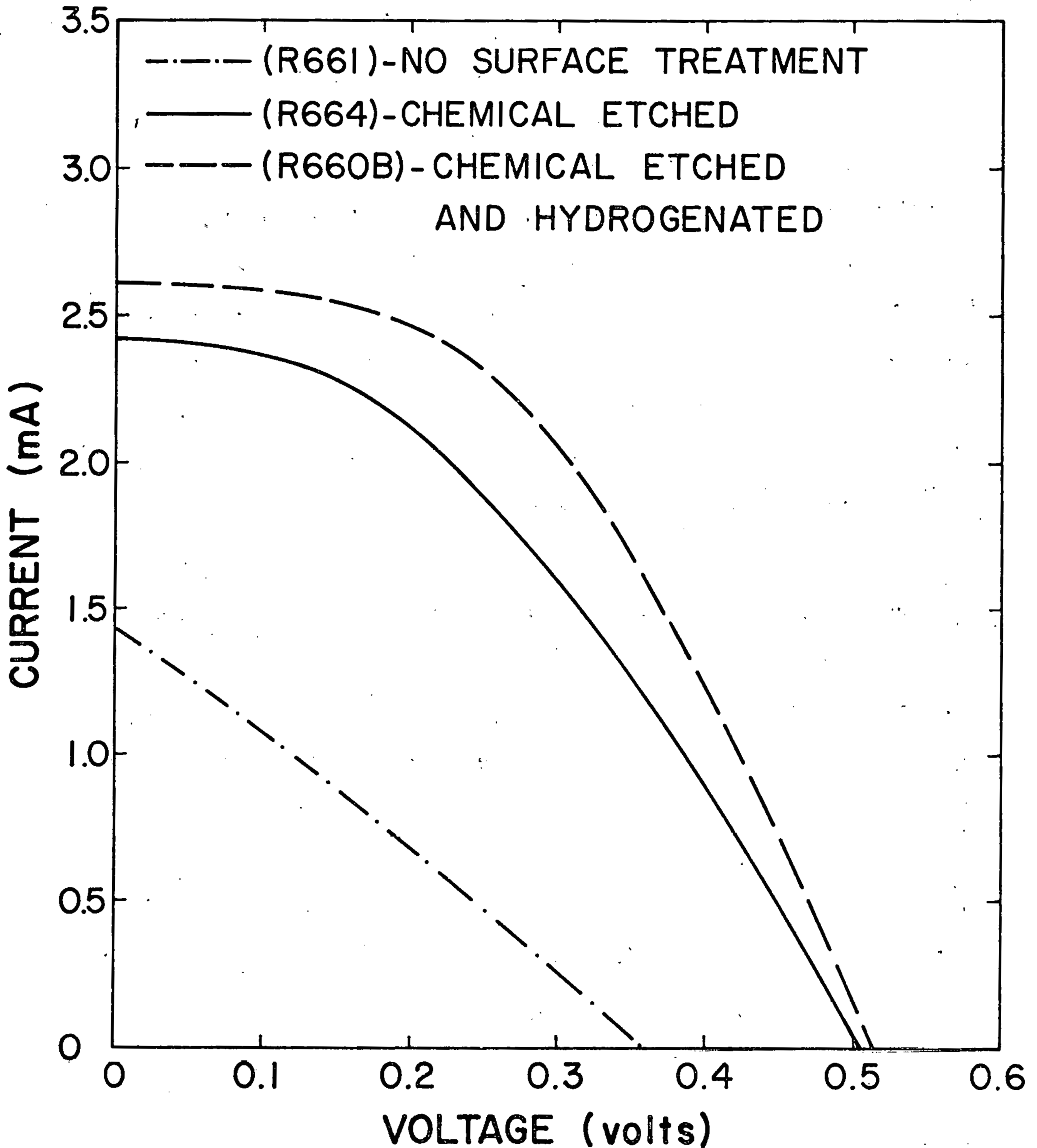


Figure 4.11: Comparison of Light I-V Characteristics of ITO/Si solar cells with no surface treatment versus the chemically etched and chemically etched and hydrogenated devices.

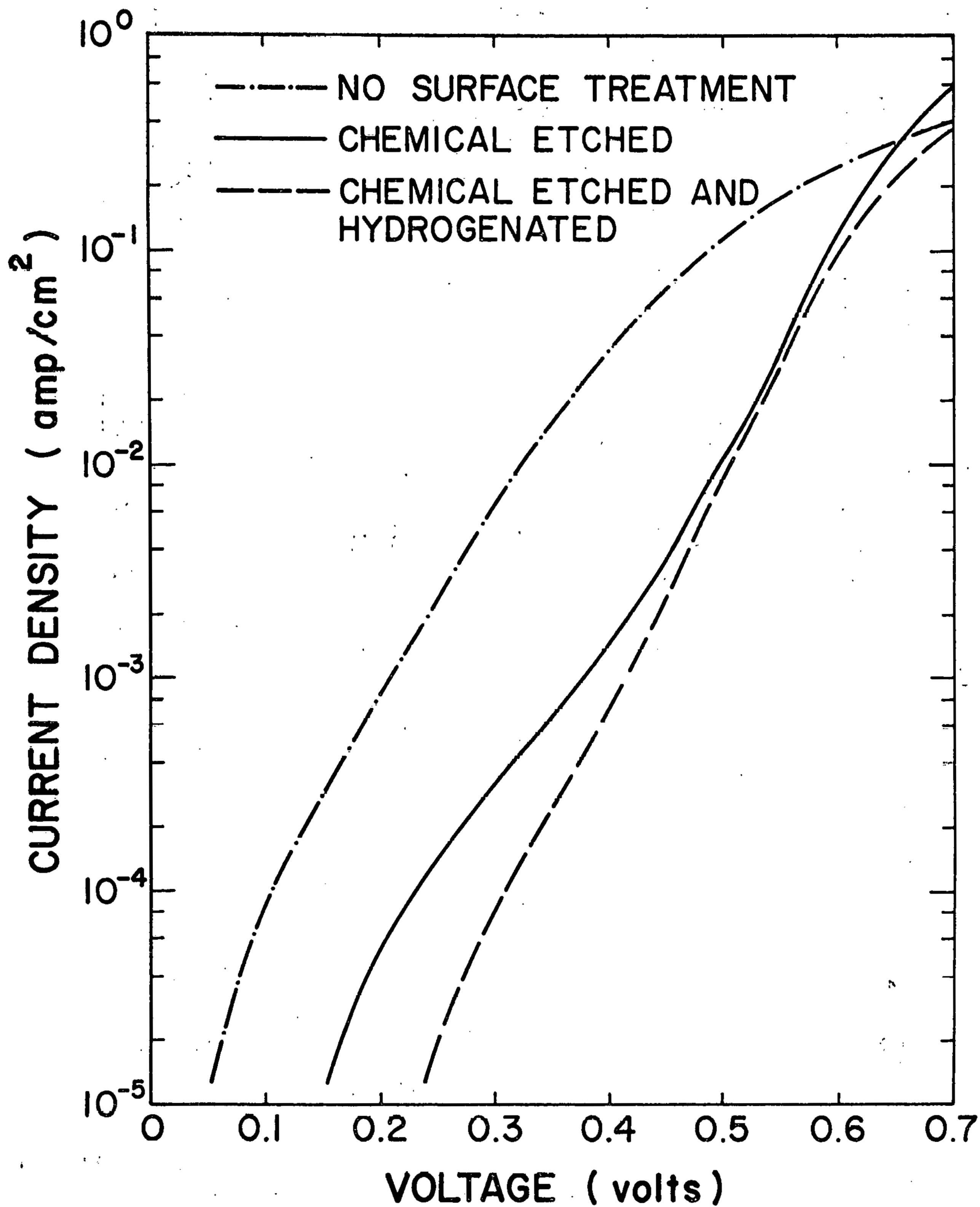


Figure 4.12: Dark I-V characteristics of the three devices shown in the previous figure.

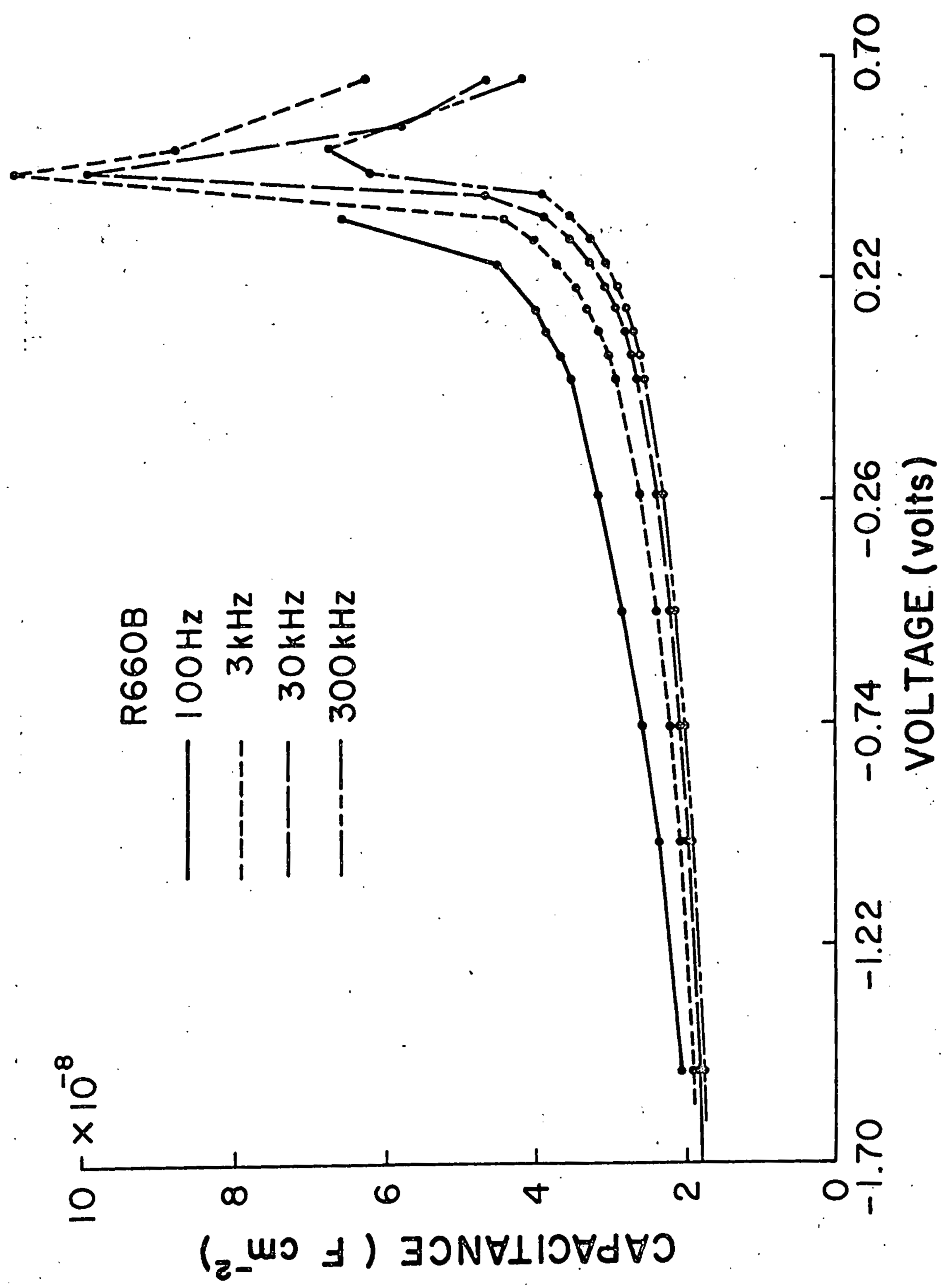


Figure 4.13: Capacitance voltage characteristics of device R660B with frequency as a parameter.

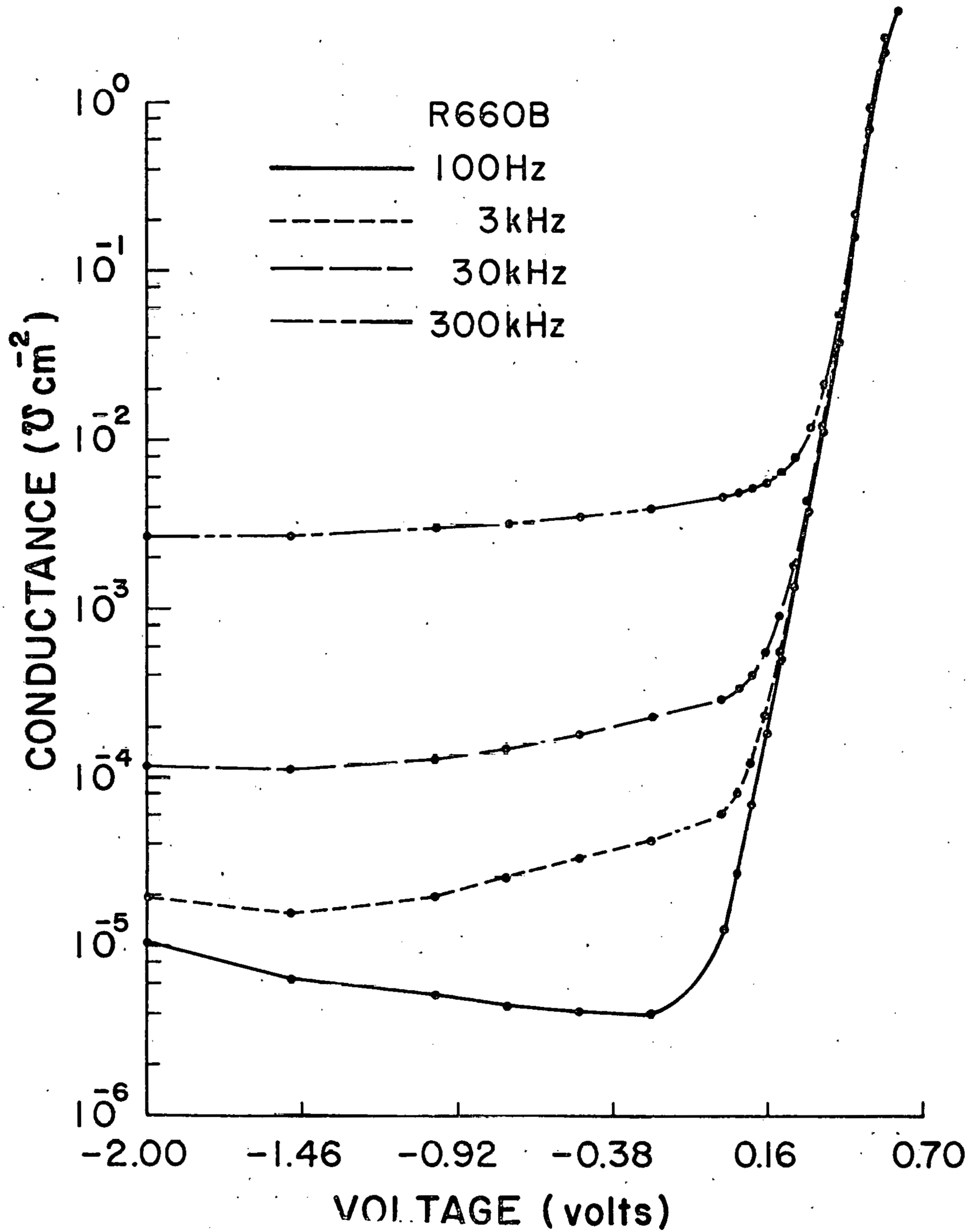


Figure 4.14: Conductance-Voltage characteristics of device R660B with frequency as a parameter.

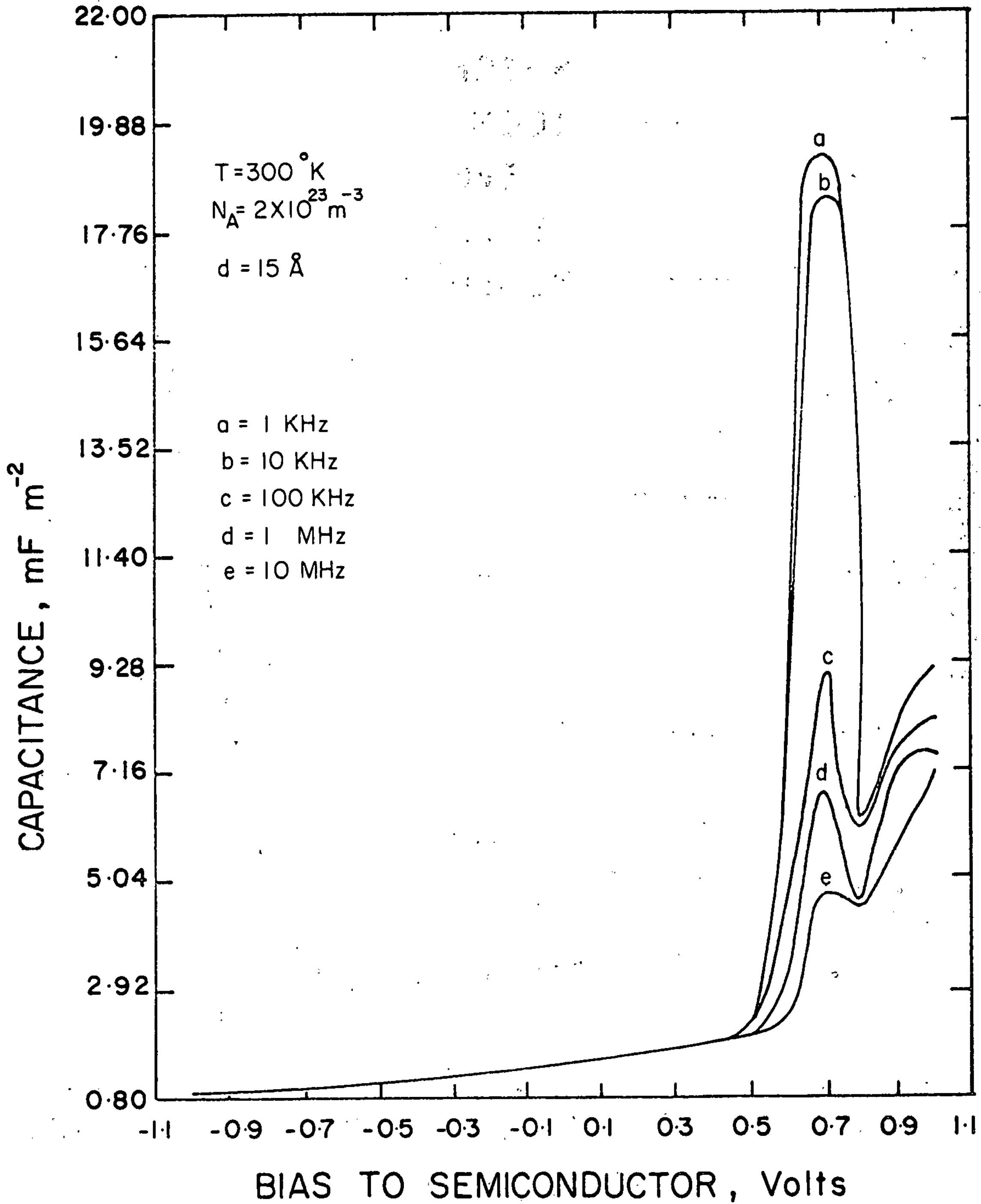


Figure 4.15: Theoretically computed capacitance-voltage characteristics of ITO/Si solar cells. Frequency is shown as the parameter.

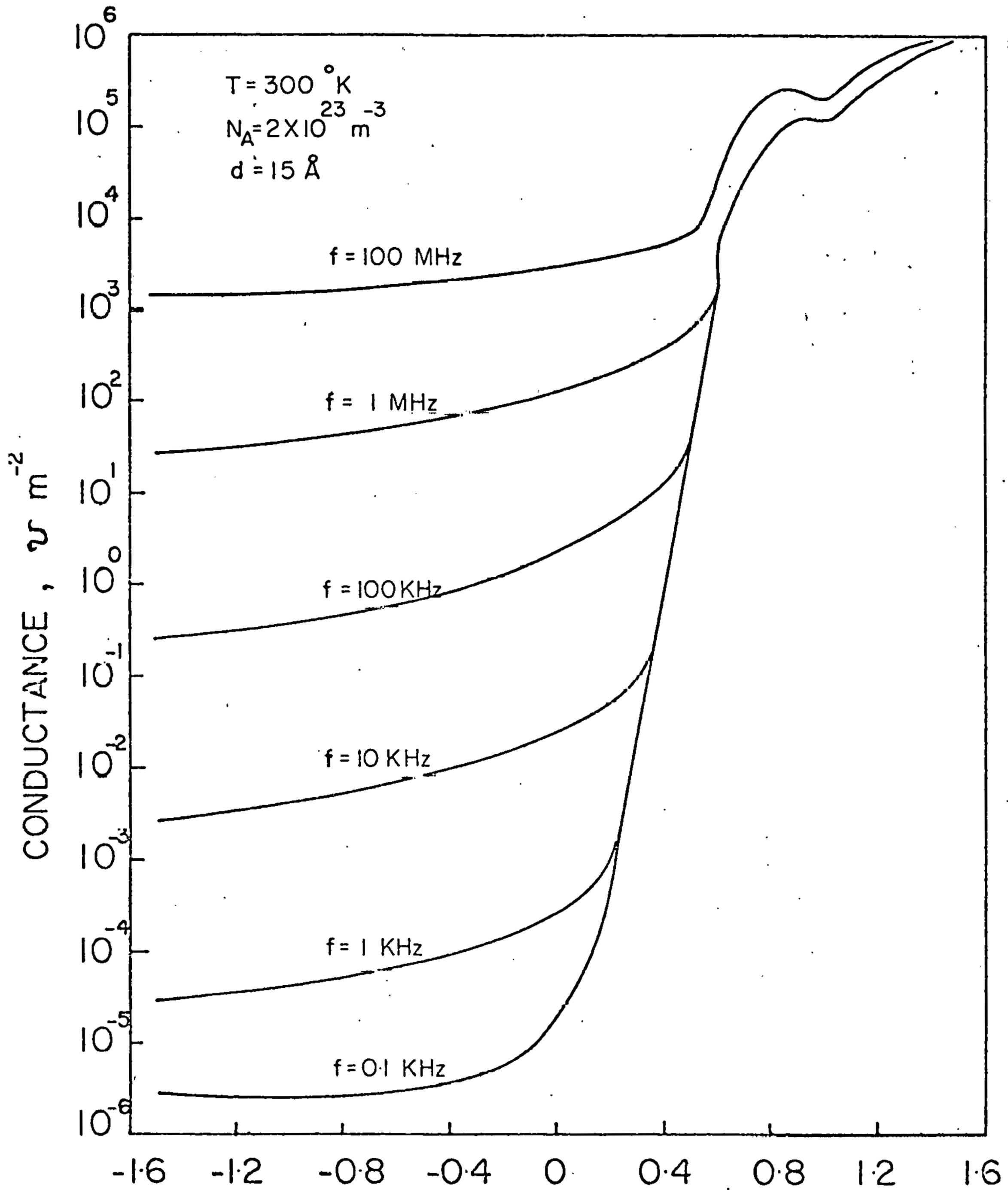


Figure 4.16: Theoretically computed conductance-voltage characteristics of ITO/Si solar cells. Frequency is shown as the parameter.

(p-type) single crystal Si solar cell as a function of signal frequency [3]. The theoretical calculations are based on the equivalent circuit approach outlined by Green [7]. The absolute values cannot be compared due to the following reasons: (a) theoretical results are for single crystal silicon and the experimental results are for polysilicon, (b) the device parameters in experimental devices and theoretical calculations are different. However, the functional dependence is roughly the same. Slight frequency dispersion in the reverse bias C-V characteristics could be due to polycrystalline nature of the substrate and/or an interface that is not strongly inverted. The hump in the C-V characteristics at about 0.4 volt is due to the clamping of the inversion layer as explained before. As expected, G-V characteristics of Fig. 4.14 shows frequency dispersion in reverse and small forward bias. Due to the large amounts of current flowing in these ultra thin interfacial layer ($\sim$ 10 - 15 Å) based devices, we could not measure the C-V and G-V characteristics above about 0.7 volt.

4.8. Results of ITO/Silicon on Ceramic Solar Cells:

Devices were also fabricated on highly defected silicon substrates such as Honeywell dip coated polysilicon on ceramic substrates. The unavailability of substrates prevented any optimization. Nevertheless, good photovoltaic behavior was observed. The device parameters measured at Honeywell Center ate the following:

AM1 (100 mW/cm^2)

V_{oc} = 483 mV

Active Area = 1.17 cm^2

J_{sc} = 24.7 mA/cm^2

FF = 0.75

Efficiency = 8.9%

It is worth mentioning here that the fill factor 0.75 observed in our ITO/Si SIS solar cells is the highest ever seen in any p-n junction device fabricated at Honeywell [9]. Also, the sample used in this work is not one of the best available and we have not optimized the fabrication procedures. The device was made near the edge of the substrate, owing to our mask pattern, and not in the center of the substrate where Honeywell claims they obtain their best devices. The results are consistent with the hypothesis that ion beam sputtering technology is promising and may even have advantages for low quality highly defected substrates.

4.9. Photovoltaic Characteristics of MoO_2/Single Crystal Si Solar Cells:

An I-V curve of a MoO_3 photodiode on 1.0 Ω cm silicon is shown in Fig. 4.17 Photodiode parameters for this cell were V_{oc} = 225 mV, J_{sc} = 14.6 mA/cm^2, and η = 1.7 percent. This I-V curve is characteristic of each of the three silicon resistivities used. In this diode, the photo response in forward bias is reduced because of the high value of series resistance. A probable explanation for the high value of series resistance could be the MoO_3 film resistivity. In comparison to ITO films, where $\rho \approx 2.5 \times 10^{-4}$ Ω cm, these MoO_3 films are 5 orders of magnitude more resistive. Further study needs to be done to identify fabrication parameters that may lower the MoO_3 film resistivity or reduce the impact of this effect.

The photovoltaic output of MoO_3/Si SIS solar cells is poor. As described above, the high resistivity of MoO_3 films may be responsible for this. Another reason could be the high work function of MoO_3 (4.58 eV). More experimental work needs to be done on MoO_2/Si solar cells in the following two directions, before final judgement about it suitability or unsuitability can be passed:

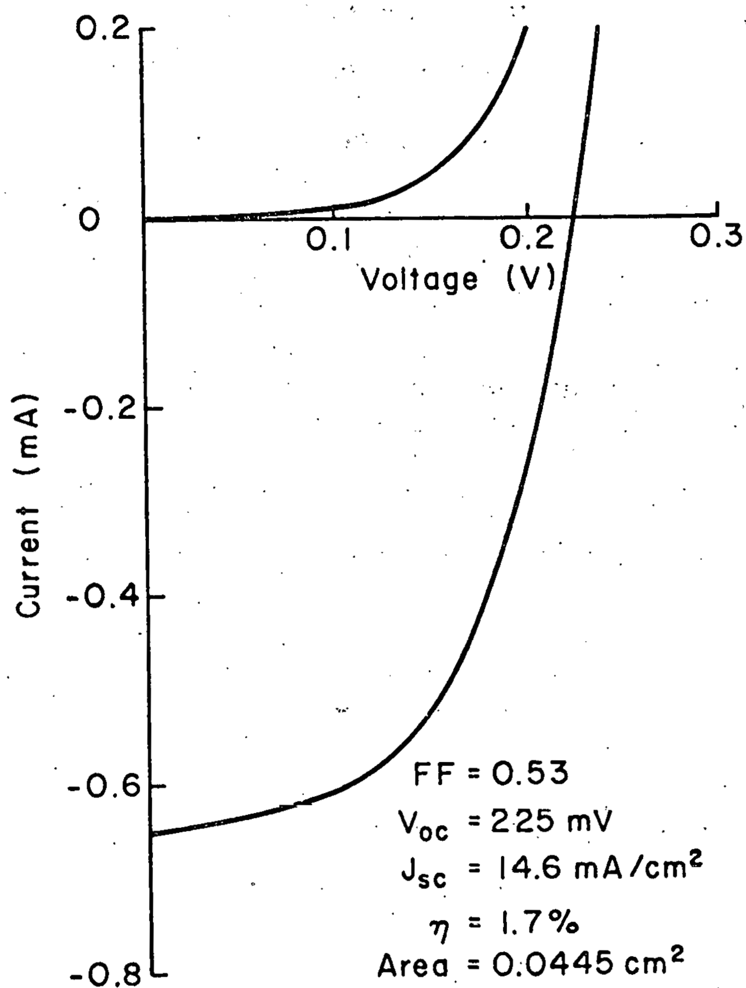


Figure 4.17: Photovoltaic characteristics of MoO_3/Si solar cells.

(i) Control on the resistivity of MoO_3 films

(ii) Measurement of work function and its variability

4.10. Best ITO/Si SIS Solar Cells:

The photovoltaic output of best large area ITO/single and polysilicon SIS solar cells are listed in Table 4.3. It is noteworthy that the efficiencies obtained on Wacker polysilicon devices approach those of single crystal silicon. This supports the conclusions concerning the relative effects of grain boundaries and intragrain defects.

TABLE 4.3

Photovoltaic Output of Best ITO/Si SIS Solar Cells Measured at AM1 (100 mW/cm^2) 28°C

Sub-strate	Total Area (cm^2)	Active Area (cm^2)	V_{oc} (mV)	I_{sc} (mA)	FF	Total Area Efficiency %	Active Area Efficiency %
Single Crystal p-Si <100>	11.46	9.67	526	328.9	0.79	11.9	14.1
Wacker poly Silicon p-type	11.46	9.67	522	322.1	0.79	11.5	13.7
Wacker Poly Silicon p-type	18.64	16.02	522	485.3	0.70	9.5	11.1
Monsanto poly silicon p-type	11.46	9.67	496	267.0	0.77	10.5	8.9

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5. ITO/SILICON INTERFACE

The ITO/Silicon solar cell function is fabricated by sputtering the silicon substrate, exposing the sputtered surface to a background oxygen pressure of 2×10^{-5} Torr at a temperature of 375^{0} C for a short period of time (20-60 sec.) and then depositing ITO over the surface. The interfacial region is a critical part of the ITO/silicon solar cell for both its experimental and theoretical aspects. We investigated four aspects of the interface:

1. Impurities
2. The presence of a SiO_2 layer
3. Growth rate of SiO_2 at reduced pressure
4. Long term stability of the interfacial region

We used Auger sputter profiles to investigate the first three of these. The fourth was considered from a thermodynamic viewpoint and was part of the degradation studies. The results of the investigations are summarized below.

A. Interface Impurities

The freshly sputtered silicon surface is highly reactive and subject to contamination as well as oxidation. Interfacial impurities can arise from a number of sources within the bell jar: residual gases, materials sputtered from the fixturing, impurities within the target, and outgassing from system components, cells revealed little or no impurity contamination in most of the cells tested. Contamination such as carbon, which would indicate the presence of an organic, was not detected despite the presence of carbon in the target. A set of cells had considerable Fe, Ni and Al contamination at the interface as shown in Fig.5.1. These elements resulted from sputtering of the fixturing on to the ITO target.

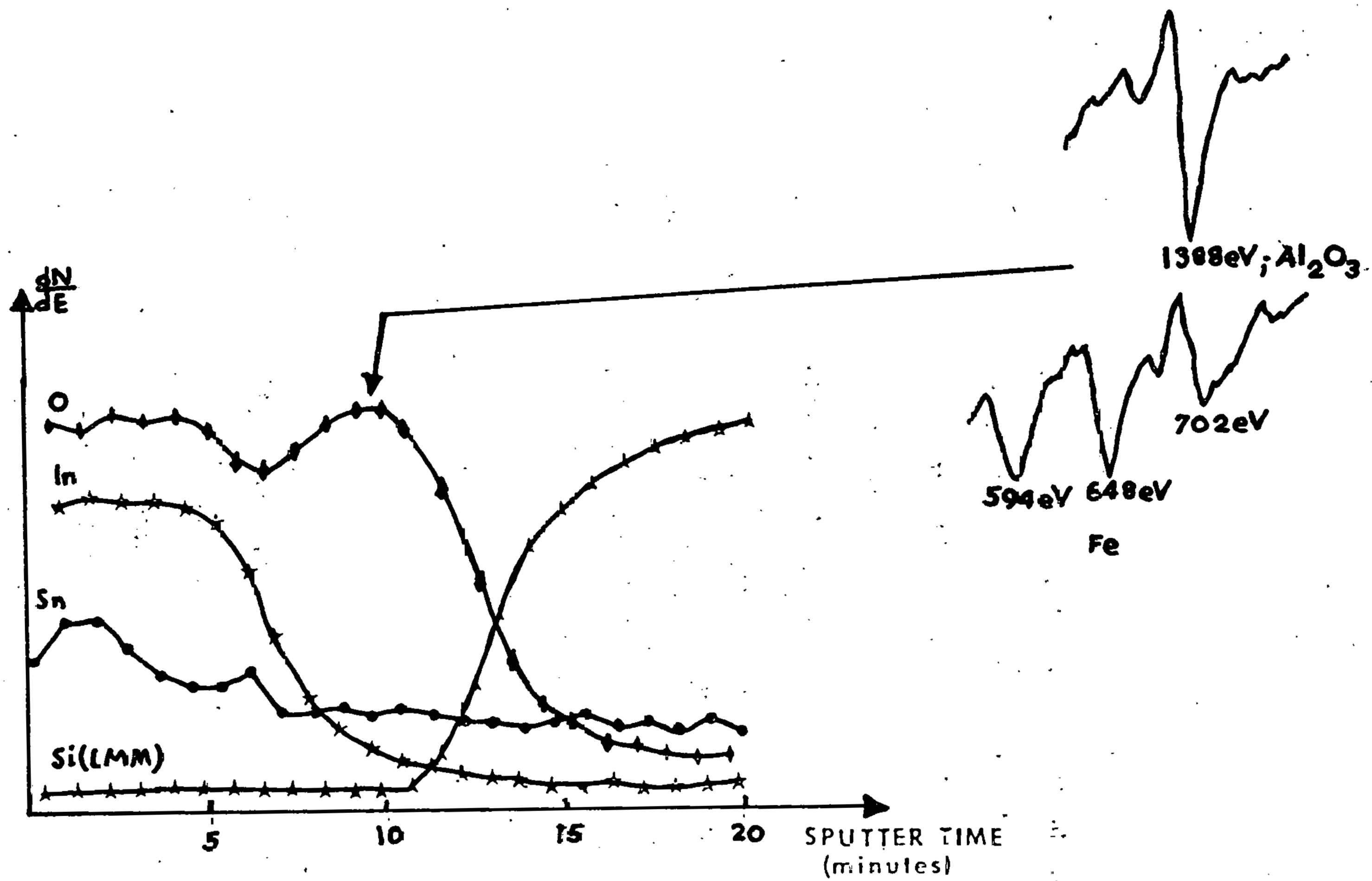


Figure 5.1 Auger Depth Profile and Energy Scan of a Cell Containing Al and Fe Impurities

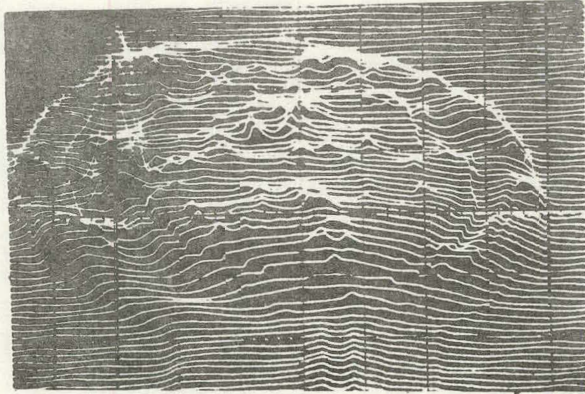
The contaminants greatly effected the cell output as shown in Fig5.2. Ta was also found distributed throughout the ITO layers, Fig5.3. It is thought that the Ta originates from the Ta neutralizer wire of the ion source.

B. Interfacial SiO_2

We have determined that a thin layer of SiO_2 forms during the short time that the sputtered silicon substrate is exposed to 2×10^{-5} Torr O_2 pressure of the vacuum chamber. This was accomplished by Auger sputter profiling thin ITO/silicon cells. The detection of oxygen and silicon at the ITO/Si interface is not sufficient to establish the presence of SiO_2 since the ITO contains oxygen and the substrate is silicon. We used the Si LVV line shape as an indication of the bonding state of the Si. A typical profile and set of line shapes are given in Fig.5.4. The negative peak at 76 eV and the positive peak at 65 eV clearly indicates the presence of SiO_2. There is also an excess layer of oxygen which correlates with the region of Si-O banding. Thus, a thin SiO_2 layer forms during cell fabrication. Further details are given in J. Appl. Phys. 50, 4172 (1979).

C. Growth of SiO_2

We examined the oxidation of chemically cleaned and sputtered silicon surfaces. The oxidation of chemically cleaned surfaces was useful for establishing Auger signatures for thin oxides and allowed us to examine the SiO_2/Si transition region. The apparent width of the transition region for various thicknesses of SiO_2 is plotted in Fig5.5. From these curves, and a knowledge of the mean escape depth of the Auger



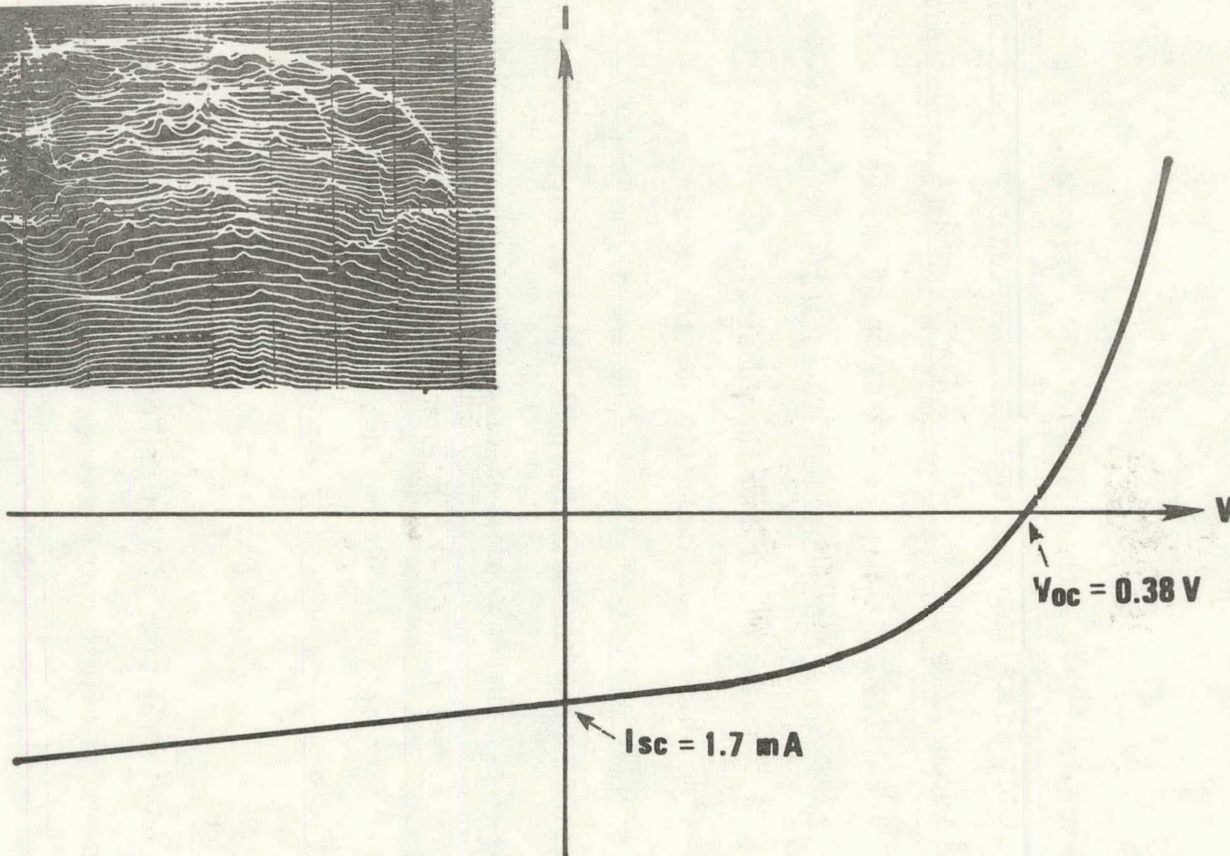
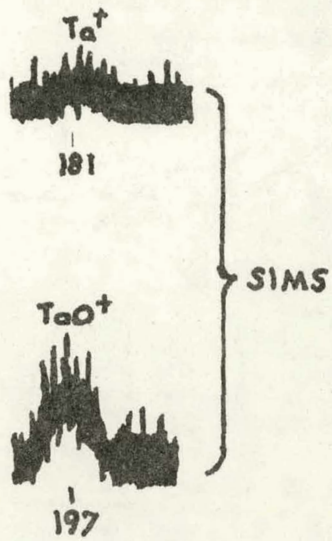


Figure 5.2. A SLS map and an I-V curve for a cell containing Al and Fe impurities.



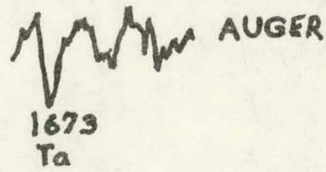


Figure 5.3. SIMS and Auger Scans Showing Evidence of Ta in the ITO

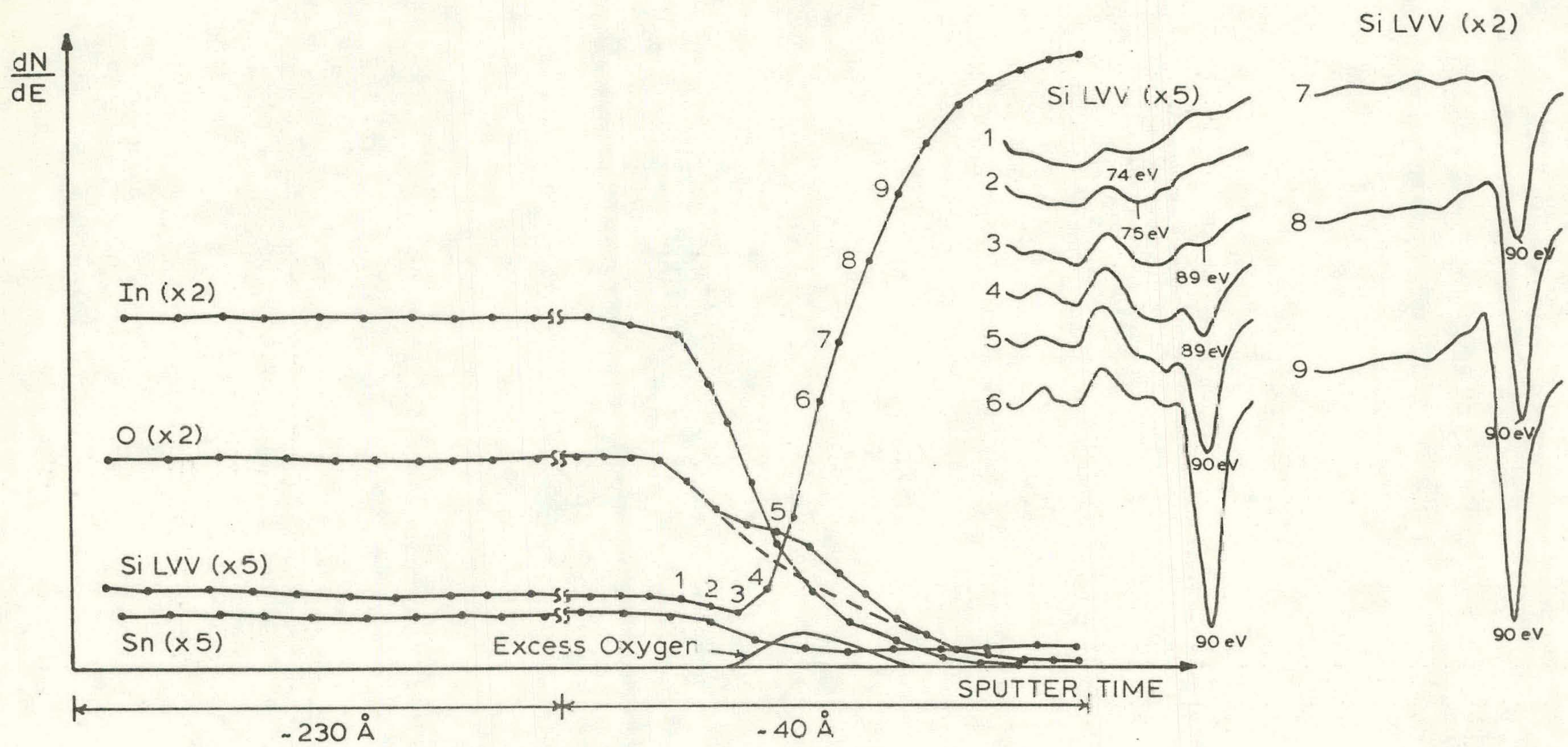


Figure 5.4. Auger profile of a ITO/Si solar cell showing the excess oxygen and the silicon LVV line for SiO_2.

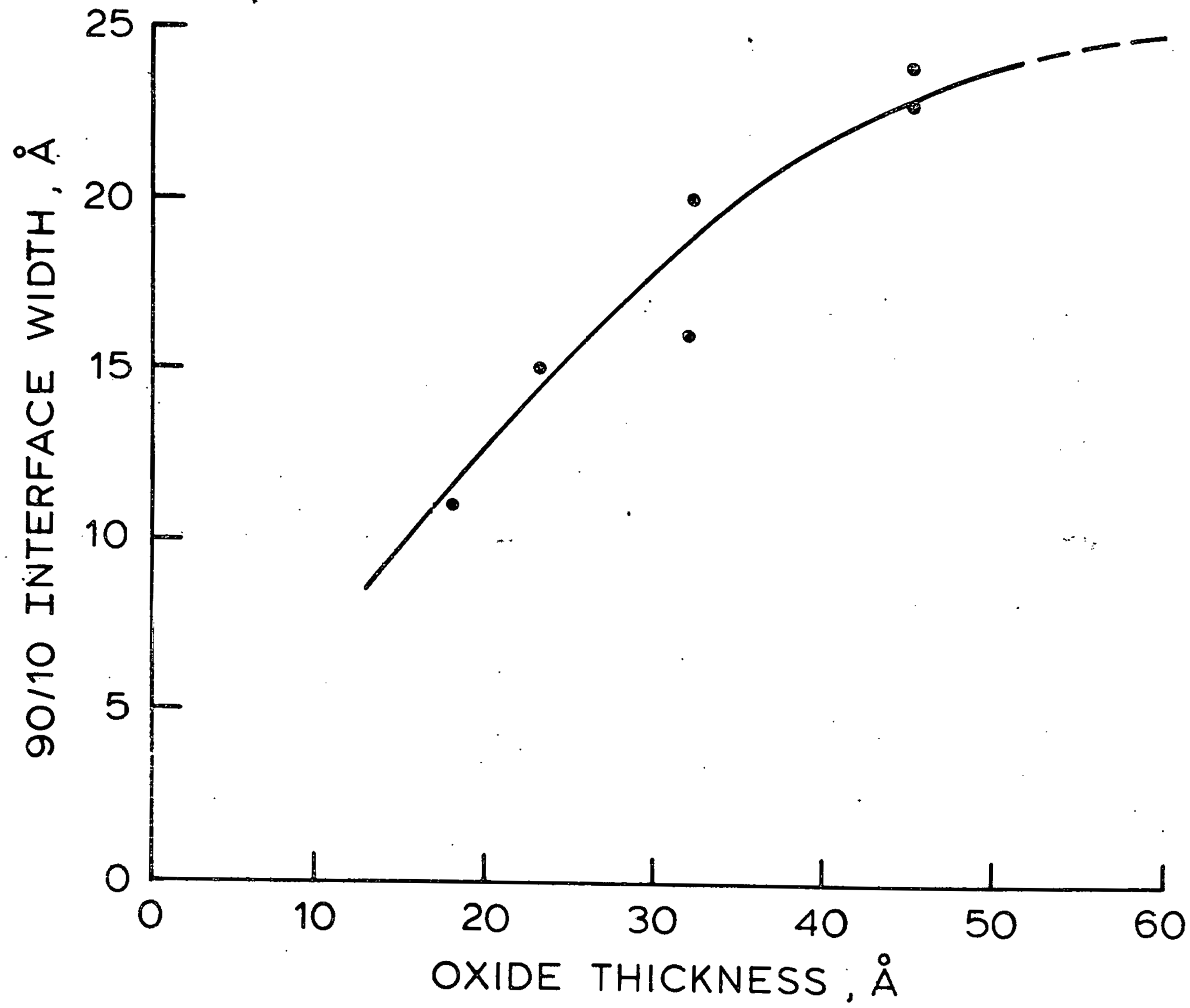


Figure 5.5. Apparent SiO_2/Si interface thickness versus total oxide thickness.

electrons and sputter broadening affects, it was determined that the oxide layers were almost 100% SiO_2 with a small (3-5Å) transition region. However, the thickness of the thin oxides is thought to be highly non-uniform as shown in Fig. 5.6.

In the experiments on the oxidation of sputtered surfaces, single crystal silicon wafers were heated to a given temperature in an UHV system which has a background pressure of less than 10^{-9} Torr. The surface was sputtered, the chamber back filled with oxygen to a pressure of 2×10^{-5} Torr to expose the surface for various lengths of time. The resulting oxides were then Auger sputter profiled. The thicknesses of these oxides were estimated by comparing their profiles with those of standard oxides grown outside the vacuum chamber.

Oxides grown on sputtered surfaces at 50, 275 and 350°C were investigated. At a substrate temperature of 275°C oxides were grown with exposure to 2×10^{-5} Torr for 10, 30 and 300 seconds, at 10^{-3} Torr O_2 for 5400 seconds and for no intensional O_2 exposures. The normalized Si Auger LVV lines profiles for these oxides are illustrated in Fig. 5.7. One can observe the monotonic progression of the curves indicating increased oxidation with exposure time. Fig. 5.8. compares the profiles of a 17Å thick standard oxide with that of the 10^{-3} Torr 5400 sec in situ grown oxide. A close similarity is apparent.

In order to obtain a more quantitative growth curve, the estimated in-situ-grown oxide thickness vs. the log of O_2 exposure in Langmuir's is plotted in Fig. 5.9. The oxide thickness was estimated by calibrating the sputter rate and taking the 90% level as the substrate surface. The resulting plot is a straight line. This suggests that the oxide growth is a logrithmic function of O_2 exposure. Using this graph a preliminary estimate of the oxide thickness grown during ITO/Si cell fabrication can

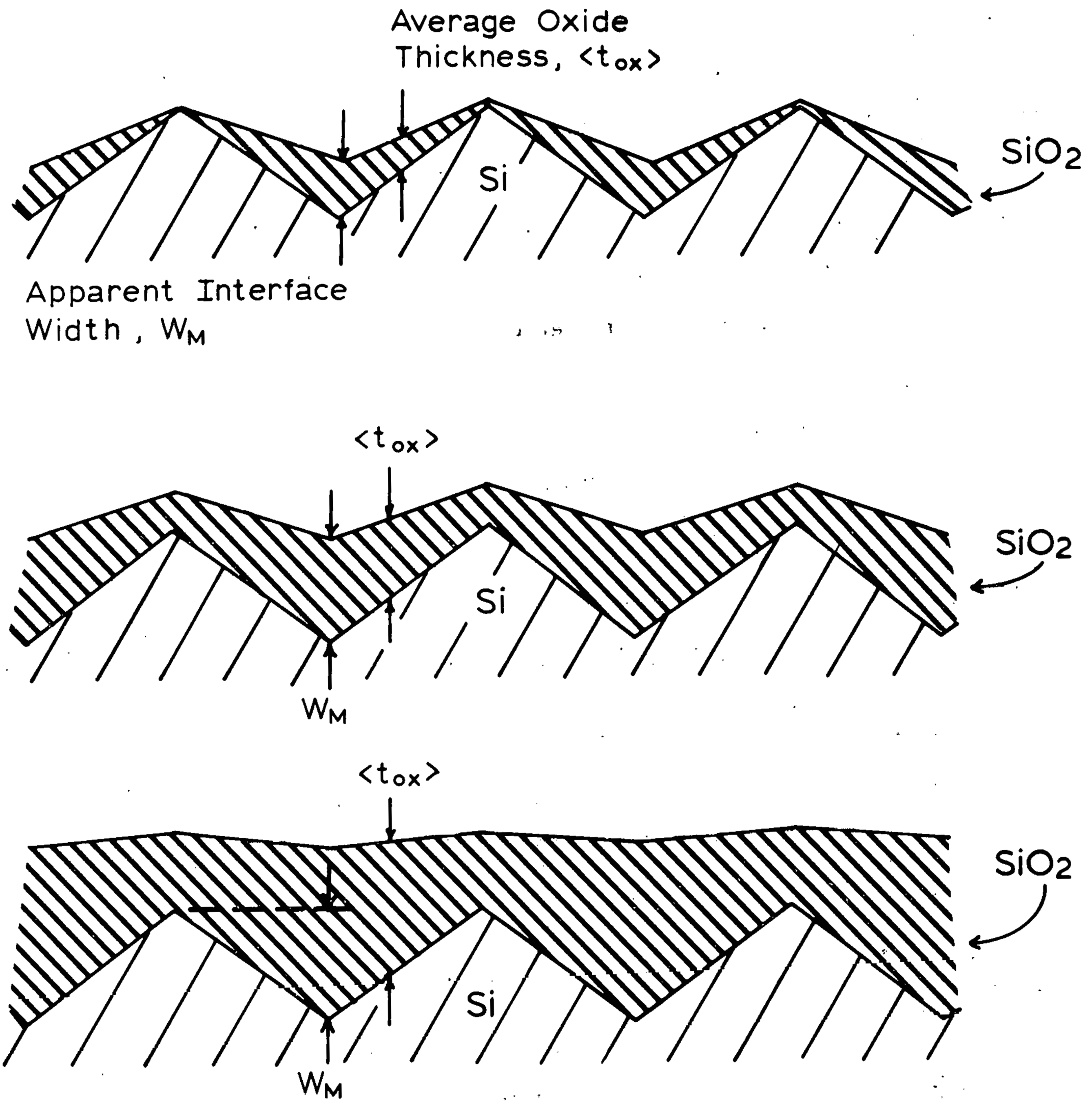


Figure 5.6. Model for nonuniform SiO_2 growth.

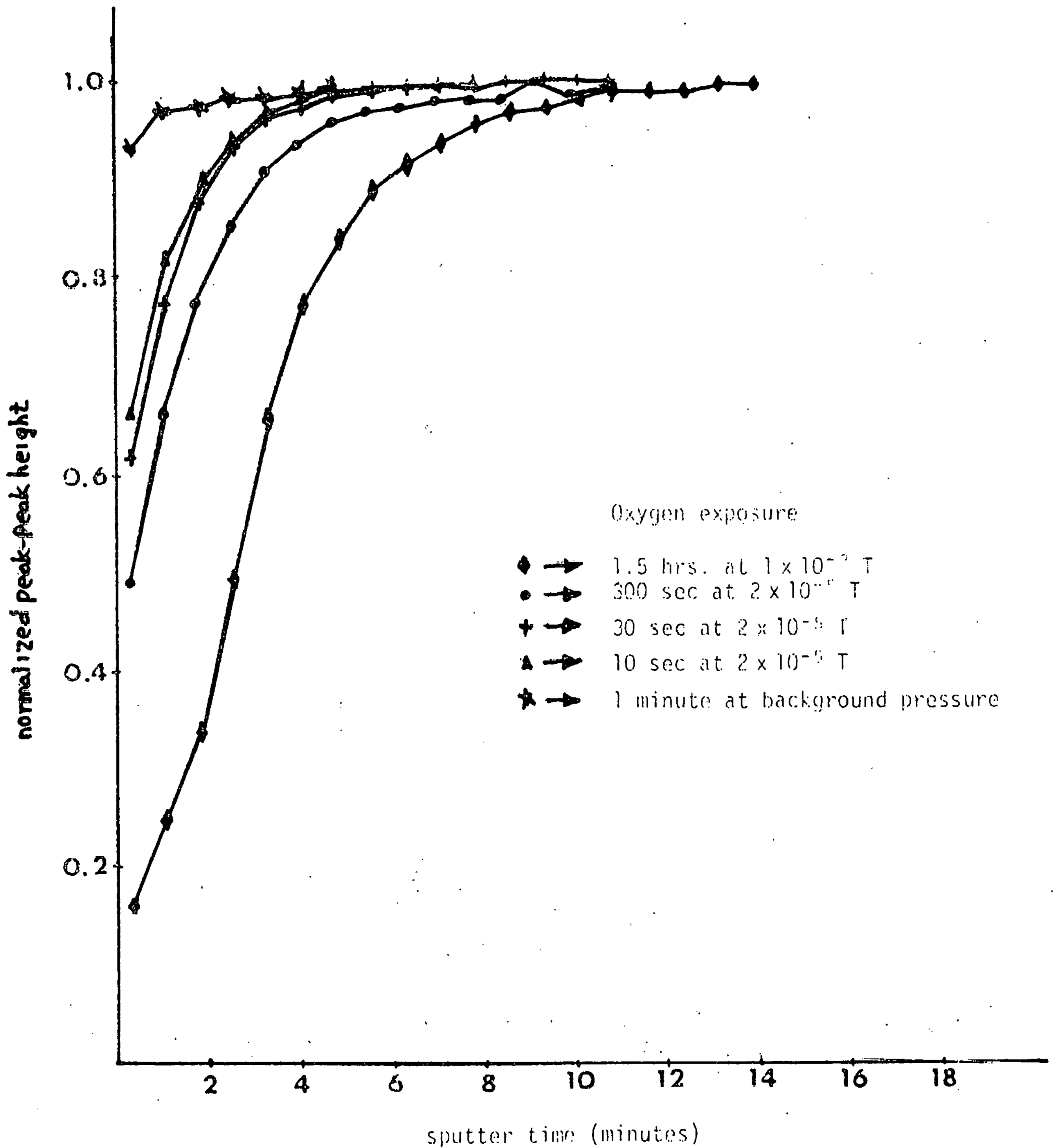


Figure 5.7. Normalized peak to peak height of Si LVV lines vs. sputter time for reoxidized sputtered silicon. In each case, silicon was prepared by sputtering with 1 keV Argon ions.

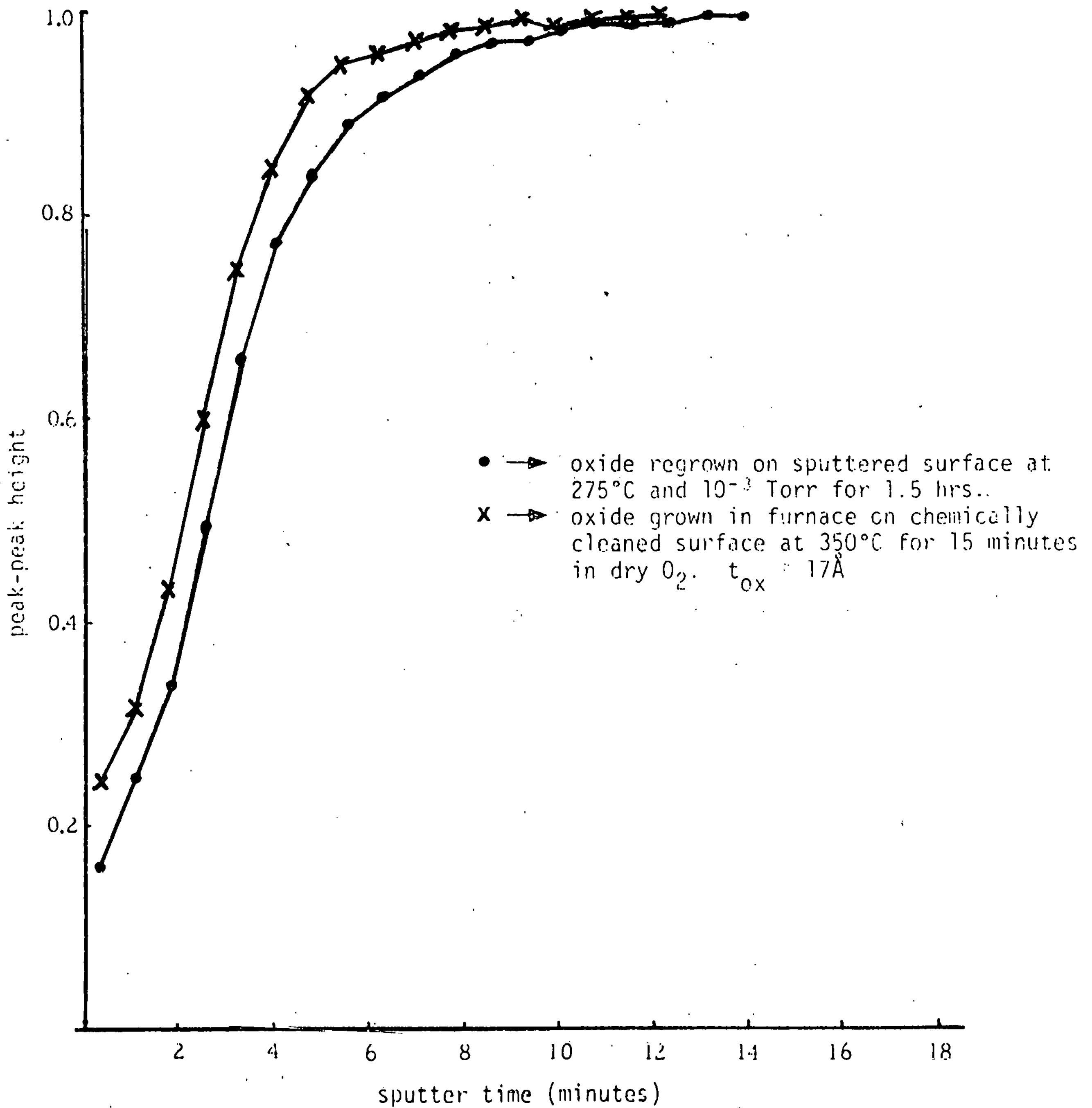


Figure 5.8. Comparison between furnace grown oxide (~17Å) and in-situ oxide grown on sputtered surface.

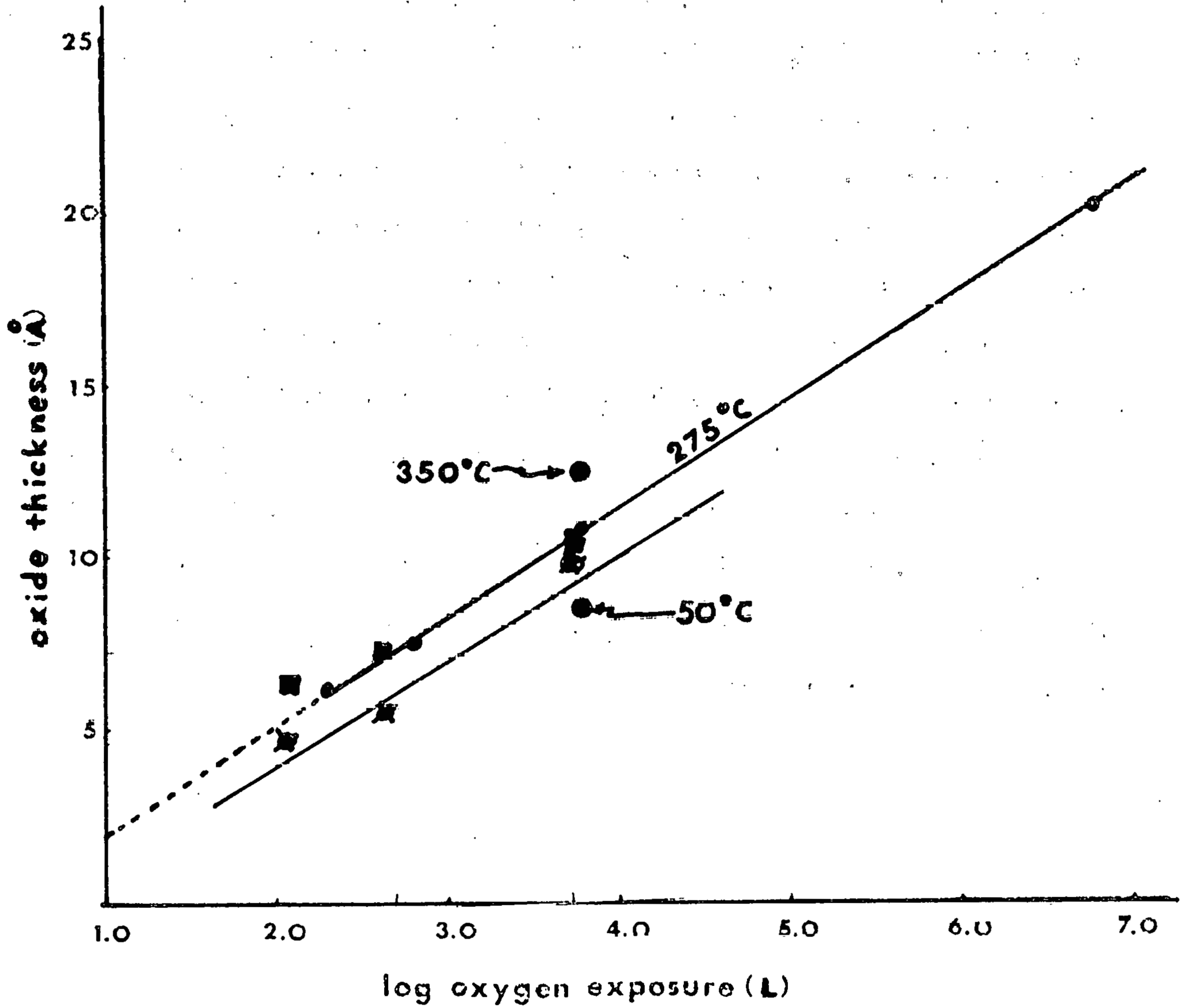


Figure 5.9. Oxidation rate of 1 KV Ar^+ sputtered silicon showing points from several temperatures.

be made. The exposure of the sputtered Si surface in cell fabrication is not a constant but varies from 20 to 60 seconds which corresponds to an O_2 exposure of between 400 and 1200 Langmuirs. From the graphs it is estimated that this would results in 7 to 11 Å of SiO_2. These values should be considered as estimates but appear to be reasonably accurate.

Additional data obtained from intensity ratios of the ESCA line show that the initial layers of SiO_2 grow very rapidly buty rapidly but then reach a near saturation thickness. The "saturation" thickness was observed to be a function of temperature, pressure and sputter conditions. For example, at 375° C the saturation thickness at 10^{-4} Torr O_2 pressure was 40% greater than for surfaces exposed at 10^{-5} Torr.

It can be concluded that an SiO_2 layer easily forms during the fabrication of the ITO/Si solar cells. Apriori control of the thickness of this layer, however, is dependent upon better understanding of oxydation as a function of pressure, temperature, and substrate surface states. The logarithmic dependence of oxidation upon O_2 exposure indicates that, with reasonable control of temperature, partial pressures, and time, repeatability may be achieved.

6. ANALYSIS OF ITO/Si SOLAR CELLS

During the course of this contract, three techniques were developed to analyze ITO/Si SIS solar cells which are equally applicable to other solar cell types. These are (i) an automated electronic test system, (ii) automated steady state admittance spectroscopy for surface-state analyses, (iii) noise spectral density measurements as a reliability predictor and contact diagnostic. In this section details of each of these techniques is described.

6.1. AUTOMATED ELECTRONIC TEST SYSTEM

A block diagram of the test system is shown in Fig. 6.1. The device under test can be mounted in a solar simulator for measurements near room temperature at intensities from 0 to 2 suns. The cell can also be mounted in a vacuum chamber on a Peltier junction attached to a cold finger at -173^{0} C for measurements from -170 to +50^{0}C with or without illumination from an ELH lamp or monochromatic light. The current is measured by monitoring the voltage across a 1 ohm precision resistor with a Keithly volt meter. The capacitance is measured with a 1 MHz Booton capacitance meter, with the analog output being monitored by one channel of the analog to digital (A/D) converter. The temperature of the device under test is measured by an Omega digital thermometer with an analog output and monitored by the 9825 through another cahnnel of the A/D. The bias voltage across the cell is also monitored by a channel of the A/D. The cell is capable of being biased from -10 to +10V automatically by writing the appropriate bit string to the digital to analog (D/A) converter.

An overview of the HP 9825 software which controls the system is presented as a Warnier-Orr diagram in Fig. 6.2. The leftmost brace represents the entire solar cell test system. The first entry at the top

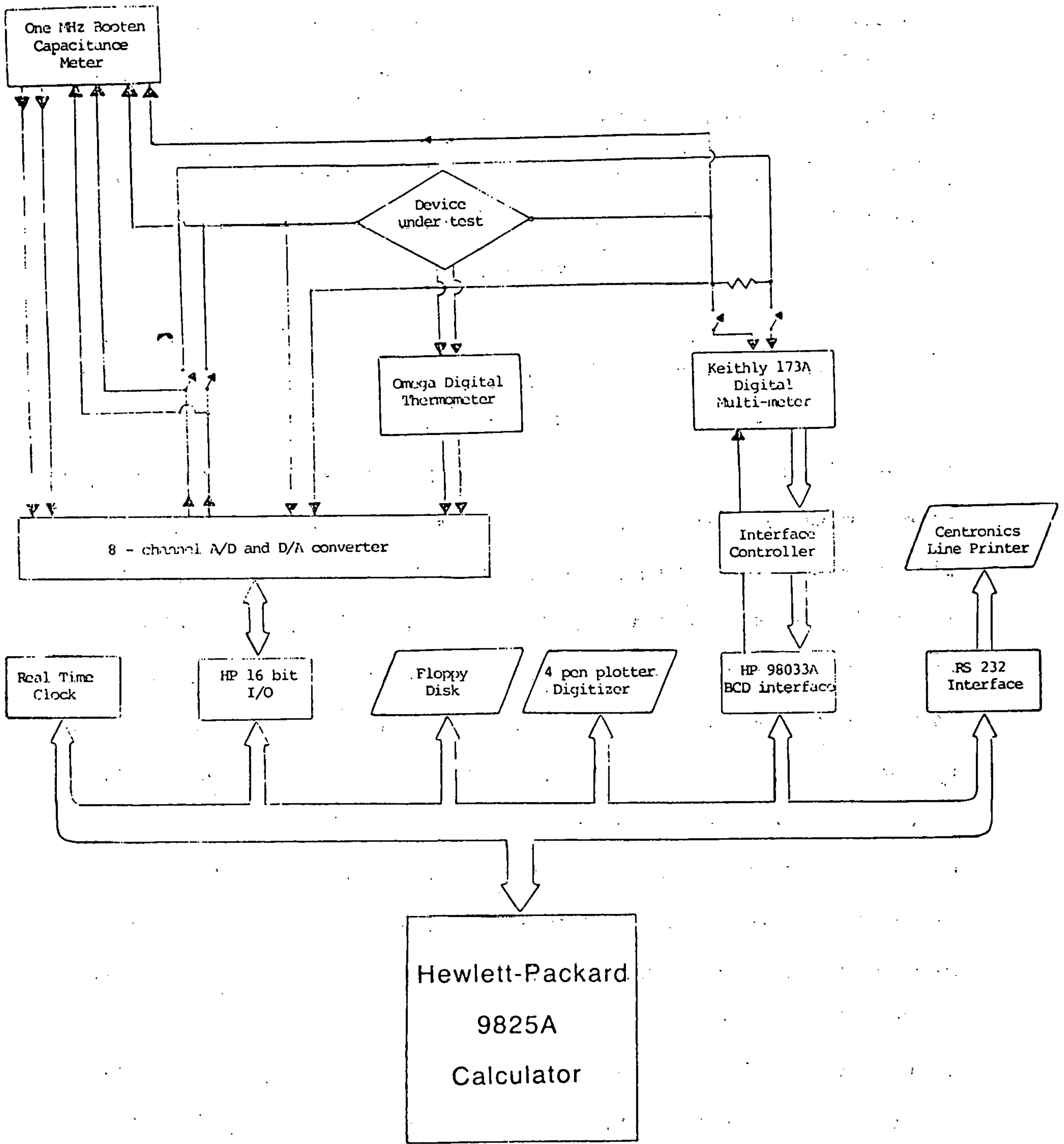


Figure 6.1. A block diagram of the automated solar cell test system.

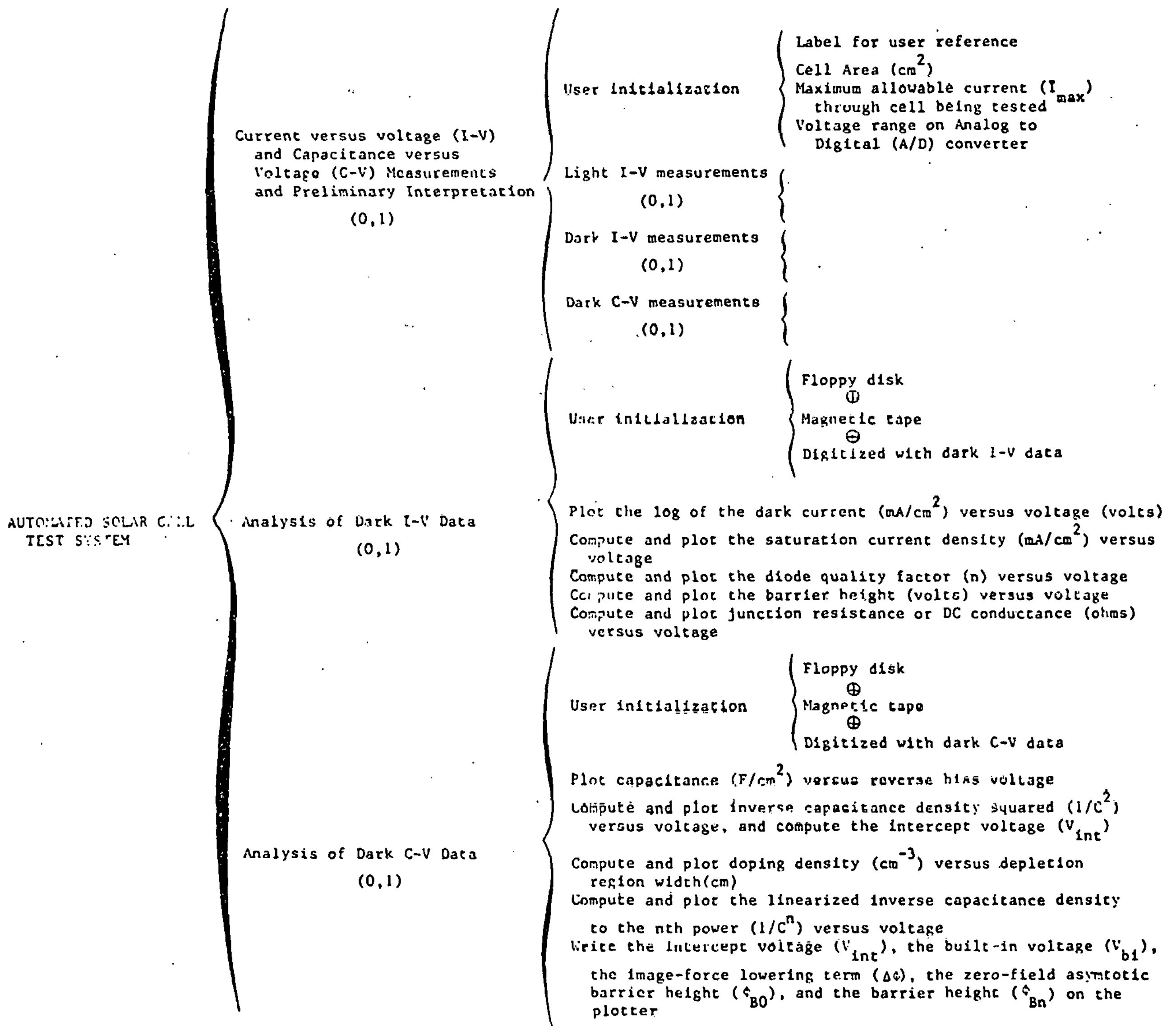


Figure 6.2. A Warnier Diagram of the Automated Solar Cell Test System

right of the leftmost brace is the process structure controlling the test apparatus in Fig. 6.1. for light I-V, dark I-V, and dark C-V measurements at a given temperature and illumination. This section also computes the efficiency, open circuit voltage, short circuit current and fill factor at a given illumination and temperature for light I-V measurements. The light I-V curve for a typical indium tin oxide (ITO) solar cell is shown in Fig. 6.3. The second section of the test system performs dark I-V analysis of the measured data at a given temperature. The barrier height as obtained from the saturation current density (J_s), based upon thermionic emission-diffusion theory for metal-insulator-semiconductor devices as given by:

$$\phi_{Bn} = \frac{kT}{q} \ell n \frac{A^{**}T^2}{J_s} \tag{6.1}$$

The third section analyzes the C-V data in reverse bias using the differential capacitance method discussed by Ngayen et al. [13] to determine the built-in voltage and barrier height. This technique allows for doping densities which are of the form

$$N_D = \alpha X^{\beta} \tag{6.2.}$$

where X is the depletion region width. The constants α and β are obtained from

$$N_D = \frac{-2}{q\varepsilon} \frac{\partial(A^2/C^2)}{\partial V^2} \tag{6.3.}$$

where ε is the dielectric constant of the semiconductor and A is the device area. Poisson's equation can be integrated to obtain:

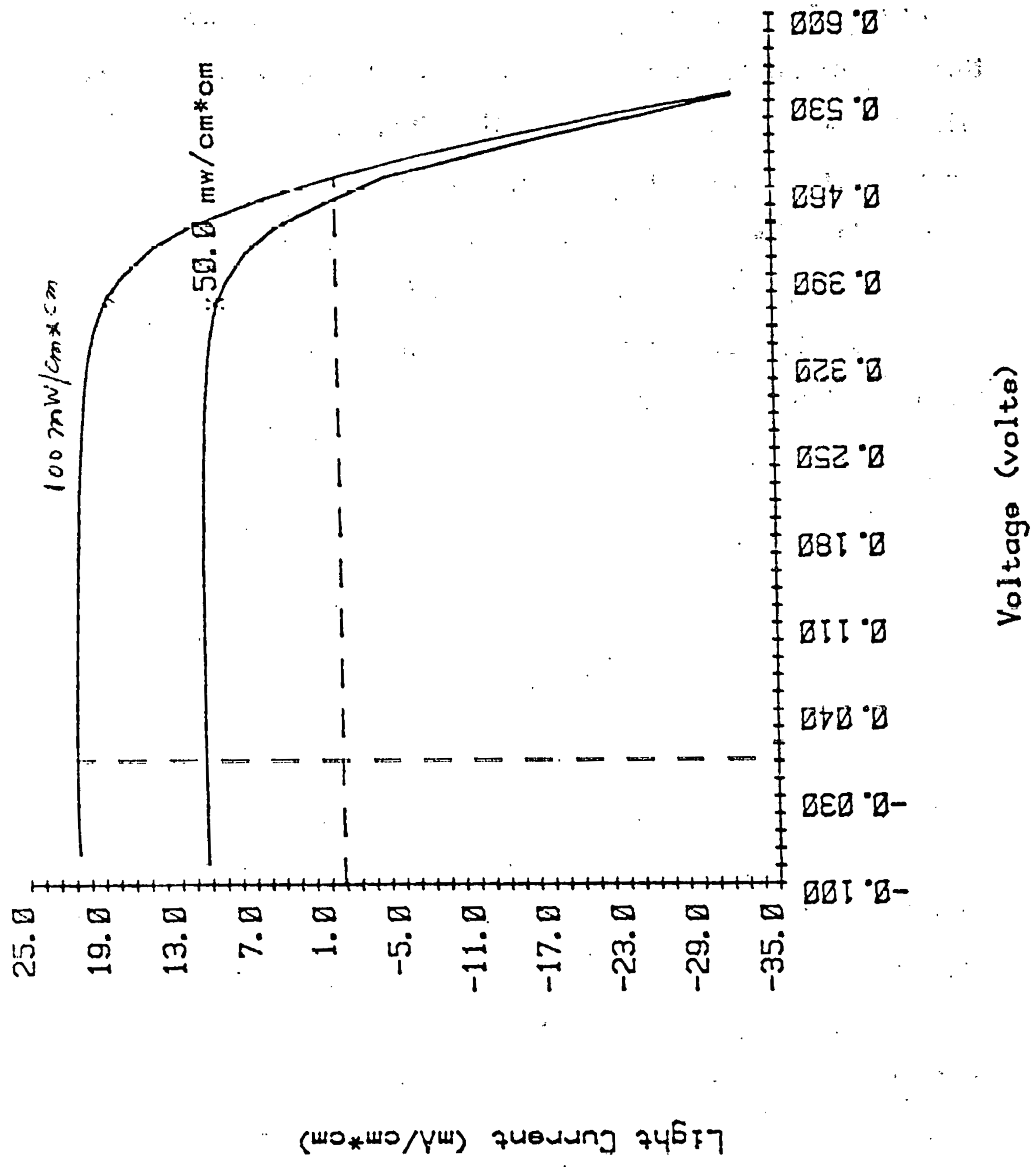


Figure 6.3, Current versus voltage for run #170 under two illumination Intensities.

$$\left(\frac{A}{C}\right)^{\beta+2} = \frac{\beta + 2}{q\alpha\ c^{\beta+1}} (V_{int} - V) \quad (6.4.)$$

which is plotted on the four pen plotter as $(A/C)^{B + 2}$versus V. The intercept voltage obtained from the above function is more reliable than V_{int} calculated from $1/C^2$ data becasue the doping profile is relaxed from being uniform with depth. This point may be quite significant. It is well known that mobility variations and doping nonuniformities have significant impact on weakly inverted MIS structures. The resulting potential fluctuations could also have significant impact on MIS/SIS solar cells in ways normally attributed to other mechanisms, but these effects have not been evaluated to date.

The built-in voltage (V_{bi}) is:

$$V_{bi} = V_{int} + \frac{kT}{q} \quad (6.5)$$

The barrier height can then be computed assuming conservation of energy

$$\phi_B = V_{bi} - \Delta\phi + \frac{E_c - E_f}{q} \quad (6.6)$$

where $\Delta\phi$ is the Schottky barrier lowering and $E_c - E_f$ is dependent on the temperature and material being studied. Equations 6.4, and 6.5., and 5.6, are shown graphically in Fig. 6.4 for a typical ITO/SI solar cell.

The fourth section is capable of performing a variety of transient capacitance measurements of processes occurring on a 1 m/sec or shorter time scale. The cell is mounted on a cold finger equipped with an optical window and a thermoelectric cooler. This permits controlled operation over a liquid nitrogen to 100°C temperature range. The thermal activation energy for traps can be measured by reverse biasing the cell and observing the change in capacitance as the temperature is varied.

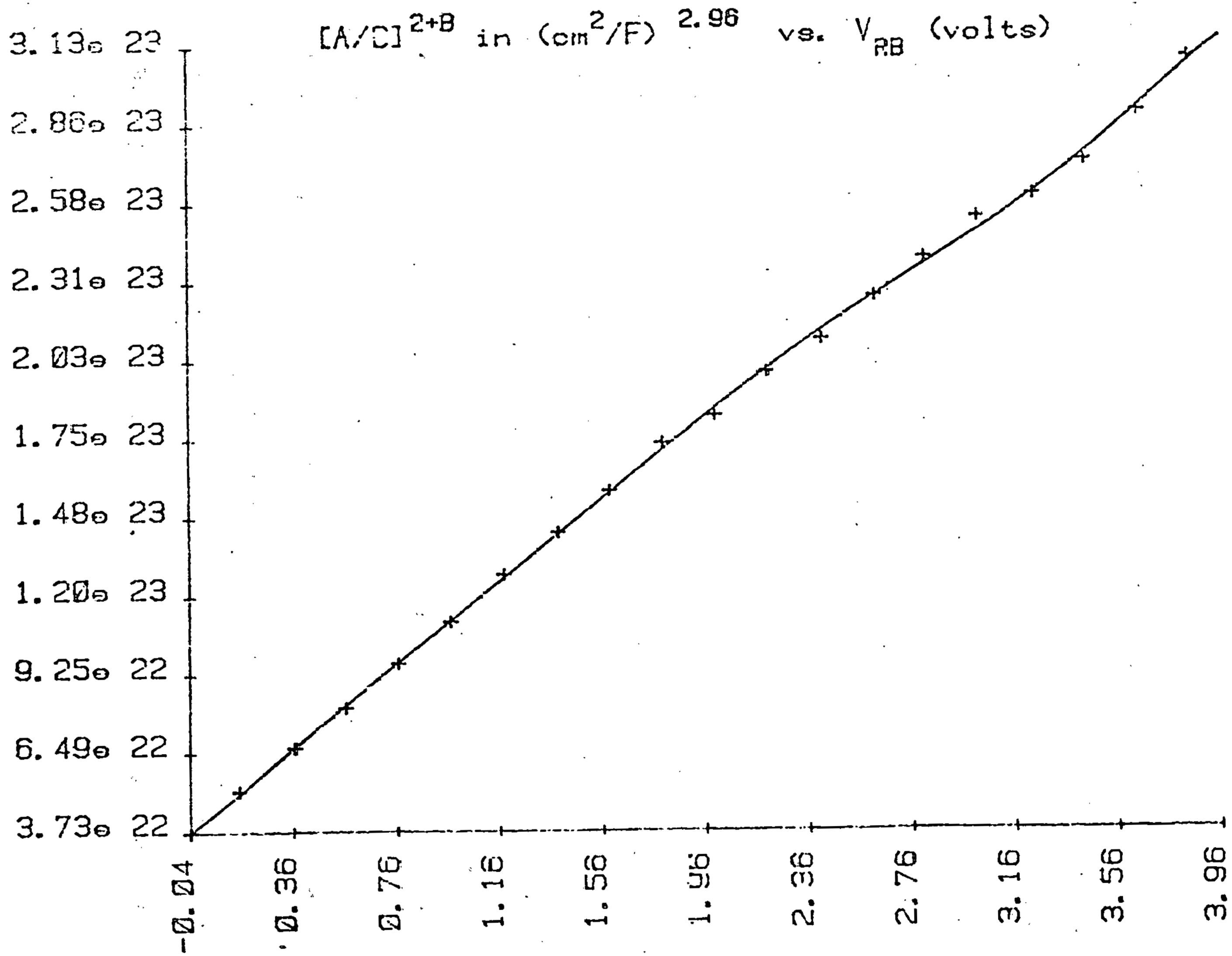


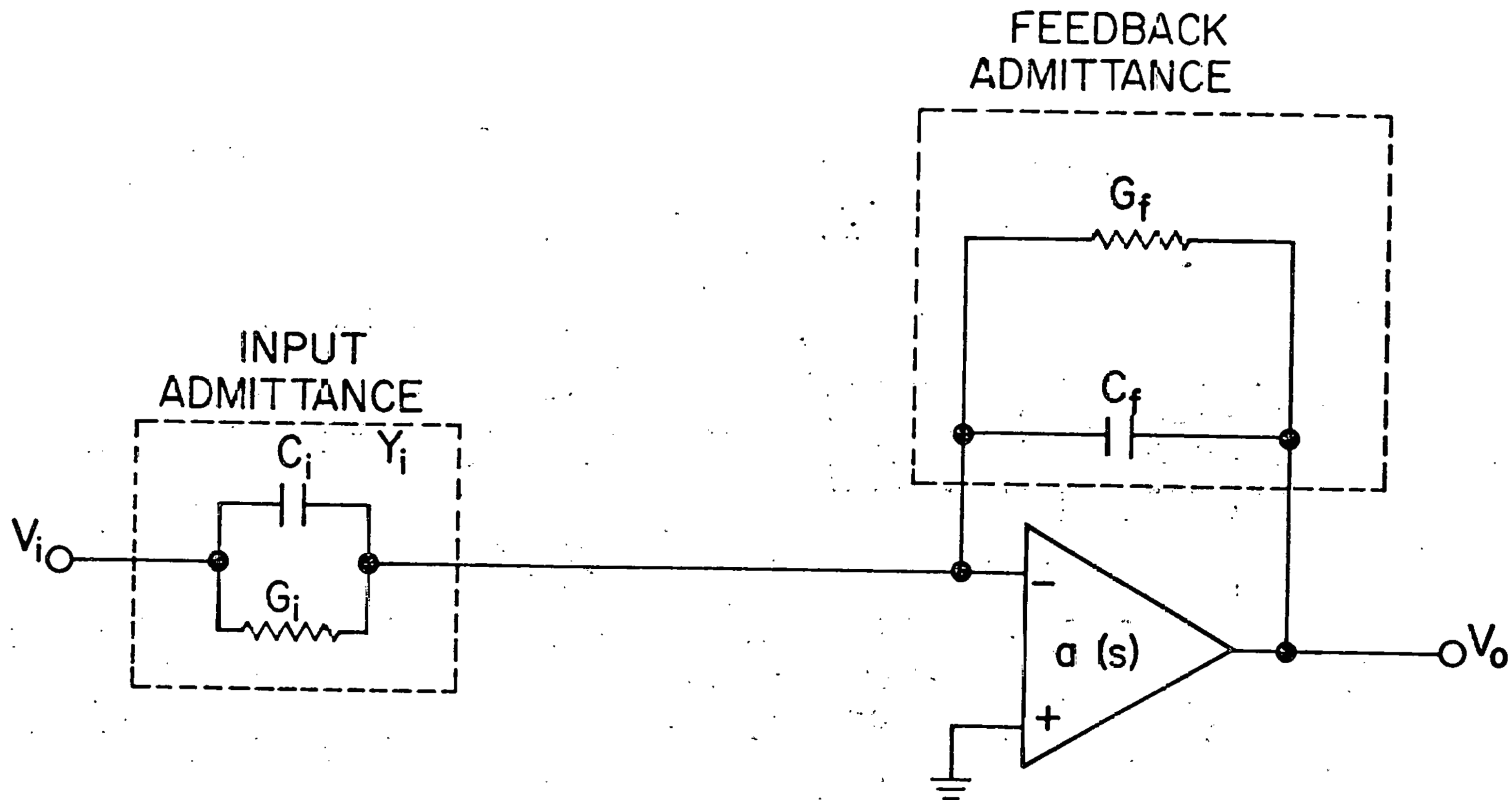
Figure 6.4. Barrier height extracted from 1 MHz capacitance versus reverse bias voltage for run# 170

6.2 AUTOMATED SURFACE ANALYSIS OF MIS/SIS SOLAR CELLS

A new technique for automated admittance measurements has been developed and applied to characterize the Si-SiO_2 interface of MIS/SIS devices. This system is quite useful in that previous data have indicated that, in weakly inverted sturctures, surface and bulk impurity states can plan a significant role in limiting device performance. The technique has improved speed/resolution capabilities in evaluating these effects. The admittance analysis system is based upon the use of an automatic network analyzer (HP 3570A) and frequency synthesizer (HP 3320B) buffered by a high speed I-V converter which has flat response up to 1 MHz. A block diagram of the I-V converter and the system are shown in Fig. 6.5, and 6.6 respectively. The synthesizer, network analyzer, and digital to analog (D/A) and A/D converter are all calculator (HP 9825) controlled. The calculator sets each bias point and can sweep 100 frequency points in approximately two minutes. The admittance is stored on flexible discs for later analysis.

Typically impedance bridges or coherent detection techniques (lock-in amplifiers) are used for these measurements, but both techniques are limited in their ability to sweep freuqency. Each point takes upwards of two minutes. All three techniques have been utilized in our laboratory. The automated network analysis system represents a significant improvement over impedance bridge or lock-in amplifier detection in this application because of increased accuracy in determining widths and heights or peaks of G/ω versus ω.

An automated analysis program, using the conductance technique, has been developed to characterize the interface. Originally the conductance method was for MIS capacitors, but it has been extended by Kar and Dahlke [1] to include thinner oxide MIS devices where there is appreciable conduction across the oxide. The analysis routine performs successive



$$G(s) = \frac{V_o(s)}{V_i(s)} = \frac{G_i + sC_i}{G_f + sC_f}$$

Figure 6.5. Basic I-V convertor circuit with ideal transfer functions G(S)

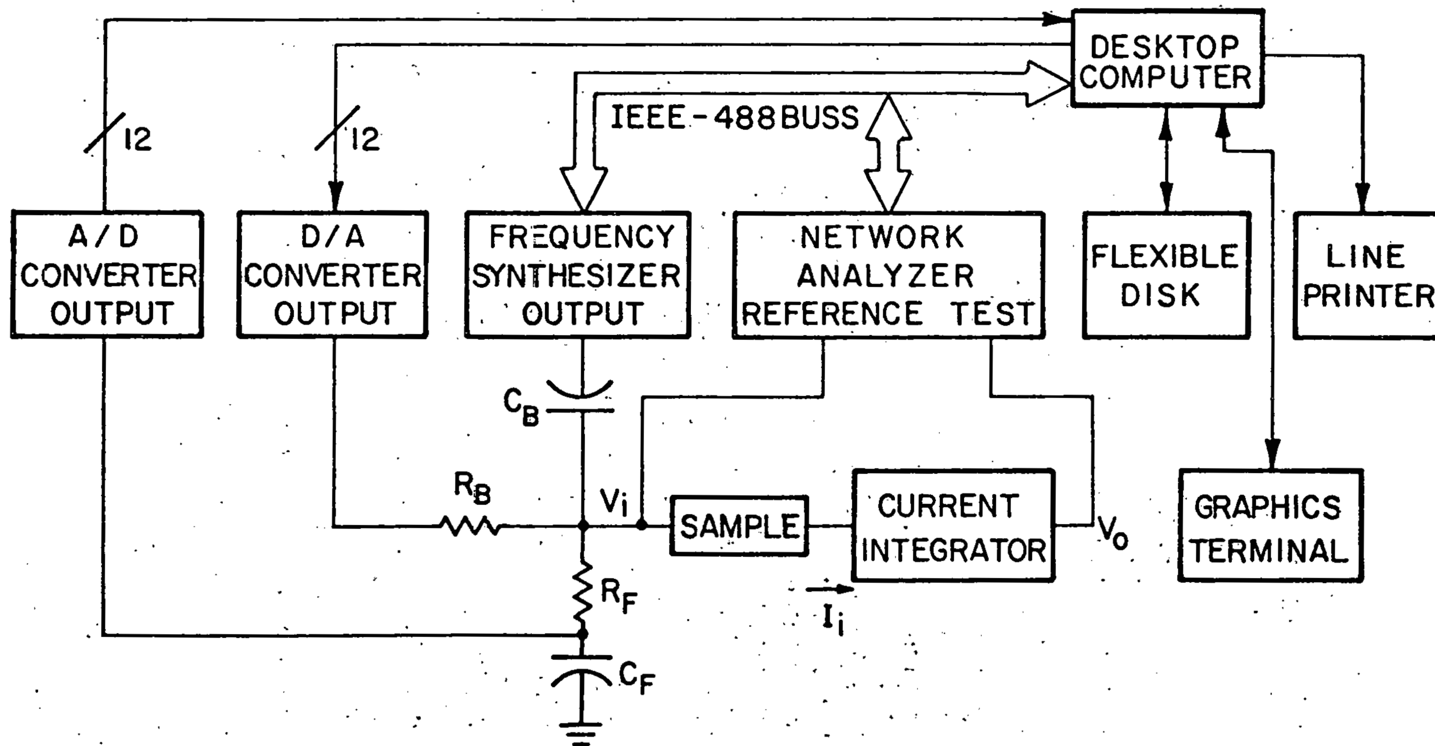


Figure 6.6. The complete automatic network analysis system.

equivalent circuit reductions to remove the effects of bulk resistance, d.c. conductance, and oxide capacitance to isolate the surface state admittance. The conductance G. and frequency ω are plotted as G/ω versus ω for each bias point as in Fig. 6.7. The peak width determines the type of surface state (e.g. single level, continuous). The peak magnitude and the frequency and surface potential at which the peak occurs, determine the surface state density. Using this system plots of N_{ss} vs E are made and compared for different processing variations.

5.3. NOISE SPECTRAL DENSITY AS A DEVICE RELIABILITY ESTIMATOR

Walsh [2] and Cocca [3] have developed tests utilizing the temperature and bias-dependent reverse current voltage characteristics. These tests detect negative hysteresis in the reverse current-voltage curve as well as doubly or more activated the reverse current versus temperature curves. This negative hysteresis refers to the change in reverse current at a given bias on increasing bias versus that observed on decreasing the bias. A positive hysteresis is said to occur when the current decreases as the bias decreases and a negative hysteresis if it increases. These tests have been shown to correlate reasonably well with extended life tests [4]. The problems with the Walsh and Cocca tests are that they are hard to interpret and are sometimes destructive. The noise spectral density test alleviates these problems by using breakdown voltages below the avalanche breakdown voltage of the device and low temperatures. The test is based upon deviations from ideal diode shot (and thermal) noise as the device is heated from below to just above room temperature. Noise in MIS and SIS devices, as well as PIN devices, has been studied previously [5-7].

Ideal SIS diodes in reverse bias exhibit shot noise plus a much smaller thermal noise component. A non-ideal device exhibits shot noise, thermal noise, generation recombination noise, and flicker noise.

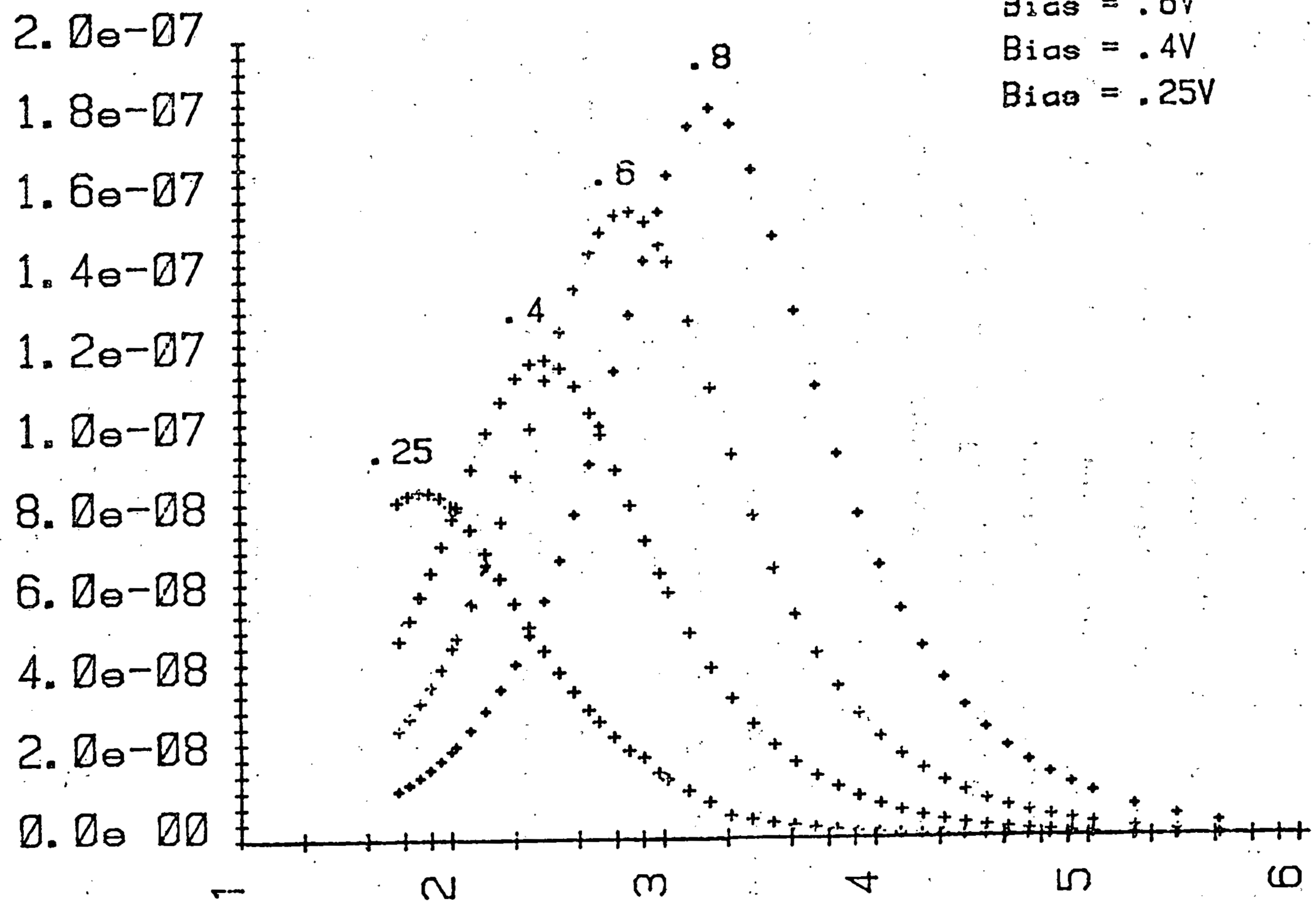


Figure 6.7. Conductance/Frequency Versus Frequency

Table 6.1 summarizes diode noise mechanisms and their spectral dependence. Ideal shot noise is only weakly temperature-dependent. At a single temperature it is difficult to interpret or separate out individual noise mechanisms. However, since the various noise mechanisms exhibit different temperature dependences, the existence of substantial amounts of leakage, recombination, and contact problems tends to show up in the temperature dependence of the noise spectral density. The applied biases involved create relatively high fields which enhance ionic diffusion. The temperature variation sweeps the Fermi level so that certain traps become recombination centers and vice versa.

Measurements were made using a cold finger with a thermoelectric cooling element for cooling, temperature control and heating. The device was attached to the thermoelectric element and connected through a batter-operated Quanted 205C pre-amp. The noise spectral density was recorded in a Hewlett-Packard 3580A spectrum analyzer. The noise spectral density and the reverse current voltage characteristics for typical devices are shown in Figs. 6.8, and 6.9, It is seen that the device with the most anomalous reverse current characteristics also exhibits the greatest variation in noise spectral density. The hysteresis in the reverse current voltage characteristics are indicative of ion motion on the surface of the devices. The relatively soft breakdown characteristics exhibited in the reverse current voltage curve of power devices are also indicative of edge effects and imperfections in the device. Low conversion efficiency does not correlate with reverse bias hysteresis and variation in noise spectral density. These devices also failed an extended high temperature test at variable rates. Other data, although preliminary, tend to confirm these trends. These trends need to be duplicated and statistically validated in future work.

Table 6.1.

Diode Current and Noise Mechanisms

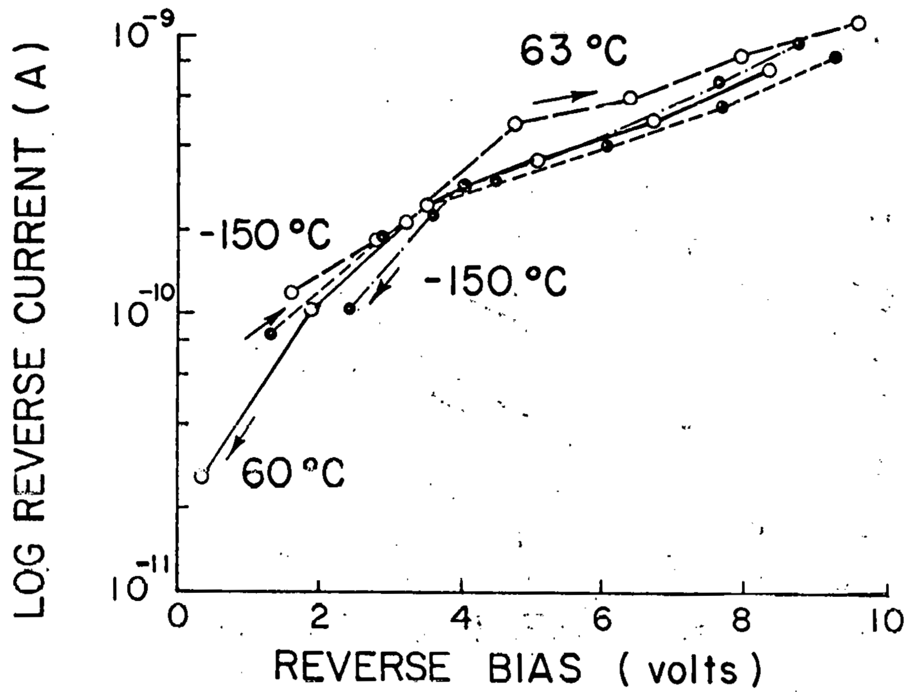
$I_s = T^{3/2} \exp -Eg/kT$

$Si(s) = 2gI_s$ - shot

$Si(\omega) = \frac{T}{1+w^2T^2}$ - G - R

$Si(\omega) = K \frac{kTN_T(\varepsilon)}{\alpha f}$ flicker

$Si(\omega) = 4KTG$ thermal



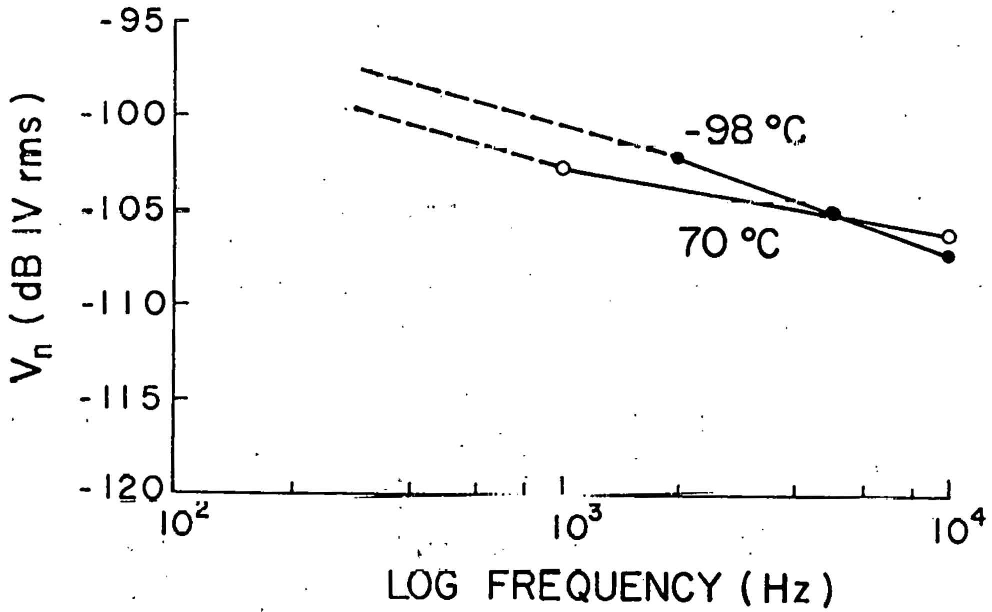
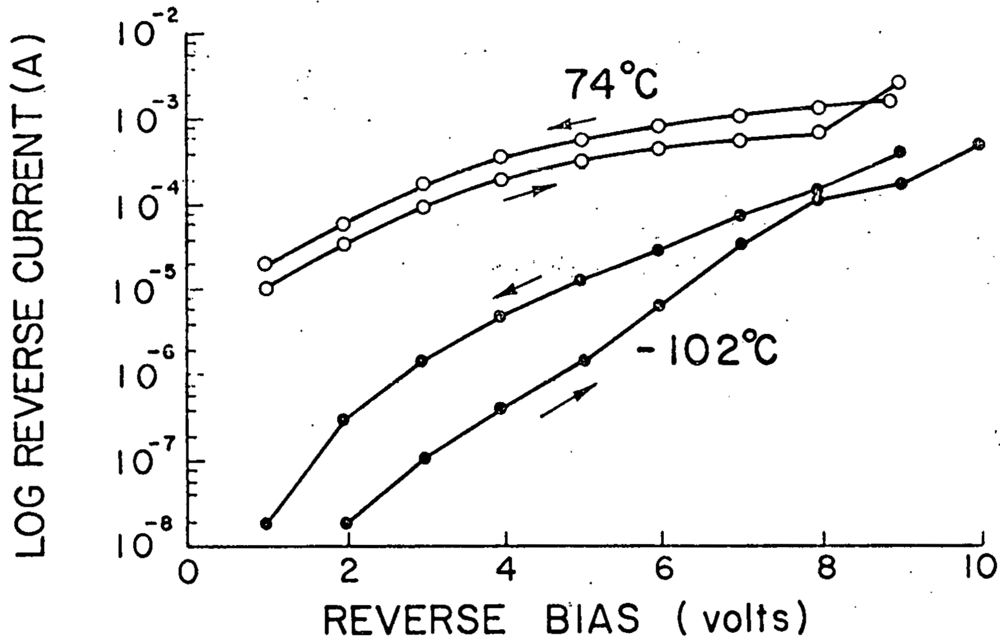


Figure 6.8.: Noise spectrum and reverse current voltage characteristics of $ITO/SiO_x/Si$ cells (device N_1)



CELL: N6
V_{oc} = 0.47V
J_{sc} = 21mA/cm^2
η = 2%

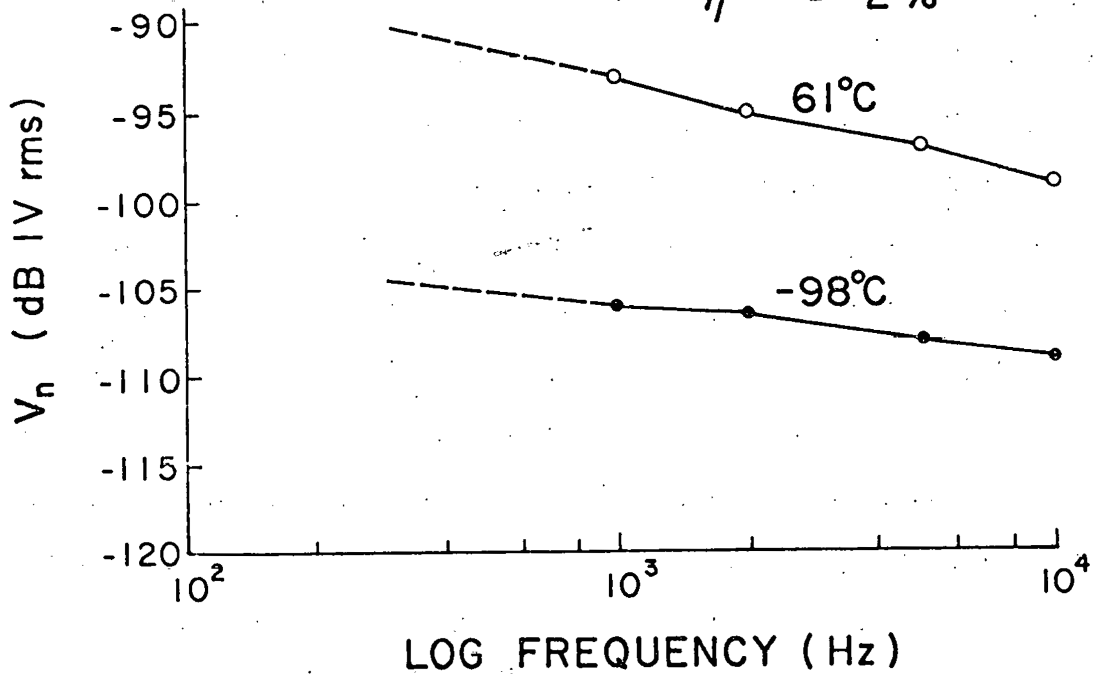


Figure 6.9.: Noise spectrum and reverse-current voltage characteristics of ITO/SiO_x/Si cells (device N_6)

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7. DEGRADATION OF ITO/Si SOLAR CELLS

Part of the degradation studies were performed under separate contract (EG-77-S-02-4518) and additional information can be found in final report number COO-4518-T1 and J. Appl. Phys. 51, 527 (1980). For completeness, a summary of all the results is given here.

A. Thermal Stress

Previously we have shown that the thermal degradation of the ITO/Si cells is a thermally activated process. Thermally accelerated aging is expected to follow Arrenhius type behavior. However, it is doubtful whether a sufficient quantity of cells have been degraded to realize a true lifetime prediction. However, enough cells have been tested that it is appropriate to evaluate the Arrenhius behavior of the data presently available.

It is first necessary to define an arbitrary end of life value, which here was chosen as 50 percent of the initial efficiency. The time to reach this value was calculated through a cubic spline interpolation routine which generated points between existing efficiency versus time data.

Figure 7.1. shows the result of plotting the failure time on a semilog scale for several runs. As may be seen, the failure times are, as would be expected, characteristically exponential with temperature. However, the degradation rate is not the same between runs, with each run having a different intercept but approximately the same activation energy. As is seen, the data points for an individual run do not exactly fit an exponential model for degradation, but the average values seem to fit. This may imply that the degradation is more complicated than a simple logrithmic dependence, perhaps multiply activated. However, this question

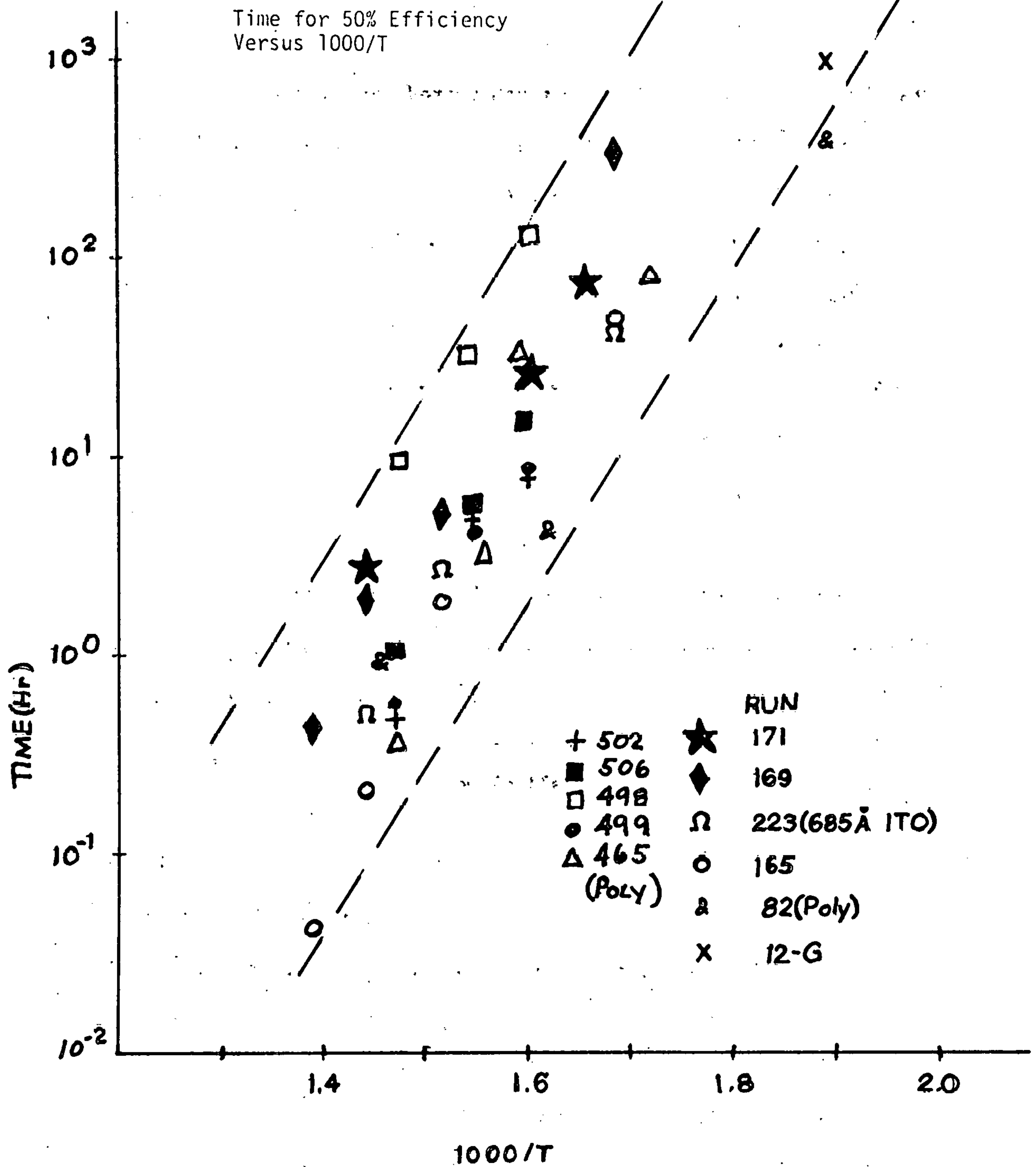

Figure 7.1. Arrenhius plot of 50% degradation time versus 1000/T for several different runs.

cannot be resolved until a more statistically significant number of samples have been tested, particularly at lower temperatures.

The stability of recently fabricated single and poly cells (Monsanto) were compared with cells fabricated some months ago. Figure 2a and b show the results of the recent tests. As can be seen the recently fabricated poly cells degrade more rapidly than previously studied single crystal cells and there are additional features such as a large drop in V_{oc}. The recently fabricated single cells appear about the same as before and thus the degradation of the poly cell would appear to be due to the substrate, however other process changes may be important in causing this change.

B. Thermodynamics of the ITO/Si Interface

The equilibrium thermodynamics of the ITO/silicon interface was investigated by considering the balanced chemical equation of possible reactions. The primary results are shown in Table 7.1. As can be seen, Si will readily reduce In and Sn oxides yielding either free In or Sn or their suboxides. However, in the presence of excess oxygen the most stable configuration is one with all elements (Si, In and Sn) fully oxidized. The thermodynamics predicts the stable conditions but does not provide kinetic information. For the ITO/silicon interface the kinetics involves the transport of elements or molecules thru the ITO and the interfacial SiO_2 layer. This transport would be expected to be slow; thus impeding the reactions. Also, the thin interfacial SiO_2 will eliminate contact between ITO and Si. Since SiO_2 is formed on the interaction and since ITO and SiO_2 do not react, the reaction tends to be self limiting. Also, SiO_2 is not a nucleation and growth type of oxide, and the oxide tends to cover the surface. These considerations help explain the stability observed to date and the potential for stability in a device which is sensitive to so thin an interfacial layer.

Table 7.1.

Summary of the Thermodynamics of ITO-Si Reactions

Reactants	Products	ΔHr (Kcal/gm atom)
$In_2O_3 + SnO_2 + SiO_2$		Always stable
$In_2O_3 + SnO_2 + Si$		-17 to -5 Kcal
$In_2O_3 + SnO + Si$		-16 to +1
$In_2O + SnO_2 + Si$		-20 to -5
$In_2O + SnO + Si$		-43 to -7
$InO + SnO_2 + Si$		-19 to -5
$InO + SnO + Si$		-35 to -7
$In_2O_3 + Si$	In, Sn, SiO_2 or the suboxides of In, Sn+Si	-16 to -2
$In_2O + Si + O_2$		-50 to -16
$In_2O + SiO + O_2$		-37 to -14
$InO + Si$		-41 to -13
$InO + SiO + O_2$		-26 to -4
$SnO_2 + Si$		-20 to -9
$SnO + Si + O_2$		-48 to -12
$SnO + SiO + O_2$		-31 to -11

Previous degradation experiments have shown that O_2 can diffuse at elevated temperatures through the ITO and the interfacial SiO_2 but that the ITO appears stable in the presence of SiO_2. Thus it would appear that the kinetics of the interfacial reactions control the cell stability and not the thermodynamics.

The mechanism for thermal degradation was determined by a series of tests in vacuum, air, forming gas and N_2. As is predicted from the above thermodynamics, the cells heated in vacuum did not degrade. The degradation in forming gas and N_2 was much slower than in air. These tests plus I-V, ellipsometric and Auger measurements all indicate that the degradation caused by the growth of the interfacial SiO_2 layer; apparently by the diffusion of O_2 through the ITO layer. Diffusion through the ITO did not appear to be the rate limiting step since the degradation was independent of ITO thickness. The interfacial kinetic properties appear to be the dominant factor in determining the degradation rate.

C. Illuminated Stress Testing

Section 7.A. discusses the results of cells thermally stressed in the dark, with the result that degradation occurred via the oxidation of the silicon at the interface. However, the reaction was found to proceed extremely slowly at room temperature, so much so that at this temperature (and in the dark) no severe thermal degradation is expected at normal operating temperature. This seems to be substantiated by the fact that cells fabricated several years prior to this research show little "on the shelf" degradation.

The results of the previous section serve only to predict the performance of the cell when stored in the dark. In actual use, the cell is subjected to a light intensity of about 100 mW per square centimeter. The device is also under load, with current densities of around 30 mA/cm^2

being drawn from the cell. The effects of these stresses is not expected to relate to the type of degradation found in the previous section (except for some sort of field-aided oxidation at the interface).

The effect of light, especially ultraviolet light, is the breaking of certain chemical bonds. This leads to increased defects in semiconductors and thus shorter surface and perhaps bulk lifetimes. For silicon, this is not a significant problem under terrestrial radiation conditions. However, the effect of long term exposure of ITO to sunlight is not well studied, especially ITO prepared by ion beam sputtering. The lifetime in the ITO is not a critical parameter in the device performance. However, increased defects in the ITO could lead to scattering and absorbtion centers which would reduce the amount of light reaching the silicon. This could be constructed as a degradation mechanism.

Current flow in devices is often responsible for failure. One mechanism, known as electro-migration, results in mass transport due to a DC current. Usually this type of degradation results in open circuits of metallization and interconnects. Electromigration is usually limited to situations where high current densities exist (10^5 A/cm^2) in planar ICs. However, the effect of long term current flow through ITO is again not well characterized, and it is possible that electromigration of the ITO could occur even at low current densities.

Another degradation mechanism associated with surface controlled devices (i.e. planar FETs, MOSFETs) is ionic drift and contamination. In this failure mode, ionic contaminants drift to the surface of the device as a result of external or internal fields. In diodes this manifests itself in barrier cancellation and shunting. In solar cells, this would result in decreased open circuit voltage.

To identify whether or not any of these factors were present to an obvious and significant degree, in the effects of normal light and load on a limited sample of ITO/Si solar cells were studied over extended periods of time. This was first done at room temperature and later at elevated temperatures. In the following, a description of test apparatus and experimental procedure is given. A comparison is then made between the results obtained here and those of Burke and Shewchun, who have performed similar experiments.

Three cells were selected from each of two different runs, numbers 165 and 169. Other cells from these two runs had been thermally degraded as described previously. Both cells de-
graded in the usual manner with heat, although 169 was found to degrade much slower than 165. Both cells also showed a reduction in V_{oc} under thermal stress, as well as suffering from the usual decrease in fill factor. As before, the cells used for illuminated stress testing were one-eighth inch in diameter and unencapsulated.

In the initial experiment, the cells were placed under varying loads at 1 sun and 25° C. This experiment was similar to those performed at McMaster University and was used to verify the results obtained by this group. Later, these same cells were heated to 82°C while maintaining normal light and load and allowed to operate at this condition for over 1300 hours.

One cell from each run was placed under conditions of open circuit, short circuit and maximum power, while illuminated. The maximum power point was determined from the initial I-V curves and a resistive load was then used to obtain this condition. This resistance remained

fixed for the duration of the test. As mentioned earlier, the light intensity was maintained using a standard p-n junction photo cell. To obtain a long bulb lifetime, the voltage to the ELH bulbs was maintained at approximately 70 volts rather than the usual 110 volts. At full voltage these bulbs emit a spectra characteristic of the AM2 solar spectrum. However, at lower voltage the bulbs operate at a lower temperature which shifts the spectra more into the infrared, hence reducing the ultraviolet radiation.

Initially the cells were maintained at a constant light and load for 200 hours at 25°C. The light source was adjusted manually, and the light intensity was found to vary ten percent between adjustments. As a check on cell performance, the voltage across the load resistors was measured fairly often. At longer intervals, complete illuminated I-V plots were made. Dark enI versus V measurements were made initially and later at the completion of testing. To minimize contact resistance problems, small silver print contacts were employed between the ITO and the probe.

After 200 hours at 25°C, the cells were removed from the text apparatus. A residue had formed on the cell surface as a result of outgassing of insulation in the box. Also, the silver print proved to have poor adhesion. The cells were cleaned and the silver print contacts replaced with an aluminun cross hair grid pattern. In the process, cell 165.3 was cracked and was replaced by another cell from the same run designated 165.0.

Upon resumption of light and load, the chuck temperature was raised to 82°C. The resistive loads were now matched for the maximum power point at this temperature. I-V measurements were made at appropriate

intervals, both at 82°C and at room temperature. The duration of the final stage of testing was in excess of 1300 hours (two months).

Long term load testing of several cells was performed by Burke and Shewchun at a temperature of 25°C to 30°C prior to the experiment performed here. Basically they found that the cells do not degrade, although small fluctuations in V_{oc}, I_{sc} and the fill factor were observed. These fluctuations appeared to be attributable to their test apparatus. For instance, fill factor changes could be related to contacting problems, and V_{oc} changes to temperature fluctuation.

The results of our experiment performed at 25°C are essentially the same as described above. For the cells tested here, 165 and 169, fluctuations were also observed. These fluctuations were not identical from cell to cell. However, there appeared to be no relationship between the load condition of the cell and the parameter fluctuation. Fill factor changes were attributable to the poor adhesion of the silver print as mentioned earlier and could be restored through repositioning the probe. V_{oc} changes are thought to be due to temperature changes in the chuck. It was found at the completion of testing that errors in measurement of the cell temperature were as much as ±5°C, which is enough to cause fluctuations of V_{oc}.

The short circuit current also fluctuated in this initial testing. Part of this is thought to be due to the non-uniformity of the light intensity across the surface of the chuck. As the bulbs aged and finally had to be replaced at different times during the experiment, the intensity and spectral distribution experienced by each cell, and thus the short circuit current, changed during the course of the measurements.

Within the margin of error imposed by the test system, it is believed that no permanent degradation of these devices occurred after 200 hours at 25°C, in agreement with the results of Burke and Shewchun.

As no appreciable degradation of these cells had occurred, the cell temperature was raised to 82° C in the hope of accelerating any previously unobserved failure mechanisms. During the more than 1300 hours of testing, the cell parameters were again observed to fluctuate, only much more dramatically. When measured in-situ, the short circuit current was found uniformly lower at the conclusion of testing. As mentioned earlier, bulb again resulted in non-uniform intensity and spectral distribution over the duration of the test, which could account for the fluctuations of this parameter. This was confirmed by independent I-V measurements which showed that I_{sc} had actually changed very little from its initial value.

The fill factors on several cells was found to have deteriorated after testing. This loss in fill factor was found in cells 165.0 and 169.3, both of which were kept at a condition of open circuit throughout the testing. The apparent cause was an eventual adhesion loss of the Al to the ITO surface. Throughout the test, high series resistances were found which could be eliminated by repositioning the probes indicating a contact problem. This could be due to oxidation of the Al. The fact that the adhesion of the Al to the ITO degraded might indicate that Al_2O_3 was forming between the ITO and the Al. This is a strongly favored reaction as discussed in the previous section. This type of reaction is often seen in planar ICs between Al and SiO_2 which has a comparable heat of formation to In_2O_3.

Early in this final stage of load testing, V_{oc} dropped noticeably and then fluctuated around a mean value lower than the initial value. All the cells, except 165.0 which did not suffer from a decrease in this parameter, followed the same pattern of fluctuation as that shown in Fig. 7.2.for cell 169.1. The cells were found to suffer a decrease of approximately 4.5 percent. As discussed earlier, the actual temperature varied about 5°C. This is more than enough to account for the observed change, as V_{oc} is predicted to change about .0063 volts per centigrade degree. However, independent tests were made on the cells outside the test chamber with care taken to record the correct temperature. These tests indicated that the open circuit voltage had permanently degraded, and was not an artifact of the test apparatus.

Anderson and Ghosh both report V_{oc} loss when SnO_2/Si cells are load tested as well as when on the shelf. The magnitude of this loss is around 10 percent compared to the 4.5 percent loss found here. ITO/Si cells fabricated by D. Burke several years prior to this research were checked to determine whether on the shelf degradation similar to that observed by Ghosh et al. had occurred. The V_{oc} of the D. Burke cells was found to be identical to their initial measurements. A close comparison here of the other parameters, I_{sc} and fill factor, is not valid as these two parameters are very sensitive to the test apparatus employed, which was quite different to the present setup. Qualitatively however, these parameters did not appear to have degraded from the original measurements.

Although these cells did not lose V_{oc} on the shelf, this does not mean that all cells will behave this way. It was found in the thermal

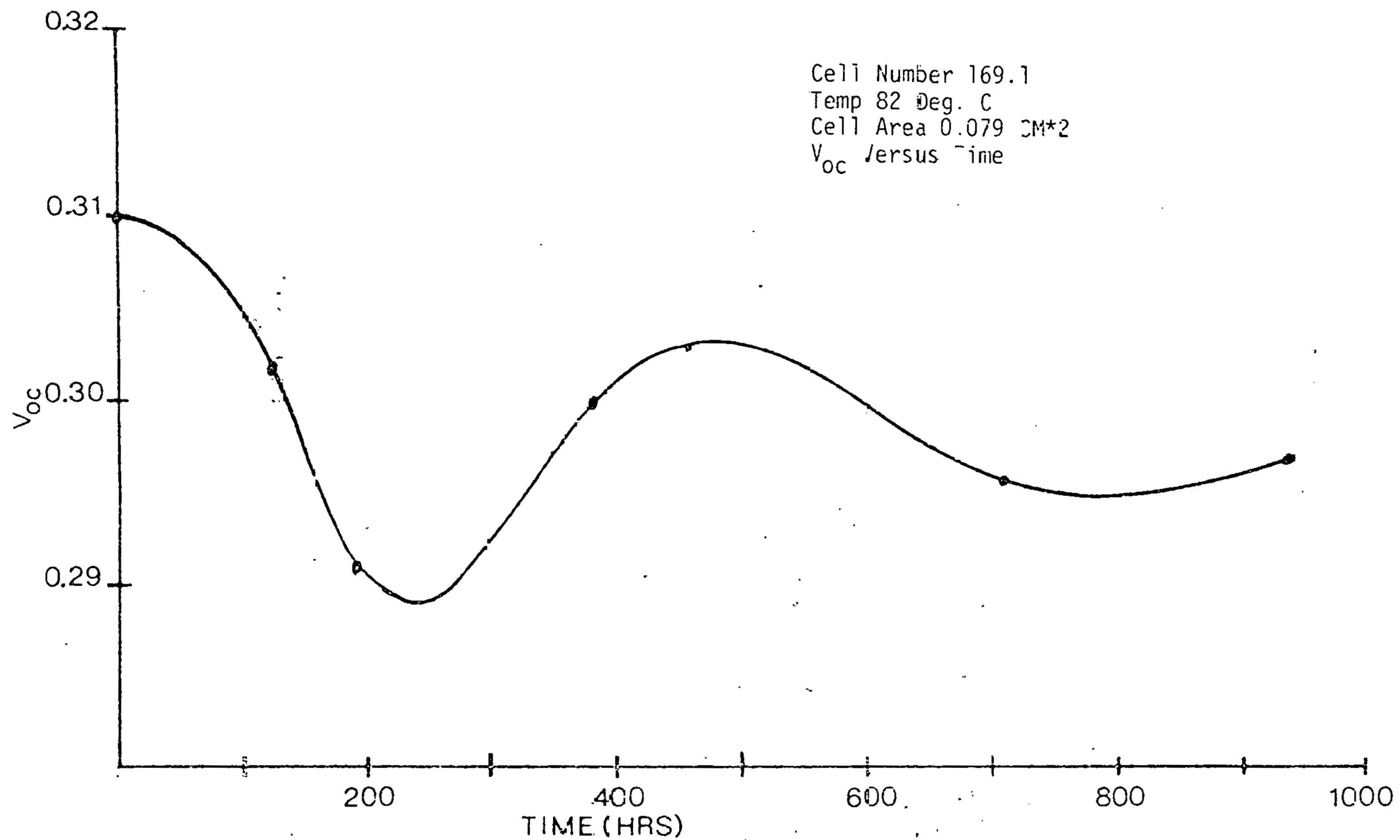

Figure 7.2. The change in V_{oc} as a function of illumination time at $82^{o}C$

degradation that some cells suffered a decreasing V_{oc} while others did not. Coincidentally, both 165 and 169 were found to suffer from reduced V_{oc} both thermally and under light and load. From thermal stress testing, this loss appeared thermally activated which might explain why it was not observed under light and load until the temperature was raised to 82°C.

It has been postulated that deterioration of V_{oc} due to thermal stress was caused by the increase in the interfacial oxide leading to reduced barrier height. However, in the case of light and load stress, the oxide thickness apparently remained constant with time. It is possible that ionic impurities drifted to the interface resulting in barrier cancellation. Ghosh et al. discuss this possibility in explaining the V_{oc} loss in SnO_2/Si solar cells when under stress. They attempted to determine if this occurred by subjecting the degraded cells to high reverse bias and temperature. The presumption is that this type of degradation is reversible by drifting the ionic contaminants away from the junction. The result of this was no change in the open circuit voltage, and it was then concluded that changes were a result of interfacial reorientation of the SnO_2 to some stable configuration which gave a higher surface state density.

It is possible that similar mechanisms appear in the ITO/Si cells and thus account for the decrease in V_{oc}. However, free energy considerations indicate that indium oxide is more thermodynamically stable than tin oxide. Nevertheless, it is not conclusive from the above experiment whether or not ionic impurities collect at the junction of the SnO_2/Si cells as this degradation may be either reversible or irreversible. The same would be true for ITO/Si solar cells.

8. INDIUM PRICE/SUPPLY PATTERN AND ECONOMIC ANALYSIS

A major conclusion of this element of the program is that indium price and availability will not limit the use of ITO solar cells. This conclusion is based primarily on the fact that large quantities of available indium are not being recovered. There are several factors that justify an optimistic outlook for indium availability. Due to slack demand, the recovery of indium has been a marginal operation. Indium is recovered as a by-product of zinc smelting. Only about one sixth of the zinc tailings are processed to yield the necessary supply of indium. Production is limited to those quantities necessary to meet the limited demand. The low profitability of the indium industry as reflected in constant actual prices over 25 years (until quite recently) has not warranted the development of new techniques or new sources of supply [1]. However, chalcopyrite copper ores are just as promising as zinc ores as a source of indium.

A second major conclusion was that ITO SIS cell fabrication is econimically competitive with LSA p-n junction technology. A computer program has been generated which automates the SAMICS IPEG costing procedure. The program has previously been utlized in conducting a first pass economic evaluation of an ITO device based solar cell factory. It is felt that this procedure yields meaningful preliminary estimates appropriate to the state of development of the technology. While a more detailed analysis is unwarranted, cost estimates within the LSA cost framework are useful for evaluating advanced technologies. Based on a fabrication sequence using currently available equipment, this analysis indicated that ITO devices could meet the near term cost goal of $2 per peak watt. However, more importantly, the results indicated that the required product price has highest sensitivity to product yield and cell efficiency. The price is also sensitive to the capital outlay

required for sputtering equipment and significantly less sensitive to the cost of materials and other factors of production.

Recent analysis has focused on sputtering technology with substantially increased throughput. One such technology is described below.

The candidate ITO/silicon device fabrication sequence centers around the use of a multifunction, linear, ion source sputter deposition station. The reference configuration of the sputter station employs an octagonal drum fixture. The wafer streams are processed simultaneously on a three minute cycle. Six plattens containing wafers are loaded (and six plattens unloaded) on two fixturing surfaces of the octagonal drum during each cycle while milling, oxide growth and film deposition proceed simultaneously in six process "vaults" over the six remaining fixturing surfaces. The number of plattens handled during each cycle was chosen as a reference. Larger fixturing drums and ion sources are technically possible.

The candidate industry "projected" for startup in 1986 employs advanced fabrication concepts which, although known to be technically workable, are in most cases unproven on the scale assumed in this analysis. This industry configuration was chosen in an effort to bound the costs of mass produced ITO devices based on techniques which although requiring further development and commercialization, appear most well matched to the industry expectation of high production volume in 1986.

Patterned after the 50¢/Wpk Candidate Technology [16] transport of devices from one work station to the next is by means of belt conveyors. The candidate factory is assumed to be vertically integrated incorporating substrate production and cell and module fabrication. Since the focus of this analysis is on the cell fabrication, other portions of the production sequence are as specified in the 50¢/Wpk Candidate Technology.

Since the prior history of the wafers is assumed known in their integrated factory, several cleaning and degreasing steps, which under other

circumstances are necessary, have been eliminated. Also, the in-situ ion milling step reduces stringent cleaning requirements.

As in the JPL 50¢/Wpk Candidate Technology the wafer surface is EFG ribbon silicon. The back surface of the wafer is aluminized. Following film deposition, silver front grids are applied by screen printing and the cells are then tested and sorted.

For reference purposes, the numerical plant output was set at 100 MWpk (20 percent of a 500 MWpk market). This is equivalent to an annual production rate of 137 million cells. The yield distribution of cell efficiency is taken to be a Beta probability density function with parameters 2 and 0.05. This implies an average cell efficiency of 9.8 percent, 2 percent lower than present average efficiencies. Cell grade silicon was assumed available at $10 (1975) Kg.

The result of the cost sensitivity study for the candidate technology shows that the required price is most sensitive to yielded cell efficiency, and ion beam sputtered ITO oxide semiconductor solar cells can be manufactured at prices well within DOE cost goals.

In addition to the cost analysis of ITO/Si solar cell, we have also calculated the fabrication cost of grating Aℓ-SiO_2-p-Si (MIS) solar cells using polycrystalline and amorphous substrates [2]. Both MIS and SIS are members of a general class of photovoltaic devices called conductor-insulator-semiconductor (CIS) solar cells [3]. The devices are assumed to have a conversion efficiency of 12.9% equal to assumed for JPL "Test Case" p-n junction factory.

By way of comparison, grating type MIS and generic "CIS" type of devices were also studied. The physical structure of a polysilicon MIS solar cell is shown in Fig. 8.1. and the cell fabrication process sequence for a candidate MIS grating cell factory is shown in Fig. 8.2. Compared to p-n junction fabrication, in the MIS sequence doping steps

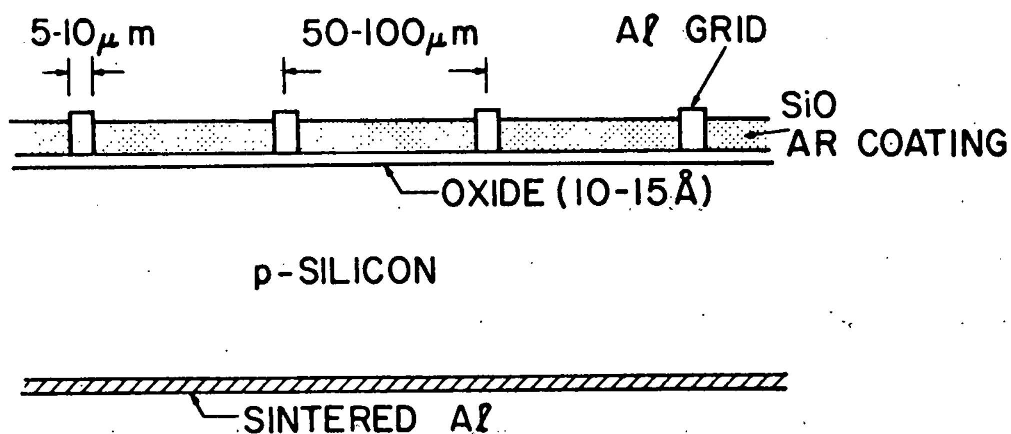

Figure 8.1. CIS Solar Cell Grating Type Structure.

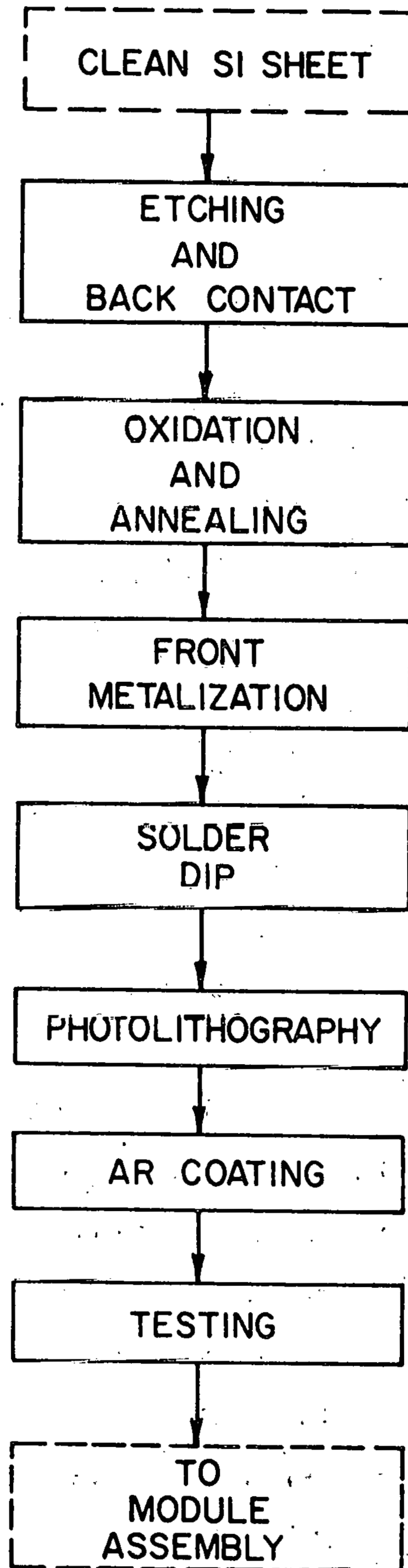

Figure 8.2. Fabrication Flow Chart for Grating Type Al-SiO_x-p-Si Solar Cell.

have been replaced by thin film deposition and photolithography processes. The corresponding direct equipment and materials costs are indicated i Table 8.1 For the 250 MW factory, direct floor space requirements for equipment in the cell fabrication section is estimated to be 500 m^2. Direct assembly line labor and utilities requirements were assumed to be comparable to those implied by the JPL Test Case. Value added costs generated by the IPEG formula are tabulated in Table 8.2.

For CIS cells, a comparison of the 1 MW and 250 MW CIS value added costs indicate the substantial economics of scale anticipated in scaling up the manufacturing sequence. Studies by JPL and RCA indicate the significant cost reductions can be achieved in scaling production from the 1 MW level to 30-50 MW. At this level substantial automation must necessarily have been achieved and cost reductions in increasing scale beyond 50 MW are less pronounced [4,5].

Figure 8.3. shows the breakdown of costs on a percentage basis for the 1 MW and 250 MW MIS factory. The clear difference in the two breakdowns in the reduction of facilities related cost in the 250 MW case. Capital equipment and labor also take a smaller fraction of costs with materials costs filling in the difference. The dominant reason for the "per watt" costs reductions in increasing plant size is the increase in thruput afforded by a high degree of automation. This is true for both the JPL test case and the candidate MIS factory. Once a certain level of automation is achieved, materials related costs become more dominant and it is in this regard that the MIS structure offers some advantage. As Table 6.2. indicates, materials costs are estimated to be 50% lower for the MIS factory versus the JPL test case.

Table 8.1

CAPITAL COSTS AND MATERIALS/SUPPLIES COSTS BREAKDOWN FOR THE FABRICATION Aℓ-SiO_x-(p-Si) SOLAR CELLS (FACTORY OUTPUT - 250 MW PER YEAR)

PROCESS	Capital Costs (millions)	Materials/ Supplies Costs (millions)
Etching and back contact	1.0	1.65
Oxidation and alloying	0.1	0.1
Front Metallization	5.5	2.0
Solder dip	0.05	1.0
Photolithography	2.15	2.0
AR coating	1.0	1.0
Testing	0.02	0.05
TOTAL	9.82	7.8

Table 8.2.

COMPARISON OF VALUE ADDED CELL FABRICATION COSTS EXPRESSED IN 1975 DOLLARS/PEAK WATT

COST COMPONENT	1 MW CIS	250 MW CIS	250 MW JPL TEST CASE (a)
Equipment	0.100	0.022	0.020
Facilities	0.337	0.002	0.006
Labor	0.332	0.018	0.018
Materials	0.026	0.026	0.054
Utilities	0.020	0.001	0.001
TOTAL	1.124	0.072	0.102

(a) JPL cost estimates stated in Ref.[[illegible]] reagregated to match IPEG cost categories.

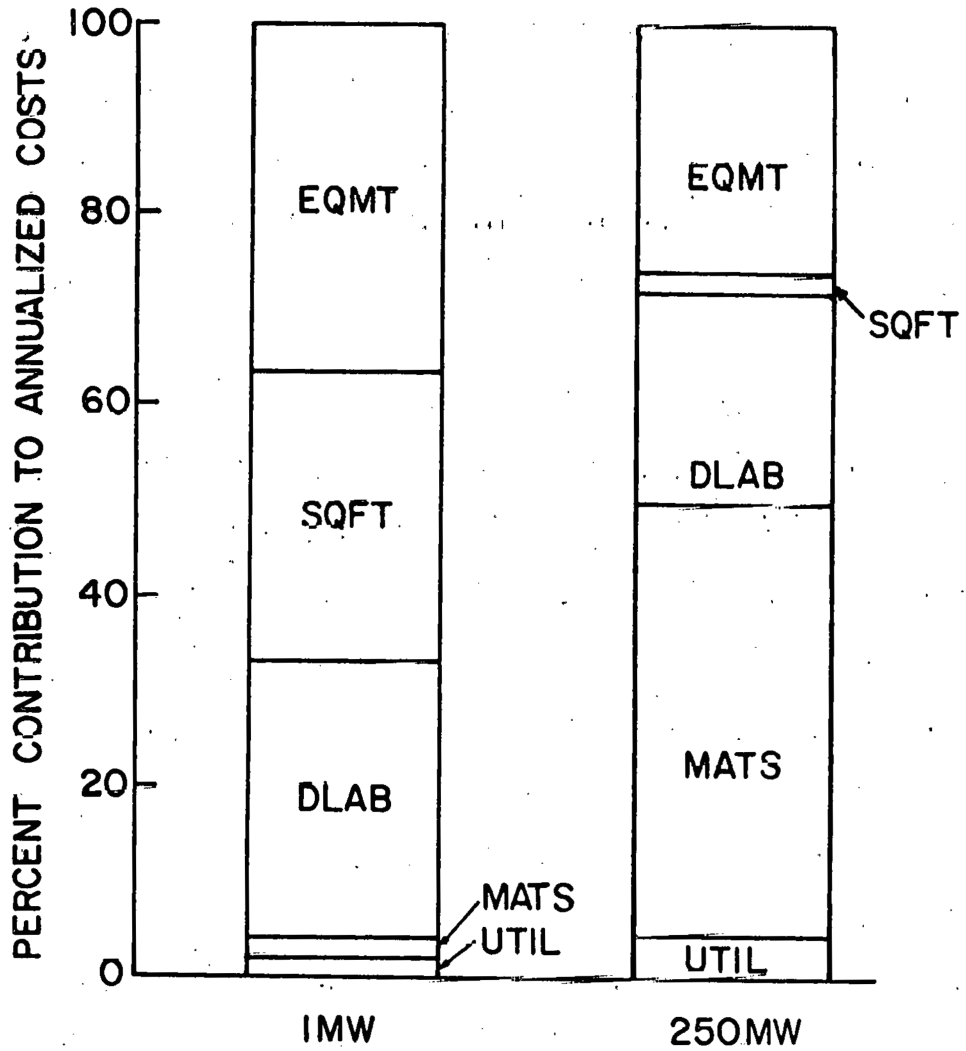

Figure 8.3. Percentage Distribution of a Annualized Costs for 1 MW and 250 MW CIS Factory.

Based on the IPEG cost formula, the variation of cell fabrication costs with variation in each of various cost components can be estimated. The cost sensitivity diagram for the 250 MW MIS factory is shown in Figure 8.4.(These results are qualitatively similar in the JPL Test Case also.) In the diagram, "inverse efficiency" means that variations with respect to the reciprocal of device efficiency have been plotted. Device efficiency has the most significant effect on "per peak watt" costs. Materials costs are the next most significant cost component. Variation in facilities and utilities related costs have the least effect on cell fabrication cost. These sensitivity results indicate most importantly that achieving high conversion efficiencies (10 to 15%) is crucial in terms of producing solar cells which can be economically competitive with other energy sources.

With respect to the project cost of complete photovoltaic modules, the MIS modules are competitive but only slightly lower in cost than the JPL test case moduels. Although MIS cell fabrication costs are 30% lower than in the test case, substrate and module fabrication costs are dominant-items in total panel costs and these are assumed equal in both cases (see Table 8.3). Where MIS structure may offer a considerable cost advantage is with amorphous structures where substrate costs can be significantly reduced as discussed below.

A schematic diagram of the amorphous MIS solar cell appears in Fig. 8.5. The fabrication sequence is similar to that for the polysilicon MIS device with the addition of an amorphous silicon deposition step. The cost of amorphous silicon was taken to be $2/kg. To date, amorphous devices have achieved conversion efficiencies in the range of 5 to 6% for small active area devices. In this analysis, a conversion efficiency of 10% was assumed to evaluate the economic feasibility of these devices. Devices with conversion

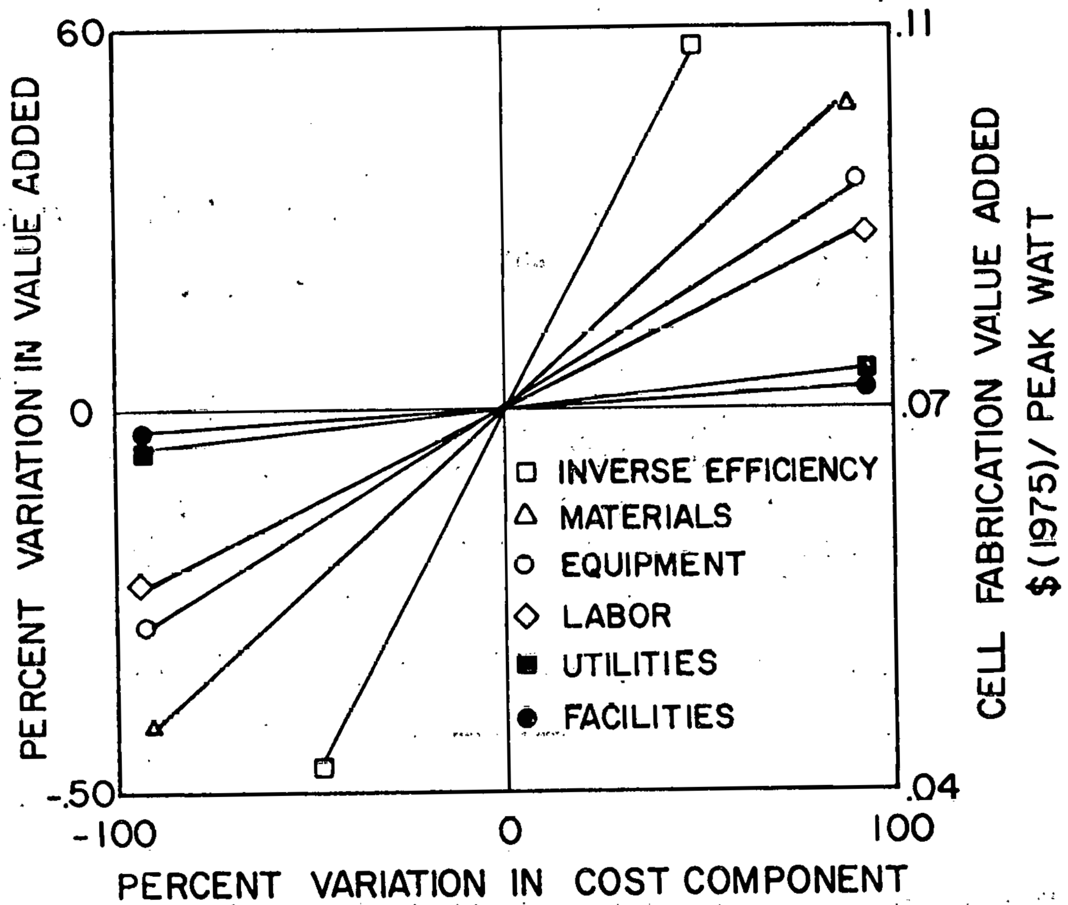

Fig. 8.4. Cost Sensitivity Diagram for 250 MW CIS Solar Cell Factory.

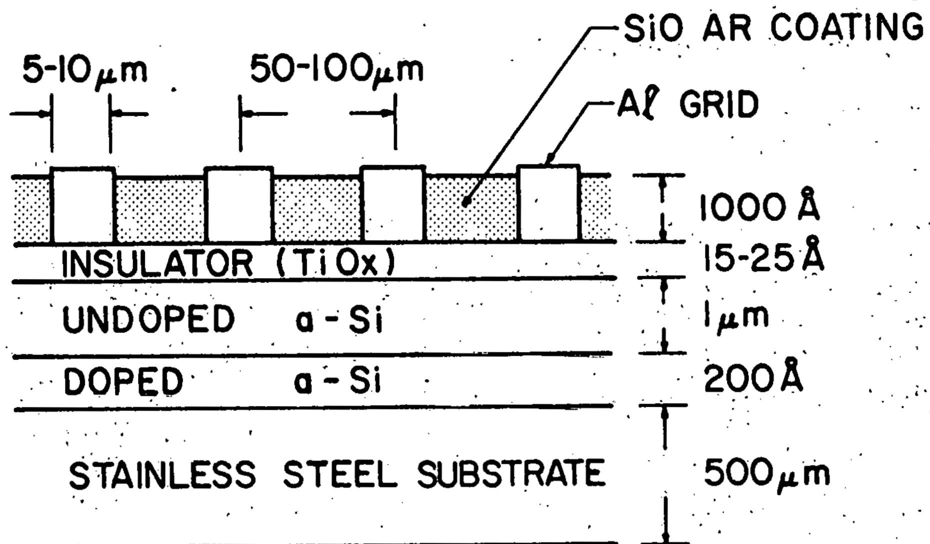

Figure 8.5. Amorphous Silicon CIS Solar Cell Structure.

efficiencies below 10% are severely penalized by area related costs both directly and in terms of installation cost.

Table 8.4 indicates the breakdown of annualized costs for amorphous CIS solar cells. Cell fabrication value added costs are estimated at 0.09 $(1975) per peak watt versus 0.07 $(1975) per peak watt for the poly-silicon CIS device. The higher cost for the amorphous cell is due principally to the lower assumed amorphous device efficiency. The promise for amorphous devices lies in the elimination of the silicon wafer substrate being replaced by a stable metal substrate - typically stainless steel.

Referring to Table 8.3 and 8.4, although reduced conversion efficiency increases cell and module fabrication costs, for the amorphouse device a 20% reduction over the JPL test case is projected for total panel cost. Although contingent on producing cells of sufficiently high efficiency, amorphous CIS solar cells may ultimately prove an important option in the photovoltaics market.

Table 8.3.

COMPARISON OF SOLAR CELL MODULE COST EXPRESSED IN 1975 DOLLARS/PEAK WATT

	250 MW CIS Factory	250 MW JPL Test Case
Wafer/Substrate	.18	.18
Cell Fabrication	.07	.10
Module Fabrication	.16	.16
TOTAL	.41	.44

Table 8.4.

IPEG COST ESTIMATE FOR a-Si CIS SOLAR CELL MODULE

COST CATEGORY	VALUE ADDED COST $(1975)/Wpk	
SUBSTRATE		0.02
CELL FABRICATION		
Equipment	0.033	
Facilities	0.002	
Labor	0.022	
Material	0.025	
Utilities	0.006	
SUBTOTAL		0.09
MODULE FABRICATION		0.19
TOTAL		0.30

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3. R. Singh, M.A. Green and K. Rajkanan, "Review of Conduction-Insulator-Semiconductor (CIS) Solar Cells", Solar Cells (In Review).

4. R. G. Chamberlin, Proc. 2nd European Communities Photovoltaics Solar Energy Conference, West Berlin, April 1979, published by D. Reidel Publishing Company, Dordchet, Holland, 1979, p. 851.

5. R. V. D'Aiello, "Automated Array Assembly", (RCA Labs, Princeton, NJ) DOE/JPL-954352-7714, December 1977.

9. CONCLUSIONS

As a result of this study, the following conclusions could be drawn:

1. Intragrain transport properties as much as grain boundary recombination and conduction barriers, limit the bulk transport properties of the substrate and reduce solar cell efficiency. Passivating these defects is just as important as grain boundary passivation in fabrication efficient cells on defected material.

2. Efficient large area solar cells of indium tin oxide on polycrystalline silicon can be repeatably fabricated using ion beam sputter deposition ITO on silicon. Efficiencies approaching 14% on 20 sq/ cm. devices were obtained on Wacker polycrystalling silicon. The major limitation on efficiency was open circuit voltage values which remained below 550 mV. Improvements in this parameter would allow efficiencies that would exceed those attained with p-n junctions.

3. The interfacial layer consists of silicon dioxide, after a 3 or 4 Angstrom transition layer. It does not appear that the interfacial layer is significantly pinholded and, based upon thermal aging and other studies, seems to be reproducible and exhibit no major enhanced degradation. However, thickness undulations in the oxide could lead to distributions of Schottky like and SIS like regions in a typical cell.

4) The use of an automated test system and automatic network analyzer provide detailed analysis of doping profiles and interface state densitites which are useful in analyzing process variations in device fabrication.

5) The noise spectral density test shows promise as a reliability predictor and also in detecting devices with particular types of defects.

6) Large area efficient devices do not exhibit major generation recombination currents nor edge leakage effects.

7) Indium supply will not impede the implementation of ITO based cells for large scale terrestrial applications.

8) Sputter deposited ITO solar cells are economically viable alternatives to p-n junctions for large scale terrestrial applicatons.

9) Data obtained on a variety of substrates indicates that the low temperature, low energy sputter deposited ITO devices may have performance advantages over p-n junction cells for highly defected polycrystalline substrates.

10) In-Situ etching, hydrogen annealing in the ion beam, and surface etching and milling techniques can significantly improve solar cell efficiencies on polycrystalline substrates.

At this time a number of factors relating to commercial viability of the technology, which were only surmised at the beginning of the program, appear clear. Given the area related substrate, encapsulation, interconnection, and panel area elements of photovoltaic modules, the junction formation step occupies a significant but not dominant place in cell fabrication economics. The dominant factor in the viability of a given technology lies in the ability to fabricate efficient devices on low-cost and highly defected substrates. For a given substrate cost and quality, when one trades off vacuum processing of ITO cells with reduced metalization, encapsulation and antireflection coating requirments, efficiency yield and long term stability become the deciding factors.

In ITO based systems, particularly using ion beam sputtering, the efficiency on polycrystalline substrates is presently competitive with p-n junctions and in highly defected materials may prove superior. Indeed, ITO sputtered deposited junctions utilize lower temperatures than diffusional based processes and lower energy than pulse processes such as ion implantation. These low temperatures and low energy processes could prove advantageous and even necessary on highly defected polycrystalline substrates for silicon and other advanced material.

It is worth noting that the efficiencies quoted in this report and the devices evaluated were not made under stringent clean room conditions. The target appeared mottled and black and was assayed at a purity less than 99%. The in-situ sputter etch provided an atomically clean surface which made the overall process relatively insensitive to prefabrication cleaning. In that regard, the sputter deposition process, wherein the substrate is etched, the interfacial oxide grown and the ITO deposited during the same pump-down underline the potential for fabrication under considerably less stringent cleanliness, with associated reduction in

costs, than usually required for solar cells and other semiconductor devices.

A critical finding of this program was that the efficiency exhibited by small devices can be readily scaled to larger area cells. The questions still remaining pertain to long term stability and reproducibility. In the former case, the question arises as to whether stability measurements on unencapsulated cells will be a good measure of field survivability. A reason for this question is that a major failure mode of present day cells is corrosion under or around a contact pad or metal grid line and not intrinsic failure of the junction itself. The encapsulation slows down or eliminates this particular failure mode. The question of reproducibility needs to be answered in a prototype production line environement. While a continuous sputtering system of the type offered by Leybold Hareaus may not be required, a planetary cassette fixtured system capable of producing ten or more wafers in a given pump down is required to develop a statistical base upon which projections may be made. Also, if this effort is undertaken, and our cell performance on large area substrates and economic studies indicate that it would be warranted, then it should be accompanied by the assembly of one or more panels so that encapsulated cells can be field tested and compared to comparable first generation cells obtained in early LSA purchases. This would seem a more reasonable comparison of ITO based devices than comparing initial panels based on ITO cells with third and fourth generation p-n junction panels from which the extrinsic and perhaps other degradation modes have been engineered out.

During the course of this investigation we corresponded extensively with our colleagues who are fabricating MIS and SIS cells using a variety of technologies. A common thread seemingly exists between all of these devices. In that regard, the concept of a conductor-insulator-

semiconductor (CIS) cell was developed. The properties of CIS cells were reviewed by a member of our group in collaboration with other researchers. These investigations and discussions conclude that CIS devices in general, and ITO sputter deposited devices in particular, presently remain viable alternatives to p-n junctions formed thermally or with pulse processing. As a result of this research program, a comprehensive understanding of ITO/Silicon solar cells was obtained. This understanding was used to improve the quality of the junction and of completed solar cells so that efficiencies competitive with p-n junctions on large area could be fabricated with a degree of repeatability. There were no fundamental limitations uncovered which would preclude the use of ITO in large scale terrestrial photovoltaic systems. While certain questions of device optimization, antireflection coatings, and reproducibility still remain, the time is near when a test of these devices simulating production line and field conditions will be warranted.

APPENDIX A - EDUCATIONAL COMPONENT

The work described in this report is part of MS/Ph.D. dissertation research of the following students:

Norm Chang	MS Thesis (1978)
Gary Cheek	MS Thesis (1979)
Chris Parsons	MS Thesis (1979)
Rajendra Singh	Ph.D. Thesis (1979)
Lou Gobis	MS Thesis (1979)*
Steve Goodnick	MS Thesis (1979)
Narumi Inoue	Ph.D. Thesis (1980)
Peter Smith	MS Thesis (1980)*
Carl Osterwald	MS Thesis (Early 1980 expected)
Alan Genis	Ph.D. Fall 1980 expected
John Wager	MS Thesis 1979
Norm Weaver	Ph.D. Thesis Fall 1980

*On the verge of completion

APPENDIX B

LIST OF PUBLICATIONS

1. "Fabrication and Characterization of Indium Tin Oxide (ITO)/ Polycrystalline Silicon Solar Cells", G. Cheek, N. Inoue, S. Goodnick, A. Genis, C. Wilmsen, and J. B. DuBow, Appl. Phys. Lett. 33, 643 (1978).

2. "Discussion on the Determination of Electron Affinity of In_2O_3 From Its Heterojunction Photovoltaic Properties", R. Singh, J. Electrochem. Soc. 126, 1081 (1979).

3. "The Operation of the Semiconductor-Insulator-Semiconductor (SIS) Solar Cell: Experiment", J. Shewchun, J. DuBow, C. Wilmsen, R. Singh, D. Burk and J. F. Wager, J. App. Phys. 50, 2832 (1979).

4. "Auger Analysis of Ultra-Thin SiO_2 Layers on Silicon", J. Wager and C. Wilmsen, J. App. Phys. 50, 2832 (1979).

5. "Detection of SiO_2 at the Indium Tin Oxide/Si Solar Cell Interface", J. F. Wager and C. W. Wilmsen, J. Appl. Phys. 50, 4172 (1979).

6. "Molybedenum Trioxide (MoO_3/Silicon Photodiodes", G. Cheek, C. Osterwald, J. DuBow and V. R. Pai Verneker, Appl. Phys. Lett 35, 775 (1979).

7. "Antireflection Properties of Indium Tin Oxide (ITO) on Silicon for Photovoltaic Applications", G. Cheek, A. Genis, J. DuBow, and V. R. Pai Verneker, Appl. Phys. Lett. (1979), 35, 495.

8. "The Semconductor-Insulator-Semiconductor (Indium Tin Oxide--On Silicon) Solar Cell: Characteristics and Loss Mechanisms", J. Shewchun, D. Burk, R. Singh, M. Spitzer and J. DuBow, J. App. Phys., Sept., (1979), 50, 6524.

9. "Optimization of Oxide-Semiconductor/Base-Semiconductor Solar Cells", R. Singh, K. Rajkanan, D. E. Brodie and J. N. Morgan, IEEE, Trans. Electron Devices, (1980) ED-27, 656.

10. "Importance of the Interface in Noncrystalline (Poly and Amorphous) Conductor-Insulator-Semiconductor (CIS) Solar Cells", R. Singh and K. Rajkanan, J. Vac. Sci. and Technol. 17, 376. (1980).

11. "Noise Spectral Density as a Device Reliability Estimate", J. DuBow and C. Osterwald, Solar Cells, In Press.

12. "Development Trends for the Mass Production of Conductor-Insulator-Semiconductor (CIS) Solar Cells", R. Singh, K. Rajkanan and J. B. DuBow Proc. 2nd Miami International Conf. of Alternative Energy Sources, Miami Beach, Florida, December 1979, (In Press).

13. "An Outlook for Automated Conductor-Insulator-Semiconductor (CIS) Solar Cell Factory", R. Singh, and K. Rajkanan, Proc. 14th IEEE Photovoltaic Specialists Conf. San Diego, CA, January 1980, (In Press).

14. "Automated Electronic Analysis of Solar Cells", K. Emery and J. DuBow Proc. 14th IEEE Photovoltaic Specialists Conf., January 1980, San Diego, CA, In Press.

15. "Automated Surface State Analysis of Solar Cells", P. Smith, J. DuBow and R. Singh, Proc. 14th IEEE Photovoltaic Specialists Conf., January 1980, San Diego, CA, In Press.

16. "Reverse Current-Voltage Characteristics of ITO/Si SIS Solar Cells Under Illumination", P. Smith, R. Singh, and J. DuBow, J. App. Phys., In Press.

17. "Thermal Degradation of Indium-Tin-Oxide/p-silicon Solar Cells", S. M. Goodnick, J. F. Wager and C. W. Wilmsen, J. Appl. Phys. (1980) 51, 527.

18. "Advances In the Fabrication and Characterization of ITO/Silicon Solar Cells", G. Cheek, A. Genis, L. Gobis, P. Smith and J. DuBow, Solid State Technology.

19. "Economic Analysis of Conductor-Insulator-Semiconductor (CIS) Solar Cells", R. Singh, W. S. Duff, J. DuBow, N. L. Weaver, and K. Rajkanan, Proc. Systems Simulation Conf., Jan. 1980, San Diego, CA (In Press).

20. "Efficient Indium Tin Oxide/Polysilicon Semiconductor-Insulator-Semicondutor Solar Cells", A.P. Genis, P. Smith, K. Emery, R. Singh, and J. DuBow, Appl. Phys. Lett (In Press).

21. "Recent Progress in Indium Tin Oxide/Polysilicon Semiconductor-Insulator-Semiconductor (SIS) Solar Cells", A.P. Genis, P. Smith, C. Osterwald, R. Singh and J. DuBow, IEEE Electron Devices Letter.

22. "Automated Steady State Admittance Spectrscopy for Surface Studies With Application to Solar Cells", P. Smith, R. Singh, A.P. Genis, and J. DuBow, IEEE Trans. Electron Devices (In Press).

23. "Fabrication of Solar Cells Utilizing Neutralized Ion Beam Sputtering", Proc. 9th International Conf. On Electrons and Ion Beam in Science and Technology ECS Meeting, May 1980 (In Press).

APPENDIX C
RESEARCH PARTICIPANTS

Professor Joel DuBow	Principal Investigator - Program Manager
Professor Carl Wilmsen	Co-Principal Investigator
Professor Bill Duff	Associate Investigator
Professor Rajendra Singh	Associate Investigator
Professor Rajeshwar Krishnan	Associate Investigator
Professor V.R. Pai Verneker	Visiting Faculty Investigator
Ara Kasanjian	Research Assistant
Gary Cheek	Graduate Research Assistant
Dan Ellsworth	Graduate Research Assistant
Keith Emergy	Graduate Research Assistant
Lou Gobis	Graduate Research Assistant
Steve Goodnick	Graduate Research Assistant
Narum Inoue	Graduate Research Assistant
Carl Osterwald	Graduate Research Assistant
David Newman	Graduate Research Assistant
Peter Smith	Graduate Research Assistant
John Wager	Graduate Research Assistant
Norm Weaver	Graduate Research Assistant
Lance Thompson	Undergraduate Assistant
Brian Prouty	Undergraduate Assistant
Larry Newell	Undergraduate Assistant
Bill Thaxton	Undergraduate Assistant
Donna McGregor	Administrative Secretary
Marcia Trepka	Secretary

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