CONF-970934--2

SAN097-0603C
SAND--97-0603C

Mechanisms for Enhanced Packaging and/or Burn-in Total Dose Sensitivity in Microelectronics

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*Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the US Dept. of Energy under Contract DE-AC04-94AL85000

Abstract. The ionizing radiation response of several semiconductor process technologies has been shown to be enhanced by plastic packaging and/or pre-conditioning (burn-in). Potential mechanisms for this effect are discussed and data on bipolar linear circuits are presented.

Introduction. In 1994 [1] it was shown that the total dose degradation of both a radiation hardened (Sandia CMOS IIIA) and a radiation tolerant (National Semiconductor Corp. NSC, FACT) bulk CMOS technology was enhanced by an elevated temperature burn-in. The static power supply current exceeded the specification value at the rated total dose level on parts which had been subjected to burn-in, whereas parts without burn-in easily passed. In another study of the NSC FACT process [2] the total dose effects of packaging (ceramic and plastic), in addition to the effects of burn-in, were characterized. For both high and low dose rates, where the failure mechanisms were different (n channel edge leakage at high rate and field oxide leakage at low rate), the plastic package greatly enhanced the effect of burn-in. The mechanism for the burn-in effect was studied on the radiation hardened technology [1, 3] using both gate and field oxide MOSFETs. Charge separation analysis performed on the gate oxide transistors showed that burn-in had very little effect on the irradiation induced increase in oxide trapped charge, ΔN_{ot}, but it significantly reduced the buildup of interface traps. ΔN_{it}. No charge separation analysis was possible in the field oxide transistors because of their design. However the field oxide transistors were studied for the effects of temperature and bias during burn-in using the irradiation induced threshold shift at 10 nA drain current [3]. It was shown that the mechanism was a function of time and temperature, with no bias dependence. The shift in the subthreshold region was nearly parallel and much larger in the burned-in devices, suggesting that the enhanced effect was due to larger ΔN_{ot}. The activation energy for the process was determined to be 0.38 eV, which is similar to that of hole compensation (0.41 eV) [4] and molecular hydrogen diffusion in bulk fused silica (0.45 eV) [5].

In the packaging/burn-in study on NSC FACT [2], the burn-in effect was shown to be greatly enhanced by the plastic package, whereas for the non burned-in parts there was little effect of packaging. Additional testing, previously unpublished, showed that the burn-in effect was not sensitive to bias, indicating that the same mechanism observed in the Sandia CMOS IIIA may be at work in the NSC FACT technology. It is not known whether the n channel edge or the field oxide leakage is a result of ΔN_{ot} alone or ΔN_{ot} compensated by ΔN_{it}, since field oxide test structures were not available. However, since the plastic alone has little effect, it appears that the plastic accelerates the burn-in effect. Additional tests are planned to vary the time and temperature of the plastic molding process to see if greater time and/or temperature causes more burn-in effect. Also tests will be performed to isolate potential plastic effects such as mobile ion charging and stress.

Although the burn-in effect has been observed in two CMOS process technologies, to date it has not been reported in any bipolar technologies. In this paper we will show new data demonstrating the burn-in effect in a bipolar linear circuit. We will also present a summary of all of the studies (to our knowledge) on the burn-in and packaging effect on total dose response.

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Experimental Details and Discussion. Characterization testing was performed on LT1014 bipolar linear quad operational amplifiers to study the effect of burn-in on the total dose response in plastic packaged parts. No comparison was made to parts in ceramic packages. All parts in the study were from the same date code (9603) and no burn-in had been performed by the manufacturer. One group of samples was burned-in prior to irradiation at 125 °C for 160 hours under static dc bias. Eight samples from the burned-in group and 8 non burned-in samples were irradiated at 90 rad (Si)/s in a Co-60 source, under static dc bias, to cumulative dose levels of 5, 10, 15, 20, 25, 30, and 40 krad (Si). All of the specification electrical parameters were measured before and after burn-in and after each irradiation level. No significant changes in preirradiation parameters were observed as a result of the burn-in alone. The total dose response of four sensitive parameters is shown in Figures 1-4 as the average value of the parameter for op amp #1 in the quad (all 4 op amps in the package showed similar response) vs. dose for the 8 burned-in (BI) and 8 non burned-in (NBI) parts. Data are not shown in the figures past the onset of functional failure, where parameter shifts become large and erratic. For the BI parts this occurred between 20 and 25 krads and for the NBI parts it occurred between 30 and 40 krads. However, even though the BI parts failed at a lower dose level, many of the electrical parameters showed *less* degradation than the NBI parts at dose levels below failure as discussed below. Figures 1-3 show the positive supply current (I_{S+}), the positive input bias current (I_{b+}) and the input offset voltage (Vos), respectively. The negative Is and Ib showed the same qualitative response as the positive Is and Ib. For each of these parameters the BI parts degraded substantially less than the NBI parts. The mechanism for this behavior is related to the excess base current in the critical transistors. For the LT1014, the input transistors are substrate pnps and the current sources use lateral pnps. A recent study on the mechanism for excess base current in lateral and substrate pnp transistors [6] shows that the dominant parameter is an interface trap induced increase in surface recombination velocity. Increases in oxide trapped charge, on the other hand, offset the effect of increased surface recombination velocity, resulting in less excess base current. Thus the better performance of I_{S+}, I_{b+} and Vos in the BI parts may be the result of both a reduction in ΔN_{it} and an increase in ΔN_{ot}. However, even though these parameters showed less effect from burn-in, other parameters, e.g. voltage gain, showed much more degradation from burn-in, which leads to earlier onset of functional failure of the BI parts. The voltage gain depends on npn transistor gain, which is more affected by ΔN_{ot} [7]. In npn transistors the total dose dependence on ΔN_{ot} is exponential, whereas the dependence on ΔN_{it} is linear.

Based on the LT1014 results, it appears that the mechanisms which explain the CMOS burn-in effect are consistent with the bipolar linear response. Data are currently being taken on NSC LM111 voltage comparators. Results will be presented in the full paper.

Summary of Data on Packaging/Burn-in Effect on Total Dose Response. In addition to the studies discussed above, the effects of packaging and/or burn-in on total dose response have been studied in bipolar transistors [8-11], power MOSFETs [11] and additional CMOS microcircuit technologies [12]. Also, previously unpublished data have been taken at NSWC Crane on the effects of both packaging and burn-in on an NSC LM119 bipolar dual voltage comparator. Table 1 is a list of all of the part types and process technologies that have been studied to date (to our knowledge) along with whether or not a sensitivity was observed for either packaging, burn-in or both. Two of the studies looked at discrete bipolar junction transistors, BJTs [8-11]. In the more recent work by Dowling and West [10] the study was performed on a single process lot of material for each of two npn BJT part types, looking at gain degradation. Die were packaged in four package types, metal can (TO5), epoxy potted in metal can, and both ceramic and plastic surface mount (SOT23). The only major effect seen for package type was that the ceramic SOT23 part degraded more than the others for both BJT types. In all package types the effect of burn-in was a 10% greater gain degradation. In the ERA study [11], two npn BJT types were characterized as a function of burn-in for both ceramic and plastic packages. Unfortunately the ceramic and plastic parts were from different process lots. Considering the spread in the data, the only clear effect of burn-in was that for one type in plastic, the burn-in resulted in significantly *less* degradation. For the other three groups there was no significant effect. In the same study [11] both n and p channel power MOSFETs were characterized for the burn-in effect in both ceramic and plastic. No packaging or burn-in effects were observed. In the NSWC study on the NSC LM119, the plastic parts degraded about a factor

of two more than the ceramic parts, but there was only a small effect of burn-in. However, the burn-in alone resulted in a significant change in the plastic parts. All die were from the same wafer intended for space and military parts, which did not have a silicon nitride overcoat. The nitride overcoat is always used for commercial plastic parts at NSC. Thus the plastic package results are not representative of available packaged product but may provide insight into effect of plastic alone on the total dose response. In a recent study by Hash, et al, [12] four additional CMOS microcircuit technologies were evaluated for the burn-in effect. Only one demonstrated a significant effect as shown in Table I. No details of the process are available, nor are there tests structures for evaluation.

The effect of packaging on the total dose response has been studied independently of burn-in, but few studies have had adequate controls to isolate effects to package alone. Because of the potentially large variation in total dose response from process lot to lot and even wafer to wafer within the same lot, it is necessary to have die from a single wafer to assure that package is the main variable. Another variable which is introduced in a packaging study is the determination of total dose in the sensitive dielectric. Many package configurations cause significant dose enhancement in sensitive regions. Only one of the studies cited [10] show a significant package effect without a burn-in effect, and this occurred in a ceramic package.

Conclusion. Many studies have been performed to look at the effects of packaging and/or burn-in on total dose response. We have presented a summary of these studies to date (to our knowledge). Only 4 process technologies (3 CMOS and 1 bipolar) show a significant burn-in effect to date. The mechanisms for this effect appears to be consistent with that reported earlier [1, 3] for the Sandia CMOS IIIA process. Additional testing with appropriate test devices and structures will be conducted to determine the universality of these mechanisms.

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Figure 1. Average Is+ vs. Dose

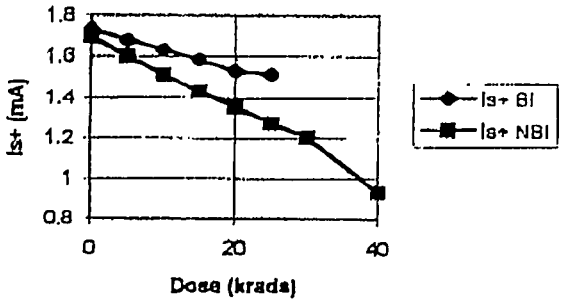

Figure 2. Average Ib+ vs. Dose

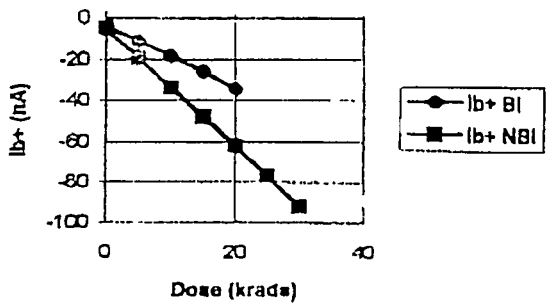

Figure 3. Average Vos vs. Dose

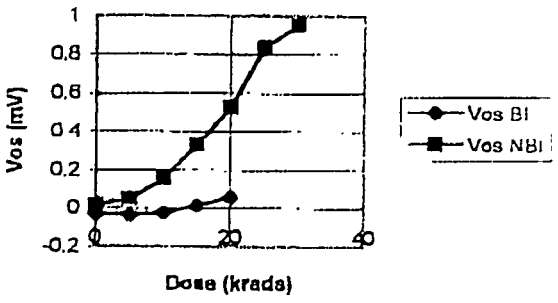

Figure 4. Average Gain vs. Dose

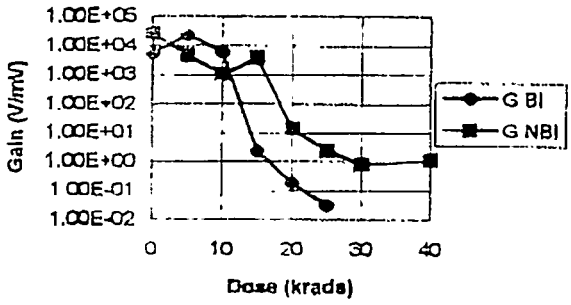

Table 1. Devices and Circuits Characterized for Packaging/Burn-in Total Dose Sensitivity

Device/ Circuit PN	Description	Manuf.	Process Technology	Category	Package(s)	Test Agency	Package Effect	Burn-in Effect
	16k SRAM	SNL	CMOS IIIA	rad hard	CDIP*	SNL		large
	line driver	NSC	FACT	rad tol	CDIP	SNL		large
	4-bit counter	NSC	FACT	rad tol	CDIP	SNL		large
HSC240	octal buffer	Harris	CMOS/SOS	rad hard	CDIP	SNL		none
	1 Mbit SRAM	LMSC	HMCMOS	rad hard	CDIP	SNL		none
	256k SRAM	Cypress	0.5 um CMOS	rad tol	CDIP	SNL		none
	256k SRAM	Paradigm	0.8 um CMOS	comm	SOP	SNL		significant
54AC02	2 input NOR	NSC	FACT	rad tol	CDIP, PDIP*	NSWC	large	large
LM119	dual comp.	NSC	bipolar linear	comm	CDIP, PDIP	NSWC	significant	none
BC106	npn BJT	ZETEX	bipolar	comm	TO18, E-line	ERA	small	small
MAT-04	npn BJT	PMI	bipolar	comm	CDIP, SOIC (P)	ERA	small	small
BUZ900	n Power FET	Siemens	DMOS	rad tol	TO3, TO247(P)	ERA	none	none
BUZ905	p Power FET	Siemens	DMOS	rad tol	TO3, TO247(P)	ERA	none	none
IRF530	n Power FET	IR	DMOS	rad tol	TO220 (P)	ERA		none
LT1014	op amp	Lin Tech	bipolar linear	comm	plastic	HAC		large
LT1021	regulator	Lin Tech	bipolar linear	rad tol	Hermetic	HAC		small
BCW60	npn BJT	ZETEX	bipolar	comm	TO5, SOT23(C,P)	CU	large	small
BC857	npn BJT	ZETEX	bipolar (SIN)	comm	TO5, SOT23(C,P)	CU	large	small

* CDIP- ceramic dual in-line, PDIP- plastic dual in-line