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DIGITAL RLC ANALYSIS OF CDU FIRESET X-UNITS

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ABSTRACT

An accurate and repeatable technique has been developed for quantitatively determining the dynamic resistance, inductance, and capacitance (RLC) of CDU Fireset X-units by digital analysis of the output current waveform.¹ The waveform is digitized with 8 bit resolution at a 10 ns sample rate. A calibration file provides correction for attenuator and digitizer errors. Data accuracy is optimized by software filtering to minimize the digitizing noise component. R, L, and C are derived by selecting any four waveform coordinates as limits for a series of multiple numerical integrations. The integrals become coefficients for a system of linear equations which are solved simultaneously to obtain the circuit impedance. The approach is independent of circuit damping, eliminates the need for determining the waveform starting point, and is accurate to 1 percent in the presence of noise. The technique has been successfully employed at Bendix to identify defects and variations in components and processes used in the manufacture of X-unit assemblies.

INTRODUCTION

This development of a digital processing approach to the analysis and troubleshooting of CDU fireset X-units is the result of a cooperative effort between Bendix Kansas City Division and Sandia Laboratories Albuquerque to develop a capability which has proven mutually beneficial.

I wish to acknowledge the major contributions of J. M. Portlock and T. D. Donham of SLA.

Firesets perform the critical function of providing the rapid transfer of high energy necessary to initiate the nuclear process in a weapon system. The heart of a CDU fireset, the so-called X-unit, is a series arrangement of an energy storage capacitor, a high-voltage switch and a load current distribution block (Figure 1). In operation, the energy storage capacitor is charged to several kilovolts and the stored energy is released through the triggered high voltage switch into a load simulator.

*Work supported by the United States Department of Energy.

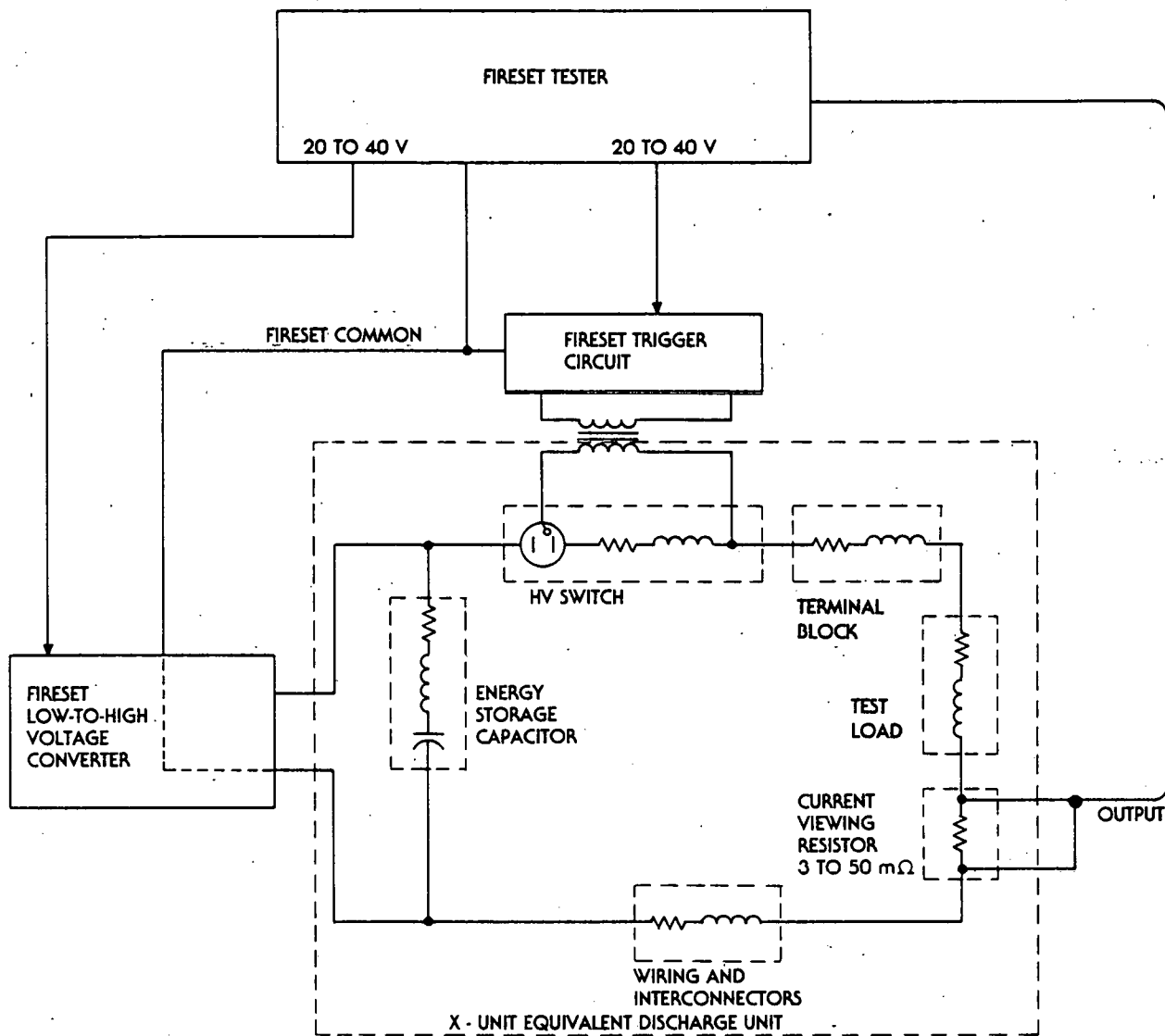


Figure 1. Typical Fireset X-Unit Test Setup, Showing X-Unit Equivalent Discharge Circuit

The discharge current flow in this series circuit is usually damped-sinusoidal in shape. The peak current can attain values as high as 30,000 A with a typical half-cycle duration of 1 μ s. For a given value of high voltage, the amplitude and shape of the current waveform are a direct function of the dynamic resistance, inductance, and capacitance comprising the discharge loop. While the circuit capacitance is effectively that of the energy storage capacitor, the resistance and inductance are distributed in nature and are constituted from the distributed characteristics of the components of Figure 1 as well as the characteristics of the wiring and interconnections. Subtle variations in these elements, such as variations in component internal construction, component placement, wire routing, and interconnect quality, can modify the loop impedance and produce undesirable changes in X-unit performance.

THE IMPORTANCE OF RLC ANALYSIS

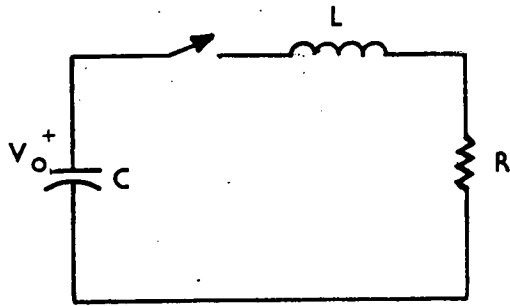
A quantitative determination of the discharge loop impedance is important for several reasons. Knowledge of the loop characteristics not only yields additional product quality information, but establishes a basis for properly directing troubleshooting activity and provides a greater insight into the effect of component variations and manufacturing processes. With this information, our ability to properly assess product manufacturability is greatly improved. Firesets, being limited-life devices, are restricted to a specific number of firing operations. RLC analysis supports efforts to obtain maximum information from a single test firing.

LIMITATIONS OF PREVIOUS TECHNIQUES

Techniques used in the past to determine X-unit RLC by analysis of the output current waveform have been based on a series RLC circuit model (Figure 2) governed by differential equation 1.1, referenced to t_0 , the time of switch closure.²

$$\frac{1}{C} \int_0^t i dt + L \frac{di}{dt} + Ri(t) = V_0 \quad (1.1)$$

Underdamped test loads producing "ringing" waveforms were often used. Solutions for R, L, and C were derived from benchmark measurements of the current waveform such as the peak current, time to peak and the half-period. The accuracy and repeatability of these techniques were limited by a number of factors. Waveform measurements were usually derived from oscilloscope photographs, introducing equipment limitations and a severe subjective element into the data. The recent advent of heavily damped test



$$\frac{1}{C} \int_0^t i dt + L \frac{di}{dt} + Ri(t) = V_0$$

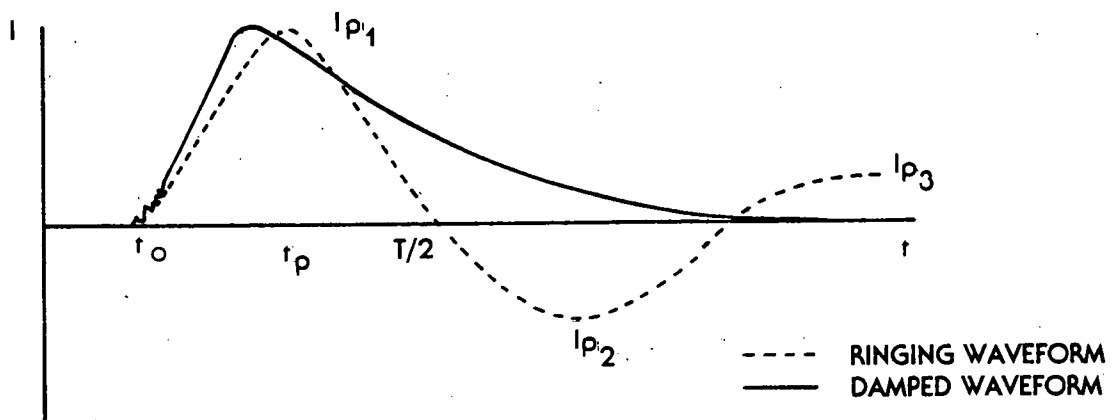


Figure 2. Series RLC Circuit Model and Typical Waveforms

loads for reliability reasons effectively removed many of the benchmark waveform characteristics, making analysis more difficult. The techniques were time-referenced to t_0 , which was often masked by leading edge noise. Some approaches required the assumption of a circuit capacitance value, thus eliminating the opportunity for self-checking against the only lumped element value that one could reference with some confidence. And finally, the dependence of these techniques on instantaneous waveform values precluded their use in a digital approach due to their sensitivity to noise and transients, which are inherent in both the waveform and the digitizing process.

THE HARDWARE SYSTEM

A hardware system, illustrated in the block diagram of Figure 3, was used to develop a new digital approach to the RLC analysis problem, overcoming the limitations of previous techniques. The computerized system automatically arms and fires the X-unit. A current-viewing resistor converts the discharge current to an analog voltage waveform which is transformed into a digital format by a Biomation 8100 digitizer. This conversion is conducted at a 10 ns sample rate with a resolution of 8 bits. Calibration techniques developed for both the pulse transmission system and the digitizer are used to ensure accuracy of the acquired data. The digital waveform data is stored on disc memory, from which it can be retrieved at any time for analysis. A CRT and printer/plotter provide I/O and hard copy capability.

DEVELOPMENT OF THE ANALYSIS TECHNIQUE

Figure 4 is a system plot of a typical digitized waveform. A technique was desired which could accurately and repeatably determine, from a waveform such as this, the resistance, inductance, and capacitance of the generating circuit.

Since the unknowns of interest (R , L , and C) appear in the differential equation (Equation 1.1) governing the series circuit model, it seemed that direct use of this equation represented the most general approach. Inspection revealed that the coefficients of the unknowns, i.e., the integral, the derivative or slope, and the magnitude of current at any time, t , were quantities which could be numerically evaluated from the digital waveform data. Evaluating these quantities at any three successive waveform points (Figure 5) would establish a linear system of three equations, from which the unknown R , L , and C could be derived (Equation 1.2).

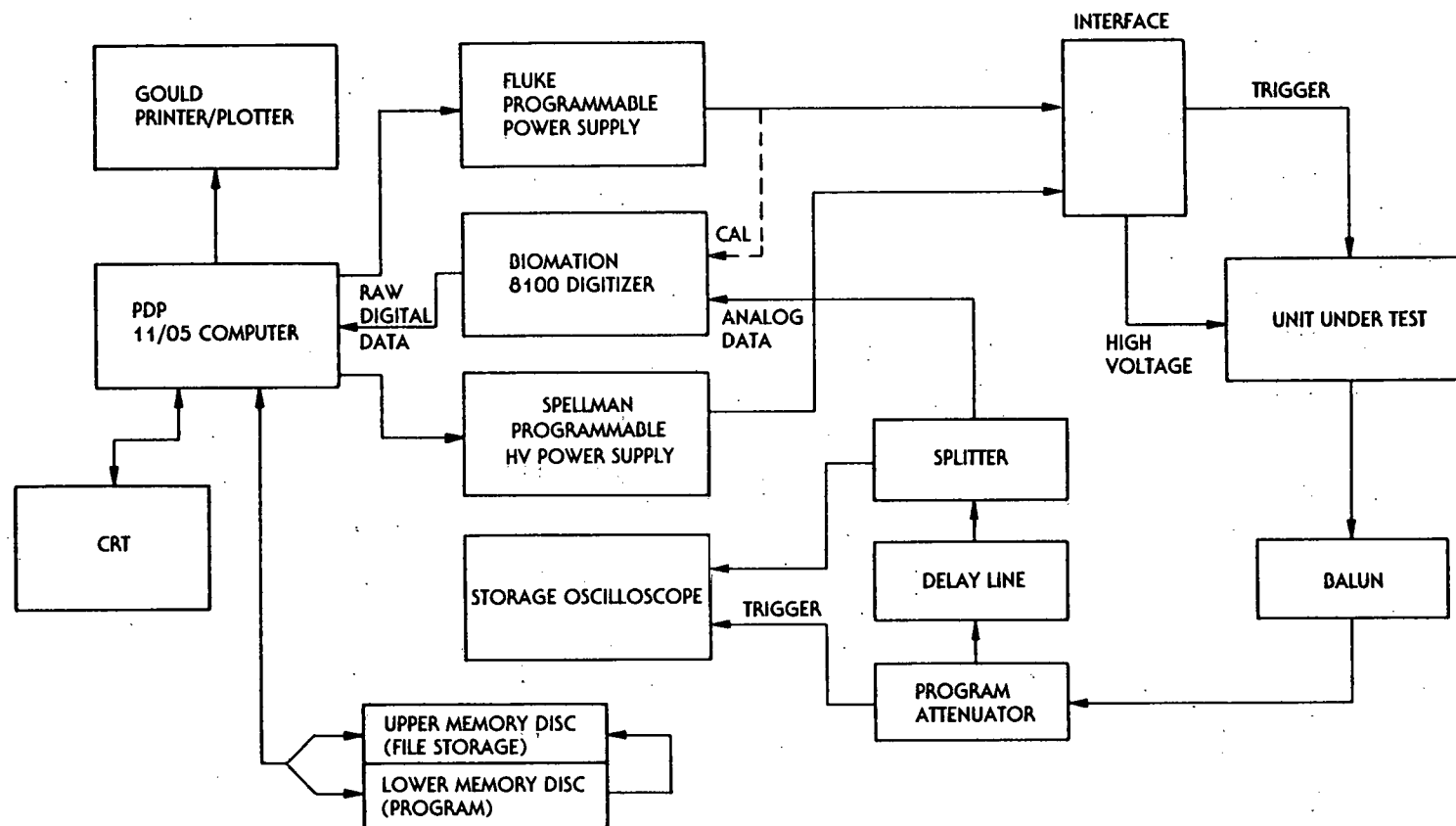


Figure 3. Block Diagram of Fireset X-Unit Analysis System

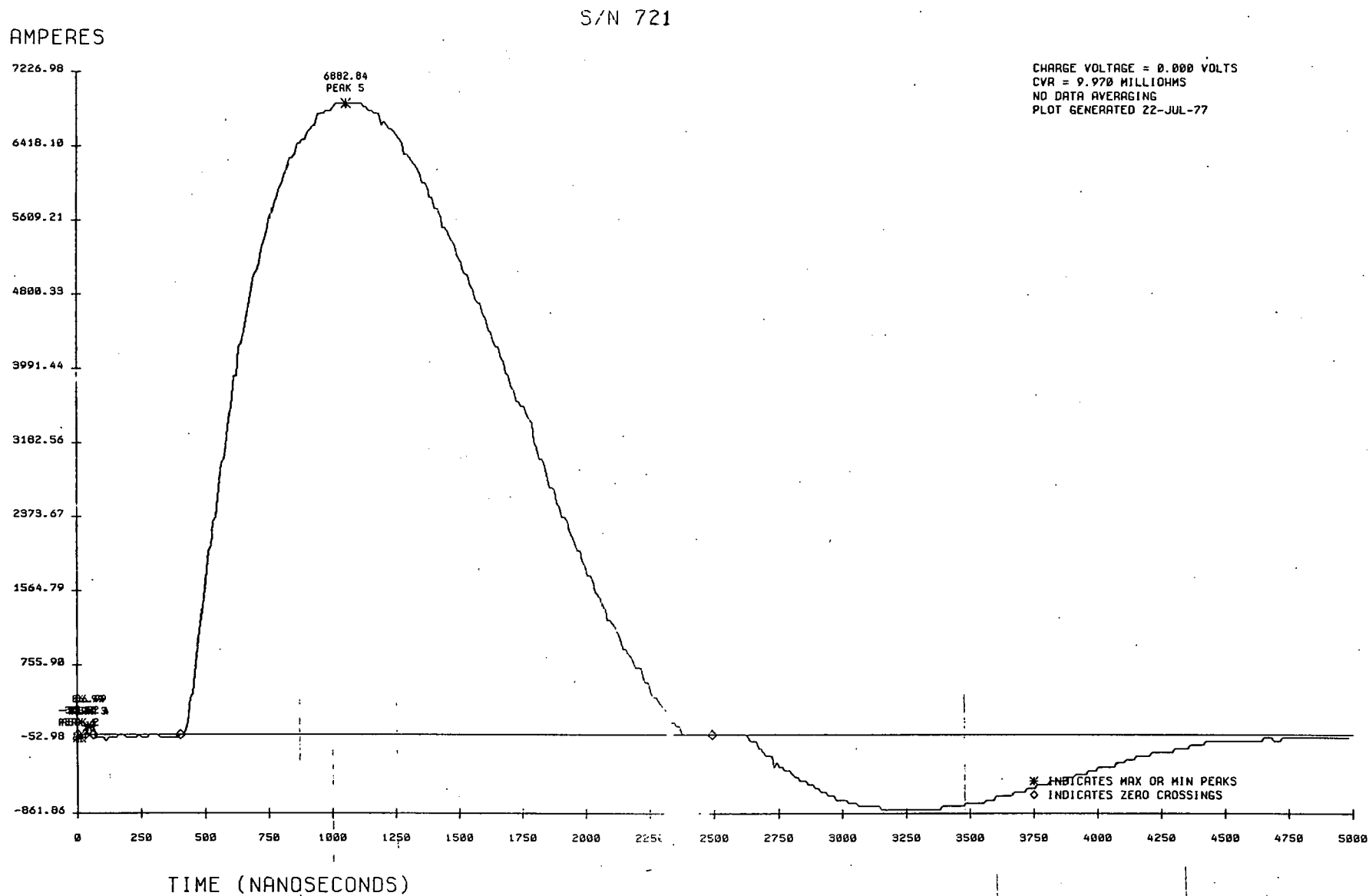


Figure 4. Plot of Typical X-Unit Output Waveform

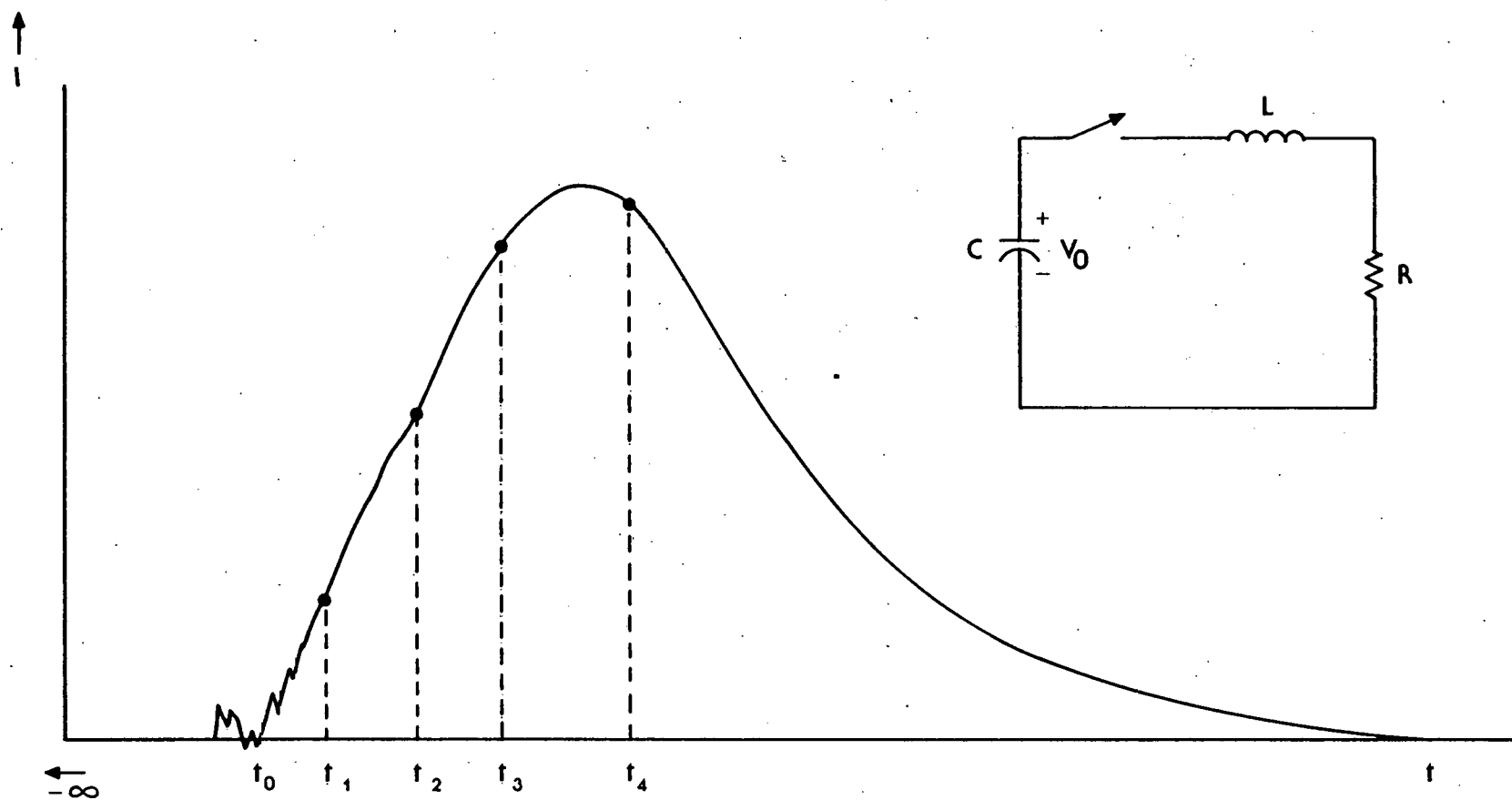


Figure 5. Exemplary Waveform Points Used in RLC Analysis

$$\left| \begin{array}{c} \int_0^{t_1} i dt \, di/dt_1 \, i(t_1) \\ \int_0^{t_2} i dt \, di/dt_2 \, i(t_2) \\ \int_0^{t_3} i dt \, di/dt_3 \, i(t_3) \end{array} \right| = \left| \begin{array}{c} \\ \\ \\ \end{array} \right| V_0 \quad (1.2)$$

Although theoretically correct, this approach suffers from two practical disadvantages. First, the location of the waveform starting point is still required for time reference. Second, the derivative or slope measurement is highly noise sensitive, and small errors in the magnitude of current are severely magnified in the final calculations.

It was suggested that the waveform starting point problem could be alleviated if one were free to select any convenient time reference point, and particularly one beyond leading edge noise, such as t_1 in Figure 5. Mathematically, this can be achieved by including a term, Q , in the equation, representing charge transfer from the capacitor prior to time t_1 (Equation 2.1).

$$\frac{1}{C} \int_{t_1}^{t_2} i dt + \frac{1}{C} \underbrace{\int_{-\infty}^{t_1} i dt}_Q + L \frac{di}{dt} + Ri(t) = V_{-\infty} \quad (2.1)$$

This term is essentially a constant of integration which becomes zero when time is referenced to switch closure.

Further, by integrating this equation from t_1 to t_2 , the derivative is eliminated and the coefficients become double and single integrals, a time interval and the relative difference between two current levels. The evaluation of these quantities at any three successive points with respect to t_1 provides the coefficients for a three equation system which can be solved for R , L and C (Equation 2.3).

$$\underbrace{\frac{1}{C} \int_{t_1}^{t_2} \left(\int_{t_1}^{t_2} [i dt + Q] \right) dt}_{D1} + L \underbrace{(i[t_2] - i[t_1])}_{W1} + R \underbrace{\int_{t_1}^{t_2} i dt}_{S1} = \underbrace{V_{-\infty}(t_2 - t_1)}_{V1} \quad (2.2)$$

$$\begin{vmatrix} D1 & W1 & S1 \\ D2 & W2 & S2 \\ D3 & W3 & S3 \end{vmatrix} = \begin{vmatrix} V1 \\ V2 \\ V3 \end{vmatrix} \quad (2.3)$$

The multiplicity of integral coefficients introduces a measure of noise insensitivity into the calculations, since integration is by nature a low-pass mathematical procedure. A Fortran algorithm for the four-point impedance analysis technique is shown in Figure 6.

ERROR ANALYSIS

As a graphic means of displaying the accuracy of this technique, a fireset waveform (Figure 7) was mathematically simulated from Equation 1.1, using specific values of R, L, and C. The simulated waveform data was truncated to represent a resolution of 8 bits. In addition, a random ± 1 increment error, which can be expected in the digitizing process, was included. The four-point analysis method was applied over a major portion of the waveform and the calculated values of R, L, and C were expressed as a percentage error with respect to the known input.

Two methods were used in this analysis. In method 1, four points (represented by the dots in Figure 7) were selected, and RLC was calculated. Then each of the points except the reference point, t_1 , was moved forward 10 ns, and the calculation was repeated. This sequence was then repeated until the coordinate X was reached by point 4. The time interval t_1 to t_4 increased by 30 ns for each calculation using this method. Method 2 is similar, except t_1 was also moved, thus maintaining a constant time interval t_1 to t_4 . The percentage error of the calculated RLC values is shown in Figures 8 and 9.

Method 1 (Figure 8) produced initial errors of ± 5 percent, which gradually decrease with time because of the increasing sample interval. The mathematics respond to error by adjusting R and C in opposition to L to satisfy the basis equations. Changing the reference point as in method 2 (Figure 9) results in a major error response in the inductance, the coefficient of which does not involve an integral. Using this method, the inductance error envelope increases dramatically as the waveform baseline is approached, due to the increasingly higher percentage error represented by the ± 1 increment built into the data.

```

0001      SUBROUTINE RLC
0002      COMMON /ANAL1/ B,ZRX,NZ,NSM,MAX,MIN,SSM,ZRXV(20),OFS
0003      COMMON /BLK1/ U,R,L,C,IT1,IT2,IT3,IT4,G
0004      REAL B(2040),U,R,L,C
0005      INTEGER IT1,IT2,IT3,IT4

0006      Q1=0.0
0007      Q2=0.0
0008      Z=0.0
0009      S1=0.0
0010      T=1.E-8
0011      DO 150 I=1,IT1
0012      Q2=Q2+(Z+B(I))/2.
0013      Z=B(I)
0014 150    CONTINUE
0015      Q=Q2
0016      D1=Q*(FLOAT(IT2-IT1))
0017      DO 200 I=IT1+1,IT2
0018      Y=S1
0019      S1=.5*(B(I-1)+B(I))+S1
0020      D1=D1+(Y+S1)/2.
0021 200    CONTINUE
0022      S2=S1
0023      D2=D1+Q*(FLOAT(IT3-IT2))
0024      DO 300 I=IT2+1,IT3
0025      Y=S2
0026      S2=.5*(B(I-1)+B(I))+S2
0027      D2=D2+(Y+S2)/2.
0028 300    CONTINUE
0029      S3=S2
0030      D3=D2+Q*(FLOAT(IT4-IT3))
0031      DO 400 I=IT3+1,IT4
0032      Y=S3
0033      S3=.5*(B(I-1)+B(I))+S3
0034      D3=D3+(Y+S3)/2.
0035 400    CONTINUE
0036      Q=Q*T
0037      S1=S1*T
0038      S2=S2*T
0039      S3=S3*T
0040      D1=D1*T**2
0041      D2=D2*T**2
0042      D3=D3*T**2
0056 460    U1=U*(FLOAT(IT2-IT1))*T
0057      V2=U*(FLOAT(IT3-IT1))*T

0058      U3=U*(FLOAT(IT4-IT1))*T
0059      W1=B(IT2)-B(IT1)
0060      W2=B(IT3)-B(IT1)
0061      W3=B(IT4)-B(IT1)
0062      DEN=S1*W2*D3+W1*D2*S3+D1*S2*W3-S1*D2*W3-W1*S2*D3-D1*W2*S3
0063      R=U1*W2*D3+W1*U3*D2+D1*W3*U2-U1*D2*W3-W1*D3*U2-D1*W2*U3
0064      R=R/DEN
0065      L=S1*U2*D3+U1*D2*S3+D1*S2*U3-S1*D2*U3-U1*S2*D3-D1*U2*S3
0066      L=L/DEN
0067      C=S1*W2*U3+W1*U2*S3+U1*S2*W3-S1*U2*W3-W1*S2*U3-U1*W2*S3
0068      C=DEN/C
0069      RETURN
0070      END

```

Figure 6. Fortran Algorithm, Four-Point Impedance Analysis

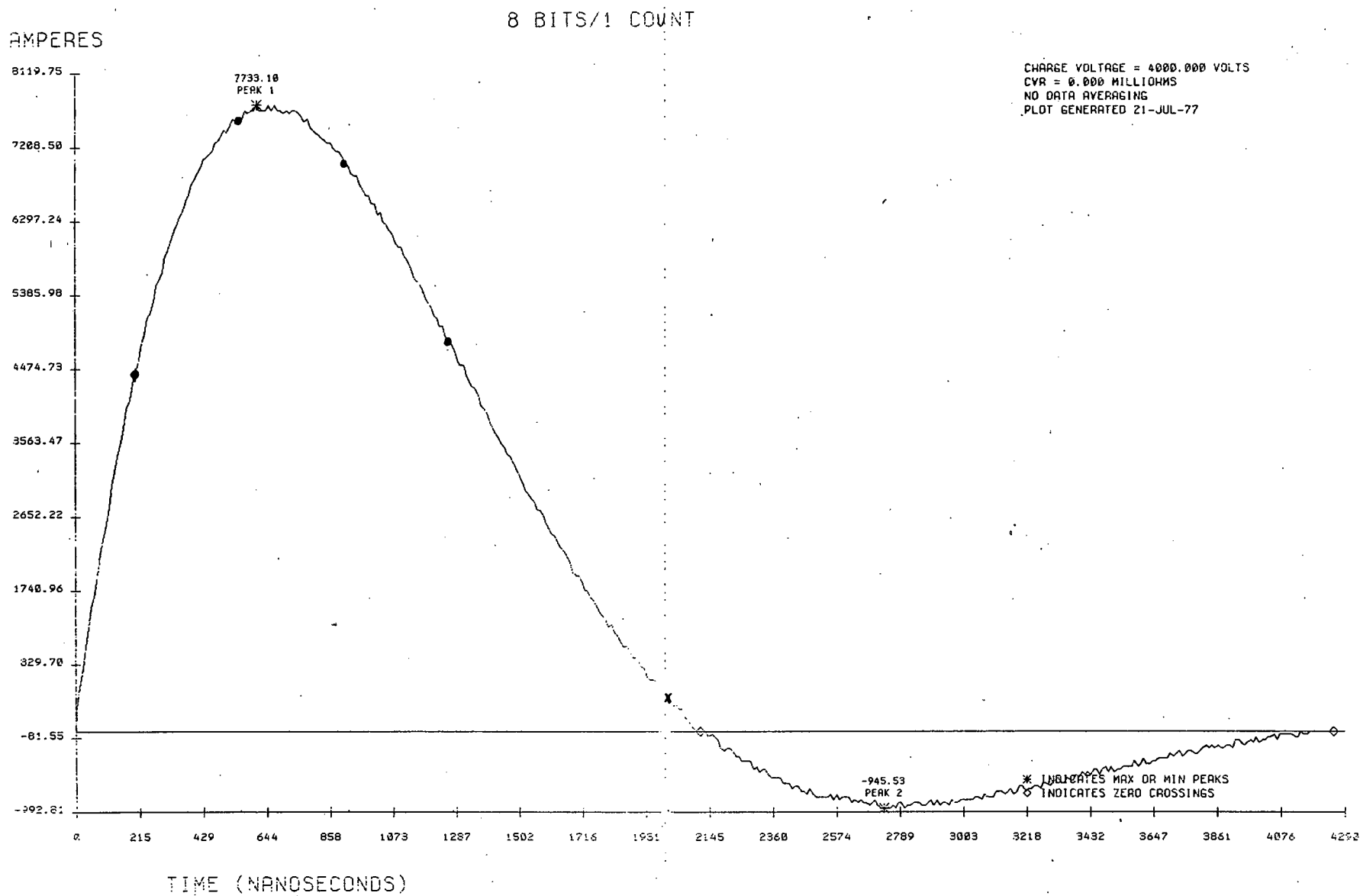


Figure 7. Simulated Fireset Waveform With Error

8 BITS/1 COUNT
COMPARATIVE PLOT OF PERCENTAGE
DIFFERENCE IN R,L,C VALUES

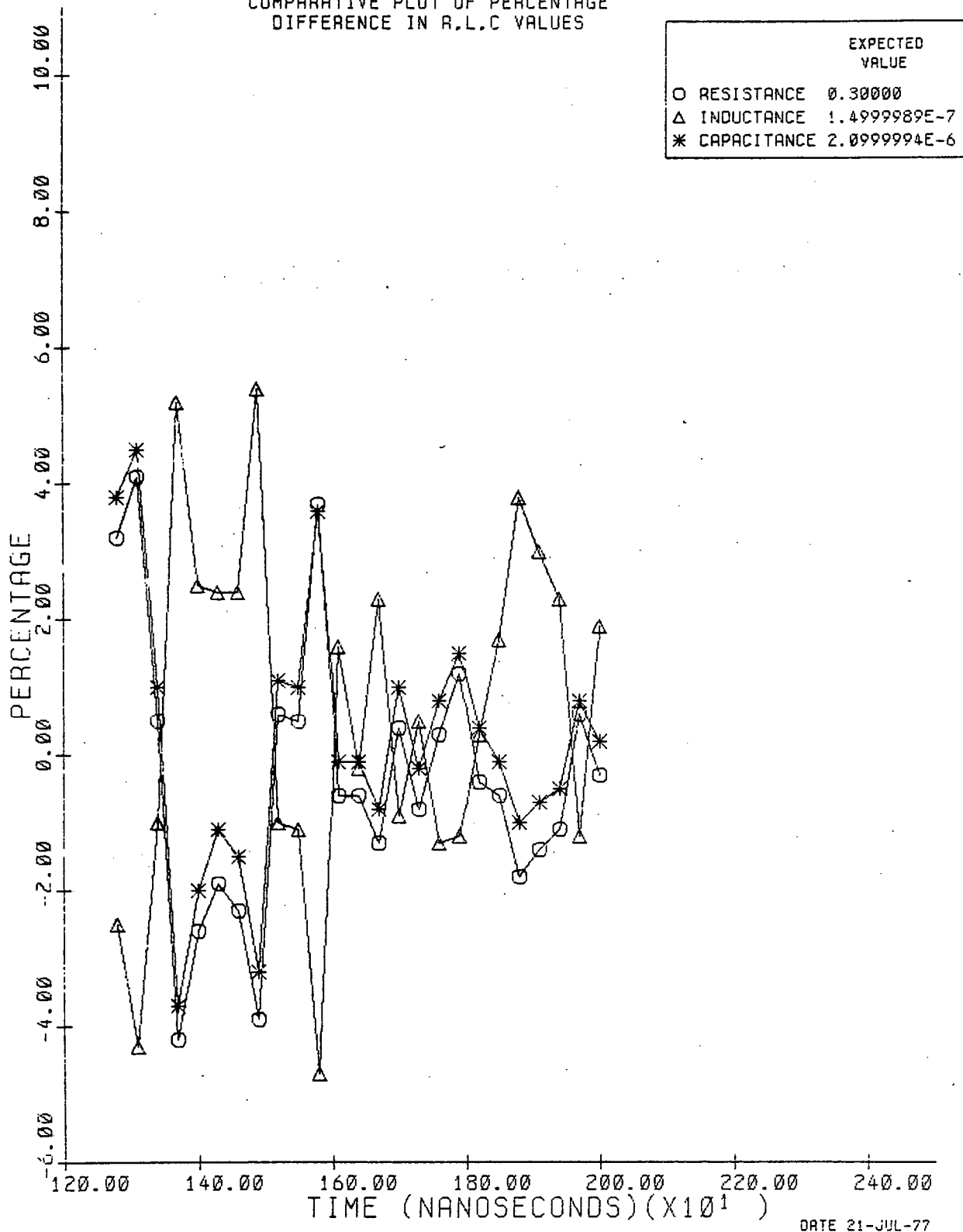


Figure 8. RLC Analysis, Using Method 1

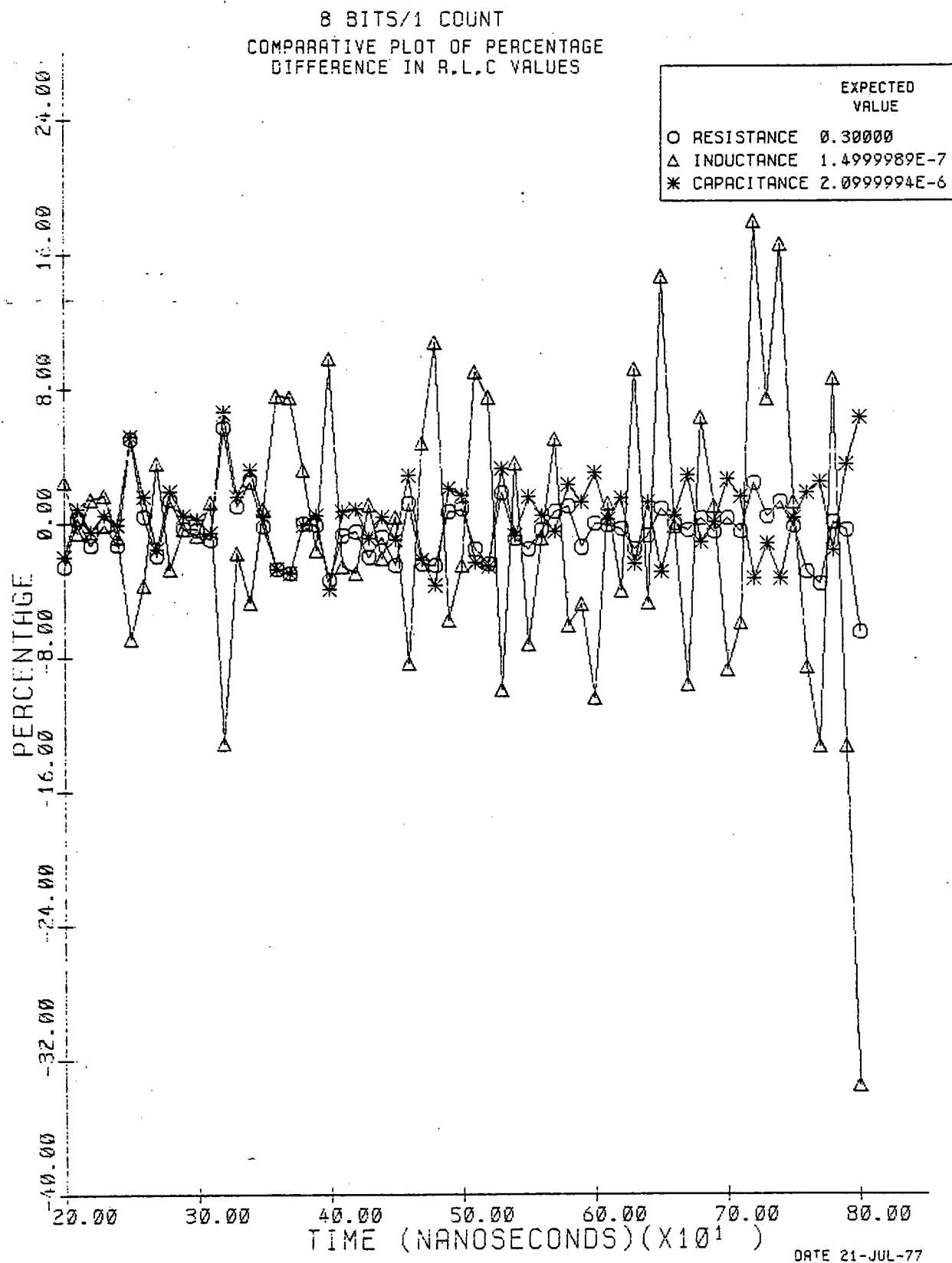


Figure 9. RLC Analysis, Using Method 2

IMPROVEMENT BY FILTERING

The errors in these calculations are a direct result of error in the digitized waveform data. This error can be viewed as a superimposed noise component resulting from discrete sampling of the data as opposed to an analog measurement. A significant part of this error can be removed by passing the digital data through a low-pass software filter (Figure 10). Ideally, one would filter at a cutoff frequency which optimizes the accuracy of the RLC calculations. This involves a compromise value, since the reduction in noise power with descending cutoff frequency is accompanied by an increasing bandpass error which operates to remove the higher frequency harmonics of the waveform. At a 10 ns sample rate and for typical X-unit waveforms, an optimum filter cutoff frequency of 5 MHz has been determined. Figures 11 and 12 show the improvement in accuracy of the previous RLC calculations resulting from use of the filtered data. The filtered waveform is shown in Figure 13, with the filtering terminated at $t=3500$ to illustrate its effect. The Fortran filter algorithm is shown in Figure 14.

APPLICATION EXAMPLES

Figures 15 through 21 are exemplary analyses of components and X-units using the method 1 analysis. The comparative plots in these figures indicate the percentage difference in RLC of the configuration under test, and a set of expected values characteristic of the reference circuit. Positive percentage indicates a value lower than the reference, while the negative percentage indicates a value greater than the reference.

Figure 15 illustrates the capability of the analysis technique to discriminate the parameters R, L, and C. The plot is an analysis of a SA659-229 400-m Ω wirewound resistor carrying a peak pulse current of 2700 A. The evaluation was performed using a special test fixture consisting of an SA2296 capacitor and a highly repeatable solid dielectric switch. Reference values for R and L were derived from a four-point analysis of the fixture with the resistor omitted. The calculated capacitance value of 2.11 μ F is within 1 percent of the 2.09 μ F value measured on a small-signal bridge. The calculated value of resistance was 410 m Ω , compared with a value of 403 m Ω as measured on a small-signal bridge at 200 KHz. The increase may be attributable to ohmic heating of the resistive element. An inductance value of 31 nH was calculated. Using the average value of R, L, and C over the time interval shown, the circuit waveform was mathematically reconstructed to within 1 percent of the original.

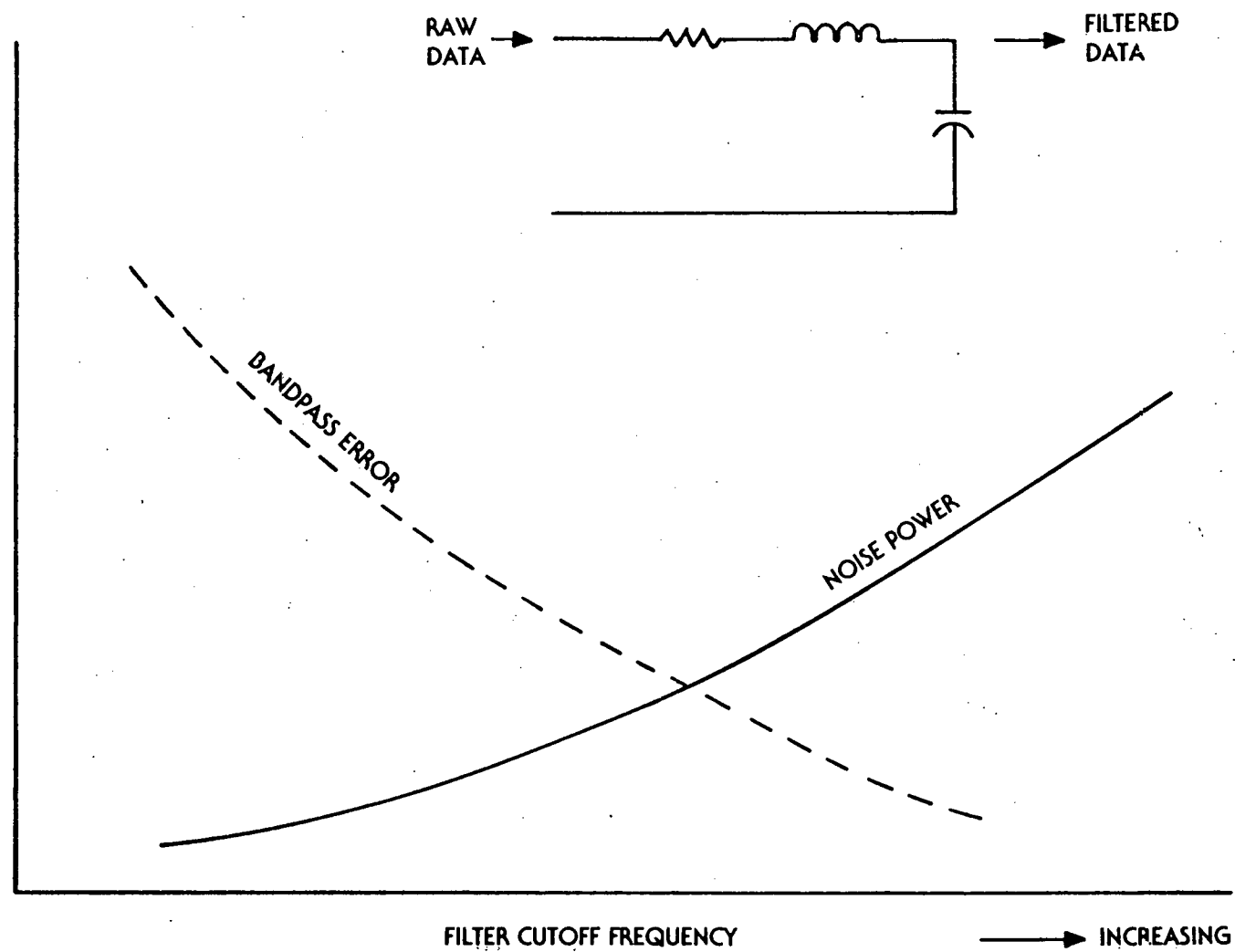


Figure 10. Software Filter Characteristics

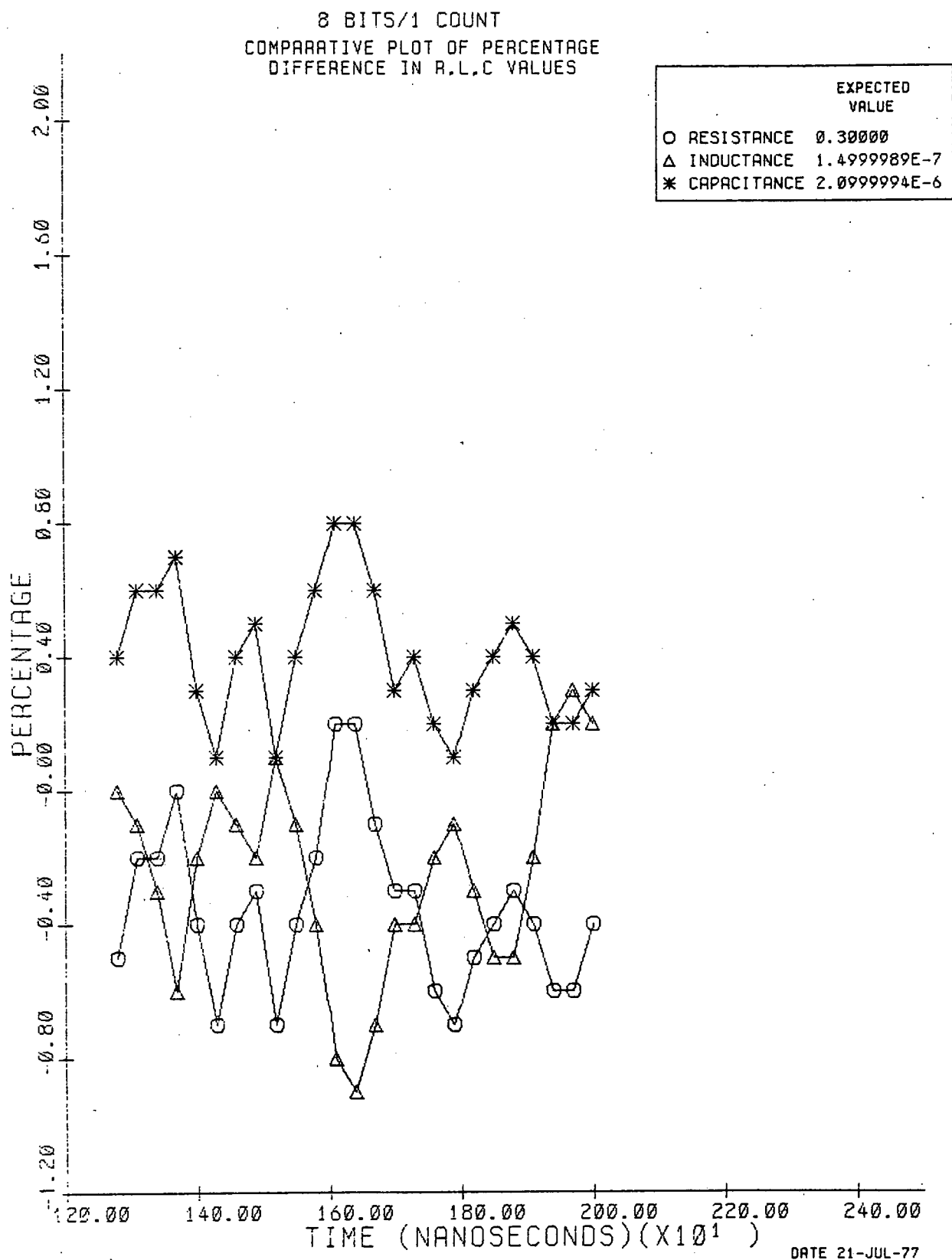


Figure 11. Method 1 RLC Analysis After Filtering

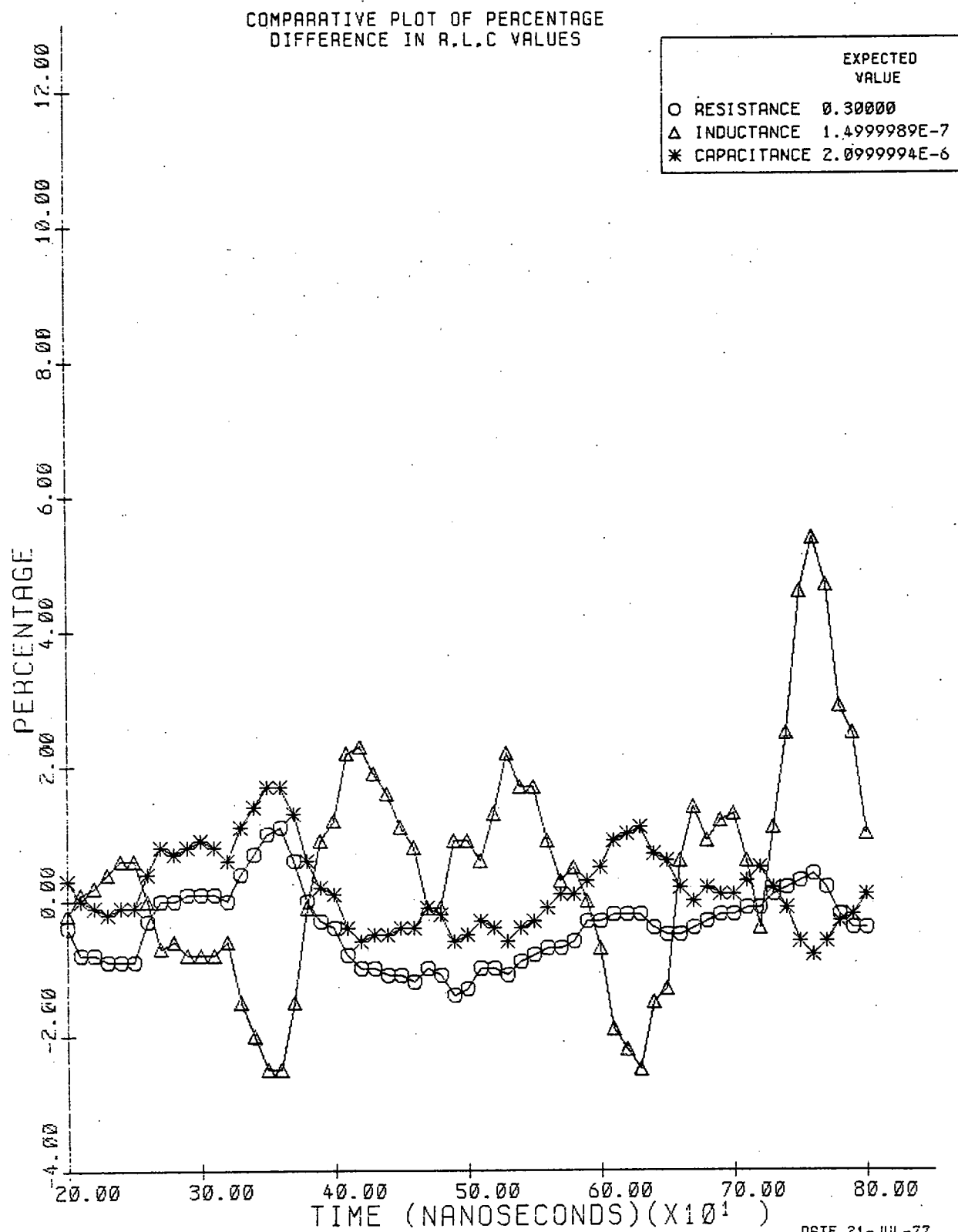


Figure 12. Method 2 RLC Analysis After Filtering

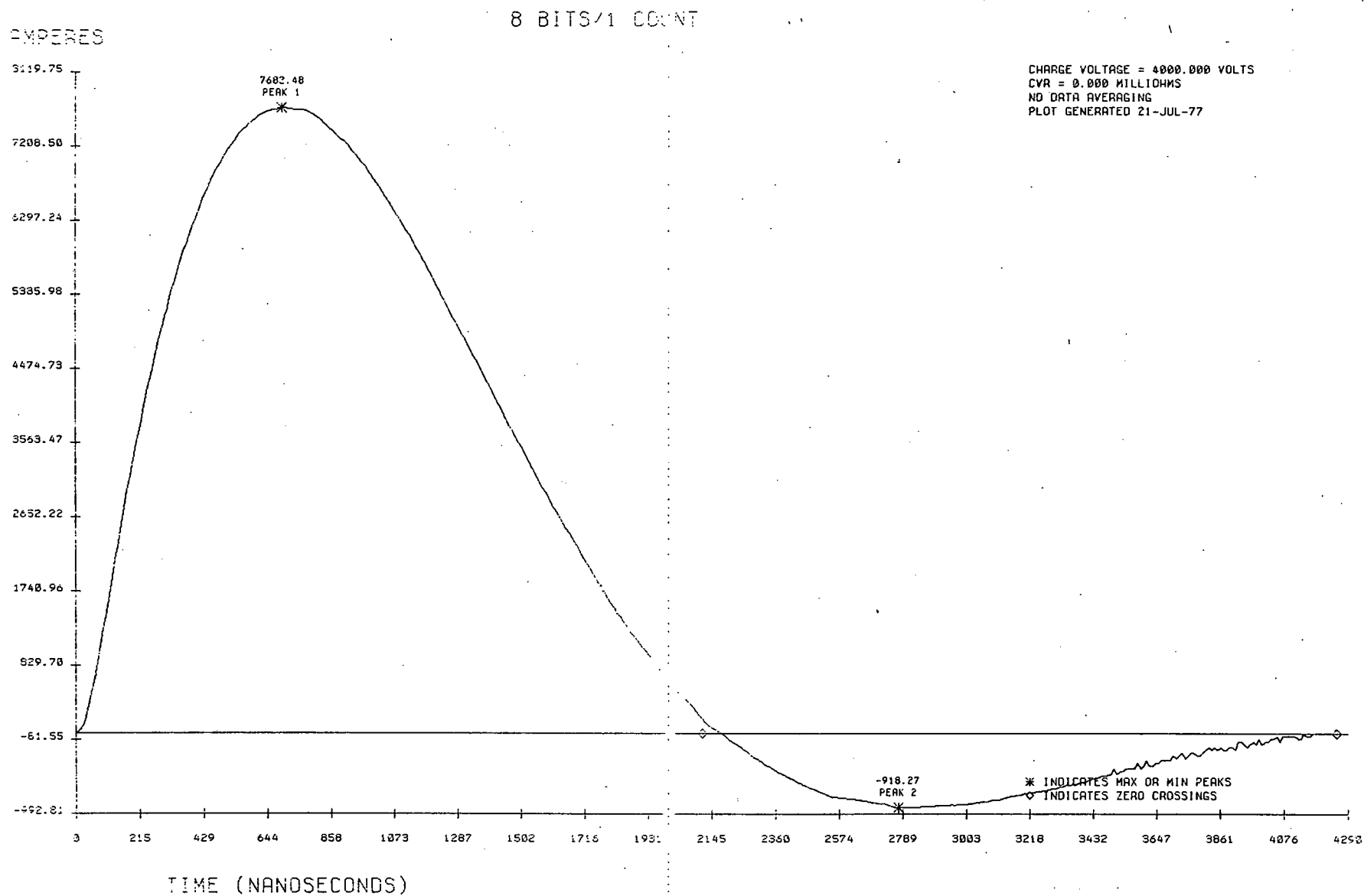


Figure 13. Simulated Fireset Waveform After Filtering

```

0001      SUBROUTINE CORRECT
0002      COMMON /ANAL1/ B,ZRX,NZ,NSM,MAX,MIN,SSM,ZRXU(20),OFS
0003      COMMON /BLK1/  U,R,L,C,IT1,IT2,IT3,IT4,G
0004      REAL B(2040),R1,L1,C1

0005      WRITE (5,10)
0006 10     FORMAT ( ' ENTER FILTER CUTOFF FREQ--XX,EX HZ' )
0007      READ (5,20) F
0008 20     FORMAT (E16.8)
0009      PIE=3.141592654
0010      L1=1.0/(2.*PI*F)
0011      C1=L1
0012      WRITE (5,30)
0013 30     FORMAT ( ' ENTER DAMPING RESISTANCE' )
0014      READ (5,31) R1
0015 31     FORMAT ( F16.8)
0016      VO=0.0
0017      CUR=0.0
0018      DT=1.E-8
0019      DO 100 I=1,350
0020      VO=VO+(CUR*DT)/C1
0021      CUR=CUR+((B(I)-VO)-(CUR*R1))*(DT/L1)
0022      B(I)=VO
0023 100    CONTINUE
0024      RETURN
0025      END

```

Figure 14. Fortran Filter Algorithm

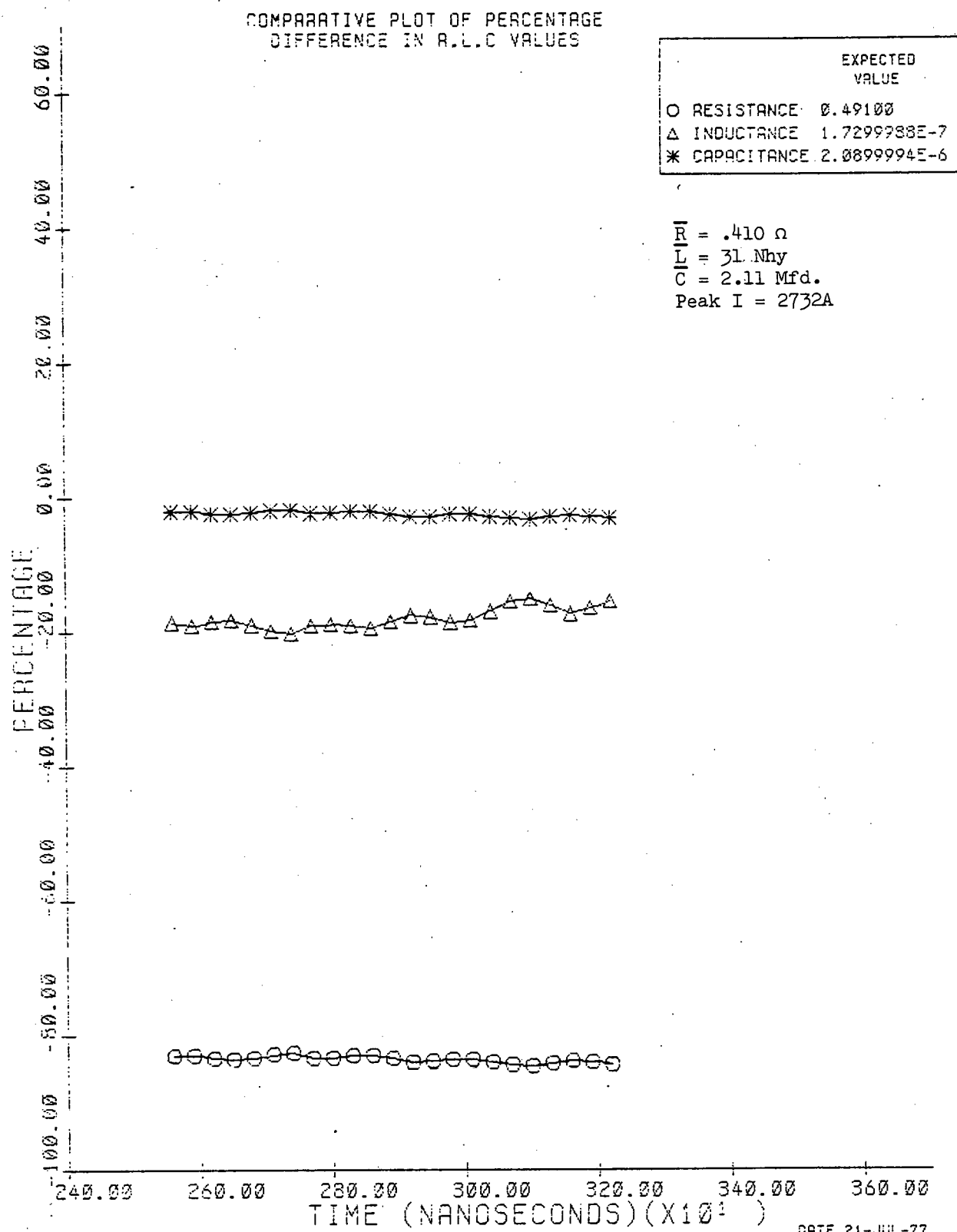


Figure 15. Resistor, 410 mΩ, Wirewound

Figures 16 through 18 show similar analyses of a current-viewing resistor, a section of braided wire, and an air gap simulating a broken connection.

EXEMPLARY X-UNIT ANALYSIS

Figure 19 is a comparative analysis of two development X-units. The plot shows the percentage difference in the RLC of S/N 311, which was producing an output current peak 4 percent below normal, compared to S/N 313 which was performing acceptably. The abnormally high resistance indicated in S/N 311 was caused by a manufacturing defect in the SA2296 energy storage capacitor, in which one of the 12 parallel flags comprising the device terminals was inadvertently isolated from the capacitor foil.

Figure 20 shows the characteristics of a group 4 development unit compared with group 3 baseline data. The indicated reduction of 11 nH in the discharge loop inductance was achieved by reorienting the high voltage switch and shortening the storage capacitor leads.

Figure 21 compares the RLC of two X-units. Although the construction of these devices is quite similar, one exhibits a higher resistance and inductance of 6 m Ω and 46 nH respectively, because of the test load adapter used on this assembly.

CONCLUSION

The RLC analysis technique represents a valuable capability in support of the design and production of firesets. RLC data as engineering information is currently being acquired on two production firesets at Bendix. Statistical analysis of all pulse data for these firesets, which includes the peak current, rise time, and pulse duration, indicates that the distribution of the RLC data compares favorably with that of the other measured parameters.

The application of the RLC analysis approach has provided a greater insight into the component and process variations which influence X-unit performance. The information gained from a single firing provides a basis for properly directing troubleshooting and analysis activity, allowing these tasks to be performed in a timely manner with a reduced manpower investment. The attendant reduction in test firings has a positive influence on fireset reliability.

The technique is useful in any application where dynamic analysis of a capacitor discharge unit is required. The approach is

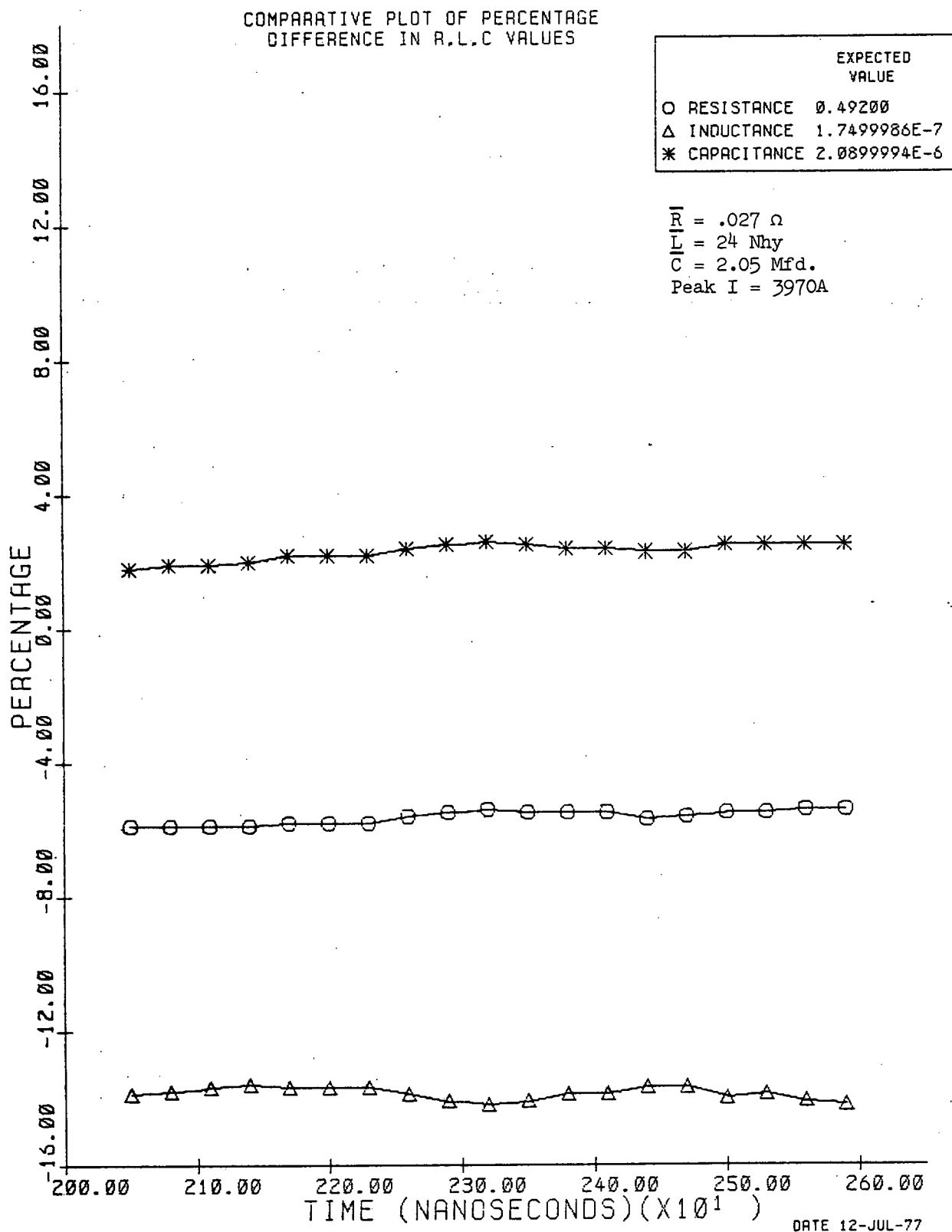


Figure 16. Current-Viewing Resistor, 25 mΩ

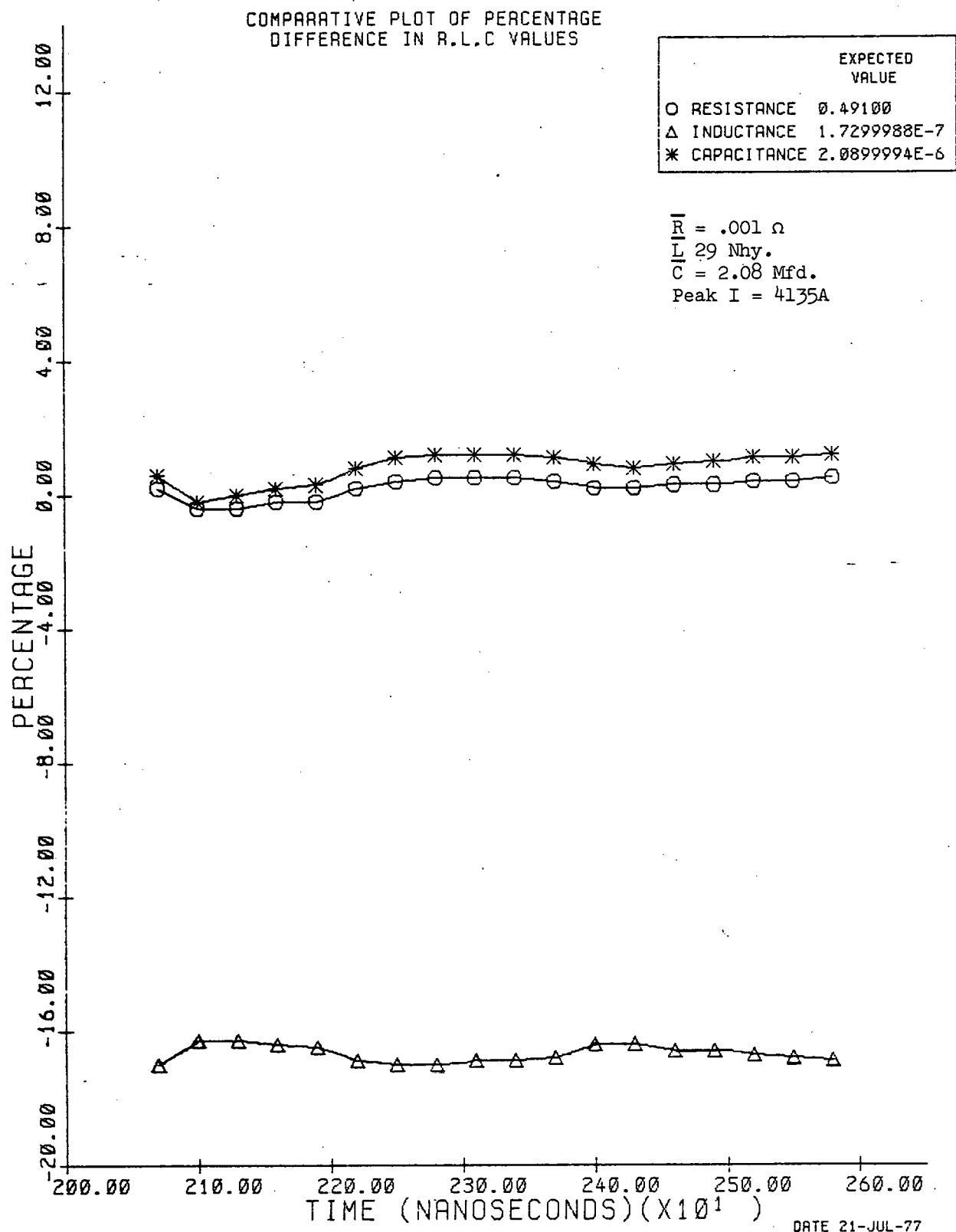


Figure 17. Braided Wire, 4.76 mm in Diameter by 25.4 mm Long

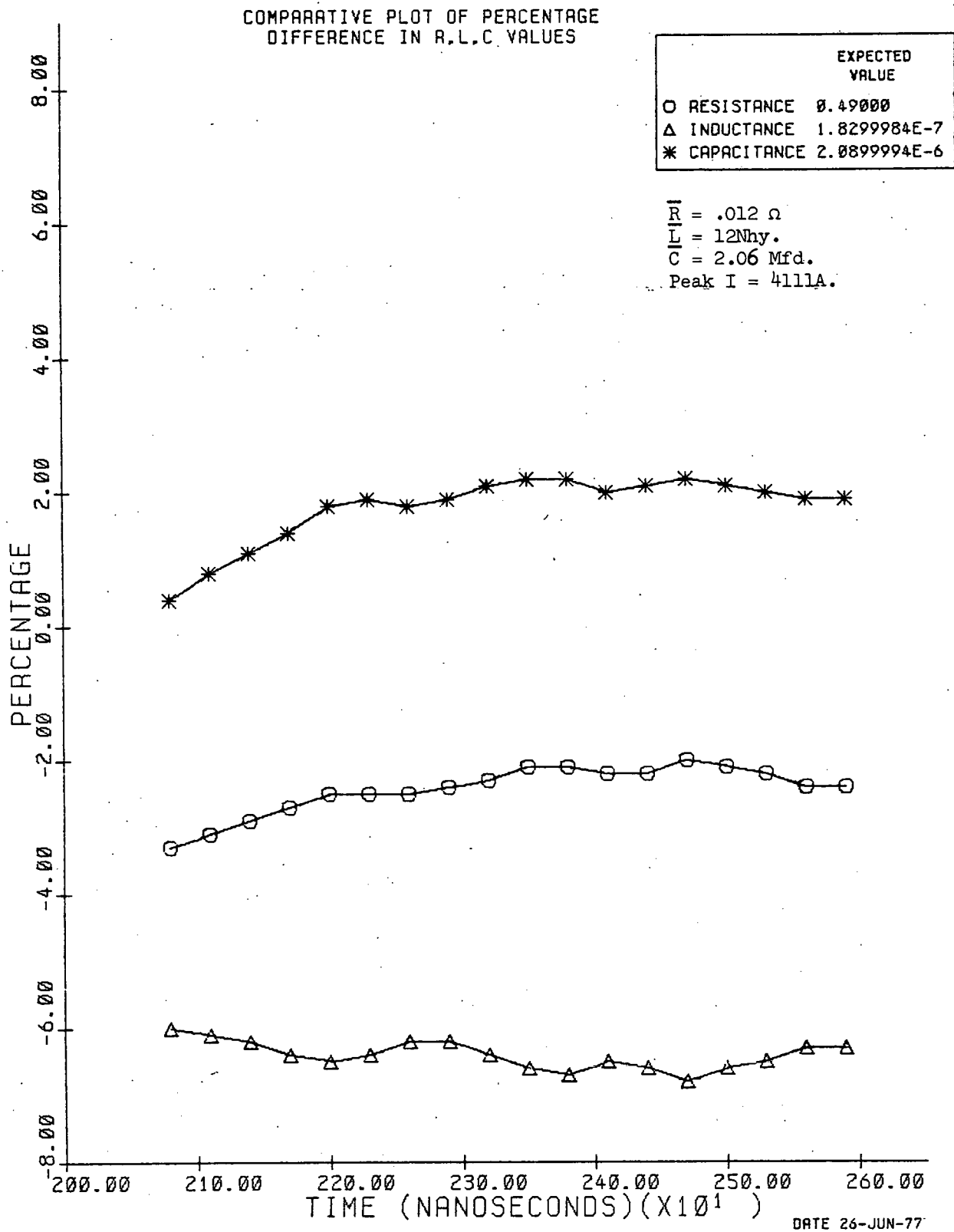


Figure 18. Gap, 0.51 mm, Simulating a Broken Connection

311 VS 313
COMPARATIVE PLOT OF PERCENTAGE
DIFFERENCE IN A.L.C VALUES

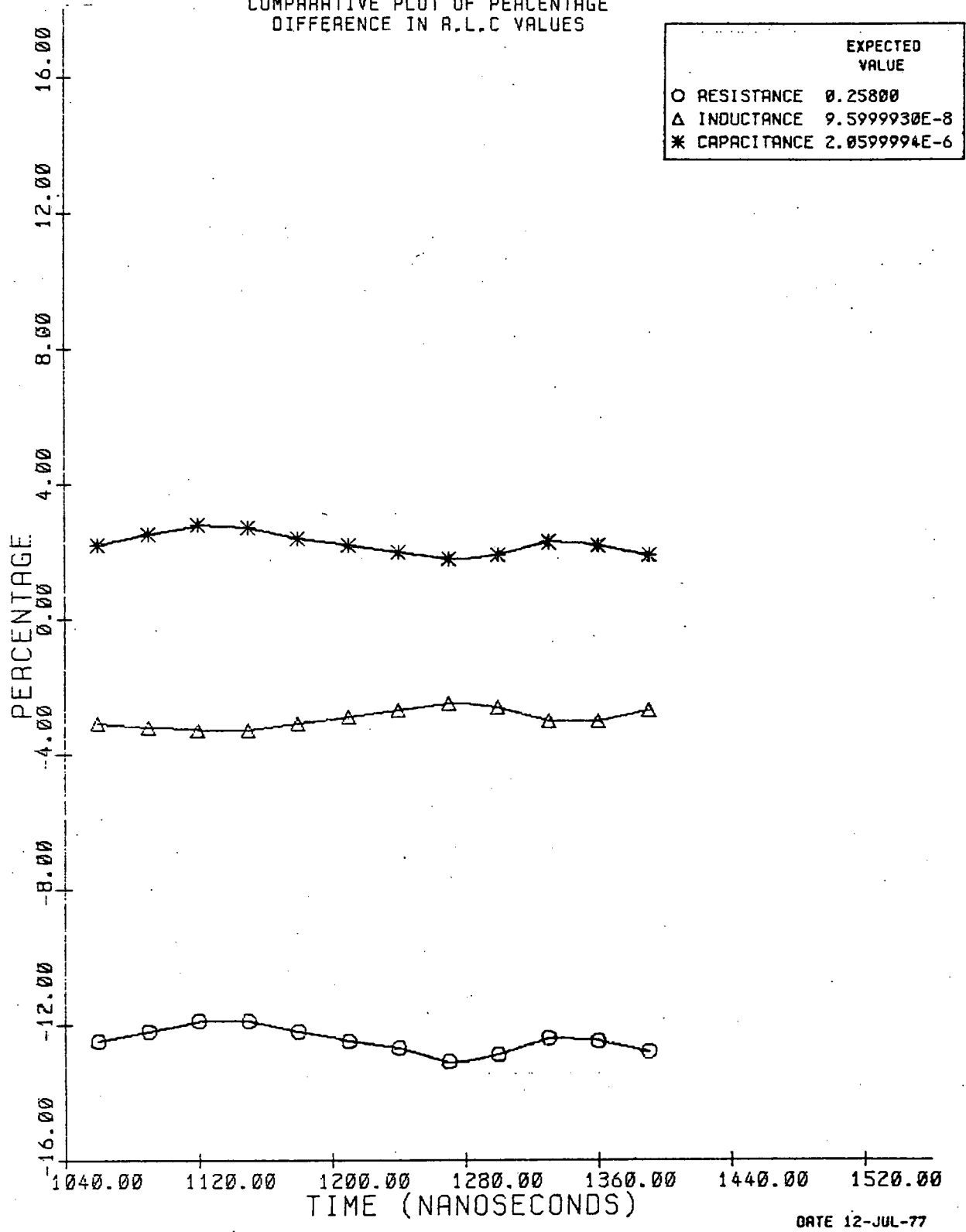


Figure 19. S/N 311 Versus S/N 313

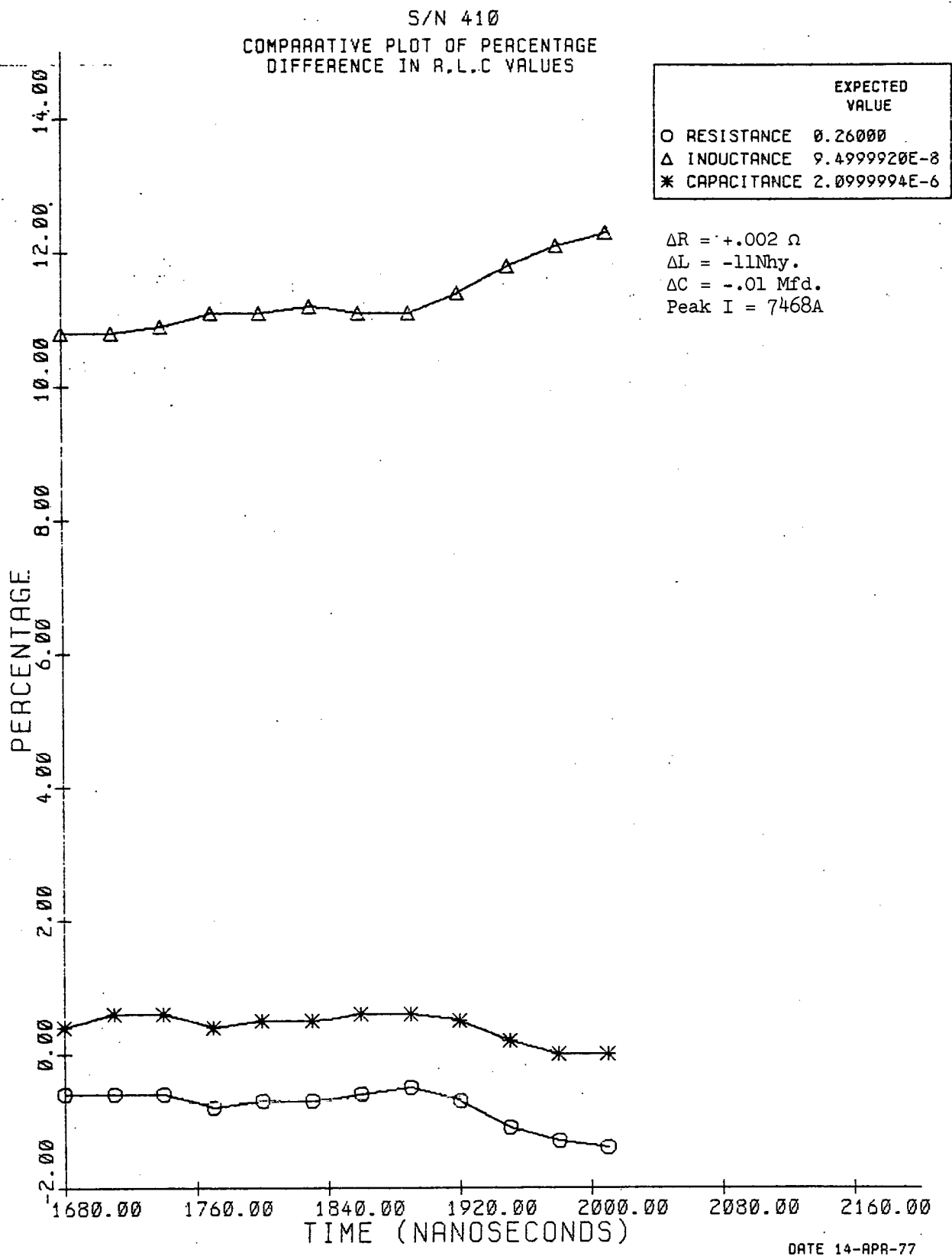


Figure 20. SN410, Group 4 X-Unit, Compared With Group 3 Baseline

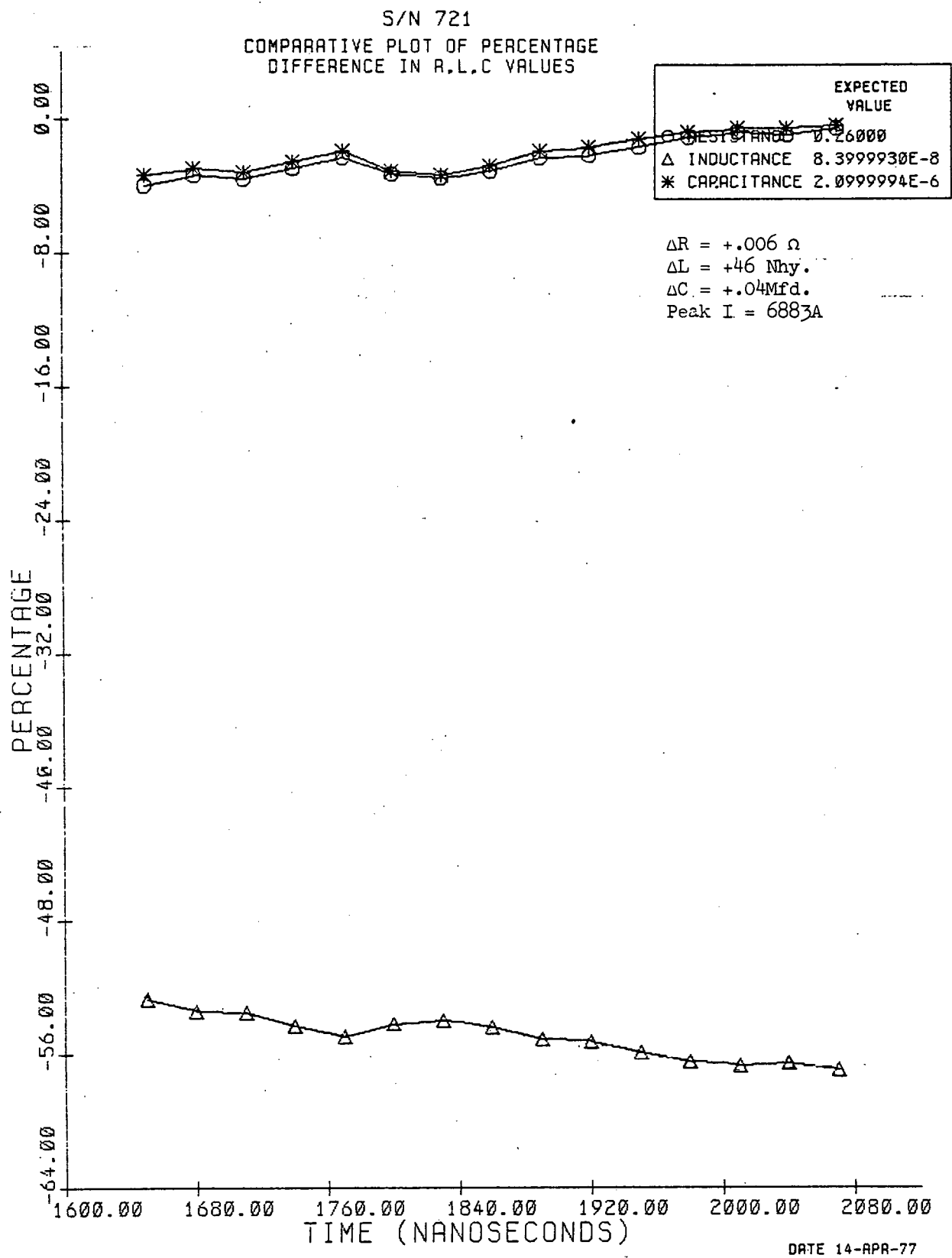


Figure 21. X-Unit, Showing Effect of Load Adapter

independent of circuit damping, eliminates the need for determining the waveform starting point, and is accurate to 1 percent in the presence of noise. Derivation of the circuit capacitance provides a measure of self-checking, and the algorithm is well-conditioned for use on a computer or calculator-based data system.

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- ²J. F. Kobs, Several Methods for CDU X-Unit Impedance Determination From a Short Circuit Current Waveform. Albuquerque: Sandia Corporation, 73-0772, 1974.

ABOUT THE AUTHOR

A. G. Bennett is a Staff Engineer at the Kansas City Division of Bendix Corporation where he is involved in many facets of fireset production. He holds a BSEE from Iowa State University and has a broad background in the fields of analog circuit design and analysis. He is the holder of one patent and the author of several technical reports.