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EFFECTS OF TEMPERATURE ON MOS RADIATION RESPONSE*

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ABSTRACT

Effects of irradiation and annealing temperature on radiation-induced charge densities are explored for MOS transistors. Both interface- and border-trap density increase with increasing radiation temperature, while the net oxide-trap charge density decreases.

INTRODUCTION

The radiation response of MOS devices can be strongly affected by the temperature during irradiation. Nevertheless, most radiation effects studies on MOS devices are performed at room temperature, and hardness assurance testing is also specified to be performed at room temperature.

Previous work has shown an enhancement of trapped oxide charge density for decreasing temperature during irradiation [1,2], at least for electric fields typical of MOS operation, and an enhancement of interface trap density with increasing temperature during irradiation [2-4]. Because systems can be exposed to ionizing radiation over a wide range of temperatures, it is important to obtain a better understanding of the effects of irradiation temperature on MOS response.

We have irradiated MOS devices at temperatures from –25 to 100°C. Effects of bulk oxide traps, interface traps, and border traps (for the first time) are evaluated separately as a function of radiation temperature.

EXPERIMENTAL DETAILS

Data are presented for polysilicon-gate transistors with 45-nm gate oxides manufactured using Sandia National Laboratories' radiation-hardened 4/3-μm process [5]. Devices were irradiated using a 10-keV x-ray source at a dose rate of 4.35 krad(SiO_2)/s. Devices were irradiated at -25, 27, and 100°C, and annealed at 100°C. The pre- and post-irradiation and anneal I-V and 1-MHz charge pumping measurements [6] were taken at 27°C for the devices irradiated at 27 and 100°C. For the irradiation at –25°C, pre-irradiation measurements were taken at both –25 and 27°C. No measurements were taken at 27°C through the irradiation sequence for the parts irradiated at low temperature to avoid oxide-charge annealing and interface-trap buildup during the period in which the device was heated. Post-irradiation and anneal measurements were taken at –25 and 27°C, respectively.

RESULTS

The effects of temperature (-25 to 100°C) during irradiation on MOS threshold-voltage shifts for n-channel transistors are illustrated in Figure 1. Following irradiation, all transistors were annealed at 100°C. The gate-to-source bias during both irradiation and anneal was 5 V. At each dose, the magnitudes of the threshold-voltage shifts increase as the temperature during irradiation decreases. At 500 krad(SiO_2) (~115 s), the value of ΔV_{th} for the transistors irradiated at 100°C begins to turn around, while it is still decreasing for the transistors irradiated at –25 and 27°C. After exposure to 1 Mrad(SiO_2) (~230 s), the magnitude of ΔV_{th} for transistors irradiated at 100°C is more than three times less than for transistors irradiated at –25°C. At 1 Mrad(SiO_2) (230 s), values of ΔV_{th} are –0.49, –1.26, and –1.73 V for the –25, 27, and 100°C irradiations, respectively. During the first 540 s of the anneal (first anneal data point), there is a significantly larger change in ΔV_{th} for transistors irradiated at either –25 or 27°C than for transistors irradiated at 100°C. At longer anneal times, the

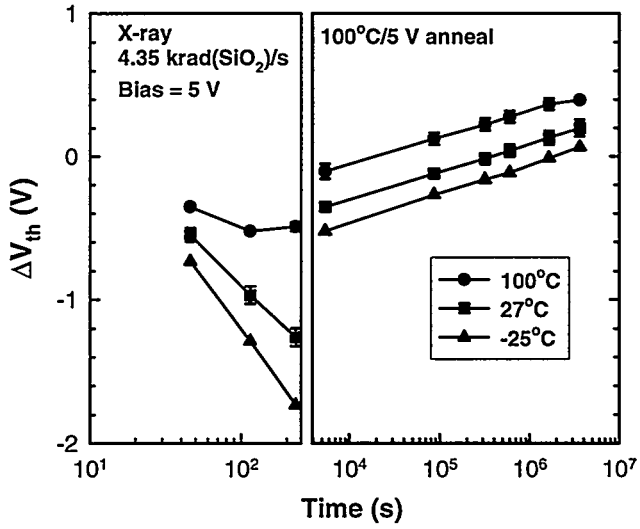

Figure 1: Threshold-voltage shift versus irradiation and anneal time for MOS transistors with 45-nm oxides irradiated at –25, 27, and 100°C and annealed at 100°C.

DISCLAIMER

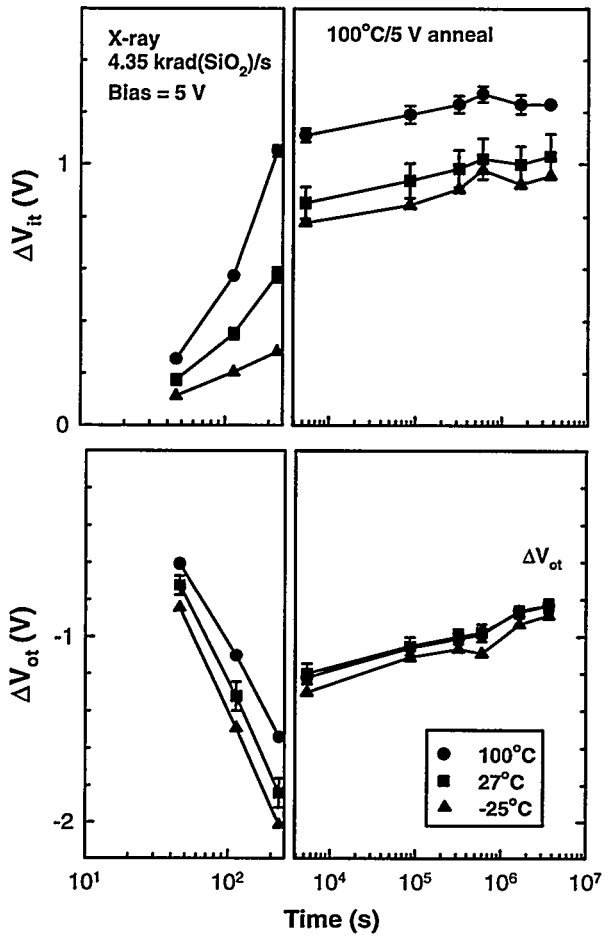

Figure 2: Threshold-voltage shifts due to interface-trap and oxide-trap charge vs. irradiation and anneal time for the transistor data of Figure 1.

rate of change in threshold voltage appears to be independent of the temperature during irradiation. Note that, even after a 3.6×10^6 s anneal, increasing irradiation temperature causes a more positive threshold-voltage shift.

In Figure 2 threshold-voltage shifts due to interface- and oxide-trap charge inferred from the midgap separation technique [7] are plotted for the transistor data of Figure 1. The midgap technique does not distinguish the contributions of interface traps and faster border traps [8,9]. Consistent with trends observed for the threshold-voltage shifts, we observe a more rapid buildup in interface traps and a more rapid decrease in oxide traps during the first 504 s of the anneal. Within the experimental uncertainty, there is no difference in the rate of buildup of interface-trap charge buildup nor in the rate of anneal of oxide-trap charge after the first 540 s anneal. Thus, for these n-channel transistors, increased interface-trap buildup with increased irradiation temperature causes the largest difference in radiation response for the transistors irradiated from -25 to 100°C. This is consistent with

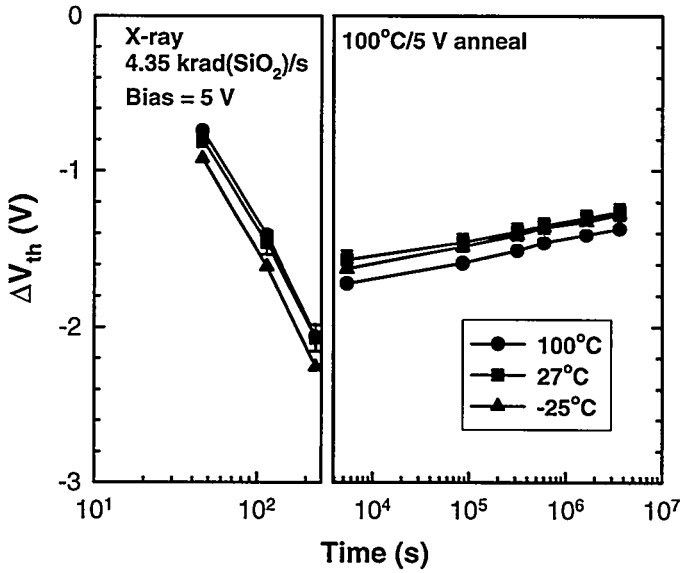

Figure 3: Threshold-voltage shift versus irradiation and anneal time for p-channel transistors irradiated at –25, 27, and 100°C and annealed at 100°C.

previous results [2] for n-channel transistors irradiated at much lower dose rates.

Figure 3 is a plot of the threshold-voltage shift for p-channel transistors irradiated at the same time and same electric field as the n-channel transistors shown in Figure 1. Interestingly, the data of Figure 3 show that the change in threshold voltage for p-channel transistors during irradiation and anneal is almost independent of irradiation temperature! This does not mean that the buildup of interface- and oxide-trap charge was not affected by the irradiation temperature. For a p-channel transistor, both interface- and oxide-trap charge are negative. For these p-channel transistors, an increase in the magnitude of interface traps offsets a nearly equal decrease in magnitude of oxide traps (to be shown in the full paper). The trends in interface- and oxide-trap charge are quantitatively similar to those observed in the n-channel transistors (see Figure 2). However, for the p-channel devices, there is nearly a one-to-one correlation between the change in interface- and oxide-trap charge as the irradiation temperature is changed. This may be coincidental, but it may also imply a link between oxide charge annealing and interface-trap buildup in these devices.

To determine the impact of border traps on the elevated temperature irradiation response, we used the DTBT charge separation method [9] to analyze 1-MHz charge pumping and I-V data. The change in the density of border traps for transistors irradiated at temperatures from –25 to 100°C is shown in Figure 4. During irradiation there are more border traps generated in the devices irradiated at 100°C than for those irradiated at lower temperatures.

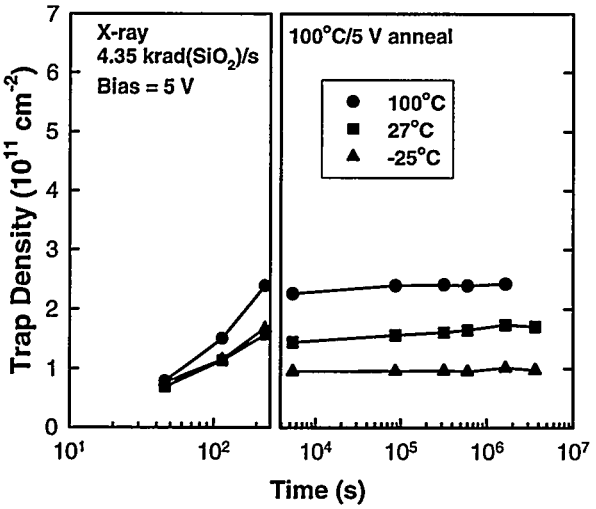

Figure 4: Change in the border trap density versus irradiation and anneal time for MOS transistors irradiated at temperatures from –25 to 100°C and annealed at 100°C.

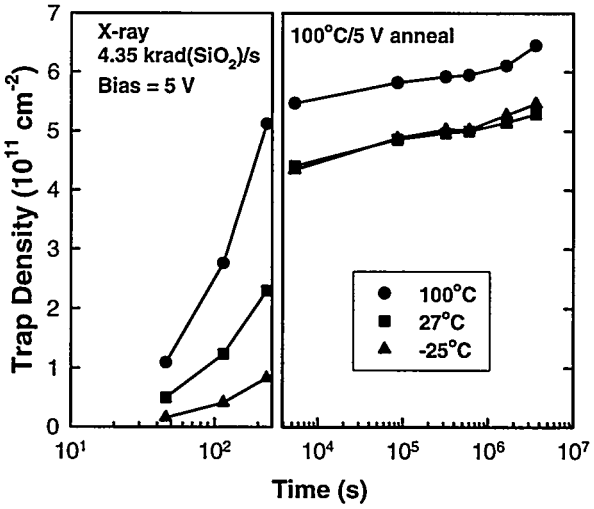

Figure 5: Change in the interface-trap density versus irradiation and anneal time for MOS transistors irradiated at temperatures from –25 to 100°C and annealed at 100°C.

During anneal we observed a reduction in the border-trap density during the first 504 s of the anneal for all parts, then little change through the remainder of the anneal.

In Figure 5, the change in interface-trap density determined by the DTBT method is shown as a function of irradiation and anneal time. The trends are consistent with the ΔV_{it} data shown in Figure 2, and show that interface traps have a more significant impact on the radiation response of these devices than border traps. At 1 Mrad(SiO_2), for transistors irradiated at 100°C the interface-trap density is larger by approximately 4.29×10^{11} and 2.83×10^{11} cm^{-2} than for transistors irradiated at –25 and 27°C, respectively. Correspondingly, the oxide-trap density (not shown) is smaller by approximately 2.68×10^{11} and 1.25×10^{11} cm^{-2}. Thus, the DTBT data confirm that increased interface-buildup with increased irradiation temperature causes the largest difference in radiation response with temperature for these devices.

SUMMARY

Effects of bulk oxide traps, interface traps, and border traps are evaluated separately for the first time as a function of radiation temperature. The data show that changes in oxide and interface traps with irradiation temperature more significantly affect the response of these devices than do border traps. Elevated temperature irradiations increase the interface-trap and border-trap densities and decrease the net oxide-trap charge. The trends for interface-trap buildup and oxide-trap charge reduction are consistent with previous work at low dose rates [2]. Hardness assurance implications of these results will be discussed in the full paper.

ACKNOWLEDGMENTS

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