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DOE/JPL/954356-79/11

SILICON-ON CERAMIC PROCESS

Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet
Task of the Low-Cost Solar Array Project

Quarterly Report No. 13, October 1—December 31, 1979

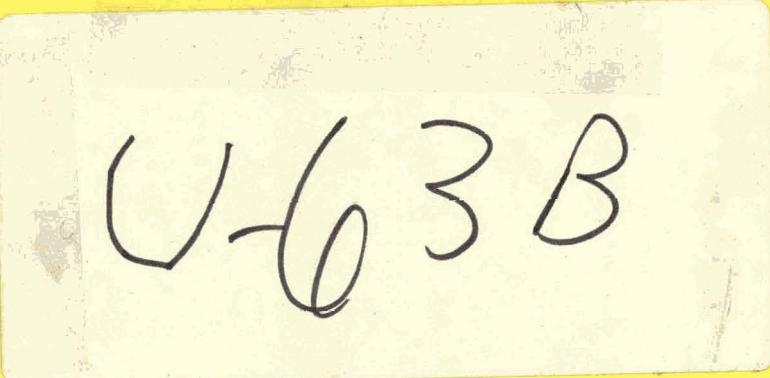
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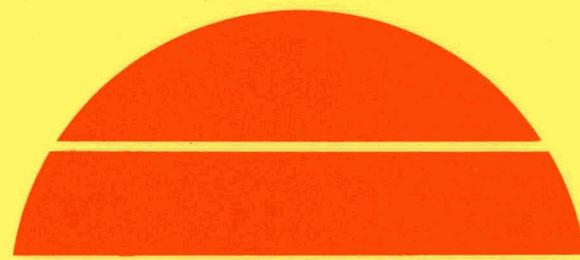
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February 15, 1980
Date Published

Work Performed Under Contract No. NAS-



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Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet Task of the Low-Cost Solar Array Project

Quarterly Report No. 13

by

P.W. Chapman, J.D. Zook, B.L. Grung,
K. McHenry and S.B. Schuldt

Period Covered: 10/1/79 - 12/31/79

Published: 15 February 1980

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The JPL Low-Cost Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, by agreement between NASA and DOE.

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SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon. We plan to do this by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt. Results and accomplishments which occurred during the quarter can be summarized as follows:

- Seventeen runs were performed on the production dip coater.
- A ceramic substrate production error at Coors Porcelain Co. limited the yield of good dipped material this quarter.
- Coors supplied us with a substrate material more closely matched with respect to the thermal expansion coefficient of silicon. This material should minimize warpage of coated substrates.
- An experiment was done in the dip coater to attempt to inhibit the transport of impurities into the melt by means of an electric field. This material is currently being evaluated.
- The experimental dip coater has produced 300- μ m nonuniform coatings at pull speeds of 0.25 cm/sec.
- The thermal conditions of the experimental dip coater are being modified to minimize substrate breakage.
- One hundred twenty cells were fabricated from dipcoated material during this quarter. The highest conversion efficiency was 9.7% on a 5-cm² cell.
- Experiments to determine the optimum diffusion conditions for silicon-on-ceramic (SOC) solar cells indicate higher-efficiency cells are obtained with deeper diffusion (850°C for 80 minutes).
- SCIM-coated (Silicon Coating by an Inverted Meniscus) material has produced photodiodes with total-area conversion efficiencies of 4.9% (AM1, AR) for diode areas of approximately 0.05 cm².

- Theoretical calculations indicate the short-circuit density represents the area which must be improved to significantly impact the conversion efficiency of SOC solar cells.
- Theoretical analysis indicates processing of SOC material which causes impurities to segregate to grain boundaries will improve the overall solar-cell performance.
- Initial hydrogen plasma annealed samples indicate partial passivation has occurred.
- Crystallographic texture studies indicate dislocations, twin planes, and grain boundaries tend to lie in planes parallel to the growth axis and perpendicular to the substrates.
- Horizontal slots do not initiate nucleation or influence structure.
- Thermal analyses were carried out to support the design of the new continuous SOC coating facility.

INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 11 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous coating process also being investigated have excellent scale-up potential which offers an outstanding, cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and the rate at which the substrate is withdrawn from the melt.

The solar-cell potential of this SOC sheet silicon is promising. To date, solar cells with areas from 1 to 10 cm^2 have been fabricated from material with an as-grown surface. Conversion efficiencies of about 10 percent with antireflection (AR) coating have been achieved. Such cells typically have open-circuit voltages and short-circuit current densities of 0.55V and 23 mA/cm^2 , respectively.

The SOC solar cell is unique in that its total area is limited only by device design considerations. Because it is on an insulating substrate, special consideration must be given to electrical contact to the base region. One method which offers considerable promise is to place small slots in the substrate perpendicular to the crystalline growth direction and contact the base region by metallizing the silicon that is exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing. The best slotted-cell results to date indicate a 10.1 percent conversion efficiency (AR-coated) on a 4-cm² (total area) cell.

Development efforts are continuing in such areas as improvement in growth rate, reduction of progressive melt contamination, and optimization of electrical contacts to the base layer of the cell. Investigation has shown that mullite substrates, to a limited extent, dissolve in molten silicon. The impurities from the substrate are believed to adversely affect solar-cell conversion efficiency. A method for reducing substrate dissolution is to reduce the contact area the substrate makes with the silicon melt. Therefore, a silicon coating facility, referred to as SCIM or Silicon Coating by an Inverted Meniscus, has been constructed which is designed to coat large (10 cm x 100 cm) substrates in a continuous manner. It is expected that this facility will not only improve the growth rate, but also minimize the silicon melt contact with the substrate. This should reduce the rate at which the melt becomes contaminated. The facility will also permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process. This machine has succeeded in demonstrating coatings exhibiting unidirectional solidification (desirable and occurring in dip coating) on substrates 18 inches long and 2 inches wide. Material characteristics indicate this material is similar in structure and purity to material obtained from our dip-coating facilities.

TECHNICAL DISCUSSION

SHEET SILICON GROWTH (J.D. Zook, K. McHenry,
D. Sauve, and V. Harris)

Dip-Coating Production

During the past quarter, 17 runs were performed on the production dip coater. These runs are summarized in Table 1. Experimentation has been conducted in doping levels and gas flow rates. The effect of varying the argon flow rate in run 219 was to promote SiO formation with decreasing gas flow. No significant change in the structure of the silicon was observed.

A more serious problem encountered during the quarter was the quality of the ceramic substrates from Coors. The overall effect of the poor surface quality of the ceramic substrates has been reduced yields as evident in Table 1. Discussion with the supplier, Coors Porcelain Co., revealed that the breakage was due to a production error and should be corrected with the next batch of substrates.

Another problem currently being addressed is substrate warpage following dip coating. We feel that this warpage is due primarily to the thermal expansion mismatch between the silicon and the ceramic substrate. Coors recently supplied a new mullite substrate designated "Q" modification. This material is supposed to have a thermal expansion coefficient much closer to that of silicon and should result in less substrate warpage.

Finally, experimentation in run 226 involved the application of an electric current through the melt during dip coating. We speculate that the current might influence the transport of impurities from the substrate to the melt. This SOC material is currently being processed and future characterization should indicate the feasibility of this technique for reducing melt contamination.

Table 1. Dip-Coating Production

Run No.	Dopant Level (cm ⁻³)	Growth Speed (cm/sec)	Number Dipped	Comments
213	1×10^{16} boron	0.06	8	Yield 87%.
214	1×10^{16} boron	0.06, 0.158, 0.093	16	Yield 75%. Some coated with DAG sprayed on.
215	1×10^{16} boron	0.06	14	Yield 43%. Preheated at 140°C prior to run to short.
216	3×10^{16} boron	0.06	14	Yield 100%.
217	3×10^{16} boron	0.06	12	Yield 83%.
218	Undoped run	0.06	12	Yield 75%.
219	2.3×10^{16} phosphorous	0.06	11	Yield 63.6%. Varied argon inlet flow rate.
220	4.6×10^{16} phosphorous	0.06	12	Yield 83.3%.
221	6×10^{16} boron	0.06	12	75% poco carbon substrate no. 8 dissolved in melt.
222	4×10^{16} boron	0.06	2	Carbon crucible run.
223	4×10^{16} boron	0.06	11	Rough side of substrate used on three samples. Yield: 81.8%.
224	5×10^{16} boron	0.06	12	Rough ceramic surfaces caused poor yield: 50%.
225	20×10^{16} boron	0.06 and 0.07	11	Heavy doping. Yield: 91.6%.
226	4.65×10^{16} boron	0.06	10	Carbon electrode in melt. Electrical conduction experiment. Yield: 70%.
227	0.12665 gram of 99.999% aluminum	0.06	12	Aluminum doping experiment. Yield: 33.3%. Had to coat backside; front surface rough.
228	Undoped run	0.06	12	Yield: 75%.
229	2.3×10^{16} phosphorous	0.06	12	Yield: 41.6%.

Experimental Dip Coater

Most of the past quarter was spent implementing minor modifications to the experimental dip coater in an attempt to produce more-uniform coatings at increased pulling speeds. The best results to date with respect to coating thickness have been 400 μm and 300 μm at pulling speeds of 0.2 and 0.25 cm/sec, respectively. These results were obtained with cooling shoes containing individual gas jets geometrically shielded from the melt surface to prevent SiO deposition. However, the resultant coatings were nonuniform in thickness and contained vertical stripes corresponding to the position of the gas jets.

The cooling shoes were redesigned by replacing the individual gas jets with a continuous slit. In addition, the cooling shoes were positioned closer to the substrate and helium was used in an attempt to provide conductive rather than convective cooling. This redesign of the cooling shoes eliminated the striated uneven coatings but because of the close proximity of the shoes and the substrate the shields on the cooling shoes had to be removed. As a result, SiO formation on the shoes again posed a problem.

This problem appears to have been corrected by the insertion of graphite felt pads within the chamber to abrasively clean the shoes after each run. The best results obtained after these modifications have been coatings 50 to 70 μm thick at a pull speed of 0.2 cm/sec. It is evident that some experimentation is still required with respect to gas flow rates and melt temperature to provide thicker coatings with the redesigned system.

During the latter part of the quarter, yields in the experimental coater were low as a result of substrate breakage. It appears that the redesign of the system altered the thermal gradients or heat flow within the substrate resulting in thermal shock. Afterheaters are currently being designed and will be positioned on either or both sides of the substrate above the cooling shoes. These heaters will be made out of carbon and will be planar in geometry. This design will provide more even heating across the width of the substrate. The heaters will also be designed to provide a temperature gradient with maximum heat generation at the bottom of the heater.

CELL FABRICATION AND DEVELOPMENT (B. Grung,
T. Heisler, and S. Znameroski)

During the quarter, we fabricated 120 cells from dip-coated SOC material. The highest conversion efficiency was 9.7% (AM1, AR), for a cell area of 5 cm². The average efficiency was 9.0% for the 34 AR-coated SOC cells. The primary characteristics of all 120 cells are given in Tables 2 and 3. The light current-voltage (I-V) characteristics of the 9.7% cell are shown in Figure 1. So far, the best SOC cells have efficiencies of 10.0% for 4-cm² cell areas and 9.9% for 10-cm² cell areas.

The objectives during the quarter were to determine the optimum diffusion conditions for SOC cells, to fabricate photodiodes on SCIM-coated material, and to calculate theoretical I-V characteristics for recent SOC cells. The results of these three investigations will be given in the next three subsections. Here we summarize some of the important results. The highest efficiency values correspond to deeper diffusions, where the diffusion temperature is 850°C and the diffusion times are 80 minutes. For these diffusion conditions, the emitter sheet resistance is 33 ohms/square, as compared with our usual value of 40 ohms/square. The SCIM-coated material has produced photodiodes with total-area efficiencies of 4.9% (AM1, AR), for diode areas of ~ 0.05 cm. The theoretical calculations indicate that the short-circuit current density must be increased to increase substantially the conversion efficiency of present SOC cells.

Optimum Diffusion Conditions

As has been noted, we fabricated 120 cells during the quarter. These cells were divided into 17 groups as indicated in Table 4. Groups A through L correspond to various diffusion conditions and Groups M through S correspond to the same diffusion conditions. For the latter, we employed our standard conditions which are a diffusion temperature of 850°C and a diffusion time of 50 minutes. This diffusion time is divided into a 10-minute preheat time, a 30-minute source time, and a 10-minute postheat time. In Table 4, those times are denoted as 10/30/10.

For each cell in Table 4, the diffusion conditions are given along with the item number, the cell number, the emitter sheet resistance, and the efficiency. The item number corresponds to the same item number in Tables 2 and 3. Thus, Tables 2 through 4 give complete information on all 120 cells.

Table 2. Conversion Efficiencies of Recent Slotted-Substrate Cells

item	Cell Number	P-type Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sq cm)	Base Sheet Resistance	Conversion Efficiencies		Total Area (cm ²)
						Before AR (%)	After AR (%)	
1	175 - 15-101	2.3e+016	0.06	1.2	44	6.28		
2	175 - 15-202	2.3e+016	0.06	0.6	44	6.49		
3	178 - 2-103	2.3e+016	0.06	1.0	81	6.84		
4	178 - 12-102	2.3e+016	0.06	0.6	48	5.40		
5	178 - 15-102	2.3e+016	0.07	1.9	34	5.60		
6	194 - 1-111	9.3e+015	0.07	1.1	148	6.43		
7	194 - 1-211	9.3e+015	0.07	1.6	148	5.48		
8	194 - 2-111	9.3e+015	0.07	1.9	190	5.35		
9	194 - 2-211	9.3e+015	0.07	1.2	190	5.32		
10	194 - 7-111	9.3e+015	0.07	0.9	130	6.67	9.37	
11	194 - 7-211	9.3e+015	0.07	1.0	130	5.48	7.74	
12	198 - 1-111	9.3e+015	0.07	1.6	111	6.18		
13	198 - 1-211	9.3e+015	0.07	1.8	111	5.52		
14	198 - 2-111	9.3e+015	0.07	1.7	128	5.76		
15	198 - 2-211	9.3e+015	0.07	1.6	128	5.52		
16	198 - 3-111	9.3e+015	0.07	1.4	188	6.20		
17	198 - 3-211	9.3e+015	0.07	1.5	188	5.79		
18	198 - 4-111	9.3e+015	0.07	1.5	250	6.09		
19	198 - 4-211	9.3e+015	0.07	3.1	250	5.09		
20	199 - 1-111	9.3e+015	0.07	0.6	101	6.57		
21	199 - 1-211	9.3e+015	0.07	0.6	101	5.87		
22	199 - 3-111	9.3e+015	0.07	0.6	92	6.80		
23	199 - 4-111	9.3e+015	0.07	0.8	174	6.84		
24	199 - 4-211	9.3e+015	0.07	0.9	174	5.44		
25	199 - 6-111	9.3e+015	0.07	0.7	116	6.13		
26	200 - 1-101	9.3e+015	0.07	2.3	220	5.37		
27	200 - 1-202	9.3e+015	0.07	3.6	220	5.99		
28	200 - 3-101	9.3e+015	0.07	0.8	164	6.58	8.88	
29	200 - 3-202	9.3e+015	0.07	0.8	164	6.73	8.99	
30	200 - 5-111	9.3e+015	0.07	2.4	173	5.03		
31	200 - 5-211	9.3e+015	0.07	1.9	173	5.39		
32	200 - 6-111	9.3e+015	0.06	0.9	144	6.66		
33	200 - 6-211	9.3e+015	0.06	0.9	144	6.30		
34	201 - 2-103	9.3e+015	0.06	2.8	97	6.35		
35	201 - 3-101	9.3e+015	0.06	1.1	92	7.01	9.47	
36	201 - 3-202	9.3e+015	0.06	1.0	92	6.93	9.38	
37	201 - 4-111	9.3e+015	0.06	2.3	120	5.72		
38	201 - 4-211	9.3e+015	0.06	5.6	120	4.90		
39	201 - 6-111	9.3e+015	0.07	1.1	93	6.89	9.34	
40	201 - 6-211	9.3e+015	0.07	0.8	93	6.55	8.98	
41	202 - 4-102	1.0e+016	0.06	1.5	101	6.48	9.06	
42	202 - 4-201	1.0e+016	0.06	1.7	101	6.61	8.91	
43	202 - 6-102	1.0e+016	0.06	1.0	116	6.87	9.24	
44	202 - 8-111	1.0e+016	0.06	1.2	152	6.33		
45	202 - 8-211	1.0e+016	0.06	1.1	152	5.83		
46	202 - 9-111	1.0e+016	0.06	0.9	108	6.20		
47	202 - 9-211	1.0e+016	0.06	0.9	108	6.10		
48	203 - 1-111	1.0e+016	0.06	2.5	171	6.15		
49	203 - 1-211	1.0e+016	0.06	2.4	171	5.98		

continued next page

Table 2. Conversion Efficiencies of Recent Slotted-Substrate Cells (Continued)

item	Cell Number	P-type Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sq cm)	Base Sheet Resistance	Conversion Efficiencies		Total Area (%)
						Before AR	After AR	
50	203 - 2-111	1.0e+016	0.06	1.8	157	6.26		
51	203 - 2-211	1.0e+016	0.06	1.6	157	5.94		
52	203 - 3-111	1.0e+016	0.06	1.1	161	6.47		
53	203 - 3-211	1.0e+016	0.06	1.5	161	5.98		
54	203 - 7-111	1.0e+016	0.06	1.7	155	6.38		
55	203 - 7-211	1.0e+016	0.06	1.2	155	6.19		
56	204 - 1-103	1.0e+016	0.06	1.7	83	6.55	8.75	
57	204 - 2-102	1.0e+016	0.06	0.7	106	6.98	9.52	
58	204 - 2-201	1.0e+016	0.06	1.1	106	6.82	9.11	
59	204 - 3-111	1.0e+016	0.06	1.0	111	6.61		
60	204 - 3-211	1.0e+016	0.06	1.2	111	6.36		
61	204 - 4-111	1.0e+016	0.06	1.3	100	6.29		
62	204 - 4-211	1.0e+016	0.06	0.9	100	6.42		
63	206 - 5-111	1.0e+016	0.06	0.9	131	6.75		
64	206 - 5-211	1.0e+016	0.06	0.7	131	6.42		
65	207 - 10-111	1.0e+016	0.06	1.1	103	6.52		
66	207 - 10-211	1.0e+016	0.06	1.8	103	5.64		
67	208 - 11-111	1.0e+016	0.06	0.9	79	6.85		
68	208 - 11-211	1.0e+016	0.06	0.9	79	6.33		
69	214 - 3-111	1.0e+016	0.06	2.7	136	5.36		
70	214 - 3-211	1.0e+016	0.06	2.8	136	5.00		
71	214 - 6-111	1.0e+016	0.06	1.1	131	4.88		
72	214 - 6-211	1.0e+016	0.06	1.4	131	5.17		
73	215 - 3-111	1.0e+016	0.06	1.2	112	6.46		
74	215 - 3-211	1.0e+016	0.06	2.4	112	3.64		
75	215 - 9-111	1.0e+016	0.06	0.9	102	5.31		
76	215 - 9-211	1.0e+016	0.06	1.0	102	5.39		
77	216 - 1-111	3.0e+016	0.06	0.4	38	6.65	9.53	
78	216 - 1-211	3.0e+016	0.06	0.6	38	6.45	9.24	
79	216 - 2-111	3.0e+016	0.06	0.4	28	6.46	9.20	
80	216 - 2-211	3.0e+016	0.06	0.5	28	6.40	9.12	
81	216 - 4-111	3.0e+016	0.06	0.7	36	6.94	9.28	
82	216 - 4-211	3.0e+016	0.06	0.7	36	6.79	9.40	
83	216 - 5-111	3.0e+016	0.06	0.6	38	6.79	9.47	
84	216 - 5-211	3.0e+016	0.06	0.6	38	6.90	9.66	
85	216 - 6-111	3.0e+016	0.06	0.6	58	6.71	9.44	
86	216 - 6-211	3.0e+016	0.06	0.7	56	6.50	9.33	
87	217 - 1-111	3.0e+016	0.06	1.0	22	5.85		
88	217 - 1-211	3.0e+016	0.06	1.1	22	5.21		
89	217 - 2-111	3.0e+016	0.06	0.9	36	5.32		
90	217 - 2-211	3.0e+016	0.06	0.8	36	5.88		
91	217 - 3-111	3.0e+016	0.06	0.6	39	4.07		
92	217 - 3-211	3.0e+016	0.06	0.9	39	4.30		
93	217 - 5-111	3.0e+016	0.06	0.6	31	6.46		
94	217 - 5-211	3.0e+016	0.06	0.6	31	6.63		
95	217 - 6-111	3.0e+016	0.06	0.6	29	6.59		
96	217 - 6-211	3.0e+016	0.06	0.8	29	6.58		
97	217 - 8-111	3.0e+016	0.06	0.5	36	6.70		
98	217 - 8-211	3.0e+016	0.06	0.5	36	6.47		
99	217 - 10-111	3.0e+016	0.06	0.7	36	6.28		

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Table 2. Conversion Efficiencies of Recent
Slotted-Substrate Cells (Concluded)

item	Cell Number	P-type Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sq cm)	Base Sheet Resistance (%)	Total Area	
						Conversion Efficiencies Before AR (%)	Conversion Efficiencies After AR (%)
100	217 - 10-211	3.0e+016	0.06	0.7	36	6.63	
101	218 - 1-111	0.0e+000	0.06	20.1	8923	0.04	
102	218 - 1-211	0.0e+000	0.06	40.1	8923	0.04	
103	218 - 4-111	0.0e+000	0.06	2.5	1213	5.37	7.28
104	218 - 4-211	0.0e+000	0.06	2.4	1213	5.64	7.85
105	218 - 8-111	0.0e+000	0.06	1.5	586	6.17	8.59
106	218 - 8-211	0.0e+000	0.06	1.4	586	6.34	8.82
107	218 - 12-111	0.0e+000	0.06	1.3	324	6.92	8.73
108	218 - 12-211	0.0e+000	0.06	1.2	324	6.48	8.85
109	221 - 1-111	6.0e+016	0.06	0.8	25	5.55	
110	221 - 1-211	6.0e+016	0.06	0.7	25	5.58	
111	221 - 2-111	6.0e+016	0.06	0.7	19	6.06	
112	221 - 4-111	6.0e+016	0.06	1.2	21	5.53	8.15
113	221 - 4-211	6.0e+016	0.06	0.6	21	6.76	9.72
114	221 - 5-111	6.0e+016	0.06	0.5	26	6.14	9.05
115	221 - 5-211	6.0e+016	0.06	0.5	26	6.48	9.35
116	224 - 2-103	5.0e+016	0.06	0.8	28	6.17	
117	224 - 4-103	5.0e+016	0.06	0.7	29	6.35	
118	224 - 5-111	5.0e+016	0.06	0.6	26	6.75	
119	224 - 5-211	5.0e+016	0.06	0.7	26	3.61	
120	224 - 7-103	5.0e+016	0.06	0.8	23	6.51	

Table 3. Characteristics of Recent Slotted SOC Cells and Their Corresponding Single-Crystal Control Cells

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
1	175 - 15-101-0	66.70	0.541	0.711	16.35	6.28
2	175 - 15-202-0	70.40	0.543	0.692	17.26	6.49
3	178 - 2-103-0	170.60	0.548	0.710	17.06	6.64
4	178 - 12-102-0	61.20	0.540	0.667	15.00	5.40
5	178 - 15-102-0	68.00	0.533	0.630	16.67	5.60
6	194 - 1-111-0	89.30	0.525	0.686	17.83	6.43
7	194 - 1-211-0	79.80	0.522	0.650	15.96	5.48
8	194 - 2-111-0	84.50	0.513	0.617	16.90	5.35
9	194 - 2-211-0	78.50	0.507	0.669	15.70	5.32
10	194 - 7-111-0	86.60	0.528	0.729	17.32	6.67
10	194 - 7-111-1	123.60	0.533	0.711	24.72	9.32 (AR)
11	194 - 7-211-0	82.00	0.516	0.648	16.40	5.48
11	194 - 7-211-1	116.50	0.523	0.635	23.30	7.74 (AR)
12	198 - 1-111-0	86.50	0.528	0.677	17.30	6.18
13	198 - 1-211-0	79.70	0.522	0.663	15.94	5.52
14	198 - 2-111-0	87.60	0.524	0.628	17.52	5.76
15	198 - 2-211-0	80.30	0.517	0.665	16.06	5.52
16	198 - 3-111-0	87.50	0.518	0.679	17.50	6.20
17	198 - 3-211-0	82.00	0.518	0.677	16.52	5.79
18	198 - 4-111-0	85.50	0.518	0.688	17.10	6.09
19	198 - 4-211-0	81.90	0.519	0.599	16.38	5.09
20	199 - 1-111-0	82.60	0.533	0.746	16.52	6.57
21	199 - 1-211-0	75.40	0.522	0.746	15.08	5.87
22	199 - 3-111-0	86.30	0.532	0.741	17.26	6.80
23	199 - 4-111-0	87.90	0.532	0.731	17.58	6.84
24	199 - 4-211-0	81.10	0.519	0.646	16.22	5.44

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Table 3. Characteristics of Recent Slotted SOC Cells and Their Corresponding Single-Crystal Control Cells (Continued)

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
25	199 - 6-111-0	82.10	0.521	0.717	16.42	6.13
26	200 - 1-101-0	70.00	0.521	0.601	17.16	5.37
27	200 - 1-202-0	71.50	0.526	0.650	17.53	5.99
28	200 - 3-101-0	69.90	0.518	0.741	17.13	6.58
28	200 - 3-101-1	92.40	0.537	0.730	22.65	8.88 (AR)
29	200 - 3-202-0	70.90	0.524	0.739	17.38	6.73
29	200 - 3-202-1	93.00	0.542	0.728	22.79	8.99 (AR)
30	200 - 5-111-0	84.00	0.513	0.584	16.80	5.03
31	200 - 5-211-0	81.00	0.519	0.641	16.20	5.39
32	200 - 6-111-0	85.60	0.525	0.741	17.12	6.66
33	200 - 6-211-0	81.20	0.526	0.738	16.24	6.30
34	201 - 2-103-0	165.80	0.536	0.715	16.58	6.35
35	201 - 3-101-0	72.20	0.529	0.749	17.70	7.01
35	201 - 3-101-1	97.20	0.541	0.735	23.82	9.47 (AR)
36	201 - 3-202-0	71.50	0.533	0.742	17.53	6.93
36	201 - 3-202-1	95.60	0.547	0.732	23.43	9.38 (AR)
37	201 - 4-111-0	87.90	0.519	0.627	17.58	5.72
38	201 - 4-211-0	83.50	0.522	0.562	16.70	4.90
39	201 - 6-111-0	89.80	0.533	0.720	17.96	6.89
39	201 - 6-111-1	124.50	0.535	0.701	24.90	9.34 (AR)
40	201 - 6-211-0	85.00	0.532	0.724	17.00	6.55
40	201 - 6-211-1	118.20	0.533	0.713	23.64	8.98 (AR)
41	202 - 4-102-0	67.50	0.532	0.736	16.54	6.48
41	202 - 4-102-1	94.20	0.542	0.724	23.09	9.08 (AR)
42	202 - 4-201-0	70.60	0.527	0.725	17.30	6.61
42	202 - 4-201-1	93.30	0.545	0.715	22.87	8.91 (AR)
43	202 - 6-102-0	71.50	0.531	0.738	17.53	6.87
43	202 - 6-102-1	95.00	0.543	0.728	23.28	9.24 (AR)
44	202 - 8-111-0	84.90	0.521	0.716	16.98	6.33

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Table 3. Characteristics of Recent Slotted SOC Cells
and Their Corresponding Single-Crystal
Control Cells (Continued)

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
45	202 - 8-211-0	78.80	0.517	0.716	15.76	5.83
46	202 - 9-111-0	85.50	0.525	0.689	17.10	6.20
47	202 - 9-211-0	78.60	0.525	0.739	15.72	6.10
48	203 - 1-111-0	83.00	0.525	0.706	16.60	6.15
49	203 - 1-211-0	79.50	0.529	0.711	15.90	5.98
50	203 - 2-111-0	83.20	0.529	0.711	16.64	6.26
51	203 - 2-211-0	79.00	0.526	0.715	15.80	5.94
52	203 - 3-111-0	85.40	0.530	0.715	17.08	6.47
53	203 - 3-211-0	82.90	0.526	0.686	16.58	5.98
54	203 - 7-111-0	85.20	0.525	0.713	17.04	6.38
55	203 - 7-211-0	81.40	0.532	0.712	16.28	6.19
56	204 - 1-103-0	167.40	0.533	0.734	16.74	6.55
56	204 - 1-103-1	226.00	0.544	0.712	22.60	8.75 (AR)
57	204 - 2-102-0	71.70	0.530	0.750	17.57	6.98
57	204 - 2-102-1	97.20	0.541	0.739	23.82	9.52 (AR)
58	204 - 2-201-0	70.50	0.531	0.743	17.28	6.82
58	204 - 2-201-1	93.30	0.544	0.732	22.87	9.11 (AR)
59	204 - 3-111-0	86.90	0.530	0.718	17.38	6.61
60	204 - 3-211-0	83.10	0.529	0.724	16.62	6.36
61	204 - 4-111-0	85.60	0.531	0.692	17.12	6.29
62	204 - 4-211-0	81.60	0.533	0.738	16.32	6.42
63	206 - 5-111-0	86.60	0.529	0.737	17.32	6.75
64	206 - 5-211-0	81.50	0.529	0.744	16.30	6.42
65	207 -10-111-0	85.00	0.530	0.724	17.00	6.52
66	207 -10-211-0	82.30	0.529	0.648	16.46	5.64
67	208 -11-111-0	87.10	0.536	0.734	17.42	6.85
68	208 -11-211-0	81.60	0.536	0.724	16.32	6.33

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Table 3. Characteristics of Recent Slotted SOC Cells and Their Corresponding Single-Crystal Control Cells (Continued)

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
69	214 - 3-111-0	85.10	0.528	0.597	17.02	5.36
70	214 - 3-211-0	80.30	0.527	0.591	16.06	5.00
71	214 - 6-111-0	85.40	0.495	0.577	17.08	4.88
72	214 - 6-211-0	83.20	0.519	0.599	16.64	5.17
73	215 - 3-111-0	86.00	0.530	0.709	17.20	6.46
74	215 - 3-211-0	59.60	0.528	0.578	11.92	3.64
75	215 - 9-111-0	81.90	0.514	0.631	16.38	5.31
76	215 - 9-211-0	76.20	0.521	0.679	15.24	5.39
77	216 - 1-111-0	80.50	0.555	0.744	16.10	6.65
77	216 - 1-111-1	114.30	0.565	0.738	22.86	9.53 (AR)
78	216 - 1-211-0	81.50	0.550	0.719	16.30	6.45
78	216 - 1-211-1	114.30	0.564	0.717	22.86	9.24 (AR)
79	216 - 2-111-0	78.20	0.549	0.752	15.64	6.46
79	216 - 2-111-1	109.00	0.561	0.752	21.80	9.20 (AR)
80	216 - 2-211-0	78.50	0.545	0.748	15.70	6.40
80	216 - 2-211-1	110.80	0.557	0.739	22.16	9.12 (AR)
81	216 - 4-111-0	82.10	0.558	0.758	16.42	6.94
81	216 - 4-111-1	116.60	0.556	0.716	23.32	9.28 (AR)
82	216 - 4-211-0	83.50	0.557	0.730	16.70	6.79
82	216 - 4-211-1	117.40	0.557	0.719	23.48	9.40 (AR)
83	216 - 5-111-0	81.50	0.555	0.751	16.30	6.79
83	216 - 5-111-1	112.40	0.567	0.743	22.48	9.47 (AR)
84	216 - 5-211-0	82.00	0.554	0.759	16.40	6.90
84	216 - 5-211-1	114.80	0.565	0.745	22.96	9.66 (AR)
85	216 - 6-111-0	81.50	0.552	0.746	16.30	6.71
85	216 - 6-111-1	113.00	0.564	0.741	22.60	9.44 (AR)
86	216 - 6-211-0	83.30	0.550	0.709	16.66	6.50
86	216 - 6-211-1	116.10	0.561	0.716	23.22	9.33 (AR)
87	217 - 1-111-0	79.10	0.547	0.676	15.82	5.85
88	217 - 1-211-0	73.40	0.550	0.645	14.68	5.21

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Table 3. Characteristics of Recent Slotted SOC Cells and Their Corresponding Single-Crystal Control Cells (Continued)

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
89	217 - 2-111-0	80.00	0.532	0.625	16.00	5.32
90	217 - 2-211-0	77.10	0.542	0.703	15.42	5.88
91	217 - 3-111-0	79.10	0.466	0.552	15.82	4.07
92	217 - 3-211-0	74.70	0.502	0.574	14.94	4.30
93	217 - 5-111-0	78.30	0.549	0.751	15.66	6.46
94	217 - 5-211-0	82.30	0.544	0.740	16.46	6.63
95	217 - 6-111-0	80.00	0.551	0.748	16.00	6.59
96	217 - 6-211-0	80.00	0.548	0.750	16.00	6.58
97	217 - 8-111-0	81.80	0.550	0.744	16.36	6.70
98	217 - 8-211-0	79.40	0.548	0.744	15.88	6.47
99	217 -10-111-0	84.30	0.544	0.685	16.86	6.28
100	217 -10-211-0	83.20	0.546	0.730	16.64	6.63
101	218 - 1-111-0	6.20	0.114	0.270	1.24	0.04
102	218 - 1-211-0	6.10	0.113	0.274	1.22	0.04
103	218 - 4-111-0	91.00	0.474	0.623	18.20	5.37
103	218 - 4-111-1	129.80	0.483	0.581	25.96	7.28 (AR)
104	218 - 4-211-0	93.30	0.478	0.632	18.66	5.64
104	218 - 4-211-1	133.70	0.489	0.600	26.74	7.85 (AR)
105	218 - 8-111-0	92.40	0.493	0.677	18.48	6.17
105	218 - 8-111-1	130.10	0.504	0.655	26.02	8.59 (AR)
106	218 - 8-211-0	95.40	0.491	0.677	19.08	6.34
106	218 - 8-211-1	132.70	0.501	0.663	26.54	8.82 (AR)
107	218 -12-111-0	98.90	0.497	0.704	19.78	6.92
107	218 -12-111-1	124.20	0.511	0.688	24.84	8.73 (AR)
108	218 -12-211-0	94.30	0.495	0.694	18.86	6.48
108	218 -12-211-1	127.00	0.507	0.687	25.40	8.85 (AR)
109	221 - 1-111-0	78.00	0.555	0.641	15.60	5.55
110	221 - 1-211-0	81.80	0.548	0.622	16.36	5.58

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Table 3. Characteristics of Recent Slotted SOC Cells and Their Corresponding Single-Crystal Control Cells (Continued)

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
111	221 - 2-111-0	78.10	0.555	0.699	15.62	6.06
112	221 - 4-111-0	80.20	0.552	0.625	16.04	5.53
112	221 - 4-111-1	110.10	0.567	0.653	22.02	8.15 (AR)
113	221 - 4-211-0	81.00	0.561	0.744	16.20	6.76
113	221 - 4-211-1	115.50	0.575	0.732	23.10	9.72 (AR)
114	221 - 5-111-0	77.00	0.558	0.715	15.40	6.14
114	221 - 5-111-1	109.50	0.574	0.720	21.90	9.05 (AR)
115	221 - 5-211-0	79.10	0.557	0.736	15.82	6.48
115	221 - 5-211-1	110.60	0.572	0.739	22.12	9.35 (AR)
116	224 - 2-103-0	148.90	0.557	0.744	14.89	6.17
117	224 - 4-103-0	152.50	0.559	0.745	15.25	6.35
118	224 - 5-111-0	80.20	0.556	0.757	16.04	6.75
119	224 - 5-211-0	76.80	0.512	0.459	15.36	3.61
120	224 - 7-103-0	156.40	0.556	0.749	15.64	6.51
(Single-Crystal)						
121	R18 - 0-111-0	89.90	0.554	0.735	20.48	8.34
122	R21 - 0-111-0	107.40	0.581	0.716	21.48	8.94
123	R21 - 0-211-0	108.30	0.580	0.735	21.66	9.23
124	R23 - 0-111-0	108.70	0.561	0.735	21.74	8.96
125	R23 - 0-211-0	108.60	0.560	0.731	21.72	8.89
126	R24 - 0-111-0	107.10	0.576	0.753	21.42	9.29
127	R24 - 0-211-0	107.80	0.574	0.753	21.56	9.32
128	R25 - 0-111-0	103.50	0.565	0.713	20.70	8.34
129	R25 - 0-211-0	105.30	0.567	0.718	21.06	8.57
130	R26 - 0-111-0	104.00	0.580	0.753	20.80	9.11
131	R26 - 0-211-0	103.50	0.580	0.754	20.70	9.06
132	R27 - 0-111-0	104.60	0.579	0.760	20.92	9.21
133	R28 - 0-111-0	96.30	0.571	0.734	19.26	8.07

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Table 3. Characteristics of Recent Slotted SOC Cells
and Their Corresponding Single-Crystal
Control Cells (Concluded)

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
134	R28 - 0-211-0	98.60	0.564	0.722	19.72	8.03
135	R29 - 0-111-0	101.30	0.578	0.737	20.26	8.63
136	R29H- 0-111-0	107.50	0.577	0.713	21.50	8.84
137	R30 - 0-111-0	103.20	0.579	0.748	20.64	8.94
138	R31 - 0-111-0	103.90	0.577	0.752	20.78	9.02
139	R31 - 0-211-0	106.30	0.578	0.750	21.26	9.22
140	R32 - 0-111-0	99.40	0.584	0.752	19.88	8.73
141	R33 - 0-111-0	91.90	0.566	0.756	18.38	7.86
142	R34A- 0-111-0	87.20	0.554	0.735	17.44	7.10
143	R34B- 0-111-0	89.90	0.554	0.738	17.98	7.35
144	R37 - 0-111-0	105.90	0.581	0.750	21.18	9.23
145	R37 - 0-211-0	105.40	0.578	0.757	21.08	9.22
145	R38 - 0-102-0	85.10	0.565	0.756	20.86	8.91

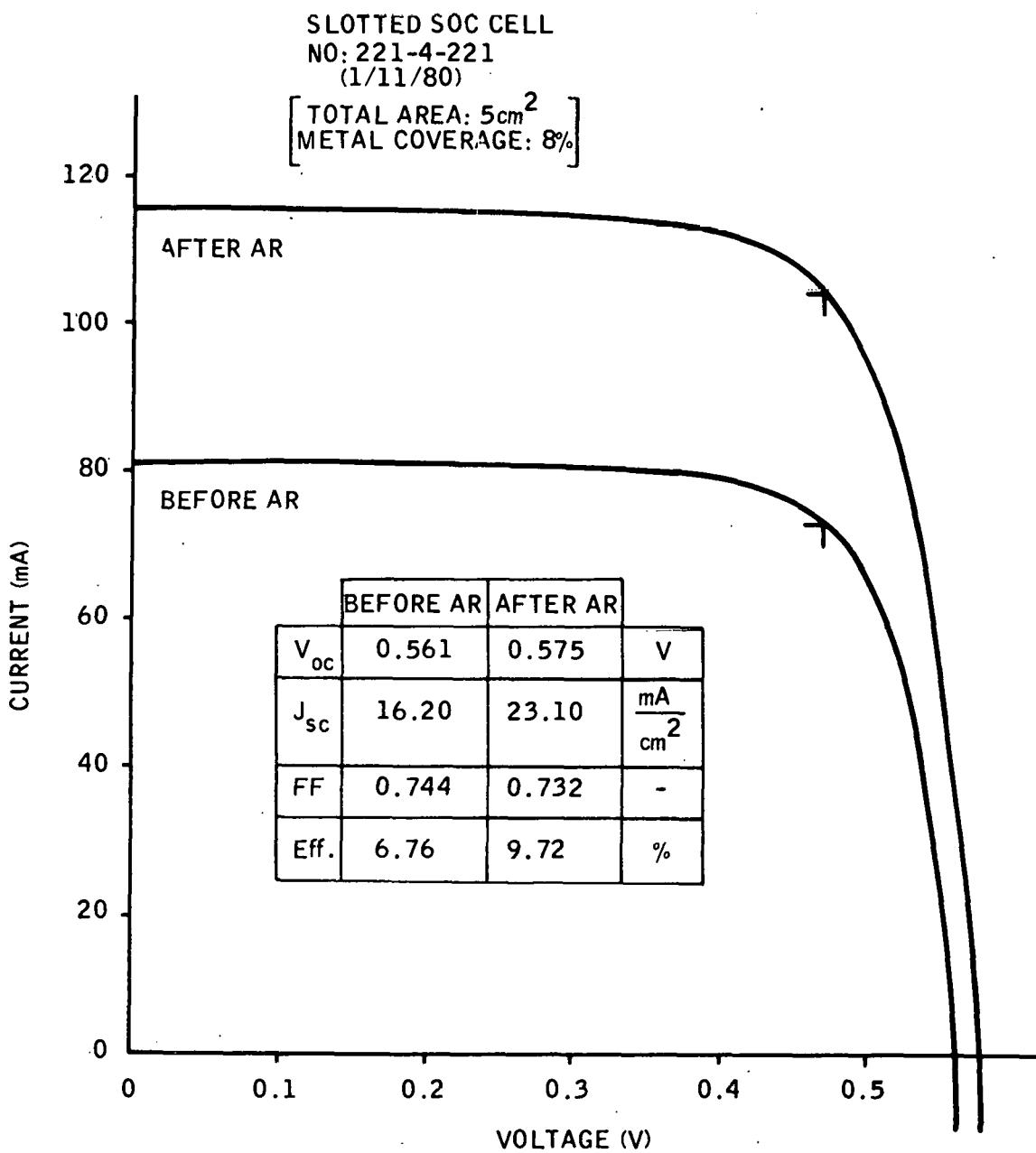


Figure 1. Current-Voltage Characteristics of the Highest-Efficiency Solar Cell Fabricated During This Quarter

Table 4. Diffusion Conditions for the SOC Cells Completed During This Quarter. Note that the values within the parentheses have been omitted for determining the average values.

Item No.	Cell No.	Emitter ρ (Ω/\square)	Eff. (%)	Group
77	216-1-111-0	24.8	6.65	5/20/10
78	216-1-211-0	24.8	6.45	
79	216-2-111-0	27.1	6.46	
80	216-2-211-0	27.1	6.40	
103	218-4-111-0	(28.2)	(5.37)	875°C
104	218-4-211-0	(28.2)	(5.64)	
81	216-4-111-0	36.0	6.94	10/60/10
83	216-4-211-0	36.0	6.79	
83	216-5-111-0	30.5	6.79	
84	216-5-211-0	30.5	6.90	
85	216-6-111-0	32.1	6.71	850°C
86	216-6-211-0	32.1	6.50	
105	218-8-111-0	(36.1)	(6.17)	
106	218-8-211-0	(36.1)	(6.34)	
56	204-1-103	33.6	6.55	10/50/10
41	202-4-102	33.9	6.48	
42	202-4-201	33.9	6.61	
34	201-2-103	35.8	6.35	
26	200-1-101	(36.3)	(5.37)	850°C
27	200-1-202	(36.3)	(5.99)	
57	204-2-102	47.1	6.98	10/20/10
58	204-2-201	47.1	6.82	
43	202-6-102	46.5	6.87	
35	201-3-101	48.2	7.01	
36	201-3-202	48.2	6.93	850°C
28	200-3-101	47.8	6.58	
29	200-3-202	47.8	6.73	

Table 4. Diffusion Conditions for the SOC Cells Completed During This Quarter. Note that the values within the parentheses have been omitted for determining the average values. (Continued)

Item No.	Cell No.	Emitter ρ (Ω/\square)	Eff. (%)	Group
87	217-1-111-0	42.3	5.85	10/20/10
88	217-1-211-0	42.3	5.21	
89	217-2-111-0	43.4	5.32	
90	217-2-211-0	43.4	5.88	
91	217-3-111-0	49.2	4.07	
92	217-3-211-0	49.2	4.30	
101	218-1-111-0	(46.6)	(0.04)	
102	218-1-211-0	(46.6)	(0.04)	
69	214-3-111-0	50.1	5.36	10/20/10
70	214-3-211-0	50.1	5.00	
71	214-6-111-0	45.6	4.88	
72	214-6-211-0	45.6	5.17	
75	215-9-111-0	39.1	5.31	
76	215-9-211-0	39.1	5.39	
73	215-3-111-0	48.9	6.46	
74	215-3-211-0	(48.9)	(3.64)	
61	204-4-111	52.9	6.29	10/10/10
62	204-4-211	52.9	6.42	
46	202-9-111	56.7	6.20	
47	202-9-211	56.7	6.10	
39	201-6-111	(72.7)	6.89	
40	201-6-111	(72.7)	6.55	
32	200-6-111	58.1	6.66	
33	200-6-211	58.1	6.30	
63	206-5-111-0	55.7	6.75	10/10/10
64	206-5-211-0	55.7	6.42	
65	207-10-111-0	53.9	6.52	
66	207-10-211-0	53.9	5.64	
67	208-11-111-0	55.1	6.85	
68	208-11-211-0	55.1	6.33	

Table 4. Diffusion Conditions for the SOC Cells Completed During This Quarter. Note that the values within the parentheses have been omitted for determining the average values. (Continued)

Item No.	Cell No.	Emitter ρ (Ω/\square)	Eff. (%)	Group
59	204-3-111	65.2	6.61	10/10/5
60	204-3-211	65.2	6.36	
44	202-8-111	67.3	6.33	
45	202-8-211	67.3	5.83	
37	201-4-111	69.0	5.72	
38	201-4-211	69.0	4.90	
30	200-5-111	(70.1)	(5.03)	
31	200-5-211	(70.1)	(5.39)	
6	194-1-111	(84.8)	(6.43)	10/30/10
7	194-1-211	(84.8)	(5.48)	
8	194-2-111	67.5	5.35	
9	194-2-211	67.5	5.32	
10	194-7-211	61.1	6.67	
11	194-7-211	66.1	5.48	825°C
12	198-1-111	108.9	6.18	
13	198-1-211	108.9	5.52	
14	198-2-111	129.5	5.76	
15	198-2-211	129.5	5.52	
16	198-3-111	133.4	6.20	
17	198-3-211	133.4	5.79	
18	198-4-111	163.2	6.09	800°C
19	198-4-211	163.2	5.09	
20	199-1-111	37.9	6.57	
21	199-1-211	37.9	5.87	
22	199-3-111	46.6	6.80	
23	199-4-111	(60.3)	6.84	10/30/10
24	199-4-211	(60.3)	(5.44)	
25	199-6-111	48.6	6.13	

Table 4. Diffusion Conditions for the SOC Cells Completed During This Quarter. Note that the values within the parentheses have been omitted for determining the average values. (Concluded)

Item No.	Cell No.	Emitter ρ (Ω/\square)	Eff. (n)	Group
48	203-1-111	37.2	6.15	
49	203-1-211	37.2	5.98	
50	203-2-111	38.9	6.26	10/30/10
51	203-2-211	38.9	5.94	
52	203-3-111	40.2	6.47	(N)
53	203-3-211	40.2	5.98	850°C
54	203-7-111	42.8	6.38	
55	203-7-211	42.8	6.19	
93	217-5-111-0	35.3	6.46	
94	217-5-211-0	35.3	6.63	10/30/10
95	217-6-111-0	39.3	6.58	
96	217-6-211-0	39.3	6.58	(P)
107	218-12-111-0	(40.3)	(6.92)	850°C
108	218-12-211-0	(40.3)	(6.48)	
97	217-8-111-0	37.2	6.70	
98	217-8-211-0	37.2	6.47	10/30/10
99	217-10-111-0	40.1	6.28	
100	217-10-211-0	40.1	6.63	(Q) 850°C
116	224-2-103-0	36.0	6.17	
117	224-4-103-0	41.4	6.35	10/30/10
118	224-5-111-0	43.4	6.75	
119	224-5-211-0	(43.4)	(3.61)	850°C
120	224-7-103-0	44.4	6.51	
109	221-1-111-0	(39.7)	(5.55)	
110	221-1-211-0	(39.7)	(5.58)	10/30/10
111	221-2-111-0	39.3	6.06	
112	221-4-111-0	37.2	5.53	
113	221-4-211-0	37.2	6.76	850°C
114	221-5-111-0	32.9	6.14	
115	221-5-211-0	32.9	6.48	

The important results of Table 4 are summarized in Figures 2 and 3, where Figure 2 corresponds to Groups A through L and Figure 3 correspond to Groups M through S. Figure 2 shows how cell performance varies as a function of emitter sheet resistance, ρ_{\square} . For example, the upper right hand figure gives V_{oc} as a function of ρ_{\square} . In this figure, each ellipse corresponds to a given group, which is identified by a letter. For a given ellipse, the following is true. The center is located at the average value of V_{oc} and at the average value of ρ_{\square} . The vertical extent of the ellipse corresponds to two times the standard deviation for V_{oc} and the horizontal extent of the ellipse corresponds to two times the standard deviation for ρ_{\square} . Thus, a smaller ellipse indicates more consistent results among the cells within a group.

Figure 2 indicates the following: The open-circuit voltage, V_{oc} , is relatively independent of the diffusion conditions. The average V_{oc} is $\sim 0.52V$ for $N_B = 10^{16}/\text{cm}^3$ and $\sim 0.55 V$ for $N_B = 3 \times 10^{16}/\text{cm}^3$, where N_B is the base doping concentration. For the higher doping concentration, the ellipse is cross-hatched. The solid line indicates approximately the behavior of V_{oc} as a function of ρ_{\square} for the lower doping concentration, and the dashed line for the higher doping concentration. The fill factor decreases as ρ_{\square} increases, which is consistent with standard theory. The short-circuit current density, J_{sc} , is relatively independent of ρ_{\square} ; it has a value of about 16.5 mA/cm^2 for the lightly-doped cells and a value of about 16.0 mA/cm^2 for the heavily-doped cells. Clearly, increasing N_B has the effect of increasing V_{oc} and decreasing J_{sc} , which is consistent with standard theory. The efficiency, η , decreases as ρ_{\square} increases, with the trend following the fill-factor. Clearly, higher efficiencies are obtained at lower values of emitter sheet resistance. As a result, we now plan to use a diffusion temperature of 850° and diffusion times of 10/60/10, for future SOC cells. Moreover, we plan to use a standard base doping concentration, N_B , of $5 \times 10^{16}/\text{cm}^3$.

Figure 3 shows SOC cell performance as a function of emitter sheet resistance ρ_{\square} , for cells having the same diffusion conditions. Groups S and R had a base doping concentration, N_B , of $\sim 10^{16}/\text{cm}^3$; groups P and Q, of $\sim 3 \times 10^{16}/\text{cm}^3$; and groups N and M, of $\sim 5 \times 10^{16}/\text{cm}^3$. As before, the highest V_{oc} 's are for highest doping concentrations, and the highest J_{sc} 's are for the lowest doping concentrations. For all groups, the FF's and the η 's are nearly independent of the emitter sheet resistance.

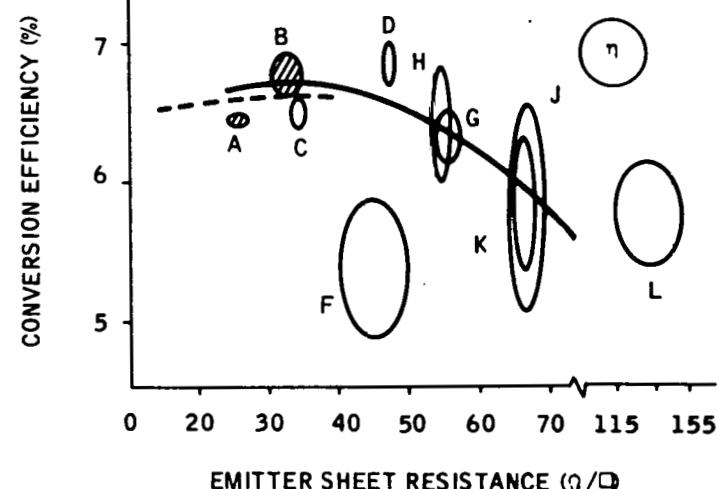
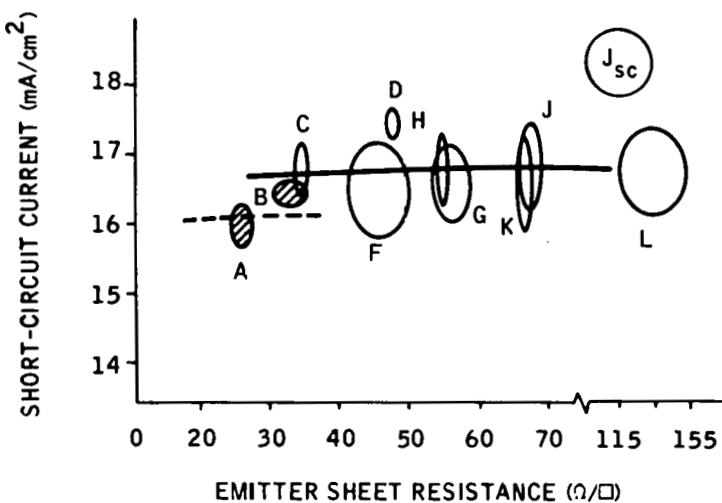
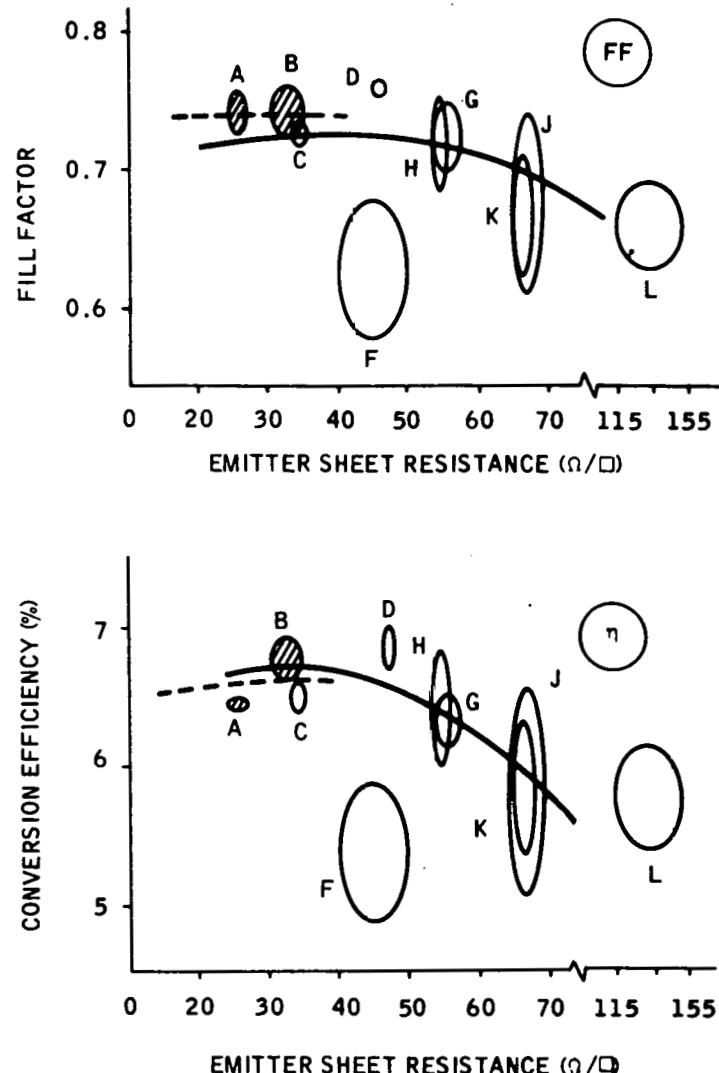
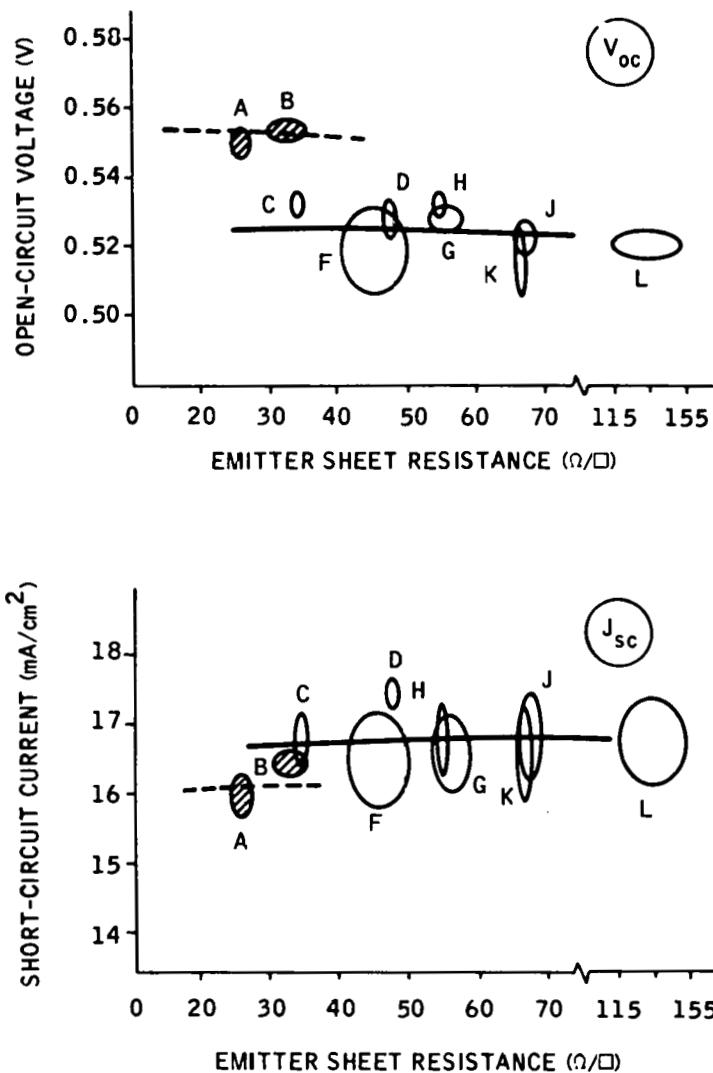


Figure 2. SOC Cell Performance versus of Emitter Sheet Resistance for Various Diffusion Conditions

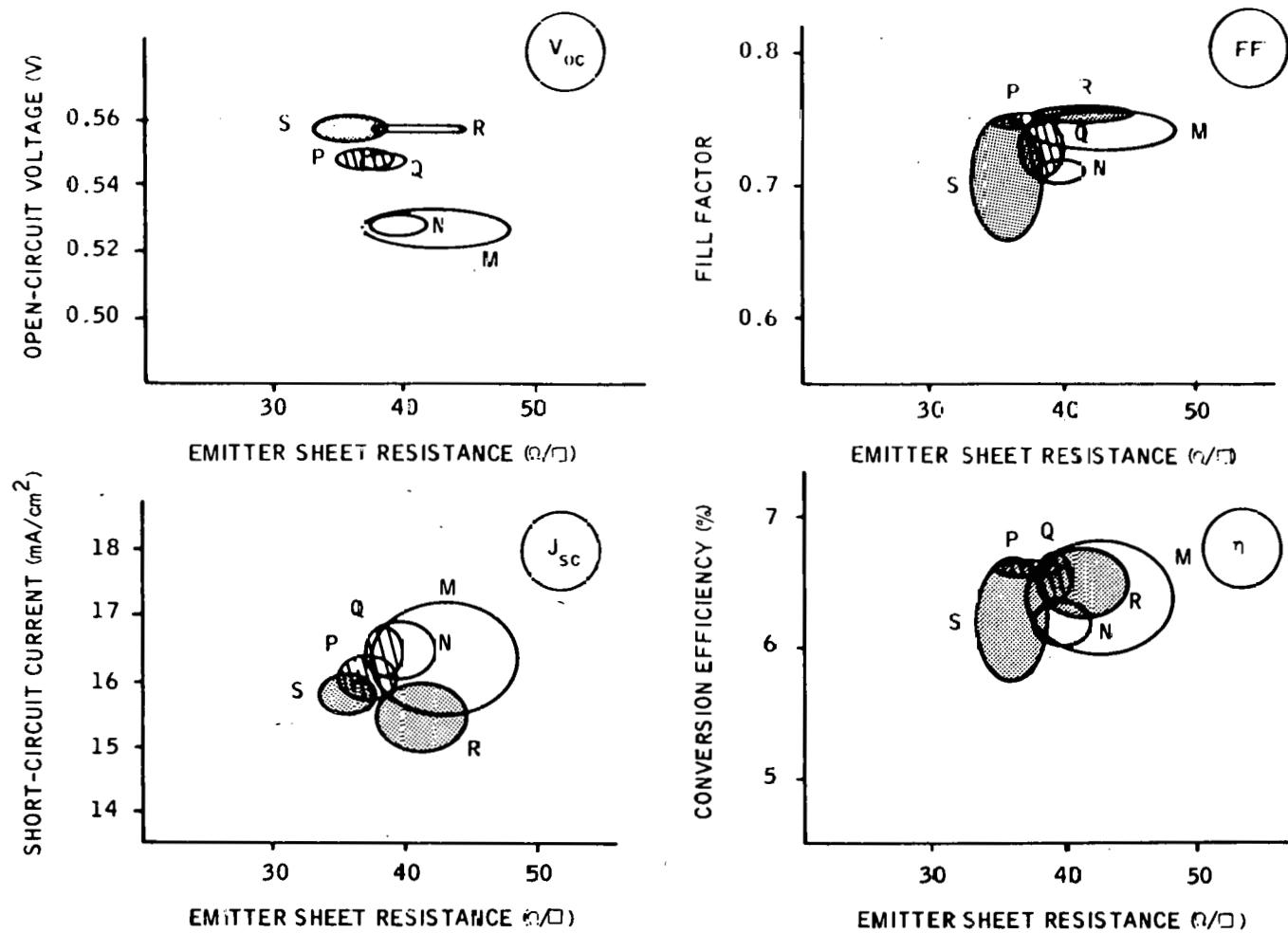


Figure 3. SOC Cell Performance versus Emitter Sheet Resistance for the Same Diffusion Conditions

Figure 4 shows single-crystal cell performance as a function of emitter sheet resistance. The single-crystal cells were fabricated at the same time as the SOC cells. For groups A through L, only one single-crystal cell was used and these are denoted by points, with the group letter written near. For groups M through S, an ellipse was used to summarize the results of these groups. Figure 4 shows that the efficiency of the single-crystal cell increases as a function of emitter sheet resistance, which is the opposite trend as compared with SOC cells. The best single-crystal cells correspond to an emitter sheet resistance of 70 ohms/square.

Photodiodes on SCIM-Coated Material

During this period, we fabricated a number of photodiodes using SCIM-coated material. The best diode has an active-area J_{sc} of 23 mA/cm^2 , which indicates good material quality. Figure 5 presents the current-voltage (I-V) characteristics of a typical photodiode. The open-circuit voltage is 0.49 V; the fill factor, 0.66; the total-area short-circuit current density, 15.1 mA/cm^2 ; and the total-area efficiency, 4.9% (AM1, AR), for a diode area of 0.05 cm^2 . The SCIM material was grown at 0.06 cm/sec , in a relatively dirty system. That is, no attempt has been made, as yet, to clean the SCIM system for producing solar-cell-quality sheet silicon. Thus, the photodiode performance is quite good considering the existing growth conditions.

Calculated I-V Characteristics

In Quarterly Report No. 11, we discussed a five-parameter equation describing the dark I-V characteristics of an SOC cell. The parameters were R_{sh} , n , I_{02} , R_s and I_{01} . In Quarterly Report No. 12, we discussed a six-parameter equation for describing the light I-V characteristics of an SOC cell. Five of the parameters were identical to the dark parameters and the sixth was the measured value of the short-circuit current, I_{sc} . In Annual Report No. 4, we presented parameter values for 21 SOC cells. These results are also given in Table 5 along with the corresponding results for eight other cells. From these results, we have determined parameter values which are typical of some recent SOC cells. These values are: $R_{sh} = 10K \text{ ohms}$; $n = 2$; $I_{02} = 5 \times 10^{-4} \text{ mA}$; $R_s = 0.20 \text{ ohm}$; and $I_{01} = 6.26 \times 10^{-8} \text{ mA}$, assuming a cell area of 5 cm^2 . Figure 5 shows the calculated I-V characteristics, using the just-given values and the following equation:

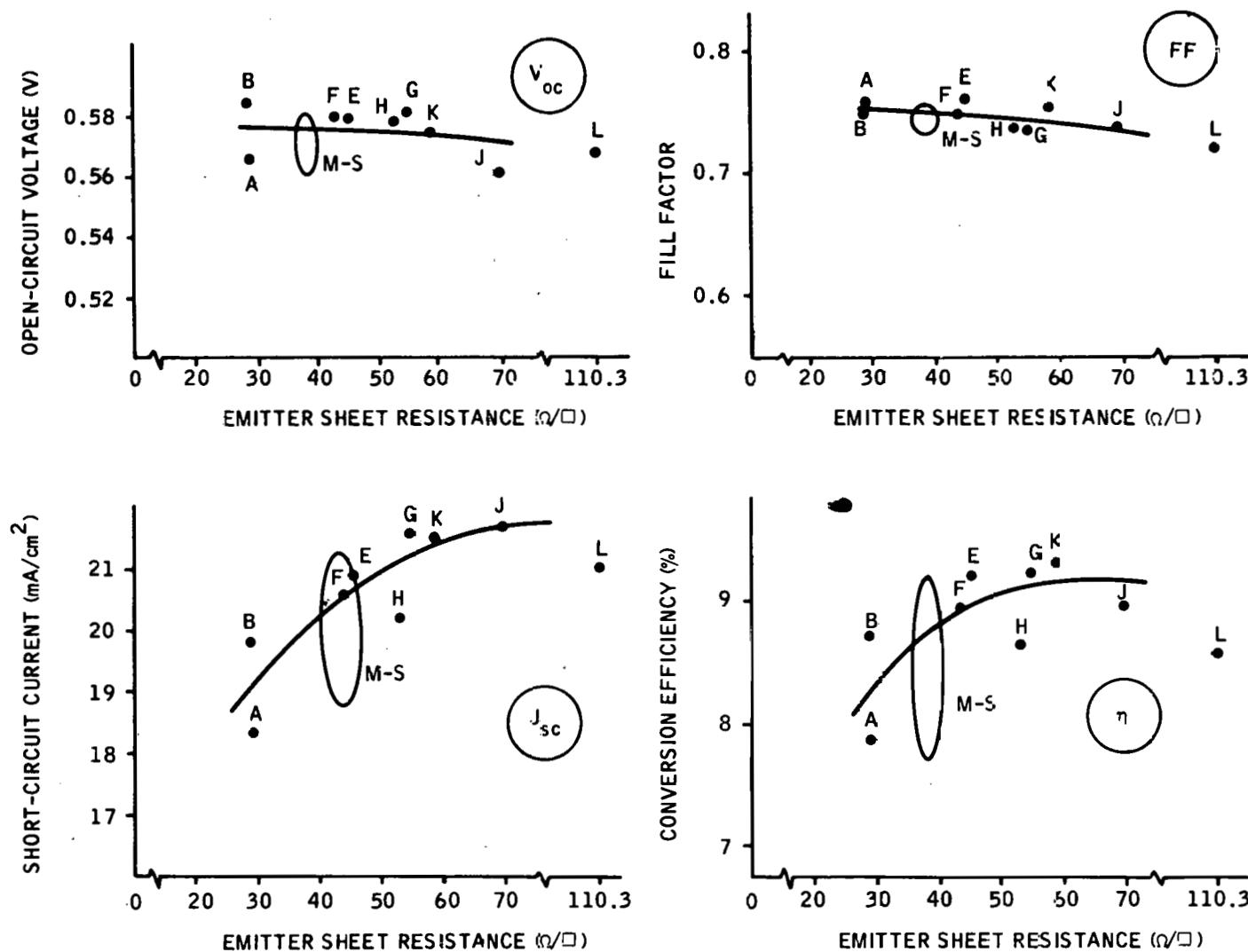


Figure 4. Single-Crystal Cell Performance versus Emitter Sheet Resistance

**SOC PHOTODIODE
FABRICATED FROM
SCIM-COATED MATERIAL
(AREA = 0.054 cm²)**

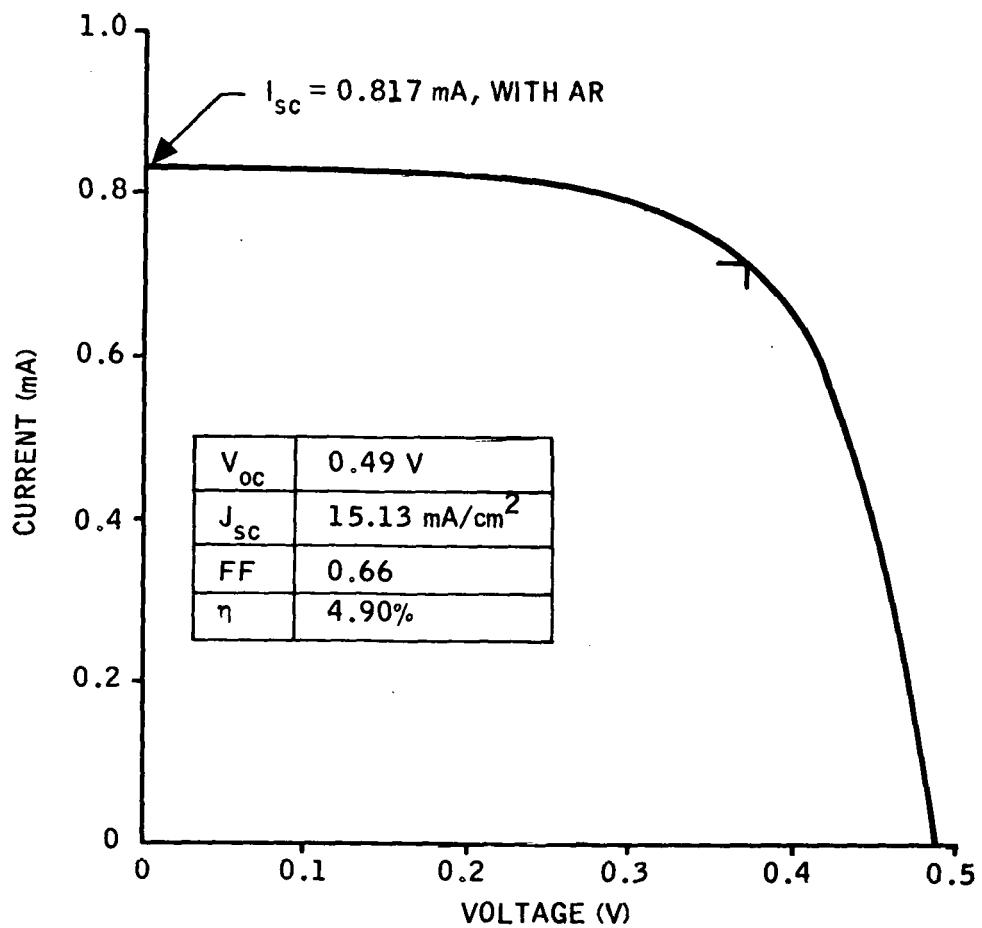


Figure 5. Current-Voltage Characteristics of an SOC Photodiode Fabricated on SCIM-Coated Material

Table 5. Calculated Values for Recent SOC Cells.
The cell area is 4.08 cm^2 .

Item No.	Cell No.	N_B (cm^{-3})	R_{sh} ($\text{k}\Omega$)	n	J_{02} (mA/cm^2)	R_s^A ($\Omega \cdot \text{cm}^2$)	J_{01} (mA/cm^2)
1	187-2-102	2.3×10^{16}	820	1.8	3.7×10^{-5}	0.9	1.0×10^{-8}
2	187-2-201	2.3×10^{16}	150	2.3	2.4×10^{-4}	0.9	1.4×10^{-8}
3	187-7-101	2.3×10^{16}	31	2.3	1.0×10^{-3}	0.8	1.3×10^{-8}
4	187-7-202	2.3×10^{16}	5.7	2.6	9.2×10^{-4}	1.0	1.6×10^{-8}
5	187-9-102	2.3×10^{15}					
6	187-9-201	2.3×10^{16}					
7	185-7-102	2.3×10^{15}	4.7	2.6	3.3×10^{-3}	0.9	2.5×10^{-8}
8	185-9-102	2.3×10^{15}	1000	1.7	7.0×10^{-5}	1.1	4.4×10^{-8}
9	185-9-201	2.3×10^{15}	29	2.0	2.6×10^{-4}	1.4	4.8×10^{-8}
10	185-1-102	2.3×10^{15}	230	1.7	6.8×10^{-5}	1.2	4.4×10^{-8}
11	185-1-201	2.3×10^{15}	180	1.7	4.8×10^{-5}	1.6	4.3×10^{-8}
12	185-2-102	2.3×10^{15}	49	2.1	2.9×10^{-4}	1.4	5.2×10^{-8}
13	185-2-201	2.3×10^{15}	140	1.8	6.2×10^{-5}	1.6	3.7×10^{-8}
14	185-2-101	2.3×10^{15}	150	1.9	1.7×10^{-4}	0.9	3.8×10^{-8}
15	185-5-202	2.3×10^{15}	370	1.7	6.4×10^{-5}	0.9	3.1×10^{-8}
16	185-8-101	2.3×10^{15}	66	2.0	2.1×10^{-4}	1.3	4.6×10^{-8}
17	185-8-202	2.3×10^{15}	3.1	3.9	8.1×10^{-3}	1.0	6.8×10^{-8}
18	185-17-102	2.3×10^{15}	70	2.2	1.8×10^{-4}	3.0	3.5×10^{-8}
19	185-17-201	2.3×10^{15}	0.4	2.1	4.9×10^{-4}	1.5	4.6×10^{-8}
20	185-20-102	2.3×10^{15}	~	1.7	4.3×10^{-5}	0.7	3.1×10^{-8}
21	185-20-201	2.3×10^{15}	125	1.7	4.4×10^{-5}	1.0	3.1×10^{-8}
22	188-2-101	2.3×10^{16}	590	1.8	2.0×10^{-5}	1.6	3.9×10^{-8}
23	188-2-202	2.3×10^{15}	0.4	2.3	1.1×10^{-3}	1.5	5.9×10^{-8}
24	182-7-202	4.7×10^{16}	31	1.8	2.5×10^{-5}	0.6	6.4×10^{-9}
25	182-5-202	4.7×10^{16}	16	2.3	2.5×10^{-4}	0.6	7.5×10^{-9}
26	182-6-202	4.7×10^{16}	400	2.5	2.4×10^{-4}	0.7	8.6×10^{-9}
27	179-4-102	4.7×10^{15}	370	1.7	3.6×10^{-5}	1.1	3.0×10^{-8}
28	179-4-201	4.7×10^{15}	650	1.8	5.9×10^{-5}	0.9	2.7×10^{-8}
29	183-5-201	1.4×10^{16}	320	1.9	7.7×10^{-5}	3.7	1.3×10^{-8}

$$I = I_{01} \left[\exp \frac{q(V - R_S I)}{kT} - 1 \right] + I_{02} \left[\exp \frac{q(V - R_S I)}{nkT} - 1 \right] + \frac{V - R_S I}{R_{SH}} - I_{DS} \quad (1)$$

To understand better the properties of an SOC cell, we can calculate how the various parameters affect the I-V characteristics shown in Figure 6. Figure 7 shows the characteristics for three values of R_{sh} . Figures 8 through 11 show corresponding characteristics for various values of n , J_{02} , $R_s A$, and J_{01} , where $J_{01} = I_{01}/A$, $J_{02} = I_{02}/A$, and $R_s A$ is the specific series resistance. In all figures, we assume that short-circuit current is a constant and that the various parameters can be independently changed. These two assumptions are certainly not valid in general but are made here for simplicity. In future reports we will discuss how the various parameters are interrelated.

Figures 7 through 11 demonstrate some well-known results. Cell performance is improved by increasing R_{sh} , n , or J_{01} or by decreasing J_{02} or R_s . One important but often overlooked result is given in Figure 9. This figure shows that the fill factor decreases substantially as J_{02} increases from zero to $5 \times 10^{-4} \text{ mA/cm}^2$. When $J_{02} = 10^{-5} \text{ mA/cm}^2$ (which is typical for SOC cells), the fill factor is 0.75, as compared with 0.78 when J_{02} is zero. Physically, the J_{02} parameter is associated with recombination in the space-charge region of a solar cell and with recombination at the grain boundaries. Thus, it can be concluded that such recombination effects are responsible for the fact that the SOC cells have a fill factor of ~ 0.75 , as compared with ~ 0.78 for corresponding single-crystal cells.

The results given in Figures 7 through 11 are presented in a different form in Figure 12, which shows how the calculated conversion efficiency varies as a function of five parameters: R_{sh} , J_{02} , n , $R_s A$ and J_{01} . As has been noted, we are assuming that the various parameters are independent and that the short-circuit current density is a constant which is equal to mA/cm^2 . Given these two rather drastic assumptions, Figure 12 shows that calculated efficiency values greater than 11% are difficult to achieve by changing a single parameter in Equation (1). For example, decreasing specific series resistance $R_s A$ from $1 \Omega\text{-cm}$ to zero increases the calculated efficiency from 10.35% to 10.89%.

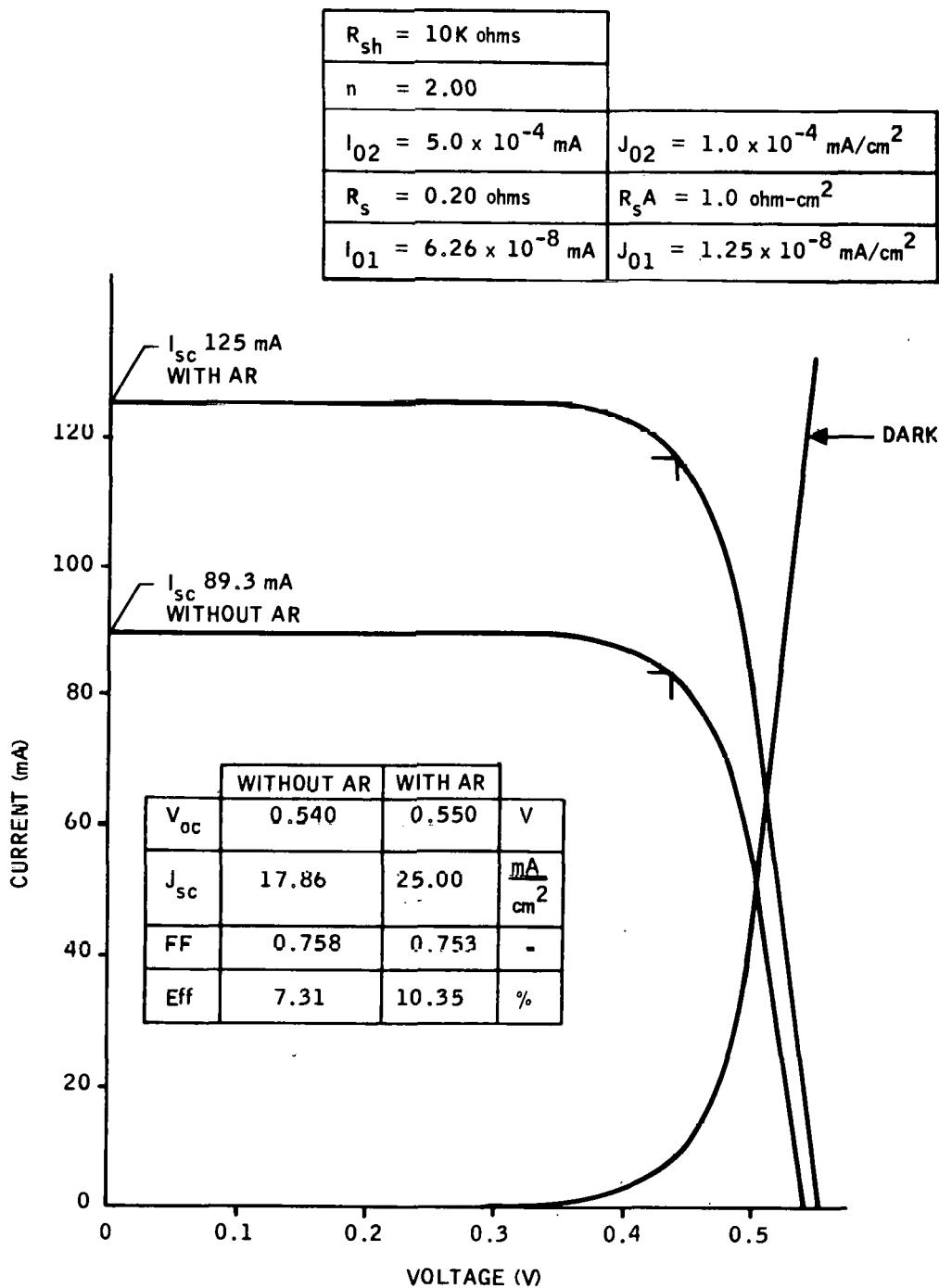


Figure 6. Calculated Current-Voltage Characteristics of a Typical SOC cell

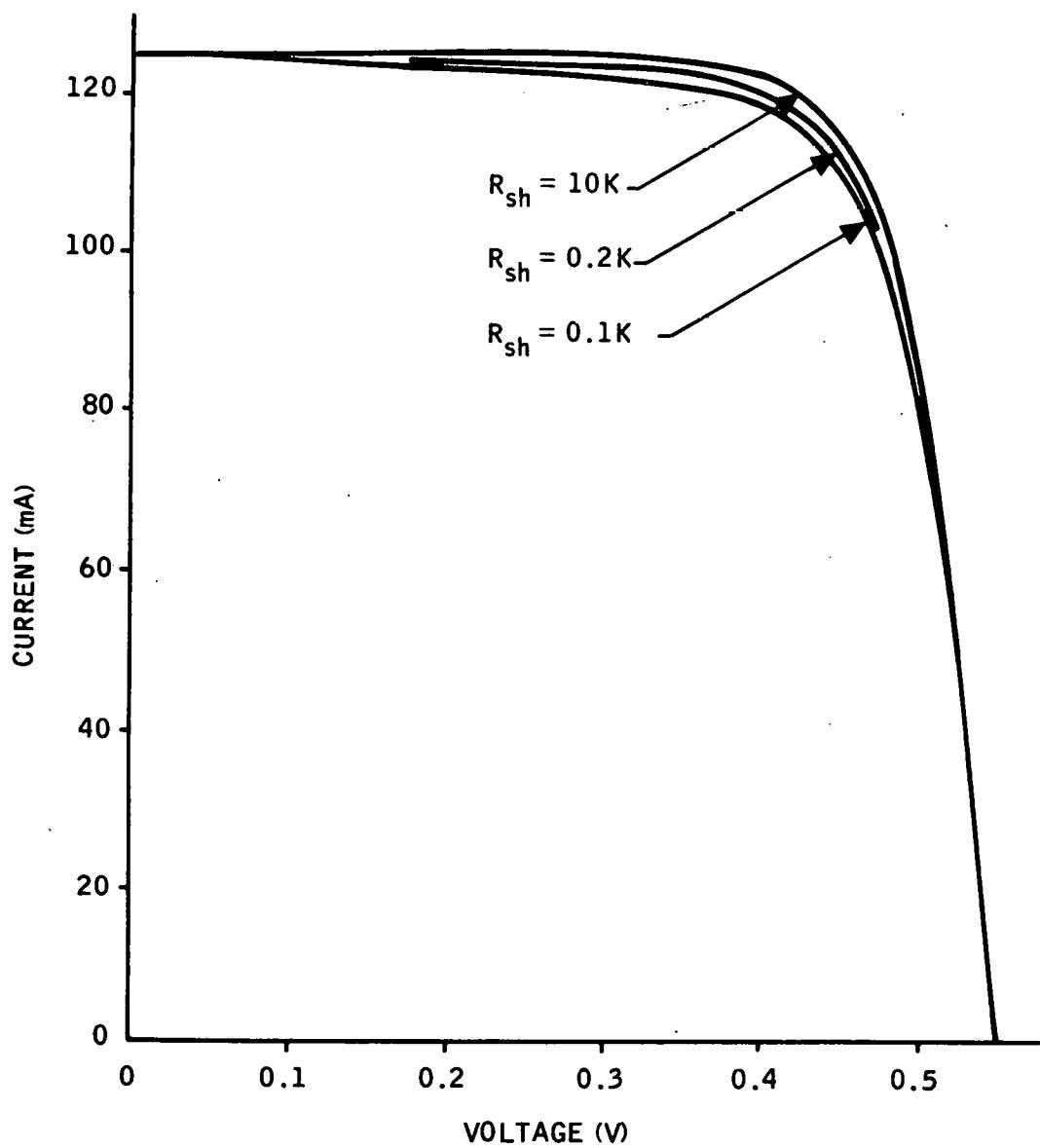


Figure 7. Calculated Current-Voltage Characteristics for Various Values of Shunt Resistance, R_{sh}

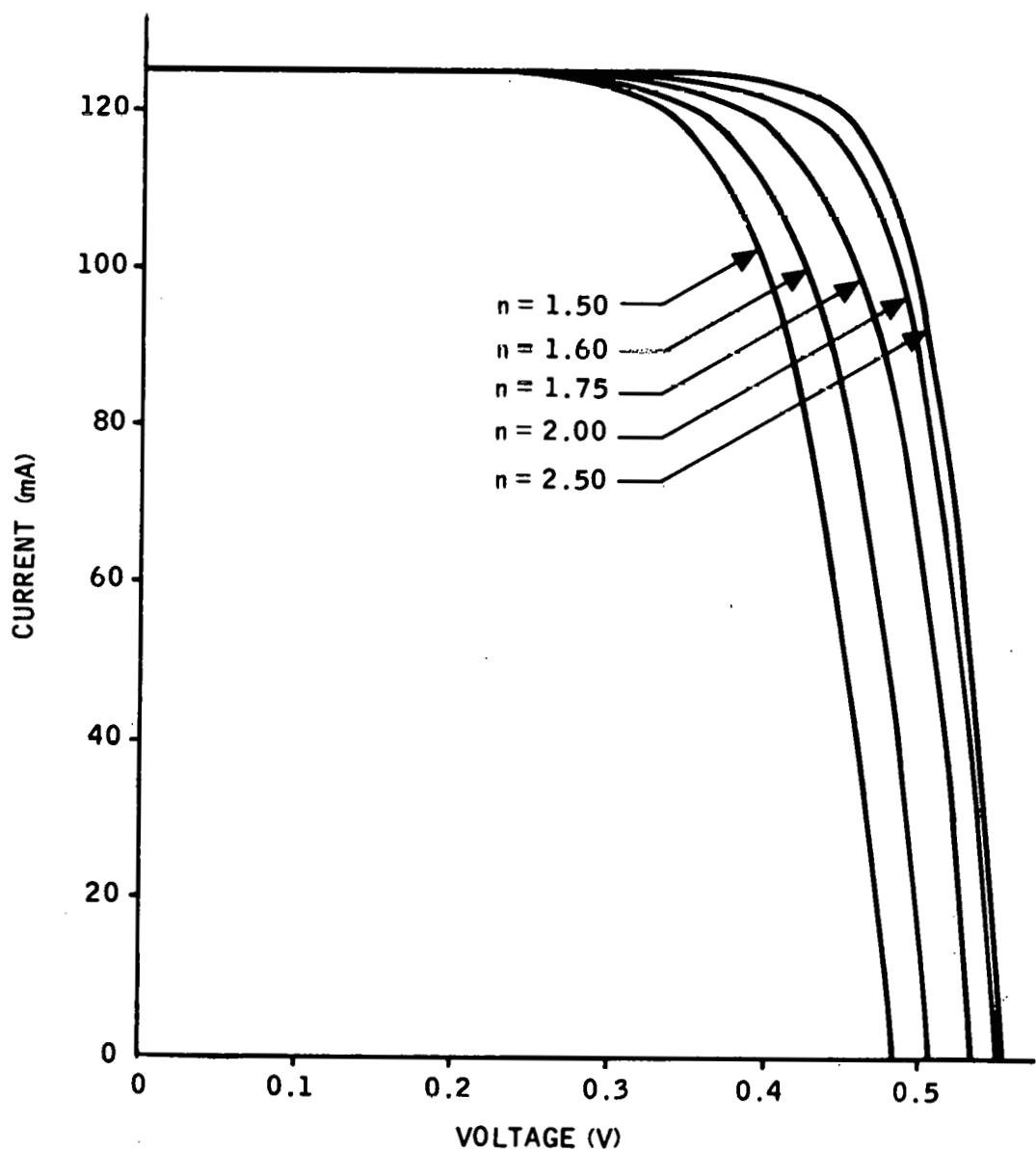


Figure 8. Calculated Current-Voltage Characteristics for Various Values of the Empirical Parameter n

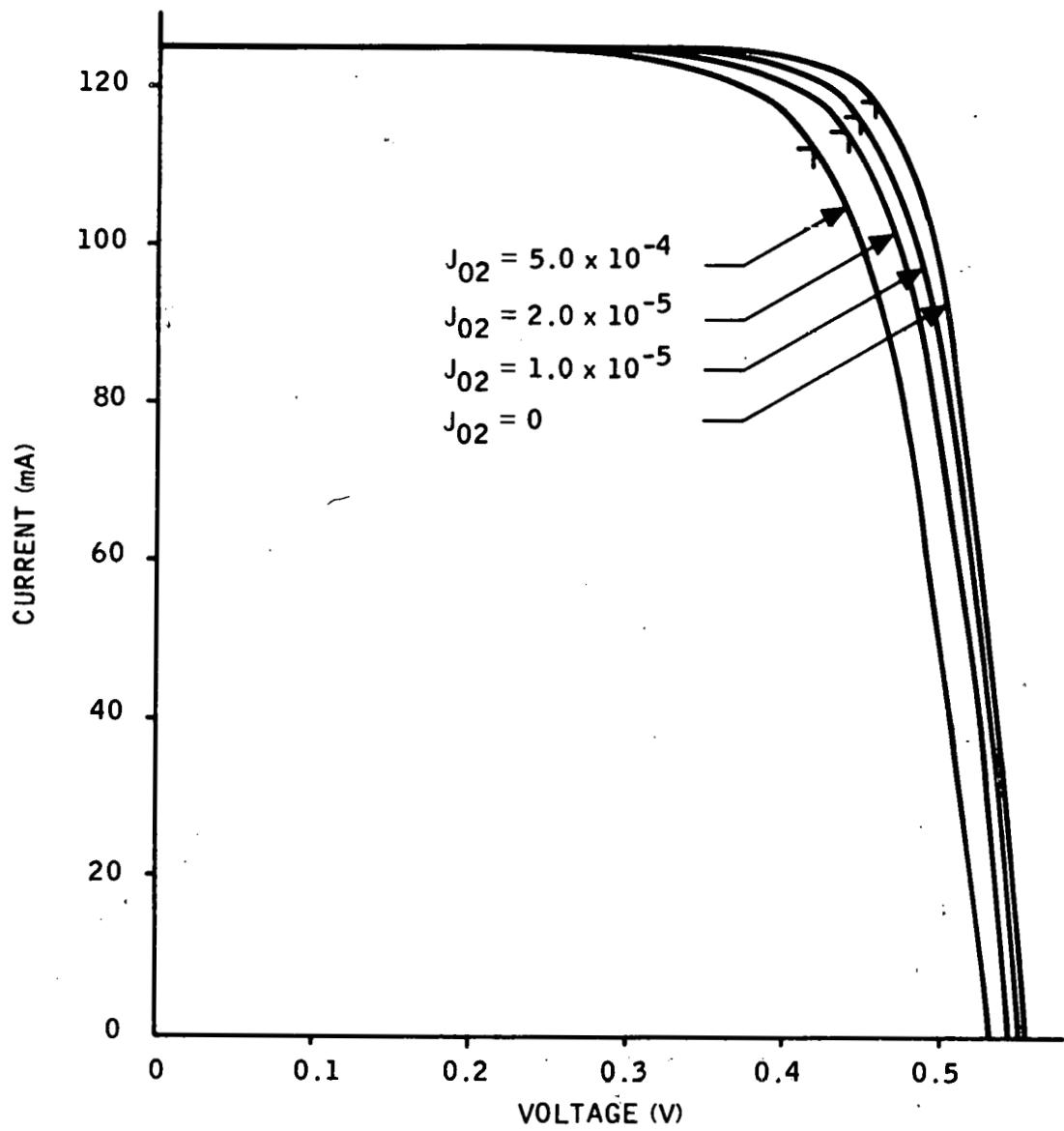


Figure 9. Calculated Current-Voltage Characteristics for Various Values of the Empirical Parameters J_{02}

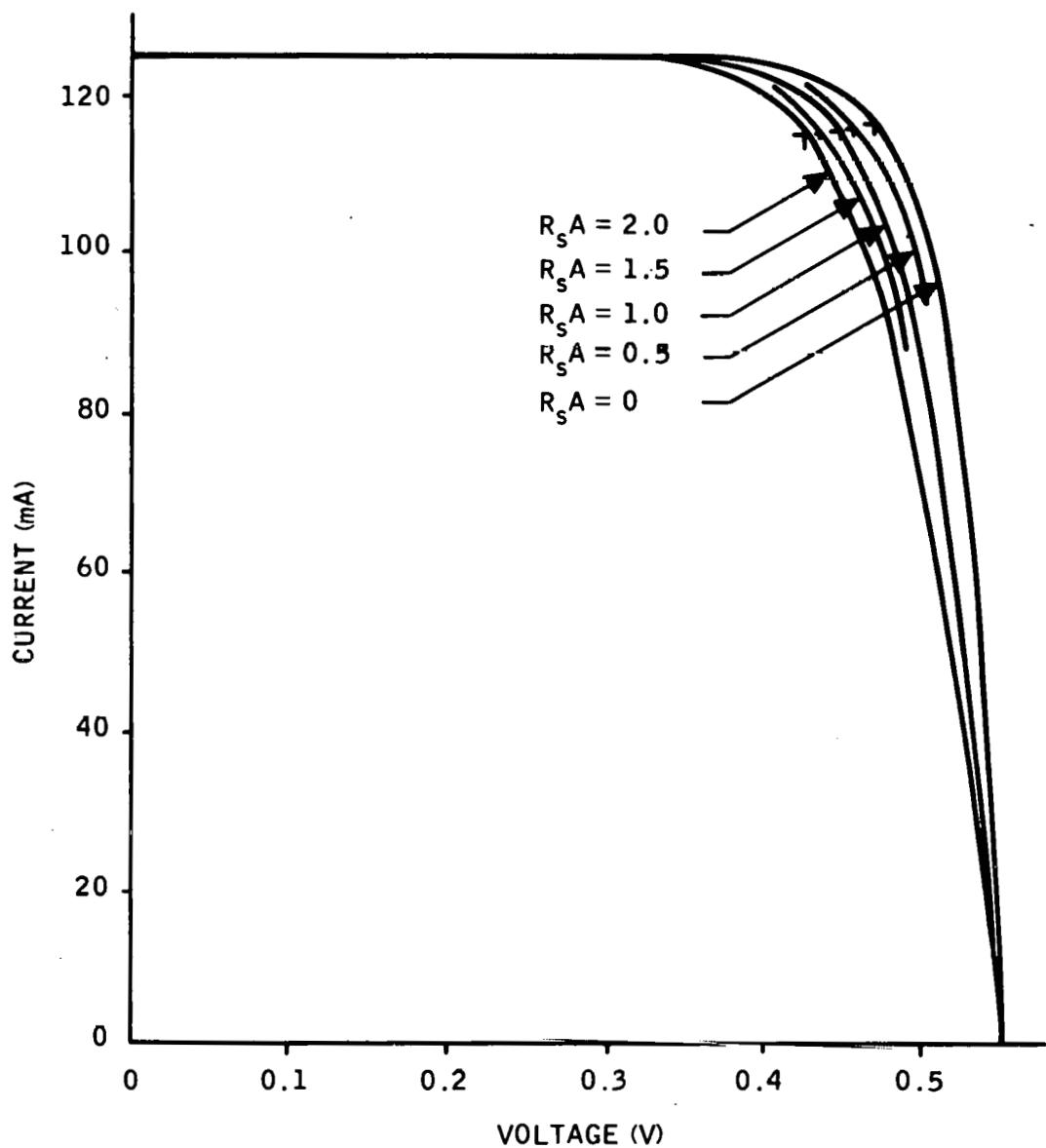


Figure 10. Calculated Current-Voltage Characteristics for Various Values of Specific Series Resistance

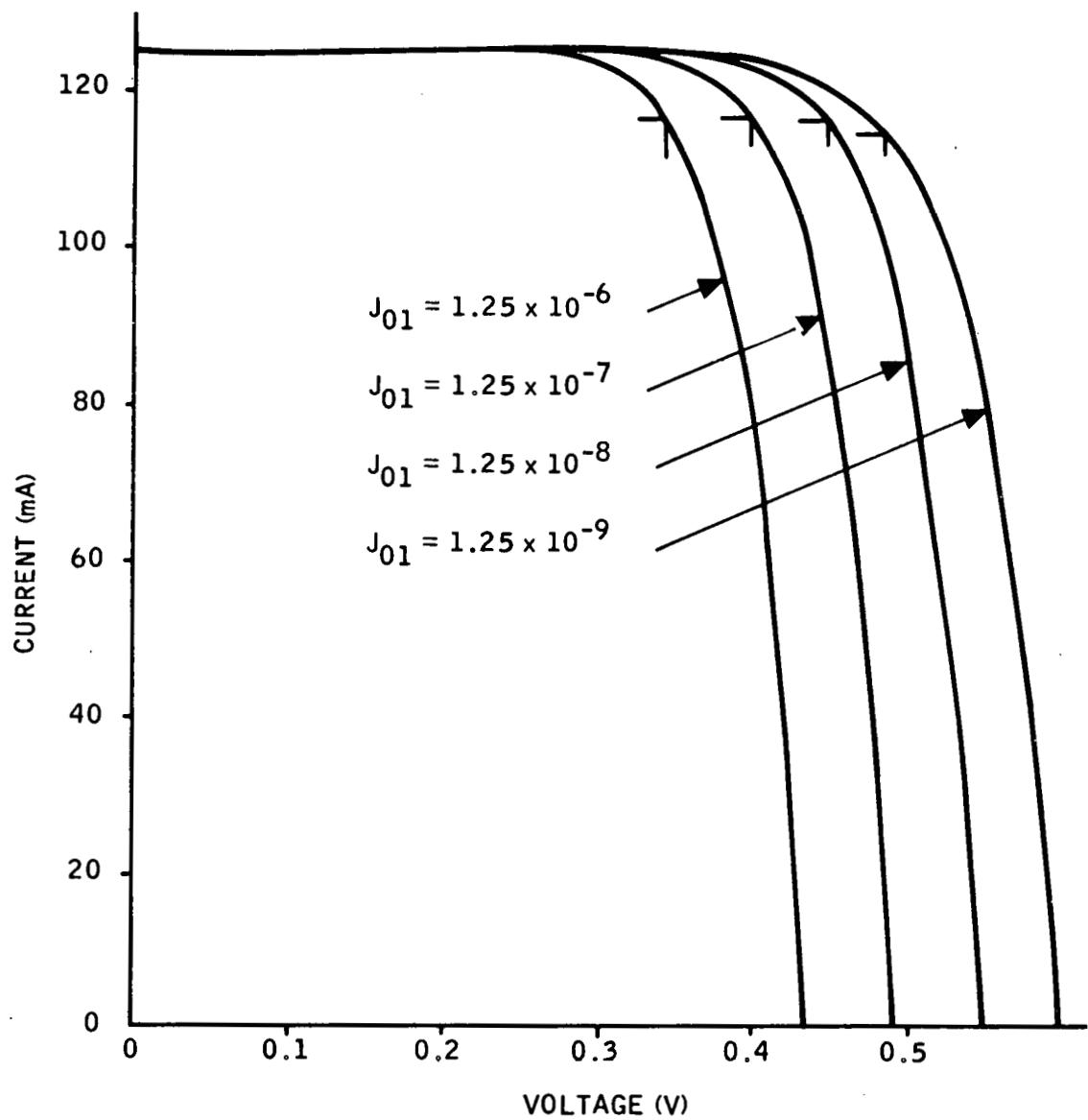


Figure 11. Calculated Current-Voltage Characteristics for Various Values of the Empirical Parameter J_{01}

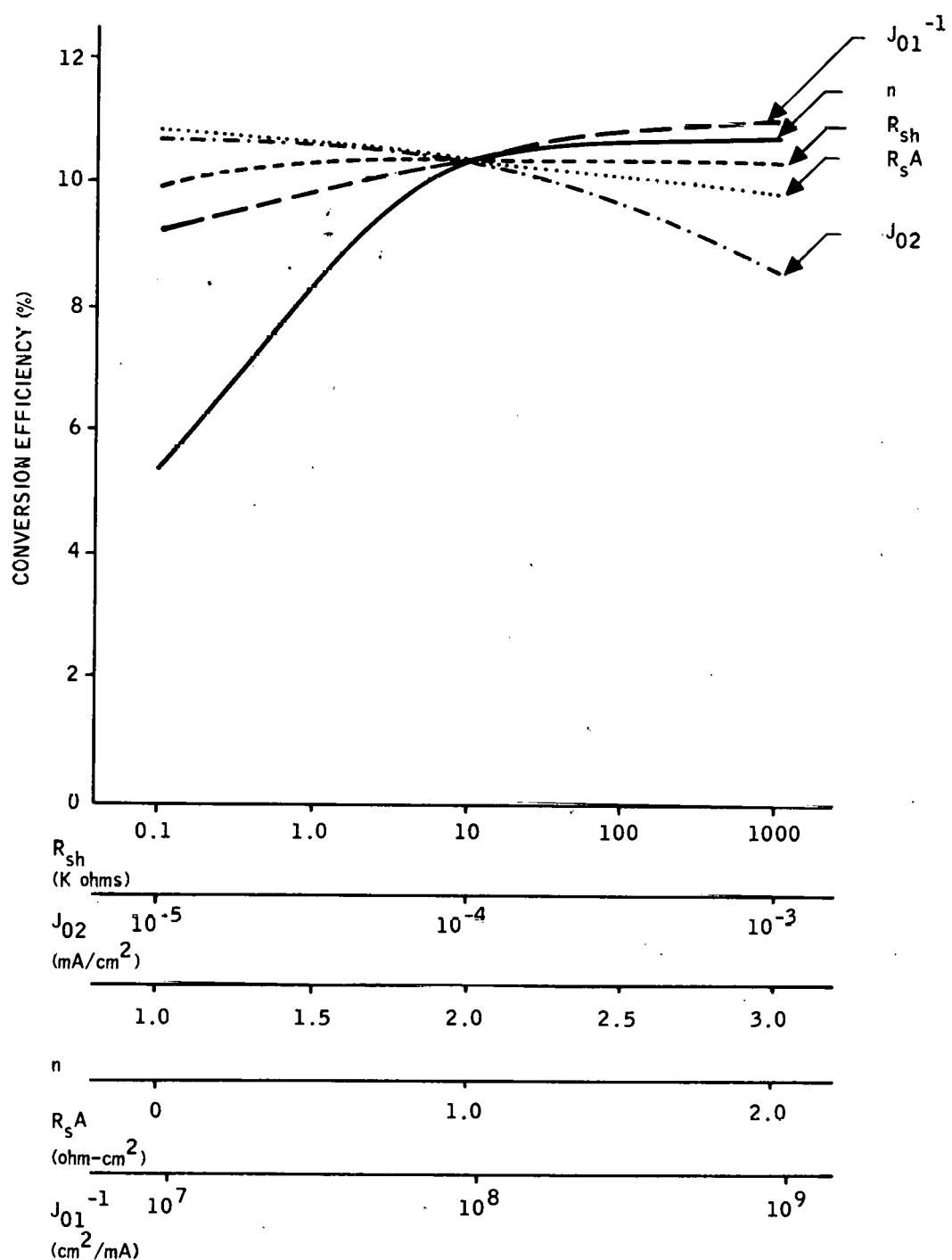


Figure 12. Calculated Conversion Efficiency as a Function of R_{sh} , J_{02} , n , $R_s A$, and J_{01}^{-1}

Based on Figure 12, we can conclude that the performance of an SOC cell cannot be drastically improved by increasing the shunt resistance or by decreasing the effects of series resistance or of recombination in the space charge region of the cell. It appears that the short-circuit current density must be increased to increase substantially the conversion efficiency of SOC cells.

MATERIAL EVALUATION (D. Zook, R. Hegel, D. Sauve, S. Marquardt, C. Wensman)

Light-Beam Scans and Diffusion Length Measurements

During this reporting period, the theory of light-beam scanning near a grain boundary was further developed, including a new method for determining effective surface recombination at a grain boundary. The number of LBIC (light-beam-induced current) scans made was increased, and some generalizations regarding LBIC behavior were noted.

The loss of short-circuit current due to a grain boundary is of particular interest to solar-cell performance. The previous quarterly and annual reports gave a theoretical expression for the quantum efficiency of a p-n junction for a ray of light in the neighborhood of a grain boundary. The quantum efficiency, Q , is a function of A , S , and X , where $A = \alpha L$, $S = sL/D$, $X = x/L$, and x is the distance from a grain boundary which is perpendicular to the junction. The total short-circuit current of a solar cell is simply the sum of the currents due to all such rays. The total loss in current due to an isolated grain boundary can be expressed as a loss in quantum efficiency:

$$W = 2 \int_0^{\infty} \frac{Q_{\infty} - Q(A, S, X)}{Q_{\infty}} dX \quad (2)$$

Here W is an effective width of a grain boundary in the sense that an opaque strip of width W on the surface the length of the boundary would cause the same loss in current. The parameter $Q_{\infty} = Q(A, S, \infty) = A/(1 + A)$ is the usual quantum efficiency.

The mathematics can be simplified considerably by using an integral representation for the Bessel functions, as pointed out by O. von Roos.¹ The result is

$$\frac{Q(A, S, X)}{Q_\infty} = 1 - \frac{2}{\pi} (1 + A) S \int_0^\infty \frac{\sinh^2 t e^{-X \cosh t} dt}{\cosh^2 t (S + \cosh t) (A^2 + \sinh^2 t)} \quad (3)$$

This expression is very rapidly convergent and can be readily evaluated using a programmable hand calculator. The effective grain boundary width can be expressed by a similar integral:

$$W(A, S) = \frac{4}{\pi} \int_0^\infty \frac{\sinh^2 t dt}{\cosh^2 t (S + \cosh t) (A^2 + \sinh^2 t)} \quad (4)$$

by substituting Eq. (3) into Eq. (2). This effective grain boundary width is plotted in Figure 13 for all values of A and S . It can be seen that W decreases as A (or the absorption coefficient) increases, thus W decreases as wavelength decreases. This certainly agrees with experimental observations. The circles in Figure 13 represent data points taken from LBIC data on SOC grain boundaries (sample 179-4). It is clear that the experimental values are in fair agreement with a surface recombination velocity close to infinite.

The significance of this result is that the grain boundaries in SOC are essentially a worst-case situation. Processing which causes impurities to segregate to grain boundaries can only make the response within grains better; they cannot make the grain boundaries worse. Thus, processing which maximizes grain boundary gettering should be beneficial to semicrystalline and polycrystalline solar-cell material.

The above discussion shows that our theoretical understanding of LBIC response is quite good. Experimentally, we have obtained LBIC scans on a large number of SOC solar cells, photodiodes, and unprocessed substrates (using the electrolyte technique). We have not as yet been able to make a good correlation between LBIC scans and solar-cell J_{sc} . At best, we can make some generalizations, as follows:

- 1) There usually is a characteristic maximum diffusion length, L_{max} . This will be seen by good response at 0.98 μm , and generally occurs in the largest visible grains (greater than 400 μm wide).

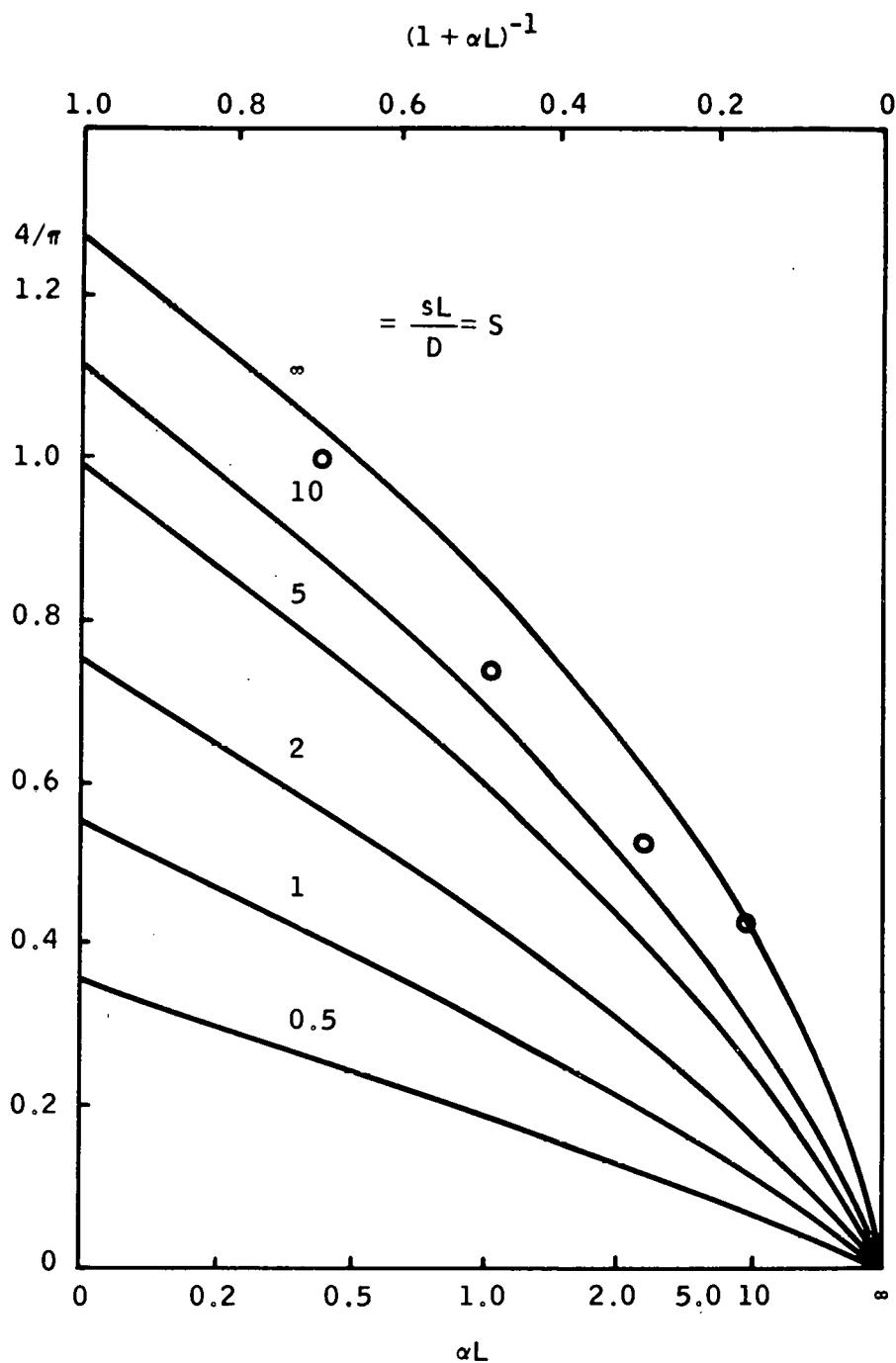


Figure 13. Calculated Effective Grain Boundary Width, W , as a Function of Wavelength for Different Values of Surface Recombination Velocity, s , at the Grain Boundary. The Wavelength dependence enters through the absorption coefficient, α

2) There usually is a characteristic minimum diffusion length, characteristic of the most active grain boundaries. Surprisingly, from a theoretical view, the depth of the minimum LBIC response at 0.98 μm does not depend strongly on the spot size or the focus of the light beam. Thus, the minima of the LBIC response tend to be constant, even if the substrate is bowed, so that part of the scan is out-of-focus. Even spot size 5 or 10 times larger than the minimum spot size ($\sim 5 \mu\text{m}$) does not significantly affect the value of the minima. Thus, a "minimum diffusion length" is a fairly well-defined experimental quantity for a given SOC cell.

Table 6 lists values of \bar{L} , L_{\max} , and L_{\min} for a number of recent LBIC measurements. The average value \bar{L} is determined from the integrated average across the entire cell, corrected for metallization. The integration was performed electronically while scanning at 0.98 μm . A uniform region within a grain was selected and spectral response at all wavelengths was measured. The procedure described in Annual Report No. 4 was used to fit the long-wavelength spectral response (six data points between 0.823 μm and 0.994 μm), to give a value of L , $1 - R$ and an rms deviation $\Delta L/L$. The values of L_{\max} and L_{\min} were then determined from the 0.98- μm scan, and represent averages of the highest and lowest response at half a dozen points.

The correlation between cell J_{sc} and \bar{L} is shown in Figure 14. It is clear that the correlation is poor. The value of J_{sc} appears to be more affected by variations in oxide thickness than by variations in \bar{L} . The value of \bar{L} , in turn, is not well correlated with the value of L_{\max} , but is more sensitive to the type of structure. Grain boundaries have a very detrimental effect on L , since all of the minima occur at grain boundaries, and frequently there are significant regions of the material that have low response at 0.98 μm because of the large number of grain boundaries fairly close together ($\leq 100 \mu\text{m}$). The H plasma annealed samples are diodes fabricated on substrates that were treated in a H plasma at Sandia Laboratories. The substrates were first diffused and the PtSi contact process was applied to the back. They then went to Sandia where different cells received hydrogen treatment at various temperatures. The hydrogenation is done in plasma which produces atomic hydrogen rather than molecular hydrogen. The atomic hydrogen has been found by C. Seager and D. Ginley of Sandia to diffuse much more readily in silicon and to reduce barrier heights in silicon, resulting in much lower grain boundary resistance.

Altogether, 49 diodes were tested with seven different diffusion conditions. Many of the diodes have unusually high J_{sc} , but we have found that these sub-

Table 6. LBIC Results

Cell No.	J_{sc} (mA/cm ²)	L (μ m) ^a	L_{max} (a)	L_{min} (a)	$\Delta L/L$	$I - R$	Comments
201-2-103	16.58	32.2	56.0	4.9	0.12	0.713	
202-4-102	23.09(AR)	30.1	66.6	6.1	0.07	0.913	AR coated
201-3-101	23.82(AR)	21.8	98.8	4.35	0.09	0.957	AR coated
201-6-111	24.90(AR)	19.2	50.6	3.76	0.10	0.962	AR coated
202-9-111	17.10	12.8	36.3	3.43	0.09	0.787	AR coated
204-3-111	17.38	14.2	55.3	4.72	0.04	0.703	
194-1-111	17.86	23.9	78.8	4.58	0.08	0.711	
198-4-111	17.10	18.2	44.5	3.19	0.04	0.715	
217-2-111	16.00	9.53	34.8	3.19	0.06	0.746	
206-5-111	17.32	10.1	35.7	3.19	0.06	0.784	
208-11-111	17.42	12.13	30.2	3.11	0.04	0.828	H_2 sinter
SCIM no. 4		12.4	25.9	6.05	0.03	0.732	Electrolyte technique
214-3-111	17.02	18.5	61.4	2.73	0.06	0.790	
182-5-202	22.50	11.9	41.0	3.56	0.07	1.00	AR coated
218-12-111	19.78	17.3	43.5	3.26	0.06	0.915	No doping of melt, visible oxide
182-7-202	22.71	11.3	27.7	4.04	0.07	1.099	AR coated
214-6-211	17.08	16.1	39.3	5.54	0.04	0.788	H_2 sinter
215-9-111	16.38	11.4	31.1	2.12	0.06	0.770	H_2 sinter
193-15-2-3	(22.1 x 0.9) = 19.9	23.1	36.1	10.5	0.03	0.855	H plasma annealed, visible oxide
193-15-2-1	(22.29 x 0.9) = 20.1	27.2	58.9	9.41	0.02	0.899	H plasma annealed, visible oxide
192-4-4-4	(18.22 x 0.9) = 16.4	31.5	60.7	7.12	0.08	0.749	H plasma annealed no visible oxide

^aCalculated from 0.98 μ m scan.

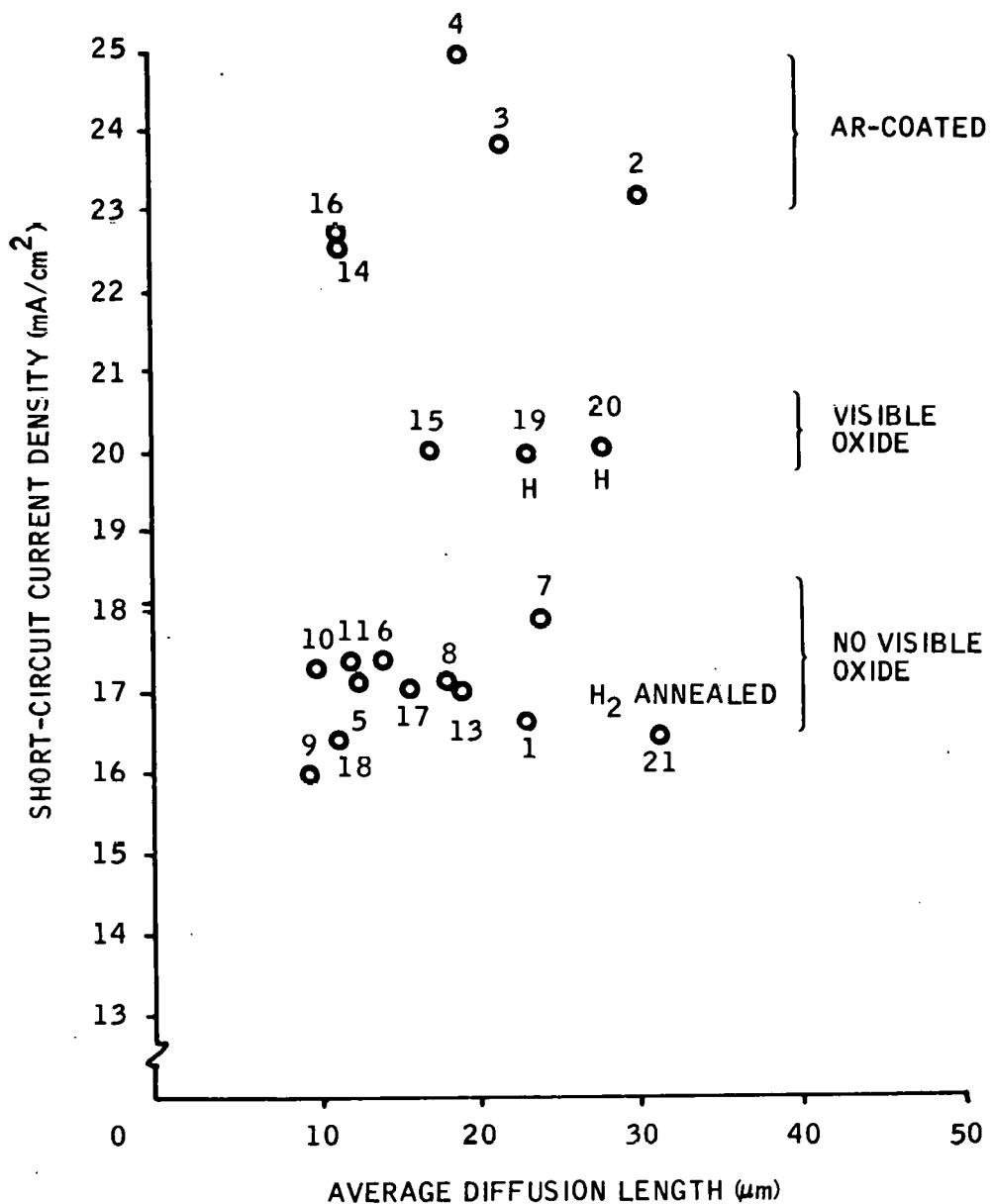


Figure 14. Correlation Between J_{sc} and I for SOC Solar Cells

strates had a visible oxide when viewed under the microscope. The LBIC results in Table 6 show the high value of $1 - R$ typical of such oxides.

Unfortunately, grain boundaries in the H-annealed samples still show a considerable recombination in the LBIC scans. Quantitatively, the effective diffusion length at the grain boundaries is perhaps $10 \mu\text{m}$, compared with 3 to $4 \mu\text{m}$ in untreated samples. Thus, partial passivation of grain boundaries occurs. Perhaps a modified treatment would produce improved passivation. In the meantime, evaluation of these cells will continue.

Crystallographic Texture Studies

During the quarter, metallographic examination of both dip-coated and SCIM-coated SOC material was continued. Figures 15 through 18 show typical cross sections of dip-coated material on slotted ceramic substrates grown at 0.06 cm/sec . The samples were polished and etched with Wright's etch to reveal defect structures.

Figure 15 shows a typical cross section in a slot, looking along the growth direction. In this orientation, a 30-minute Wright's etch is about optimum for revealing dislocation, twin planes, and grain boundaries as shown. In marked contrast, a cross section containing the growth axis shows no structure after a 30-second etch, and very little structure even after a 4-minute etch, as shown in Figure 16. This figure shows some SiC particles at the interface, very little carbon at the interface, and excellent contact between the silicon and ceramic. These are all typical features as noted in previous reports.

Figure 17 shows two cross sections at lower magnification so that the entire horizontal slot is shown. Both samples were etched for 4-minutes with Wright's etch, and the photographic exposure was adjusted to show the structure. No dislocations are visible. Some twin planes are visible in (b) but they must be intersecting the plane of the micrograph at very shallow angles because of the low contrast, even after the long etch. The arched shape of the silicon cross section is typical.

Figure 18 shows the surface of a SCIM-coated sample. The appearance is quite similar to that of dip-coated material. Figure 19 shows a cross section which is also quite similar to dip-coated material as seen by comparison with Figure 15. In both cases, the samples were etched with approximately the same as the sample in Figure 15. This substrate was non-slotted.

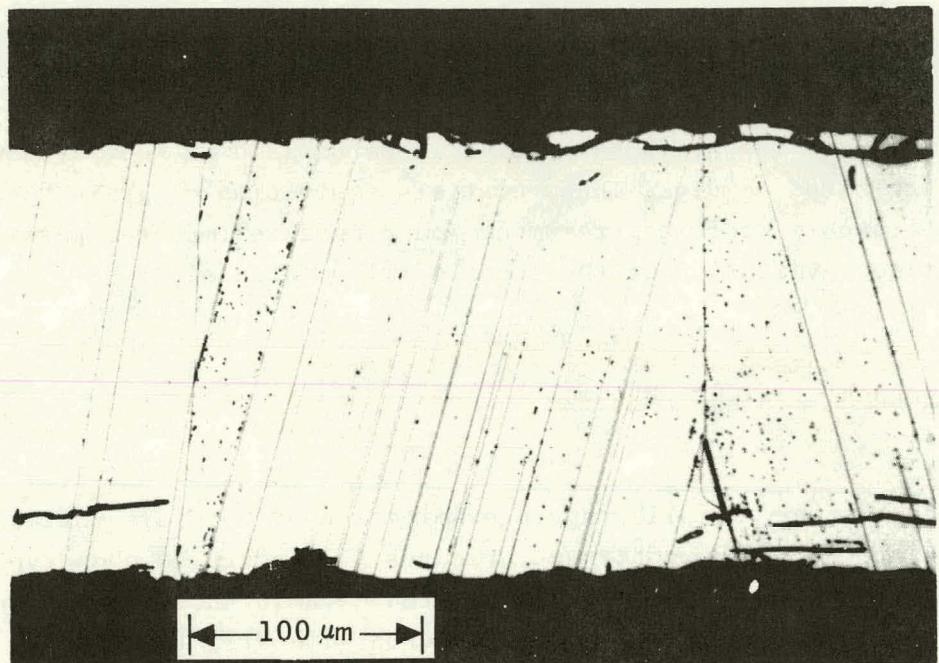


Figure 15. Cross Section of Dip-Coated Sample in Slot. Growth axis perpendicular to plane of micrograph. Thirty seconds of Wright's etch.

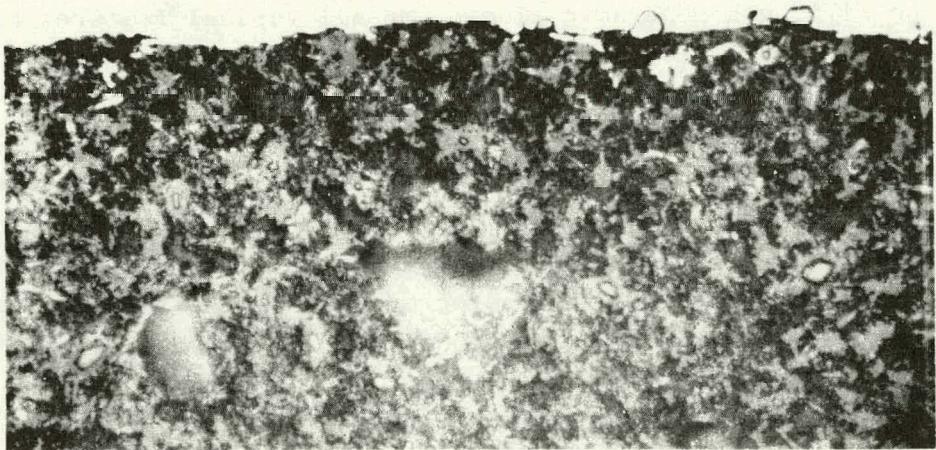
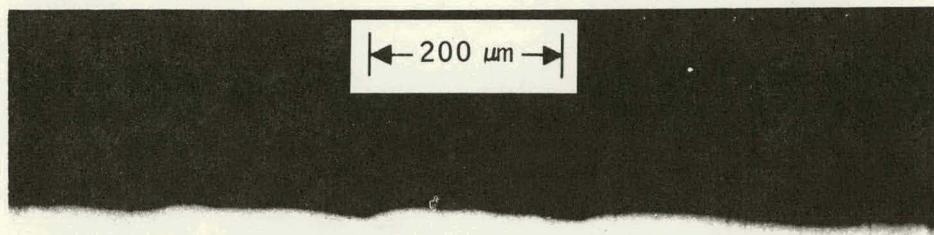
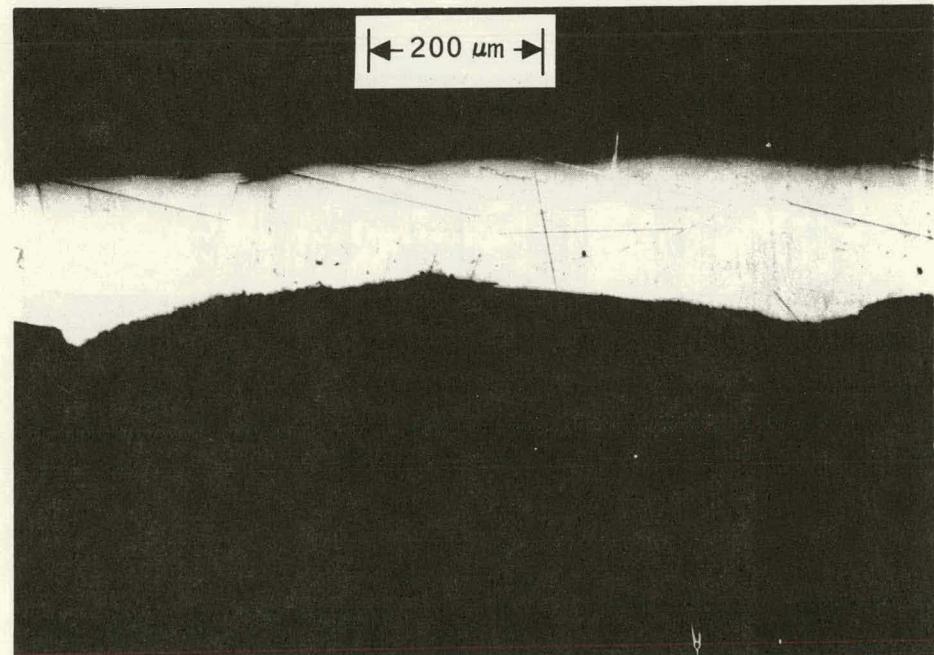


Figure 16. Cross Section of Dip-Coated Sample. Growth axis parallel to plane of micrograph. Four-minute Wright's etch.



(a)



(b)

Figure 17. Micrographs of Entire Cross Section
Across a Horizontal Slot

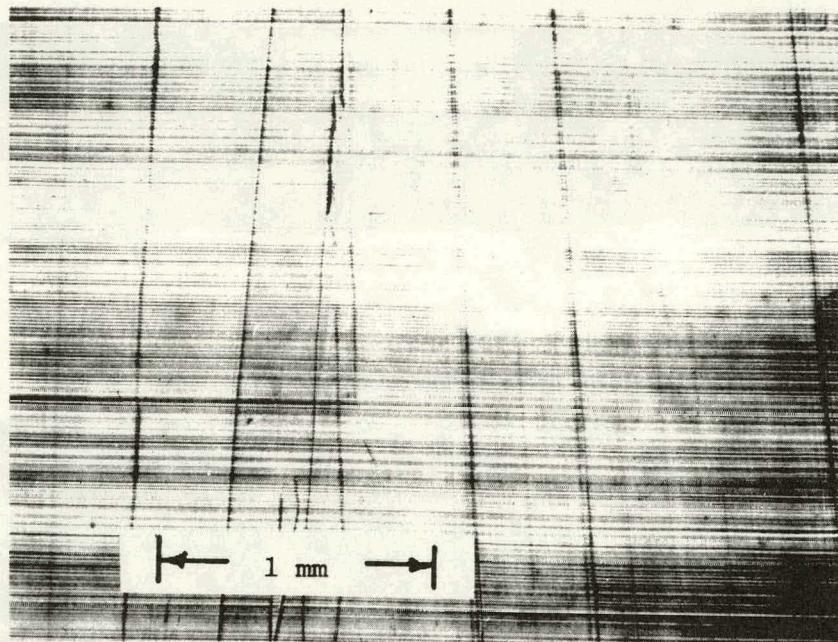


Figure 18. Surface of SCIM-Coated Sample

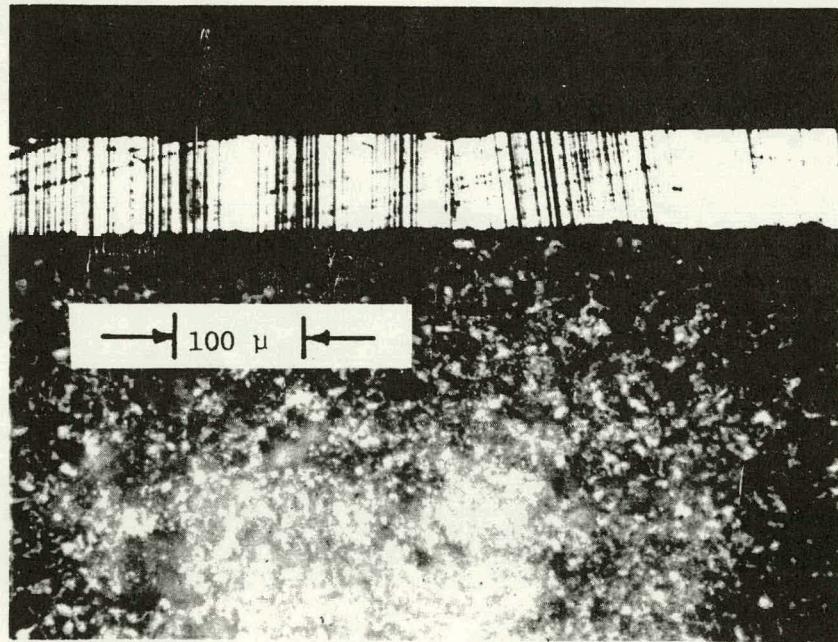


Figure 19. Cross Section SCIM-Coated Sample

In summary, the columnar crystallographic texture of SOC material has been found to result in highly anisotropic etching behavior. Dislocations, as well as twin planes and grain boundaries tend to lie in planes parallel to the growth axis and perpendicular to the substrates. Horizontal slots do not initiate nucleation, nor appear to influence the structure, other than to produce nonuniform thickness.

GROWTH MODELING (S.B. Schuldt)

The new SCIM coater is being designed to demonstrate continuous growth of sheet silicon on ceramic substrates. Any continuous SOC process poses some new thermal problems with respect to preheating the substrates and then cooling them after the silicon coating step. The preheating and cooling must be completed during times which are limited to the transit time through the heating and cooling portions of the apparatus. This constraint is absent in our experimental dip-coating procedure, which allows the operator to program the preheating and cooling times at his discretion. The most dramatic consequence of too rapid heating or cooling is substrate fracture due to excessive temperature gradients in the ceramic. The problem is best avoided by applying careful thermal analysis to the design of the SCIM-coating apparatus. This analysis is separate from the thermal analysis of SOC growth, which predicts the tradeoffs involving the silicon coating thickness, pull speed, and (in the case of supported growth) substrate thickness. The latter analysis has been applied to both unsupported and supported (SOC) silicon growth,¹ and will continue to be useful in the SCIM procedure.

Entrance Tunnel (Preheater)

The substrate panels are transported at ambient temperature to the entrance tunnel, which is shown in schematic gross section Figure 20. This is made up of pairs of active heaters, carbon guides (also functioning as the passive heaters), and insulating layers. The 1-mm-thick ceramic panels move left to right between the guides, acquiring heat by radiation from the guides, so that they reach 1693K when they arrive at the right end of the tunnel. At this temperature, the melting point of silicon, they are ready for silicon coating in the chamber, not shown, which would lie immediately to the right. It will be noted that the moving panels extract a total of $\rho C w t \Delta T$ joules of heat per centimeter of length, where ρ and C are the density and specific heat,

¹Chapman, P.W. et al., "Silicon-on-Ceramic Process," Annual Report No. 4, DOE/JPL 954356-79/3. Published 31 October 1979.

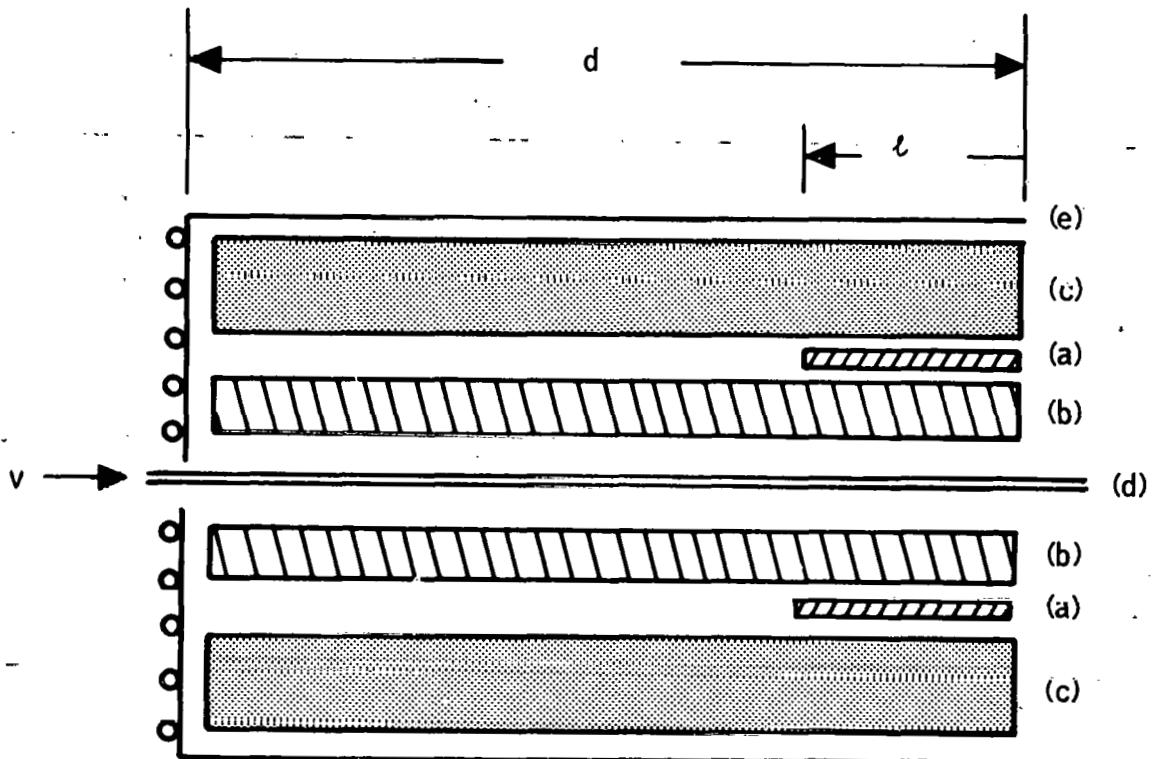


Figure 20. Vertical Section Through Coater Entrance Tunnel Showing (a) Active Heaters, (b) Passive Heaters (Guides), (c) Carbon Felt Insulation, (d) Substrate, and (e) Case

w and t are panel width and thickness, and ΔT is the temperature rise. If the panel feed rate is v cm/sec, the active heaters then must supply energy at a rate greater than $\rho C w t v \Delta T$ watts. The "greater than" may be made to approach "equal to" if wasted heat is minimized; that is, the quantity and placement of insulation are such as to prevent significant losses to the water-cooled case.

A gradient of 45 deg/cm has been determined to be the acceptable limit for 1-mm-thick ceramic below 850°C. Above this temperature, the material is more plastic and not as susceptible to thermal fracture; in fact, the cooling gradient just beyond the silicon solidification front ($\sim 1700K$) is known to be several hundred degrees per cm with no evidence of stress problems.

The total length, d , of the tunnel is constrained to be 17 inches, whereas the width, 13 inches, is large enough to justify the two-dimensional model illustrated in Figure 20. Heat flows from the active heaters into the carbon guides and then into the moving ceramic panels. Of interest is the steady-state temperature distribution in the guides and, in particular, in the ceramic. Although the ceramic actually slides along the top surface of the lower guide, the heat entering the ceramic is assumed to be radiative from the lower as well as the upper guide. Since the vertical separation between guides is only 0.5 inch, it is assumed that the radiative exchange between two surfaces is locally dominated; that is,

$$J = \iint f(T_i, T_j) dx dy \quad (5)$$

where T_i and T_j are temperatures at points opposite to one another on the two surfaces. This approximation, which avoids fourfold integration with a Green's function, becomes exact in the limit of vanishing separation between the surfaces. If ϵ_i and ϵ_j are the "total emissivities," the integrand function in (5) becomes

$$f(T_i, T_j) = \epsilon_{ij} \sigma (T_i^4 - T_j^4) \quad (6)$$

$$\text{where } \epsilon_{ij} = \epsilon_i \epsilon_j / [1 - (1 - \epsilon_i)(1 - \epsilon_j)] \quad (7)$$

Equation (7) is derived later. A further simplification is made, by using an average emissivity for the two ceramic surfaces rather than specifying a somewhat higher emissivity for the bottom surface, which is carbon-coated. This makes the calculation completely symmetric between the top and bottom halves of Figure 20, and only two temperature distributions need to be considered: $U(x)$ in the ceramic and $T(x)$ in both guides. Finally, the heat flux

density from each of the active heaters to its guide is assumed to be constant over the length, ℓ , of the heater:

$$H(x) = \begin{cases} 0 & 0 \leq x < d - \ell \\ 1/2 \rho C t v \Delta T / \ell & d - \ell \leq x \leq d \end{cases} \quad (8)$$

The required temperature distributions are the solutions of the coupled heat equations (G = guide and S = substrate):

$$\frac{d}{dx} \left(t_G k_G \frac{dT}{dx} \right) = f \left[\bar{T}(x), U(x) \right] - H(x) \quad (9)$$

$$\frac{d}{dx} \left(t_S k_S \frac{dU}{dx} \right) - \rho C v t_S \frac{dU}{dx} = -2f \left[T(x), U(x) \right] \quad (10)$$

with $U(d) = 1693K$ and $U'(d) = T'(d) = 0$.

The heat conductivity, k_G , was taken to be that of graphite:²

$$k_G \approx 2.0(300/T)^{0.592} \text{ W/cmK}$$

The boundary conditions give continuity of substrate temperature with the coating chamber temperature and also express the fact that thermal conduction between the entrance tunnel and the coating chamber is zero for both substrate and guides.

Solution profiles of U , T , and U' are shown for various design parameters in Figures 21 through 23. All are based on a 1-mm ceramic substrate and a heater length of $\ell = 3.5$ inches. The interesting feature is the dependence of the substrate temperature gradient on the panel feed rate, v , and guide thickness, t_G . Figure 21 shows that 0.5-inch guides are about right for a fast feed rate, $v = 2.5$ mm/sec. For a slow rate, $v = 1.0$ mm/sec, a much thinner guide should be used. Even with a 0.25-inch guide, as in Figure 22, the substrate heating is much too rapid at the beginning. As one might guess, the cure is to reduce the guide thickness still further. This increases the thermal resistance from the active heater to the left end of the passive heater, hence reducing the substrate heating rate there. Figure 23 shows a marked improvement using 0.19-inch guides. If a more uniform gradient were desired, one could experiment with the variable guide thicknesses in the solution (9) and (10).

²Truloukian, Y.S., Powell, R.W., Ho, C.Y. and Klemens, P.G., Thermophysical Properties of Matter, Vol. 1, IFI/Plenum, New York-Washington, 1970.

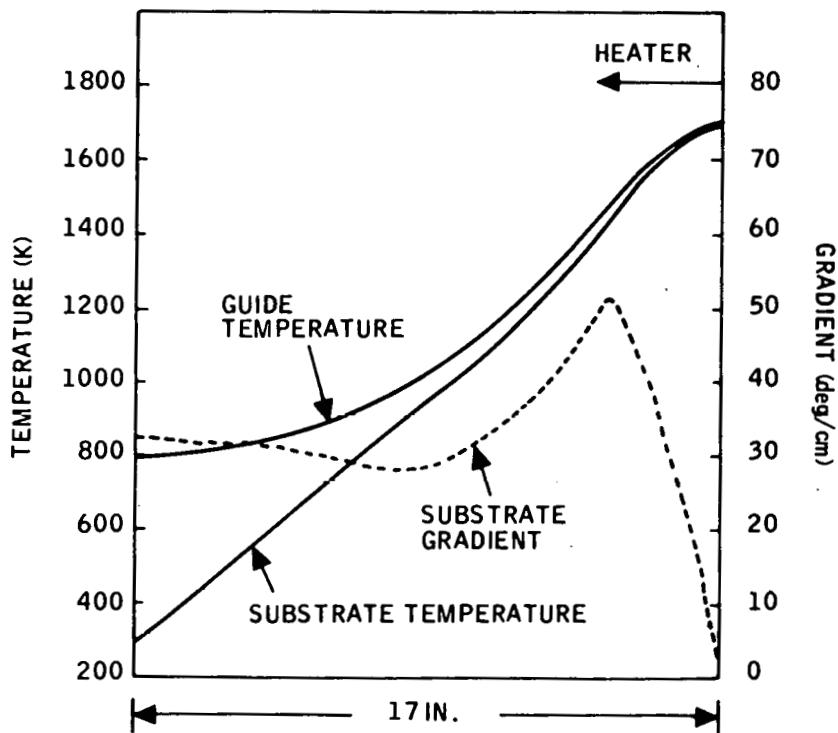


Figure 21. Steady-State Temperature Profiles in Entrance Tunnel (Substrate feed rate = 2.5 mm/sec, guide thickness = 0.5 inch)

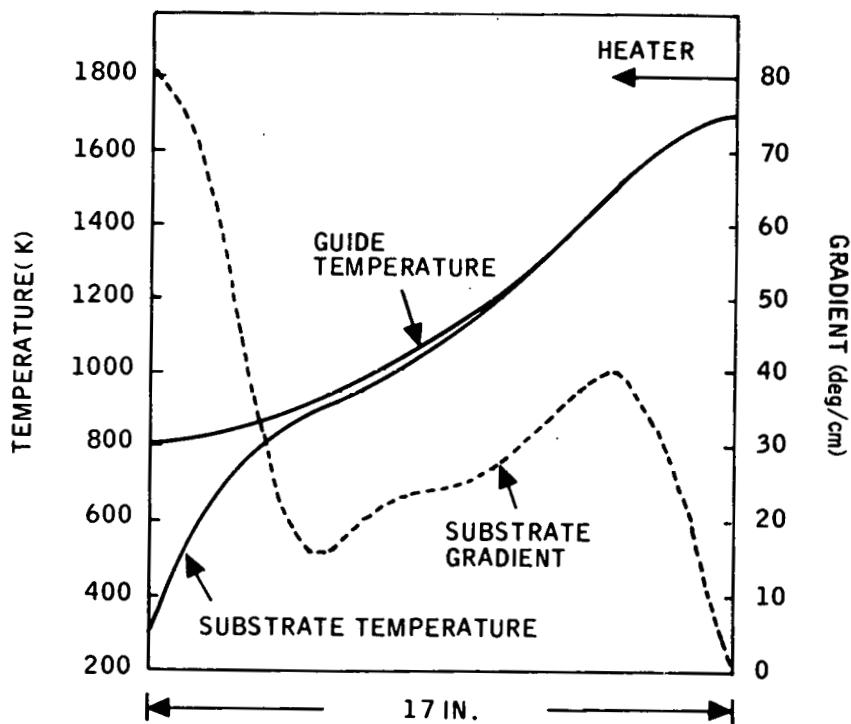


Figure 22. Steady-State Temperature Profiles in Entrance Tunnel (Substrate feed rate = 1.0 mm/sec, guide thickness 0.25 inch)

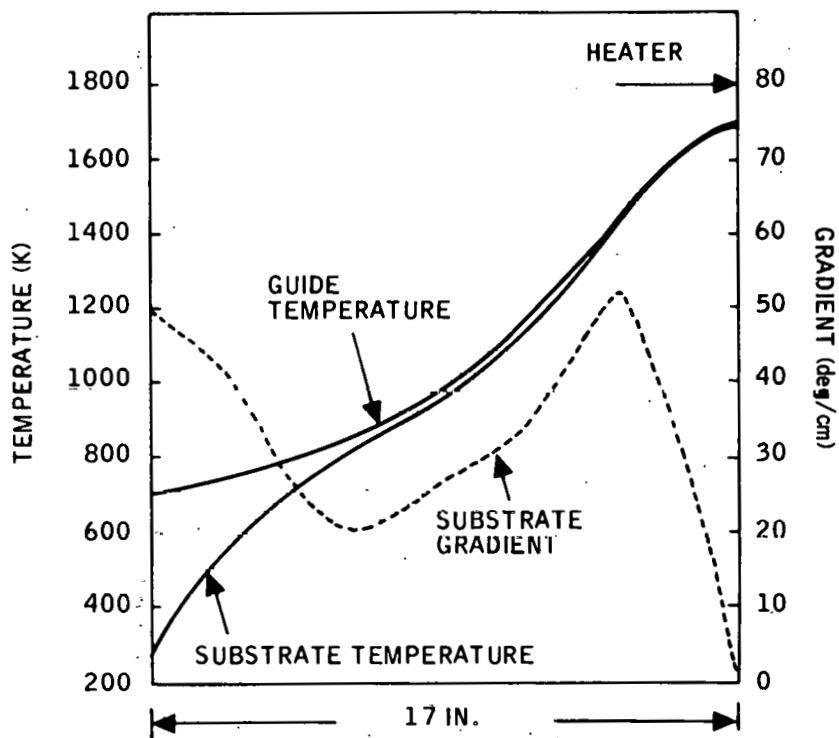


Figure 23. Steady-State Temperature Profiles in Entrance Tunnel (Substrate feed rate = 1.0 mm/sec, guide thickness = 0.19 inch)

Exit Tunnel

After the silicon-coating step, the panels traverse an exit tunnel (Figure 24) of similar geometry to the entrance tunnel. The important difference is the omission of the active heaters and the insulation. However, the water-cooled case is essential. Inasmuch as cooling is passive with the case being the heat sink, the carbon guides are a hindrance to cooling though needed for mechanical support. The guides act like heat shields interrupting the radiative transfer from silicon-coated panels to the case. In contrast to the entrance tunnel, the important heat escape path is vertical from panel to guide to case, with a minor contribution by way of longitudinal conduction through the guides. A simplified model is used which neglects the latter route. This allows the cooling equations to be decoupled, and the panel temperature distribution is given by the solution of the following equation (C = ceramic and S = silicon):

$$\frac{d}{dx} \left(A \frac{dU}{dx} \right) - Bv \frac{dU}{dx} = F(x, U) \quad (11)$$

where

$$A = t_C k_C + t_S k_S$$

and

$$B = \rho_C t_C C_C + \rho_S t_S C_S$$

The cooling function, $F(x, U)$, is given by

$$F(x, U) = (E_S + E_C) \sigma (U^4 - T_0^4) \quad 0 \leq x \leq d \quad (12)$$

$$F(x, U) = (\epsilon_S + \epsilon_C) \sigma (U^4 - T_0^4) \quad x > d \quad (13)$$

In Eq. (12), the effective emissivities of the silicon and ceramic surfaces are respectively E_S and E_C . In Eq. (13), the graybody emissivities ϵ_S and ϵ_C are used, since it is assumed that the background outside the tunnel is a blackbody at temperature T_0 . Inside the tunnel, the effective emissivities are reduced because of the heat-shielding effect of the guides, so that $E_S < \epsilon_S$ and $E_C < \epsilon_C$. Expressions for E_S and E_C are derived at the end of this section. Boundary conditions for Eq. (11) are $U(0) = 1693K$ and $U(\infty) = T_0$.

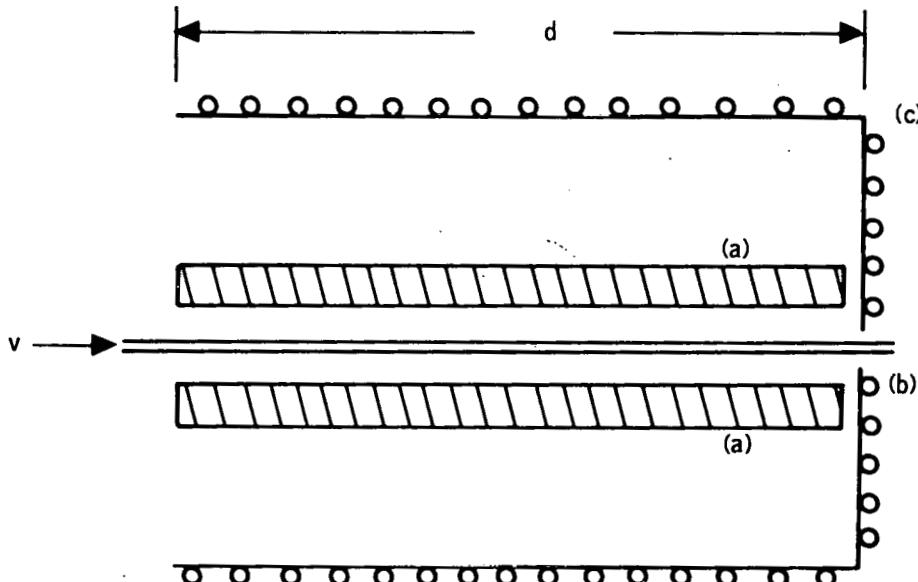


Figure 24. Vertical Section Through Exit Tunnel Showing
 (a) Carbon Guides, (b) Substrate, and (c)
 Water-Cooled Shoes

A good way to observe the heat-shielding effect is to compare the solution of Eq. (11) with and without the guides. For the latter, $F(x, U)$ is given by Eq. (13) for all x , and Eq. (12) is not used. Solution curves are shown in Figures 25 and 26 for $v = 2.5$ and $v = 1.0$ mm/sec. The tunnel length is 16 inches, and a 100- μm layer of silicon covers one surface of the substrate. The temperature gradient in Figure 26 is much higher than desired, around 140 deg/cm at 1123K (850°C). There are several ways to reduce the gradient, including insulating portions of the guides from the case. In order to estimate the improvement due to a design change, the model equations, (11) through (13) would have to be appropriately modified.

Derivation of $\epsilon_{ij} = \epsilon_i \epsilon_j / [1 - (1 - \epsilon_i)(1 - \epsilon_j)]$

As we shall see, this relation depends upon ϵ_i and ϵ_j being true graybody emissivities; that is, the emissivities have a flat spectrum over the wavelength range of appreciable thermal significance. This happens to be a good assumption for graphite³ but may be a poor one for other materials. On the other hand, we do not require temperature independence:

$$\frac{\partial \epsilon_k}{\partial \lambda} = 0, \quad \frac{\partial \epsilon_k}{\partial T} \neq 0 \quad k = i, j$$

For the moment, let ϵ_k^λ depend on both λ and T . Also let the spectral reflectivity, ρ_k^λ , depend on both λ and T .

Let the two infinite parallel surfaces be at temperatures T_i and T_j . By the usual definitions of spectral emissivity and reflectivity, we note that the spectral flux density incident on surface j is

$$J_j^\lambda = \epsilon_i^\lambda w_i^\lambda + \rho_i^\lambda J_i^\lambda, \quad (14)$$

where $w_i^\lambda \equiv w(T_i, \lambda)$, the spectral blackbody function. The first component of J_j^λ is flux emitted from surface i , and the second component is the flux reflected from surface i . Similarly,

$$J_i^\lambda = \epsilon_j^\lambda w_j^\lambda + \rho_j^\lambda J_j^\lambda \quad (15)$$

³Mantell, C.L., Carbon and Graphite Handbook, Interscience, New York, 1968, p. 344.

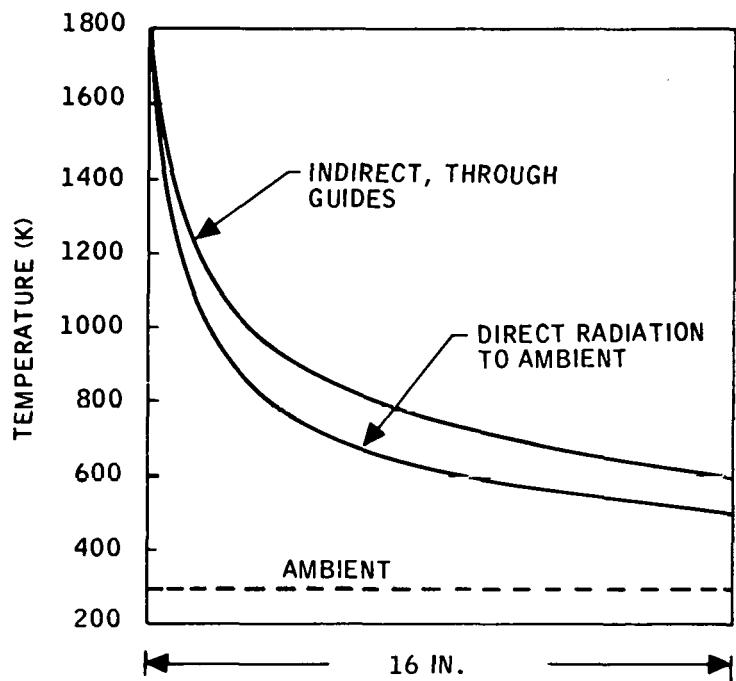


Figure 25. Steady-State Temperature Profiles of Coated Substrate in Exit Tunnel and Indirect Radiation to the Heat Sink (Substrate feed rate = 2.5 mm/sec)

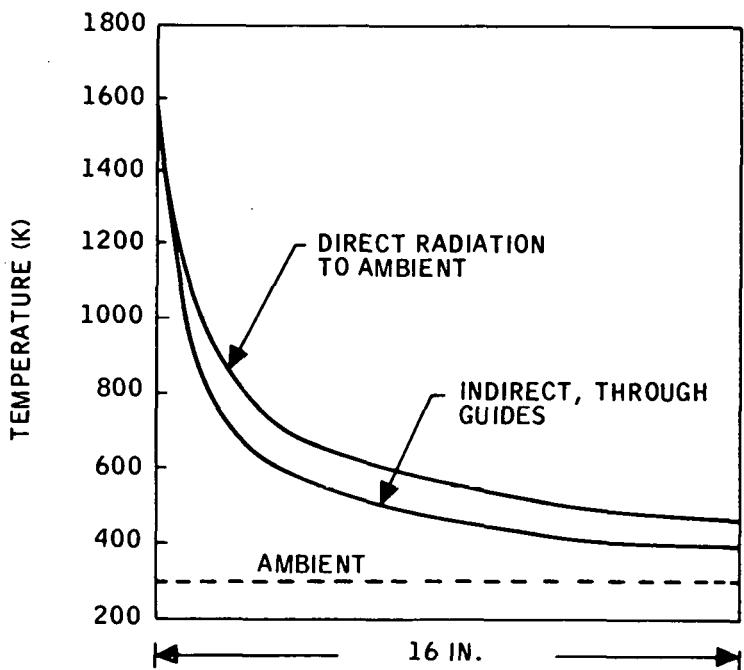


Figure 26. Steady-State Temperature Profiles of Coated Substrate in Exit Tunnel and Indirect Radiation to the Heat Sink (Substrate feed rate = 1.0 mm/sec)

These two equations may be solved for J_i^λ and J_j^λ and combined to give the net spectral flux density transferred from material i to material j:

$$J^\lambda = J_j^\lambda - J_i^\lambda = \frac{\epsilon_i^\lambda (1 - \rho_j^\lambda) w_i^\lambda - \epsilon_j^\lambda (1 - \rho_i^\lambda) w_j^\lambda}{1 - \rho_i^\lambda \rho_j^\lambda} \quad (16)$$

For the parameters ϵ_j^λ and ρ_j^λ to make any physical sense, they should not depend on the properties of surface i. In particular, let $T_i = T_j$ so that the surfaces are in thermal equilibrium. By the detailed balance principle, $J^\lambda = 0$.

Also assume that material i is a blackbody so that $\epsilon_i^\lambda = 1$ and $\rho_i^\lambda = 0$. It follows that

$$J^\lambda = 0 = (1 - \rho_j^\lambda - \epsilon_j^\lambda) w_j^\lambda$$

In other words, $\rho_j^\lambda \equiv 1 - \epsilon_j^\lambda$. Since the argument is symmetrical, it also follows that $\rho_i^\lambda \equiv 1 - \epsilon_i^\lambda$. Equation (16) may now be rewritten as:

$$J^\lambda = \frac{\epsilon_i^\lambda \epsilon_j^\lambda}{1 - (1 - \epsilon_i^\lambda)(1 - \epsilon_j^\lambda)} (w_i^\lambda - w_j^\lambda) \quad (17)$$

The total radiation transfer, $J = \int J^\lambda d\lambda$, is given by:

$$J = \frac{\epsilon_i \epsilon_j}{1 - (1 - \epsilon_i)(1 - \epsilon_j)} \cdot \sigma (T_i^4 - T_j^4)$$

only if $\epsilon_i^\lambda = \epsilon_i$ and $\epsilon_j^\lambda = \epsilon_j$, independent of λ . However, it was not necessary to assume that ϵ_i and ϵ_j are independent of the respective temperatures.

Expressions for Effective Emissivities E_S and E_C

We need an expression for the net radiative transfer from a surface at temperature $T_2(x)$ through a heat shield at temperature $T_1(x)$ to a heat sink at temperature T_0 . Since the vertical spacing (see Figure 27) between the high-temperature surface and the heat shield is small, we again assume only local temperatures are important:

$$J(x) = \epsilon_{12} \sigma \{ [T_2(x)]^4 \} - [T_1(x)]^4 = \epsilon_{10} \sigma \{ [T_1(x)]^4 - T_0^4 \} \quad (18)$$

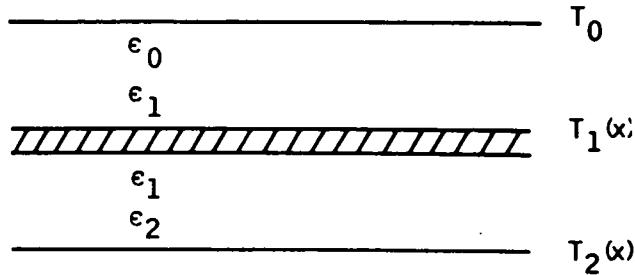


Figure 27. Radiative Transfer

where

$$\epsilon_{12} = \epsilon_1 \epsilon_2 / [1 - (1 - \epsilon_1)(1 - \epsilon_2)]$$

and

$$\epsilon_{10} = \epsilon_1 \epsilon_2 / [1 - (1 - \epsilon_1)(1 - \epsilon_0)]$$

The quantity $[T_1(x)]^4$ can be eliminated from (18) to give

$$\begin{aligned} J(x) &= [\epsilon_{12} \epsilon_{10} / (\epsilon_{12} \epsilon_{10})] \sigma \{ [T_2(x)]^4 - T_0^4 \} \\ &= E_2 \sigma \{ [T_2(x)]^4 - T_0^4 \} \end{aligned} \quad (19)$$

For example, taking

$$\epsilon_0 = 1.00 \text{ (heat sink)}$$

$$\epsilon_S = 0.46 \text{ (silicon)}$$

$$\epsilon_C = 0.71 \text{ (ceramic)}$$

$$\epsilon_G = 0.80 \text{ (graphite)}$$

we find

$$\epsilon_{SG} = \epsilon_S \epsilon_G / [1 - (1 - \epsilon_S)(1 - \epsilon_G)] = 0.39$$

$$\epsilon_{CG} = \epsilon_C \epsilon_G / [1 - (1 - \epsilon_C)(1 - \epsilon_G)] = 0.60$$

$$\epsilon_{GO} = \epsilon_G \epsilon_0 / [1 - (1 - \epsilon_G)(1 - \epsilon_0)] = 0.80$$

$$E_S = \epsilon_{SG} \epsilon_{GO} / (\epsilon_{SG} + \epsilon_{GO}) = 0.26$$

$$E_C = \epsilon_{CG} \epsilon_{GO} / (\epsilon_{CG} + \epsilon_{GO}) = 0.34$$

The graphite barrier reduces the effective emissivity of silicon from 0.46 to 0.26 and the effective emissivity of ceramic from 0.71 to 0.34.

CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

From the work performed during the quarter, we conclude that:

- Changing argon gas flow rates in the dip coater has little effect on the structure of the silicon.
- Deeper diffusions provide higher conversion efficiencies in SOC material.
- Initial SCIM material produce photodiode results very similar to dip-coated material.
- The short-circuit current is the main area needing improvement in order to significantly improve SOC solar-cell performance.
- Processing which maximizes grain boundary gettering should improve SOC cell performance.
- Hydrogen plasma-annealed samples processed at Sandia indicate partial passivation of grain boundaries.
- Dislocations, twin planes, and grain boundaries tend to lie in planes parallel to the growth axis and perpendicular to the substrates in SOC material.
- Horizontal slots do not initiate nucleation nor appear to influence structure other than to produce nonuniform thickness in SOC material.
- Analysis indicates that substrate guide thicknesses at the entrance tunnel of the new SCIM coater should vary with substrate travel speed.

RECOMMENDATIONS

Recent indications are that SOC solar cells have better performance when doped to a concentration of 5×10^{16} atoms/cm³ and diffused at 850°C for 80 minutes. We therefore recommend that these become our standard diffusion processing techniques.

PROJECTION OF FUTURE ACTIVITIES

Future activities are projected as follows:

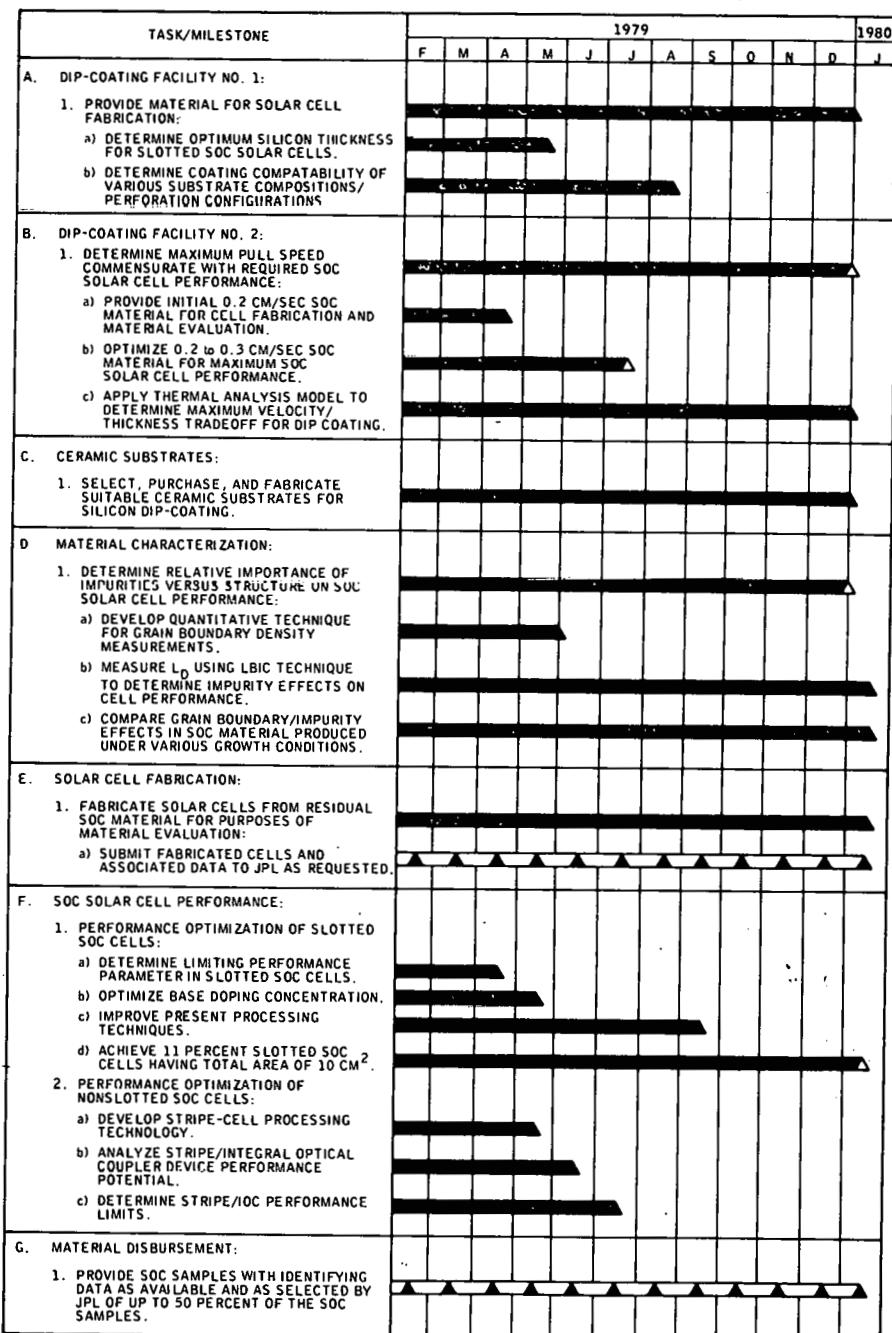
- Ceramic substrates made of a mixture which closely matches the thermal expansion coefficient of silicon will be dipped.
- Experiments will be conducted to determine whether the application of an electric field can inhibit transport of impurities from the ceramic substrate to the melt.
- Modifications to the experimental dipper will be completed so as to provide "fast" dipped (0.2 to 0.3 cm/sec) material for cell evaluation.
- Modified diffusion conditions will be incorporated in our cell processing activity to raise the overall efficiency of SOC solar cells.
- More SCIM-coated material will be processed into photodiodes.
- A new SCIM (continuous) coating facility will be designed and fabricated.
- Work will continue to evaluate the effects of H_2 plasma annealing on SOC solar-cell performance.
- Thermal annealing studies will begin an attempt to improve SOC solar-cell performance.
- Thermal/growth modeling activities will continue to support the design and construction of our new continuous coating facility.

NEW TECHNOLOGY

There were no reportable "new technology" items uncovered during this reporting period.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 28, 29, and 30, respectively.



NOTE: IN ADDITION TO THE ABOVE PROGRAM PLAN, THE HONEYWELL CORPORATE TECHNOLOGY CENTER WILL PROVIDE THE REQUIRED DOCUMENTATION, ATTEND THE REQUIRED MEETINGS AND DELIVER THE REQUIRED SAMPLES AS PER CONTRACT AGREEMENT.

▲ PLANNED
▲ ACCOMPLISHED GOALS

Figure 28. Updated Program Plan

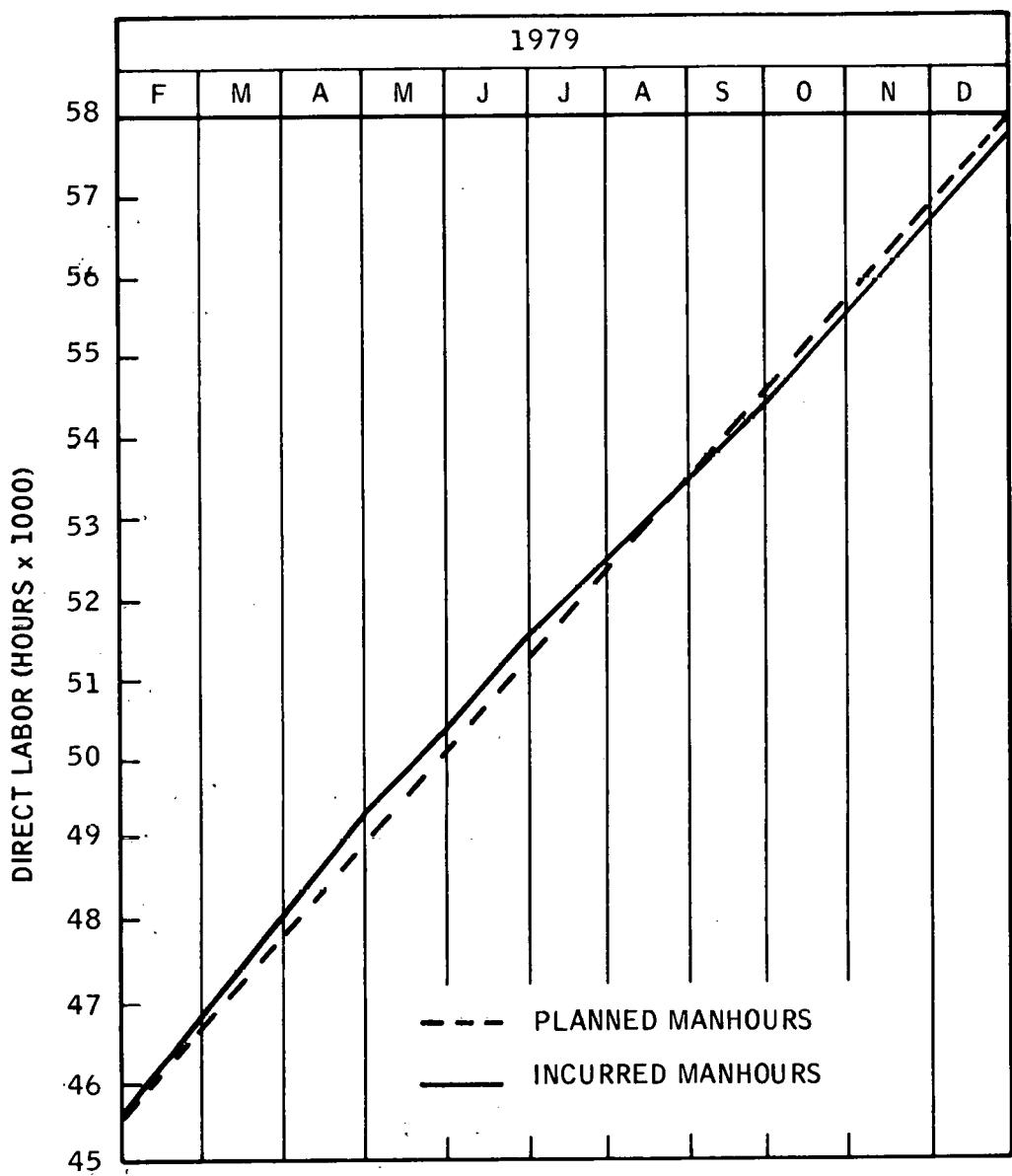


Figure 29. Updated Program Labor Summary

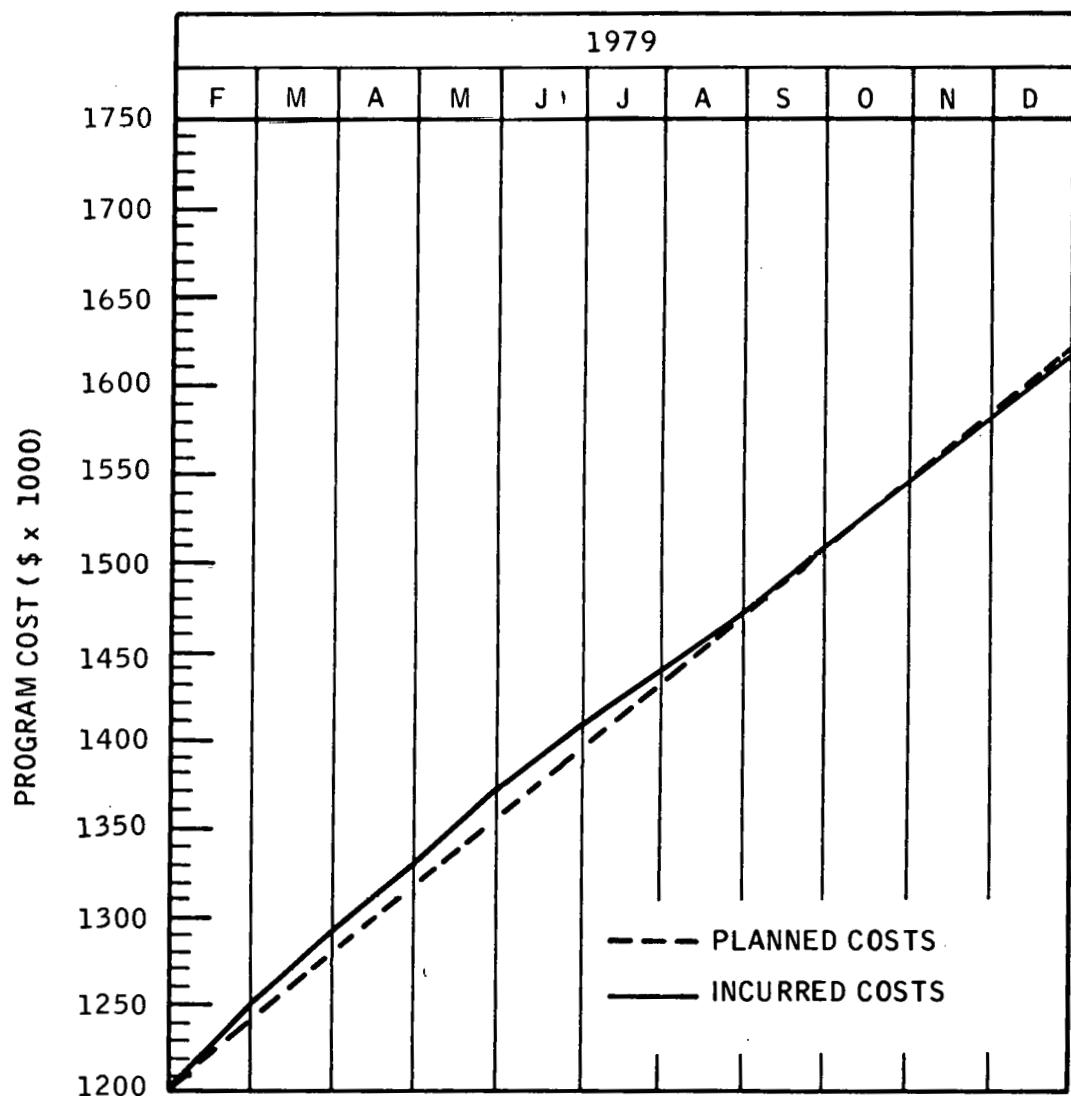


Figure 30. Updated Program Cost Summary

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1. Chapman, P.W. et al., "Silicon-on-Ceramic Process," Annual Report No. 4, DOE/JPL 954356-/79-3.
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* U.S. GOVERNMENT PRINTING OFFICE: 1980-640-258/2330