LATCH-UP ELIMINATION IN BULK CMOS LSI CIRCUITS*

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Latch-up prevention in CMOS LSIs requires a more fundamental understanding of the SCR phenomena, especially as LSI structures become more prone to latch-up due to reduced geometries. In this paper we will present recent data on latch-up prevention by the use of epitaxial starting material, present a modification of the lumped transistor-SCR model and describe a useful graphical solution to the latch-up problem.

Latch-up characteristics of parasitic SCRs have the general features shown in Figure 1. Region I corresponds to the normal operational region of the CMOS circuits where the parasitic SCR is in its blocking state. It extends from the origin to Point I. Region II corresponds to the latch-up status where regeneration occurs. It is characterized by a large drop in terminal voltage from that at point I, and by the flow of large terminal currents. This region extends to Point III at which point latch-up is no longer sustained due to a reduction in device current gain with large currents. The terminal voltage increases as the devices exit saturation. Basically, latch-up is prevented if operation in Region II is not allowed. This has been accomplished in deep p-well structures (> 7 microns) by minority lifetime reduction methods of gold doping (1) and neutron irradiation (2). The use of epitaxial substrates has also been shown to prevent latch-up by increasing the holding current to levels unatainable in normal circuit operation (3).

The present work differs from that in Reference 3 by including the dependence of transistor current gain on collector current. The effect, a result of increasing the holding current sufficiently by decreasing the shunt parasitic resistances R_S and R_W in Figure 2, is that the loop gain becomes less than unity prior to reaching the holding current and therefore preventing latch-up.

From Figure 2, we write

$$I_{c_p} \geq I_{R_w} + I_{c_n}/\beta_n \qquad (1)$$

$$I_{c_n} \geq I_{R_s} + I_{c_p}/\beta_p \qquad (2)$$

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The current gains β_n and β_p are functions of collector current. The inequalities are written to include the saturation regions.

These equations are plotted in Figure 3 where the β dependence was obtained from measurements of test devices on the CMOS LSI shown in Figure 4. Curve A is obtained by plotting I_{c_p} versus I_{c_n}/β_n, I_{c_n} being the independent variable; curve B is I_{c_n} versus I_{c_p}/β_p with I_{c_p} the independent parameter. The allowed regions of operation defined by the inequalities of Equations 1 and 2 is that space above A and below B. The allowed region of operation of the coupled pair of equations is the overlap area designated II in Figure 3. Point 1 defines the onset of saturation. The holding current determined from this point is

$$I_H = \frac{I_{RW}\ \beta_n\ (\beta_p + 1) + I_{RS}\ \beta_p\ (\beta_n + 1)}{\beta_n\ \beta_p - 1} \qquad (3)$$

in agreement with Reference 3. Point III represents the current level at which the devices go out of saturation.

The intercepts along the axis are the shunt currents flowing through R_s and R_w. Decreasing R_s moves curve B to the right; decreasing R_w moves curve A up. This results in a larger holding current, a lower latch-up exit current and a smaller overlap region where SCR action is allowed. It is obvious that, by proper selection of R_s and/or R_w, the curves will not intersect; under these conditions latch-up is impossible at any current level. Curve C in Figure 3 shows a shift of curve B due to the reduction in R_s afforded by the use of epitaxial substrate from a value of $\sim$100 Ω to $<$15Ω which prevents latch-up.

The CMOS LSI circuit shown in Figure 4 was fabricated on both conventional and n on n+ epitaxial substrates. While in the standard structure latch-up was induced by a $\dot{\gamma}$ pulse of $\sim 10^9$ rad (Si)/sec, no latch-up was induced in the epi-structure at fluences of up to $\sim 6 \times 10^{10}$ rad (Si)/sec (4). Further, no electrically induced latch-up could be attained so long as the epi-shunt resistors were not removed from the circuit.

In addition to the discussion of the model, sensitivities for latch-up due to process variations such as epi thickness and p-well depth and resistivities will be discussed. Possible effects due to scaling will also be presented.

References

1) Dawes, W. R., and Derbenwick, G. F., IEEE Trans. on Nuclear Science, NS-23 pp. 2027-2030, December 1976.

2) Adams, J. R., and Sokel, R. J., IEEE Trans. on Nuclear Science, NS-26 pp. 5069-5073, December 1979.

3) Ochoa, A., Dawes, W. R., and Estreich, D., IEEE Trans. on Nuclear Science, NS-26 pp. 5065-5068, December 1979.

4) Abare, W., Private Communication, Harris Semiconductor.

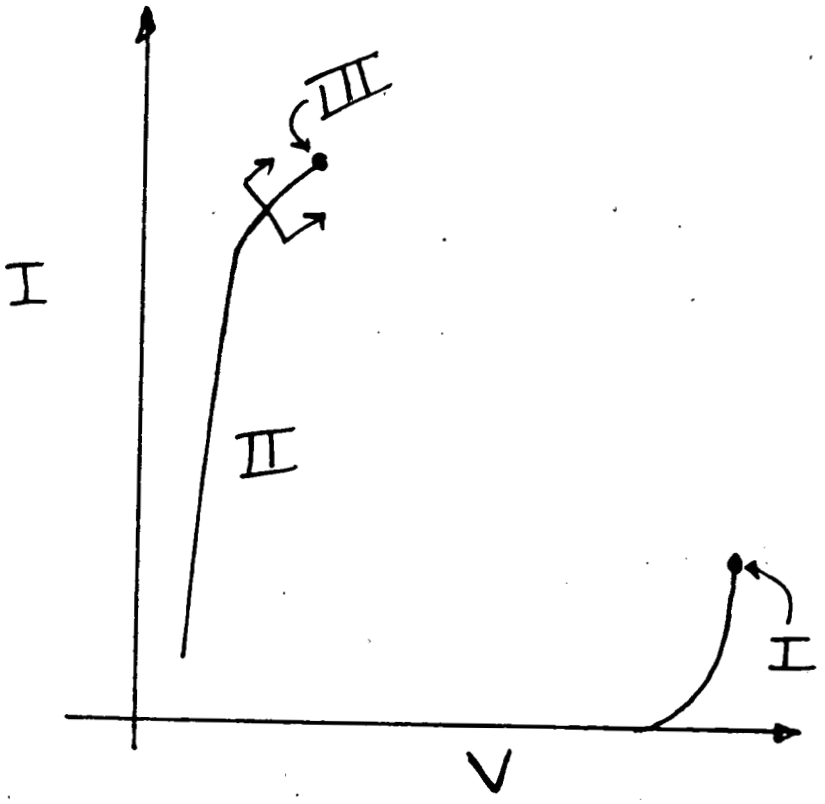

Figure 1: Current vs. Voltage relation for typical SCRs showing major regions of operation.

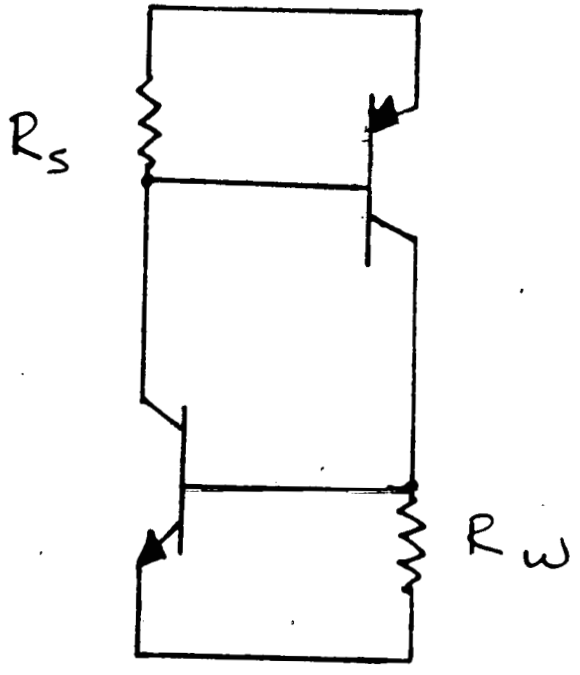

Figure 2: Lumped element model for parasitic SCRs in Bulk CMOS structures.

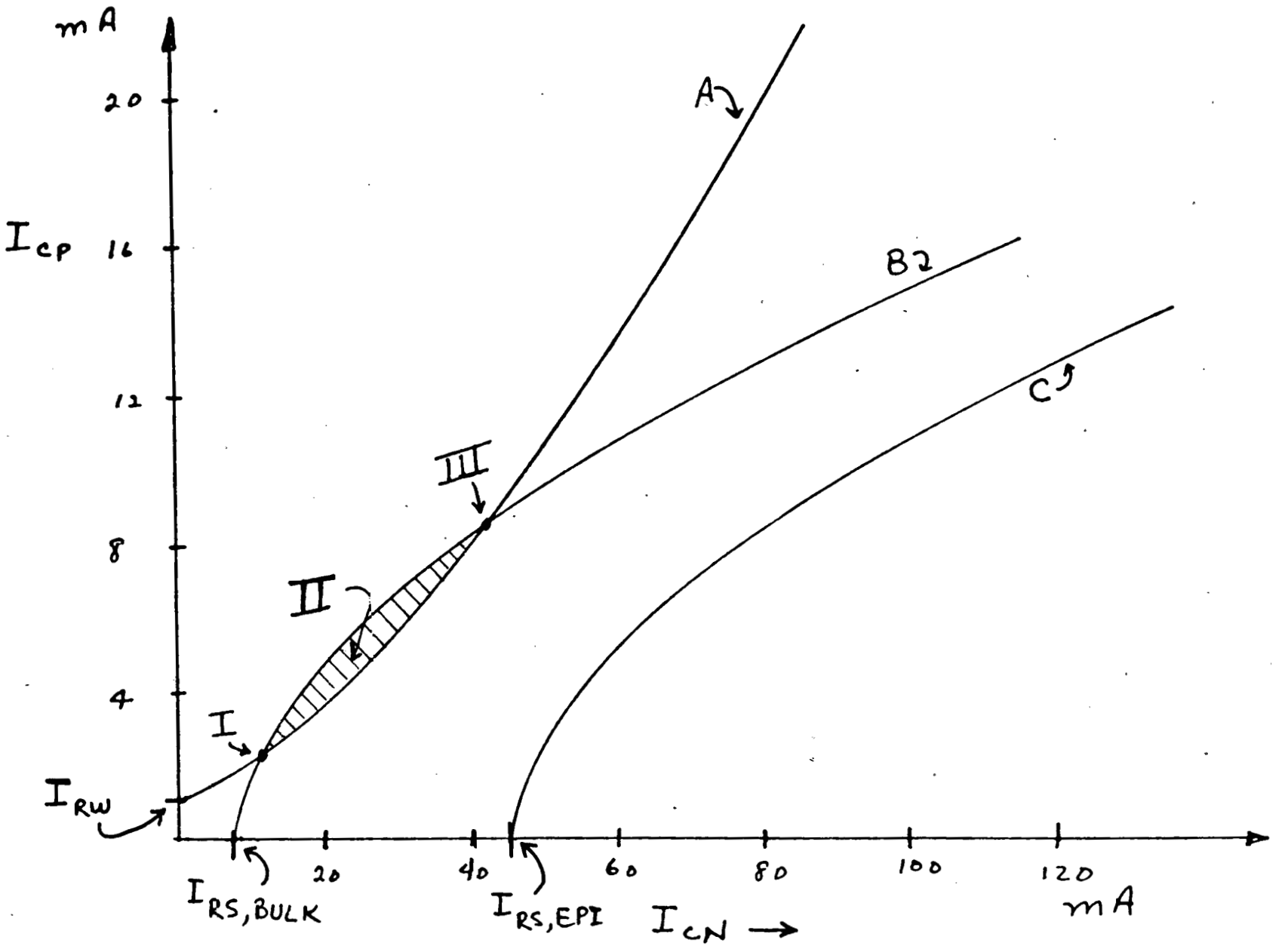

Figure 3: Current characteristics of parasitic bipolar transistors as given by inequalities 1 and 2.

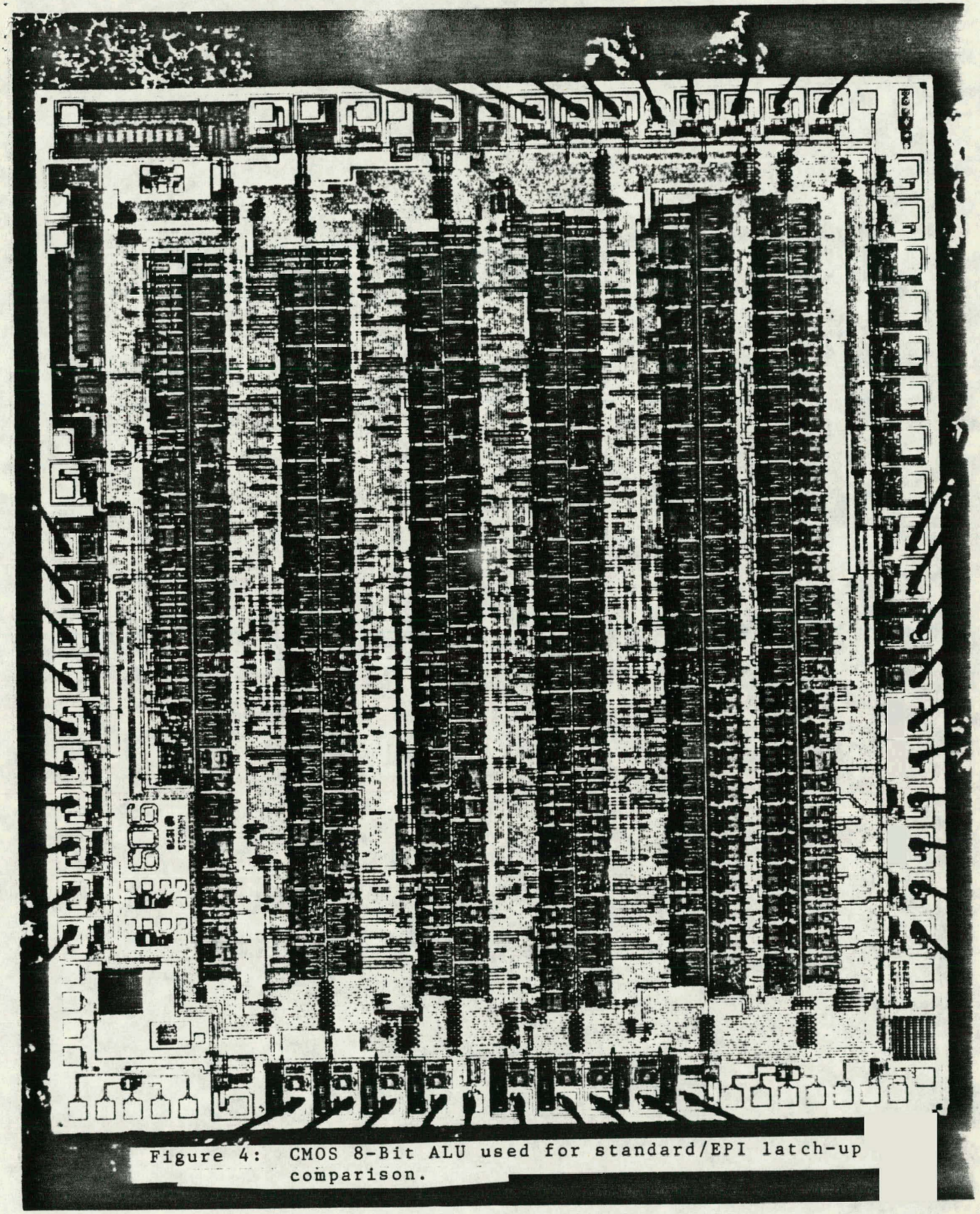

Figure 4: CMOS 8-Bit ALU used for standard/EPI latch-up comparison.