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THERMIONIC INTEGRATED CIRCUITS: ELECTRONICS FOR HOSTILE ENVIRONMENTS

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ABSTRACT

Thermionic integrated circuits combine vacuum tube technology with integrated circuit techniques to form integrated vacuum triode circuits. These circuits are capable of extended operation in both high-temperature and high-radiation environments.

INTRODUCTION

Thermionic integrated circuits (TICs) combine thermionic emission of vacuum tube technology with the thin-film deposition and photolithographic delineation techniques of conventional silicon integrated circuits to form microminiature-integrated vacuum triode circuits. The resulting integrated circuits are extremely tolerant to both high-radiation and high-temperature environments.^{1,2}

TIC STRUCTURE AND PROCESS

A typical single TIC device is shown in Fig. 1. The grid and cathode are shown on the lower heated insulating substrate, and the anode is shown on the upper heated substrate. As in a standard triode, the cathode emits electrons, the anode collects electrons, and the grid provides gain by modulating the electron flow. The typical vacuum triode $v - i$ characteristics of this device are shown in Fig. 2.

The TIC process is a simple, high-yield process, capable of producing a high-component density. The process uses four masking steps to photolithographically delineate thin films of refractory metals and cathode material deposited on insulating substrates. The cathode-coating technique was developed by Geppert, Dore, and Mueller at the Stanford Research Institute in 1969.³ This technique uses a standard oxide cathode coating mixed with photoresist. The cathode can then be delineated photolithographically.

Figure 3 shows a side view of the TIC metalization on the circuit side of the substrate (on the opposite side of the substrate is a resistive heater used to maintain the 750°C operating temperature of the TIC). Currently sapphire is used for the substrate; however, as explained in the radiation section the polycrystalline structure of alumina offers advantages in high-radiation environments.

All the metals used are refractory because of the high-temperature operation. The base metal under the cathode is tungsten since this provides a long lived cathode. On the other hand, titanium base metal produces a short lived cathode. Titanium is used on the surface of all the other electrodes since it inhibits spurious emission if cathode coating is inadvertently present. The bond pads are platinum since platinum bond wires are used. The titanium under the bond pad enhances adherence to the sapphire substrate.

TIC DEVICE CHARACTERISTICS

The structure of Fig. 1 is similar to that of a conventional triode. The anode is in the natural path of the electrons and the closely spaced grid cathode structure maximizes grid control. The TIC device is much like a standard triode but with the grid moved down into the plane of the cathode. The characteristics shown in Fig. 2 also suggest that the TIC device behaves much like a conventional triode. In fact, it has been shown with computer simulation, and experimentally verified that, with some modification, the conventional triode equation can be used to describe the performance of a TIC device.

The modification arises because there are many devices on each substrate pair. The electrode potentials of one device can interact with another device by modulating its cathode current. The modified triode characteristics, which include the interactions, are given by

$$I_p = k(V_G + V_p/\mu + \lambda V_S/\mu_S)^{3/2} \quad (1)$$

where

I_p = anode current

k = perveance

v_G = grid-to-cathode voltage
 v_P = anode-to-cathode voltage
 v_S = interaction electrode to cathode voltage
 μ = triode amplification factor
 μ_S describes the effect of electrode S on the device characteristics

The standard triode equation includes only the first two terms inside the parentheses of Eq. (1), the $\sum v_S/\mu_S$ terms model the electrostatic interactions. The amplification factor, μ , describes the relative influence of the grid and anode and is the maximum voltage gain of the device (the open circuit voltage gain). The μ_S terms describe the relative influence of the interaction electrode and the grid.

While improvements will certainly be made in the future, Eq. (1) has proved to be an important TIC device model. It has been used to analyze simple TIC circuits and has provided insight into the effects of device interactions on circuit gain and bias levels. Once this model is incorporated into a circuit simulation program such as SPICE, more complicated TIC circuits can be analyzed.

HIGH-TEMPERATURE OPERATION

TIC devices have been operated in ambient temperatures of 500°C for over 13 000 hours. The longest-lived device showed no degradation in device characteristics just before failure; device failure resulted from oxidation of a pin seal on the package causing air to leak into the vacuum. That is, lifetime was determined by a package failure.

The 500°C temperature is not a fundamental limit for TIC devices, but is a limit of current packaging technology. With the development of better gettering techniques and better packaging techniques, longer lifetimes and higher temperature operation can be expected.

OPERATION IN RADIATION ENVIRONMENTS

Under funding from the Department of Energy, Office of Basic Energy Sciences, the TIC program has been directed primarily toward high-temperature operation, although a limited number of radiation tests have been performed on single active devices and on different electrode configurations.

Active devices were tested to total dose levels of 10^{17} n/cm² and 2.5×10^8 Rad (Si) gamma in a Triga Reactor at the University of Arizona. During these tests the devices were active and were continuously monitored for changes in characteristics. The devices showed no degradation in either case; the tests were terminated because of reactor time constraints. The Triga reactor was also used to test to 1.4×10^{16} n/cm²/s, again with no degradation.

TIC devices were tested to dose rates of 4.5×10^{10} Rad (Si)/s gamma at the Air Force Weapons Laboratory (AFWL) Febetron and to 2×10^8 Rad (Si)/s protons at the Weapons Neutron Research Facility of the Los Alamos National Laboratory. These tests showed no permanent degradation, but did show transient effects with an immediate return to normal operation. These results are summarized in the following Table.

THERMIONIC INTEGRATED CIRCUIT OPERATION IN HOSTILE ENVIRONMENTS

High Temperature	500°C For Over 13,000 Hours, Pin Seal
Total Radiation Dose - <u>Tested To</u>	10^{17} neutron/cm ² , No Degradation 2.5×10^8 Rad(Si) (gamma), No Degradation
Radiation Dose Rate - <u>Tested To</u>	4.5×10^{10} Rad(Si)/sec (gamma) 2×10^8 Rad(Si)/sec (proton) 1.4×10^{16} n/cm ² /sec
Projected Upset Level	4×10^{11} Rad(Si)/sec (gamma)

Because the total dose tests produced no observable degradation in the TIC characteristics and because the initial dose rate tests showed transient effects, effort was concentrated on analyzing, measuring, and understanding the dose rate response. Specifically, the goals were to

- o Gain an understanding of the dose rate response mechanisms by analyzing a number of device and electrode configurations and then conducting measurements to verify the analyses.

- o Design structures that would have reduced responses and then verify that the responses are indeed reduced.
- o Project the dose rate tolerance of a TIC flip-flop when improved substrate and device structures are used.

Photon Interactions. The photon energies produced by the AFWL Febetron are in the 1 MeV range. In this energy range the dominant interaction mechanism is the Compton scattering of photons by electrons. Compton scattering imparts energy to the electrons; the average motion of these electrons is in the direction of the incident photons. Thus, there is a net transport of negative charge in the direction of the photons which produces a dose rate response in the TIC electrodes.

For a thin sample of material in a photon beam, approximately one electron is ejected for each captured photon. Then the ejected charge is

$$q = eN_e \approx e\Delta p = ep\mu x \quad \text{C/cm}^2 \quad (2a)$$

$$= \frac{\mu x \gamma_1}{E_p (\mu_1/p_1)} 10^{-5} \quad \text{C/cm}^2 \quad (2b)$$

where

$$\begin{aligned} e &= 1.602 \times 10^{-19} \text{ C} \\ N_e &= \text{ejected electrons/cm}^2 \\ \Delta p &= \text{photons removed/cm}^2 \\ p &= \text{incident photons/cm}^2 \\ \mu &= \text{photon absorption coefficient (cross section), cm}^{-1} \\ x &= \text{material thickness, cm} \\ \gamma_1 &= \text{dose in rads (material 1)} \\ E_p &= \text{energy of incident photons, eV} \end{aligned}$$

The subscript 1 in Eq. (2b) indicates the reference material (e.g. silicon).

The thin electrodes should have much less effect than the much thicker substrate. For 1 MeV photons the charge ratio for 5000 Å tungsten and 750 μm sapphire is

$$\frac{q_W}{q_S} = 4.3 \times 10^{-3}$$

This indicates that for the current substrate and device structures the transient gamma response is dominated by the sapphire substrate.

A second transient radiation effect that can occur in the substrate is radiation induced conductivity (RIC). However, RIC can be reduced by several orders of magnitude by use of chromium-doped sapphire, neutron irradiated sapphire or polycrystalline alumina^{4,5}. Because of this, RIC effects are not expected to be a problem.

Transient Radiation Measurements. In order to confirm the results of the analysis, additional tests were performed on operating triodes, on electrode pairs with different Z numbers, on electrode pairs with different thicknesses, and electrode pairs with different areas. These tests were conducted in a screen room with short lengths of coax cable between the test device and shielded line drivers. For these tests the package, pins, bond wires, and bond pads were also shielded so that only the electrode response was measured. In all cases the transient response was proportional to the electrode area but different Z numbers and different electrode thicknesses did not produce a measurable difference in transient response. These tests verify that the dominant mechanism in the TIC photo response is the Compton scattering of electrons in the sapphire substrate. The charge displaced from the substrate causes a replacement charge to flow in the electrodes which constitutes the TIC transient response.

These tests indicate that thinner substrates should reduce the transient photo response. Further, if the conclusion is correct, a ground plane on the opposite side of the substrate should supply about half of the replacement electrons and so should reduce the response by about a factor of two. In order to verify this, the test structure shown in Fig. 4 was designed. The ground plane should reduce the response of electrode A to about half that of electrode B. The test results are shown in Fig. 5.

These results indicate that the Compton response could be greatly reduced by electrically shielding the TIC devices from the bulk of the substrate support structure. The ground plane in the layered structure shown in Fig. 6 should accomplish this isolation. Such a device was fabricated and tested; the results are shown in Fig. 7. The response appears to be noise with a maximum amplitude of 3 mV (the response of an empty socket had an amplitude of about 3 mV).

Projected $\dot{\gamma}$ Response. Based on these results the $\dot{\gamma}$ response of a TIC flip-flop has been calculated. The electrodes and interconnect metal associated with each node must supply replacement electrons for those ejected from the substrate. The node potentials will change by an amount

$$\Delta V_n = \Delta Q_n / C_n$$

where ΔQ_n is the total replacement charge supplied by node n, and C_n is the total capacitance associated with node n.

The analysis assumes that the charge is deposited in a time short compared to the flip-flop response time, that the most critical node is the cross coupled node, that the logic swing is 5 volts and that a ΔV of 2 volts is sufficient to upset the flip-flop. ΔQ is calculated from Eq. (?) and the total area of the node metal. For a flip-flop built on a 25 μm thick insulator on a ground plane, the calculated upset level is 4×10^{11} rad (Si)/s. If the logic swing is increased above 5V, the upset level is increased proportionately.

CIRCUITS

The first completely integrated circuit fabricated with the TIC technology was a simple flip-flop consisting of ten triodes on two closely spaced substrates. One of these substrates is shown on the top in Fig. 8.

Since this flip-flop was designed, much smaller test triodes have been designed and tested. The device whose characteristics are shown in Fig. 9 has 1/28th the cathode area and 1/5th the total area of the flip-flop devices. Except for the reduced current level, the characteristics are similar to those of the large device shown in Fig. 2.

The flip-flop was redesigned with these smaller devices and modified to function as a clocked RS flip-flop. A preliminary layout of a 16-bit shift register, which uses the new flip-flop, is shown on the bottom in Fig. 8. The shift register contains 199 devices in the same area previously occupied by 10 devices.

NEAR-TERM PERFORMANCE LEVELS

Projection of the near-term level of integration, device speed, and power consumption are addressed. These projections are based on the current TIC technology. Significant improvements in processing such as raised electrodes, cathode improvements, addition of resistors and capacitors, two-layer interconnect capability, or closer anode/ cathode spacing could improve TIC performance dramatically.

Because there are many devices on a substrate, one device can be affected by parasitic electrostatic interactions from other devices that can modify the expected device current. These interactions are reduced to an acceptable level by placing shield electrodes and ground planes between devices and by placing the devices sufficiently far apart. These shields occupy most of the wafer area so that the interactions limit the level of integration. The 16-bit shift register shown in Fig. 8 has about 1000 devices/in.² of active area. However, the high yield process makes 1-in.² wafers possible so that MSI level circuits with 1000 devices would be practical.

The gain bandwidth product of current TIC devices is on the order of 100 MHz. These devices are relatively large; the gain bandwidth will improve as the TIC devices are scaled down in size.

Most of the power consumed by current TIC devices is used to heat the substrate. Most of the heat loss is through radiation, but heat shields can reduce this loss substantially. The power required per substrate pair can be reduced by placing multiple pairs in a single vacuum package. With proper heat shields, 10 substrate pairs per package and 1000 devices/in.², the projected power requirement is 2.5 mW/device. Lower-temperature cathodes appear to be a real possibility.^{6,7,8} This would reduce TIC power consumption substantially because radiation losses vary as T^4 .

FUTURE PLANS

The near term plans include developing an improved substrate to increase the transient radiation upset levels, develop an improved package, and design and fabricate TICs at the SSI to MSI level. The initial emphasis will be on analog circuits with a line driver and an operational amplifier being early goals.

The longer-term plans involve developing advanced processing techniques, including 3-D structures, smaller feature sizes, advanced cathodes, crossovers, resistors, and capacitors. This will lead to a higher level of integration, higher speed, lower power consumption, and a much higher circuit complexity.

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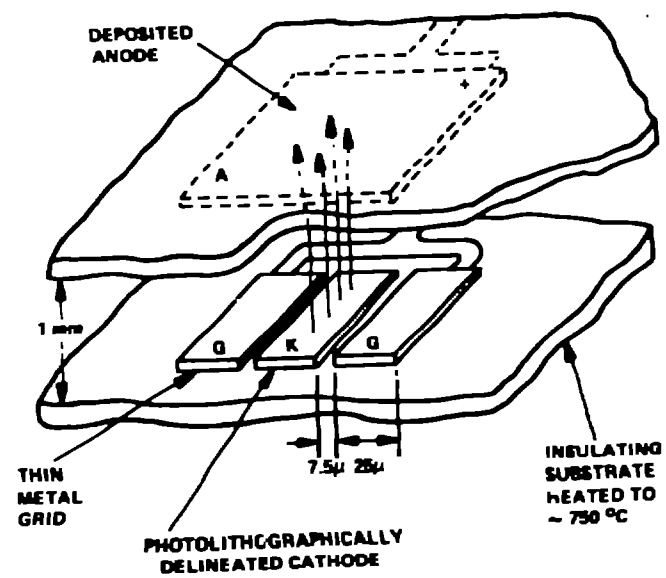


Fig. 1. Structure of the vertical TIC active device.

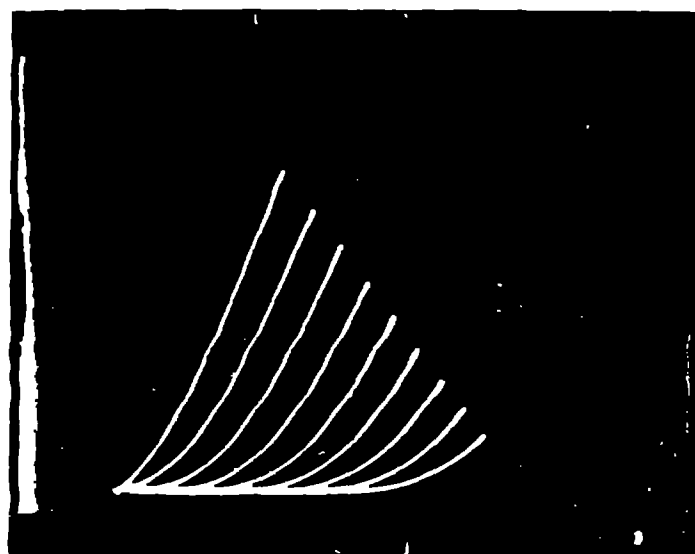


Fig. 2. TIC $v - i$ characteristics.

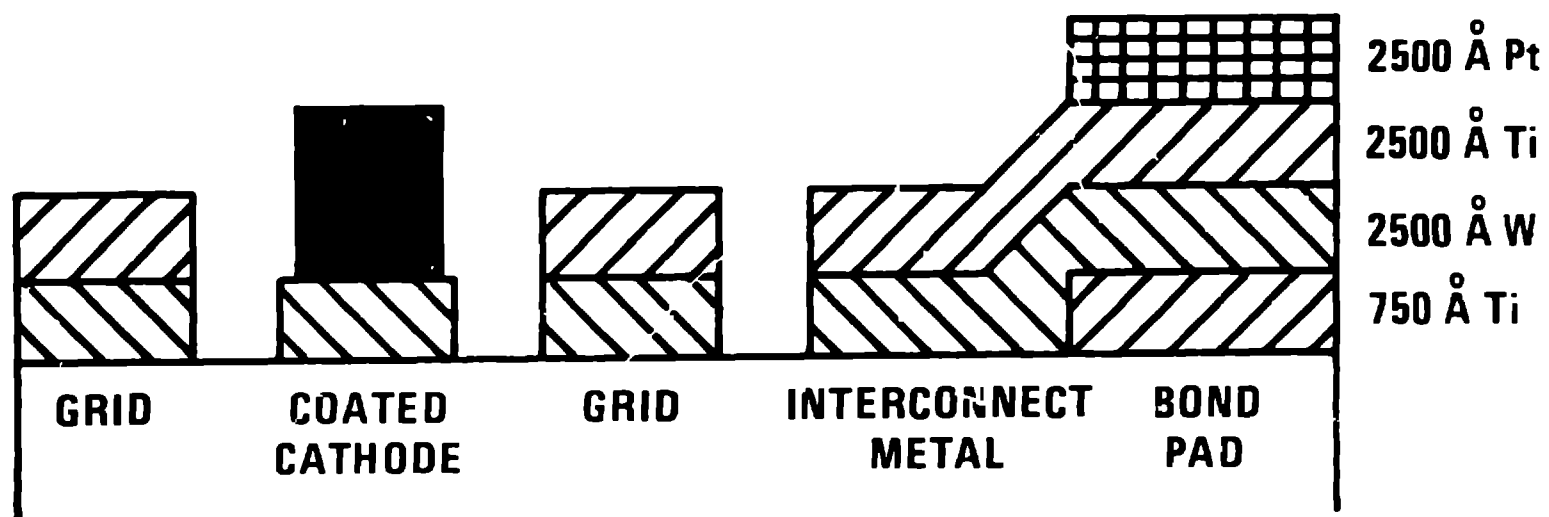


Fig. 5. TIC Metallization

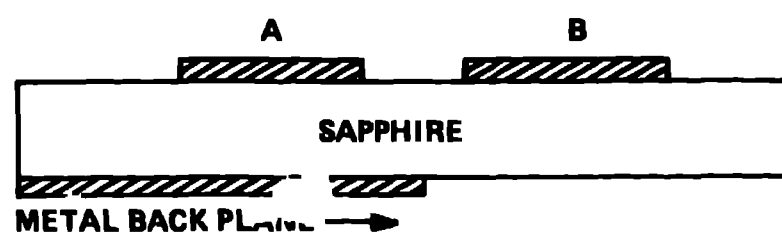


Fig. 4. Ground plane test structure.

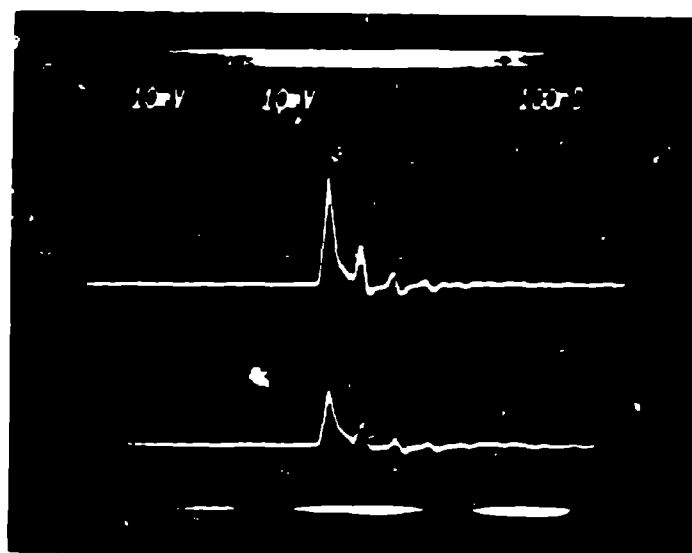


Fig. 5. γ response of the ground plane test structure. Bottom sweep is pin A (with ground plane), top sweep is pin B (without ground plane).

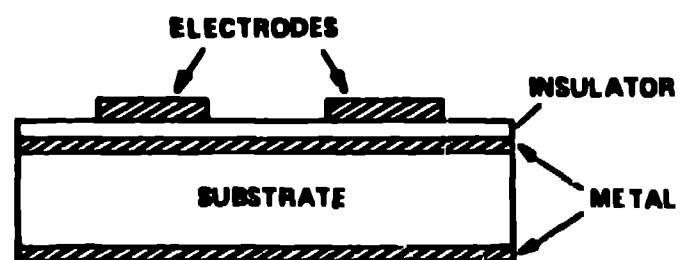


Fig. 6. Thin insulator on metal ground plane.

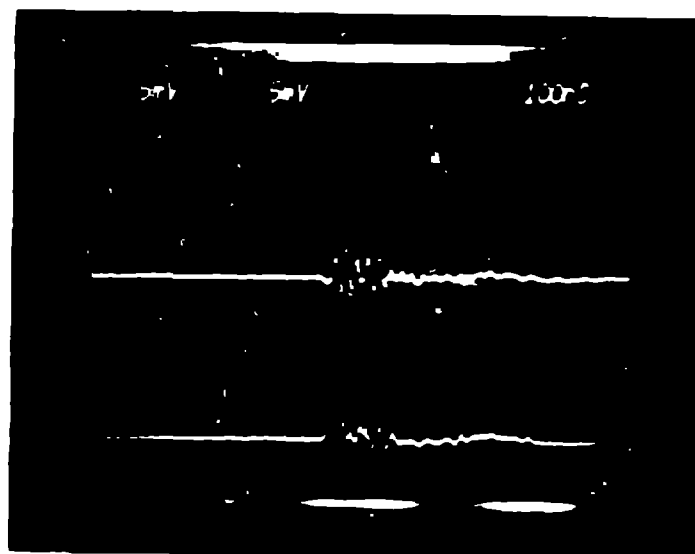


Fig. 7. γ response of the electrodes on a thin insulator on metal ground plane.

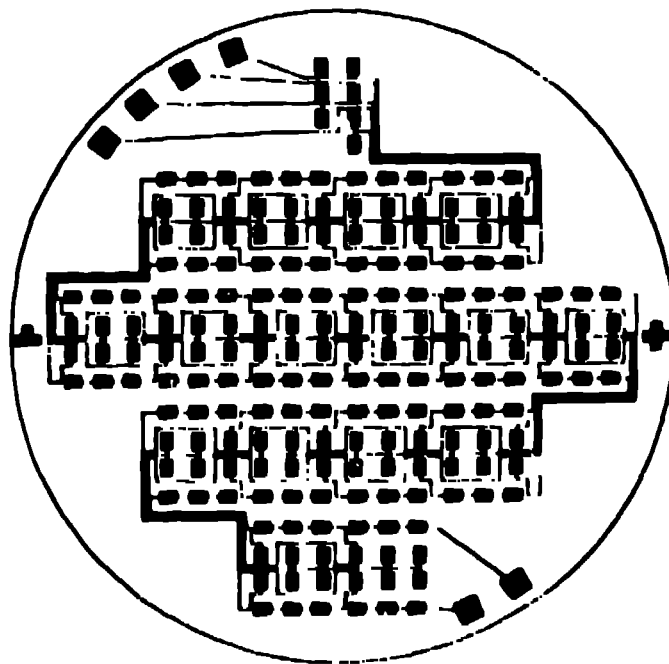
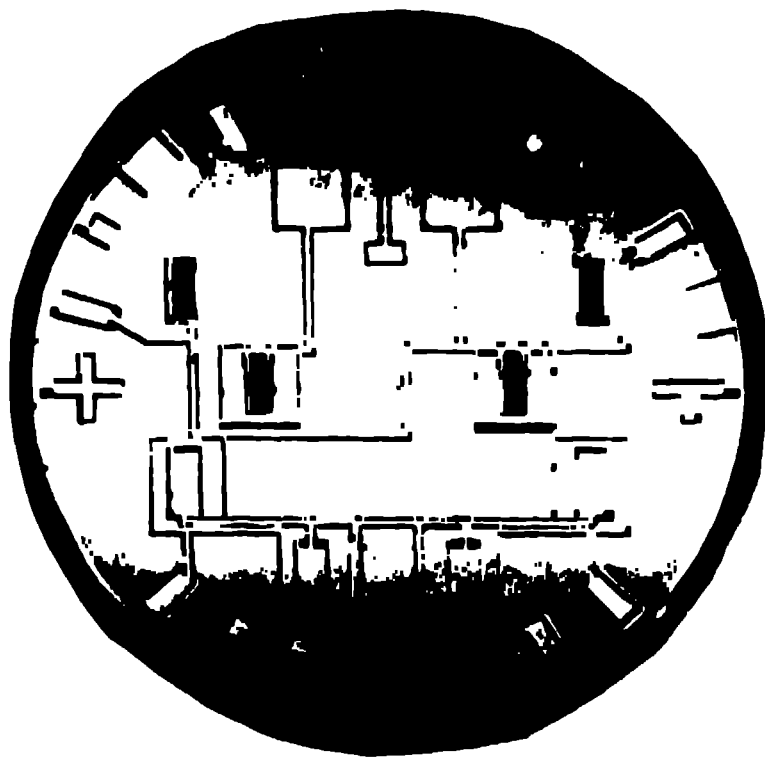


Fig. 8. TIC Integration. The original 10 device flip-flop is shown on the top; a preliminary layout of a 16-bit shift register with 199 devices is shown on the bottom. Both circuits fit on a 19-mm-diameter wafer.

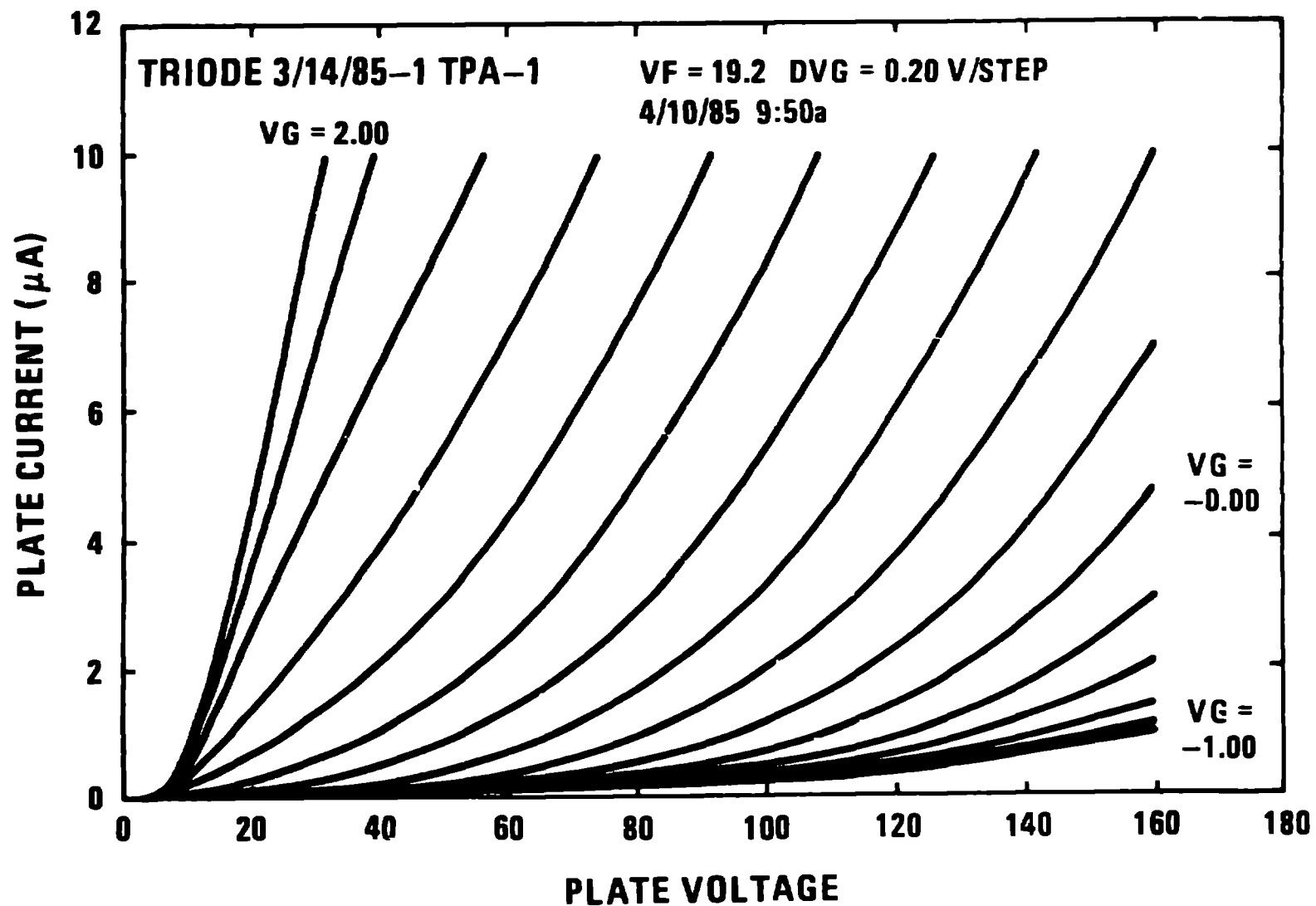


Fig. 9. v - i characteristics of the redesigned IIC device. This device has a single cathode stripe and a cathode area of 20 square mils. (The device used in the original flip-flop had 7 cathode stripes and a cathode area of 567 square mils.)