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Light-Trapping Concentrator Cells

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Sandia Contract: 02-7063E

ABSTRACT

The objective of this project was to develop a thin, light-trapping silicon concentrator solar cell using a new structure, the cross-grooved cell. A process was developed for fabricating V-grooves on both sides of thin silicon wafers, the grooves on one side being perpendicular to those on the other side. A novel way of minimizing flat spots at the tops of the V-grooves was discovered. We experimentally verified the theoretical light-trapping superiority of the cross-grooved structure. We also demonstrated a reduction in grid line obscuration for grid lines running parallel to the V-grooves due to light reflection into the cell. High short-circuit current densities were achieved for p-i-n concentrator cells with the cross-grooved structure, proving the concept. The best efficiencies achieved were 18% at concentration, compared to 20% for a conventional planar low-resistivity cell. Recombination in the full-area emitter was identified as the major intrinsic loss mechanism in these thin, high-resistivity bifacial cells. Recombination in the emitter limits Voc and fill factor, and also leads to a large sublinearity of short-circuit current with light intensity. Reduction of the junction area is a major recommendation for future work. In addition, there were persistent problems with ohmic contacts and maintaining high minority-carrier lifetime during processing. We believe that these problems can be solved, and that the cross-grooved cell is a viable approach to the limit-efficiency silicon solar cell. This report covers research conducted between March 1987 and July 1989.

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INTRODUCTION

1.1 BACKGROUND

The silicon concentrator solar cell field has seen rapid advances recently in both cell design and fabrication. For example, using a microgrooved n^+pp^+ design, the University of New South Wales has fabricated cells with a conversion efficiency of 25%.[1] At Stanford University, efficiency exceeding 27% has been demonstrated with a p-i-n interdigitated-back-contact (IBC) point-contact design.[2] Even though highly efficient cells have been fabricated in the laboratory, further improvement in silicon concentrator cell technology remains possible. It is generally agreed[3-7] that the optimal bifacial or IBC silicon cell will have a thickness in the range of 50 to 150 microns, almost irrespective of the specifics of the actual cell design, if light trapping and surface (or interface) passivation can be achieved. This project is aimed at improved methods of light trapping leading to limit-efficiency cells.

1.2 GOALS

The overall objective of this project was to develop a thin, light-trapping silicon solar cell using a new structure conceived at Spire, the cross-grooved cell.[8] A recent study concluded that the special geometry of this structure gives it superior light-trapping characteristics compared to any known approach.[9] Intermediate goals of the project included experimentally demonstrating the theoretical advantage of this structure in terms of light-trapping effectiveness, and developing cell fabrication procedures for realizing such cells.

1.3 TASKS

The program was divided into the following four technical tasks:

Task 1 - Research on Light-Trapping Optics

The purpose of this task was to obtain and evaluate light trapping in the cross-grooved structure. The degree of light trapping was to be experimentally quantified and compared to other structures involving various combinations of V-grooved, pyramid-etched, and planar surfaces.

Task 2 - Research on Surface Passivation and Junction Design

The purpose of this task was to perfect minority-carrier collection, particularly in thin cells. This involved developing fabrication procedures for minimizing surface recombination, bulk recombination in the heavily doped regions, and recombination at the metal contacts.

Task 3 - Development of Solar Cells

The purpose of this task was to fabricate and test thin high-efficiency cells with the cross-grooved structure. It incorporated the results of Tasks 1 and 2 in a full solar cell fabrication process.

Task 4 - Reporting

The objective of this task was to supply monthly reports and a final report to Sandia.

1.4 ACCOMPLISHMENTS

The accomplishments of the project and the degree to which the goals have been met can be summarized as follows:

Task 1 - A process was developed for fabricating cross-grooved light-trapping structures in silicon, including a novel way of minimizing flat spots at the tops of V-grooves. The effectiveness of a number of light-trapping structures was measured experimentally. We verified the theoretically-predicted advantage of the cross-grooved structure relative to all others. However, it was only slightly better than the next-best structure with pyramid-etched front and polished back surfaces. We also demonstrated reduced grid line obscuration losses for grid lines running parallel to the V-grooves. More than half of the light incident on the grid lines was reflected onto the active cell area. All of the goals under this task were met.

Task 2 - We identified recombination in the full-area emitter as the major loss in these thin bifacial cells. Although some work was done to reduce the emitter area, time did not permit the incorporation of point-contact-type junctions in the cross-grooved structure. Point-contact back-surface regions were evaluated, and found not to provide a significant improvement at this stage of cell development. The recombination at

oxide-passivated surfaces was found to be insignificant. Although the various sources of recombination were evaluated under this task, we were not successful in reducing them all to low enough levels to produce very high efficiency cells.

Task 3 - A fabrication process for thin cross-grooved concentrator cells was developed. Very high short-circuit currents were demonstrated for thin light-trapping cells, proving the concept. As part of the cell development, we produced low-resistivity concentrator cells with 20% efficiency at 124 suns. The best high-resistivity V-grooved concentrator cells were 18% efficient. These cells were limited by short-circuit current sublinearity and poor ohmic contacts. We have identified process improvements necessary to increase efficiencies in the thin cross-grooved cell. These include small-area junctions, better control of minority-carrier lifetime during cell processing, and a more reproducible ohmic contact formation process. Although very high efficiencies were not achieved in this program, we see no reason that they could not be in future work.

Task 4 - This report completes the work under task 4.

SECTION 2
LIGHT-TRAPPING STRUCTURES

2.1 SURFACE PREPARATION

Wafers of various thicknesses and surface conditions were prepared in order to determine the optimum cell thickness and surface to maximize light absorption. Samples for this purpose were processed in two separate groups. The first group consisted of textured (pyramid surface) and polished surfaces, and the second group consisted of V-grooved and polished surfaces. Silicon wafers used for this work were high-resistivity (100 ohm-cm), n-type, (100) orientation, two-inch diameter, float zone wafers polished on both sides. Table 2-1 shows the various surface combinations prepared for light-trapping measurements.

TABLE 2-1. SAMPLES FABRICATED FOR LIGHT-TRAPPING MEASUREMENTS.

Surface Front/Back	Thickness (mils)			
Texture/Texture	2	4	6	10
Texture/Polish	2	4	6	10
V-Groove/Polish	2	4	6	10
V-Groove/V-Groove right angles to one another	2	4	6	10
V-Groove/V-Groove parallel to one another	2	4	6	10
Polish/Polish	2	4	6	10

Wafer thicknesses investigated were in the range of 50 μm to 300 μm. The first step in sample preparation was thinning of the silicon. Thinning of the silicon was done by etching in potassium hydroxide (KOH). Target thicknesses were 2, 4, 6 and 10 mils. This type of etch is commonly used at Spire for thinning wafers and allows for control over thickness within 0.2 mils. Once wafer thinning was completed, preparation for surface

treatment was started. In the first group of wafers texture etching was done. Some wafers were textured on both sides, others were textured on one side only. In the latter case an etch mask of silicon dioxide was deposited on the side to be left unetched. The second group of samples, using V-groove surfaces was processed at a later time. In order to form V-groove structures, (100) silicon is required. As a first step, the wafers were coated with an etch mask consisting of silicon nitride. Next, nitride stripes were patterned by fine line photolithography. For this purpose, a photolithograhic etching mask was designed and purchased. The mask consisted of 5 μm wide lines on 15 μm centers. The stripe pattern on the photomask was aligned with the trace of the (111) plane in the (100) surface, which is accomplished by using the flat of the wafer as a reference. The etching of the V-grooves was done in a KOH-based etch. The process development required to consistently etch V-grooves with narrow ($\sim 1\,\mu$m) plateaus at the tops was extensive and will be covered in a later section (4.1). Figures 2-1 and 2-2 show profiles of V-groove samples prepared for light-trapping measurements.

Following the completion of the second group of wafers, all samples required for investigating light-trapping maximization were fabricated and ready for reflectance and transmission measurements.

2.2 BACK-SURFACE MIRROR

For any of the structures described above, light trapping is further enhanced by the presence of a highly reflective back-surface mirror, which traps the light that would otherwise escape from the back surface. Accordingly, we tested the wafers both with and without such a mirror.

2.2.1 Design

While the presence of a metal at back surface of the silicon can cause reflection of light that would otherwise escape, it can also interfere with the total internal reflection on which the light trapping depends. Table 2-2 gives the calculated reflectance for various angles of incidence of the silicon-metal interface. Calculations were done for a wavelength of 1100 nm, using 3.536, 1.203-10.89i, and 0.24-17.47i for the refractive indices of silicon, aluminum, and silver respectively.

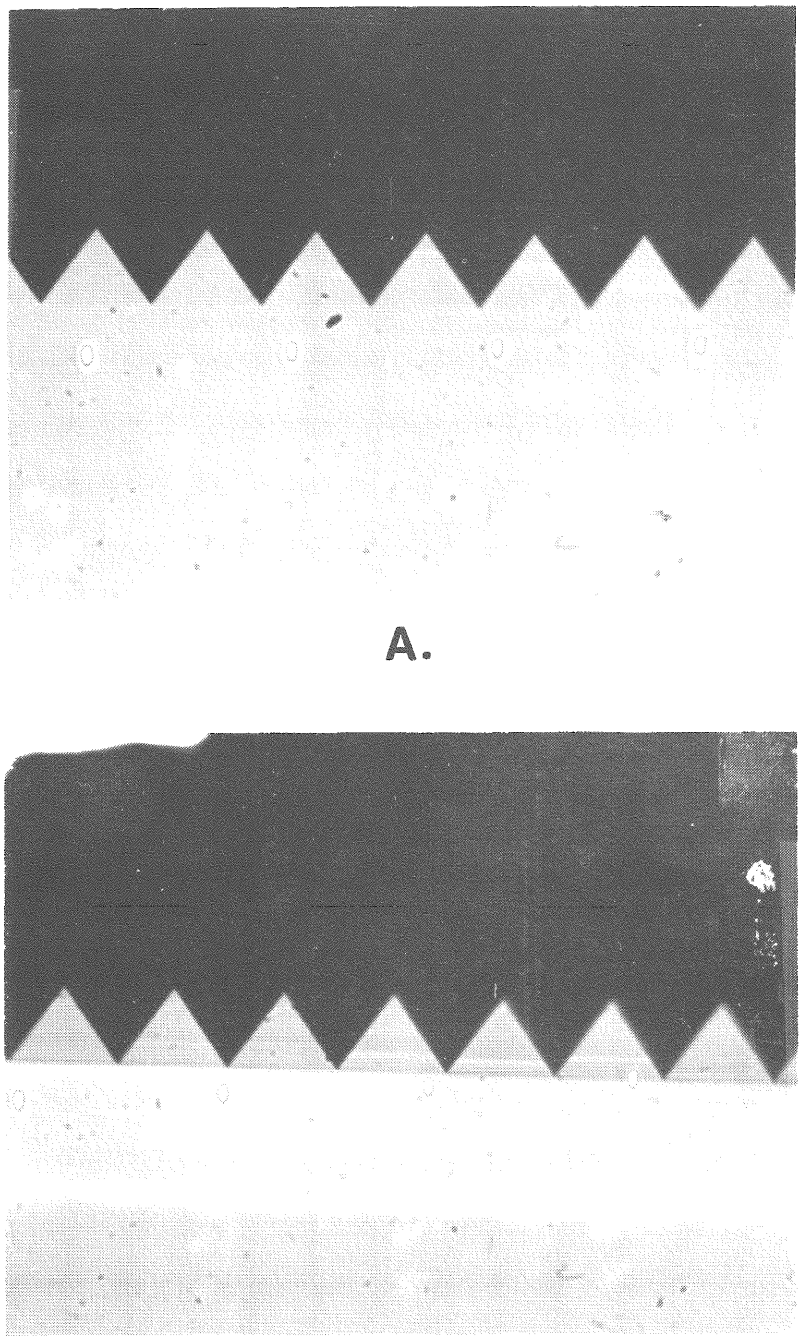
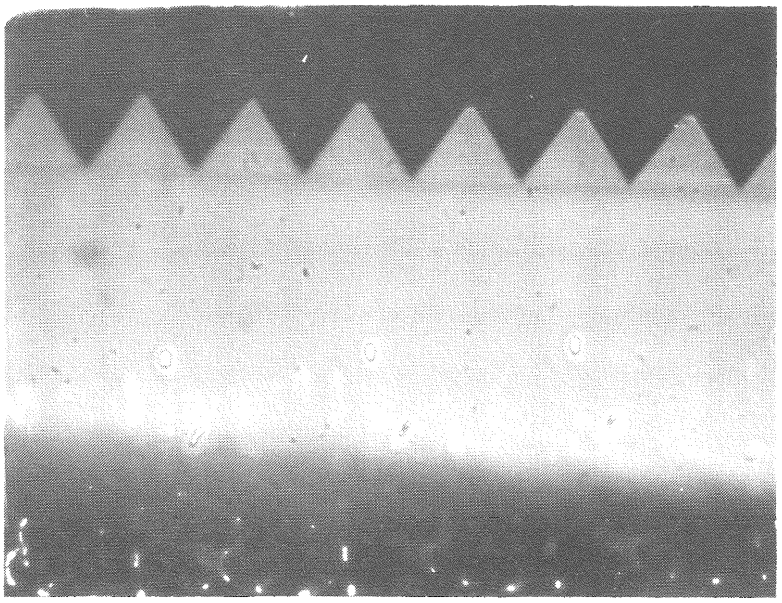
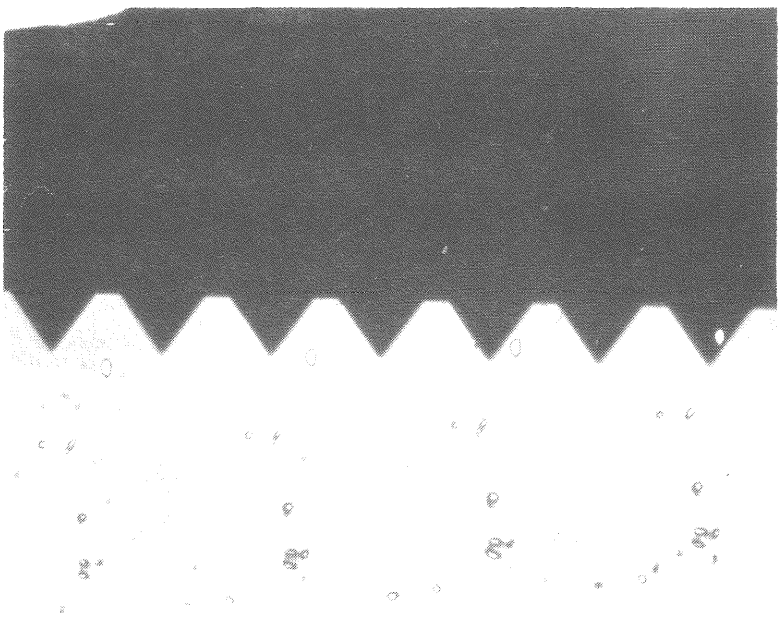


FIGURE 2-1. SIX MIL CROSS-GROOVE SAMPLE SHOWING: (a) Front Grooves; (b) Back Grooves.



A.



B.

FIGURE 2-2. FOUR MIL CROSS-GROOVE SAMPLE SHOWING: (a) Front Grooves, (b) Back Grooves.

TABLE 2-2. REFLECTANCE OF Si-METAL INTERFACE.

Metal	Angle of Incidence		Polarization	
			Parallel	Perpendicular
Al	0.0°	(polished wafer)	0.8794	0.8794
Al	13.5°	(parallel groove)	0.8759	0.8826
Al	48.8°	(polished back)	0.8297	0.9210
Al	64.4°	(cross groove)	0.7946	0.9479
Ag	0.0°	(polished wafer)	0.9513	0.9513
Ag	13.5°	(parallel groove)	0.9497	0.9529
Ag	48.8°	(polished back)	0.9330	0.9695
Ag	64.4°	(cross groove)	0.9292	0.9803

The angles given in the table are the angles of incidence for the first reflection from the back of the wafer for each of the structures investigated.

This problem can be avoided by using a layer of dielectric between the silicon and the metal. In this case, the light which is incident at greater than the critical angle penetrates only a short distance into the dielectric and so is not affected by the metal. The light incident at less than the critical angle enters the dielectric layer and, although slightly absorbed by the metal, is mostly reflected back into the silicon. Table 2-3 shows the corresponding calculations for this case. A thickness of 1900 Å and a refractive index of 1.46 was used for the dielectric layer, corresponding to half-wave optical thickness of SiO_2, which was seen to be the peak in reflectance for the rays incident at less than the critical angle. This combination increases the critical angle from 16.4° (the value for the Si-air interface) to 24.4°, but the high reflectance of the metal makes this less important than it would be on an exposed surface.

TABLE 2-3. REFLECTANCE OF Si-DIELECTRIC-METAL INTERFACE.

Metal	Angle of Incidence		Polarization	
			Parallel	Perpendicular
Al	0.0°	(polished wafer)	0.9761	0.9761
Al	13.5°	(parallel groove)	0.9664	0.9832
Al	48.8°	(polished back)	0.9997	0.9991
Al	64.4°	(cross groove)	1.0000	0.9998
Ag	0.0°	(polished wafer)	0.9897	0.9897
Ag	13.5°	(parallel groove)	0.9858	0.9930
Ag	48.8°	(polished back)	0.9999	0.9997
Ag	64.4°	(cross groove)	1.0000	0.9999

2.2.2 Fabrication - Test Samples and Cells

For the light-trapping test samples described in this section, a back-surface mirror consisting of 200 nm of MgF_2 (which acts very similarly to SiO_2) followed by 110 nm of aluminum was applied, to give the best reflectance as described above. For the cells described in Section 4, however, it did not prove possible within this project to fabricate the complex structure required to do this and also make ohmic contact to the back surface. The grooved and textured cells were made with metal directly on the silicon, and this difference may explain some of the differences seen between the optical light-trapping measurements and the final cell results.

2.3 LIGHT-TRAPPING MEASUREMENTS

In order to assess the light-trapping capabilities of different wafer surface treatments, transmission and reflectance spectra (300-1300 nm) were measured and upper limits of short-circuit current were determined for each structure.

2.3.1 Apparatus

Optical transmission and reflectance measurements were carried out using an Optronic Laboratories modular spectrophotometer, which includes a quartz-halogen light source, monochromator, and four-inch diameter integrating sphere. Figure 2-3 shows a top view of the optical layout of the instrument.

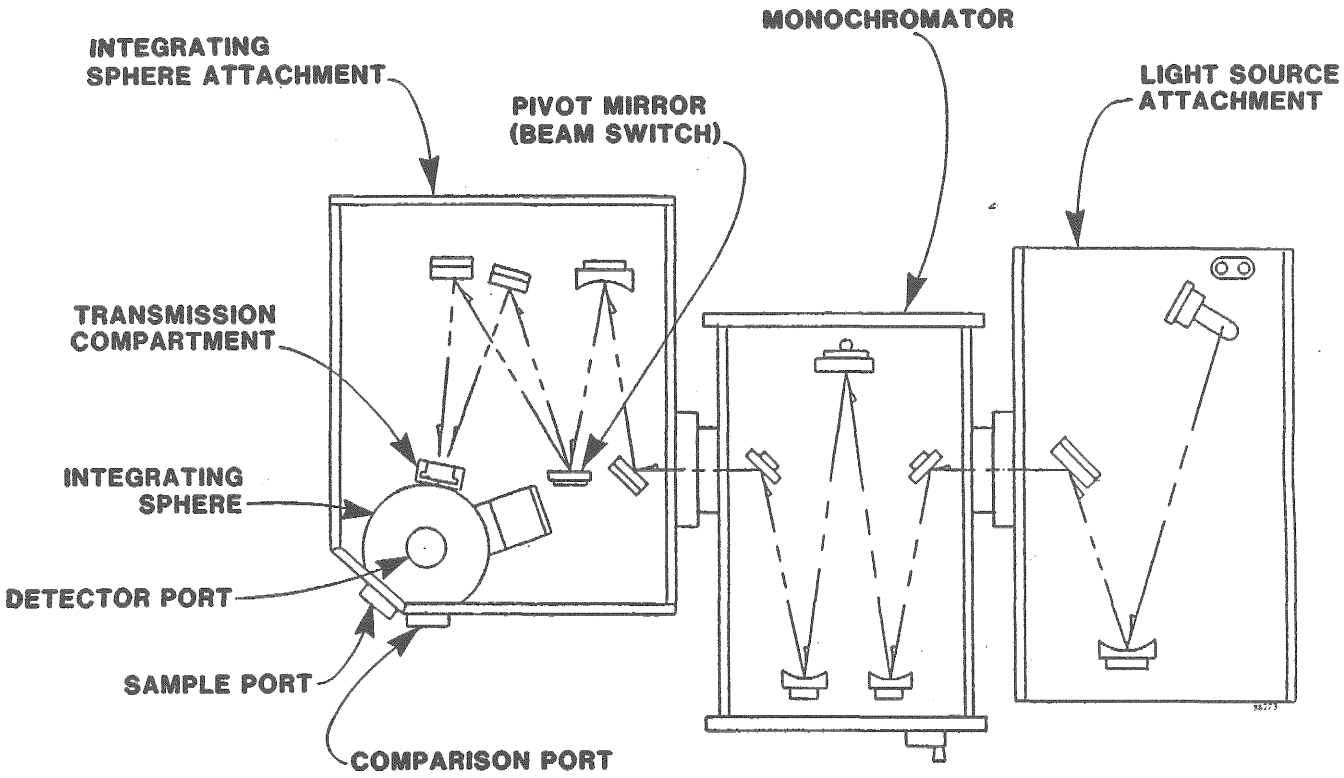


FIGURE 2-3. TOP VIEW OF OPTRONIC LABORATORIES SPECTROPHOTOMETER.

With the proper choice of optical detector and holographic grating, measurements can cover the spectrum from 280 to 1800 nm. The beam diameter is 3 mm and the angle of incidence is fixed at 10°.

2.3.2 Data Reduction

The goal of the light-trapping measurements was to determine the short-circuit current that would result if all the absorbed light were converted to photocurrent. Prior to this calculation, however, it was necessary to correct the transmission data for the limited acceptance angle of the spectrophotometer.

2.3.2.1 Scattered Light Correction

Figure 2-4 shows the integrating sphere in transmission mode. Since the sample does not rest against the entrance port of the sphere, any light that is scattered by more than some critical angle will not enter the sphere. This scattering loss, which is more pronounced on samples with textured surfaces, results in anomolously low transmission. Accordingly, the measured transmission $T_m(\lambda)$ is some fraction σ, of the total transmission $T(\lambda)$ as in

$$T_m(\lambda) = \sigma T(\lambda), \qquad (2.1)$$

and the quantity $(1-\sigma)\,T$ represents the light scattered outside the acceptance angle.

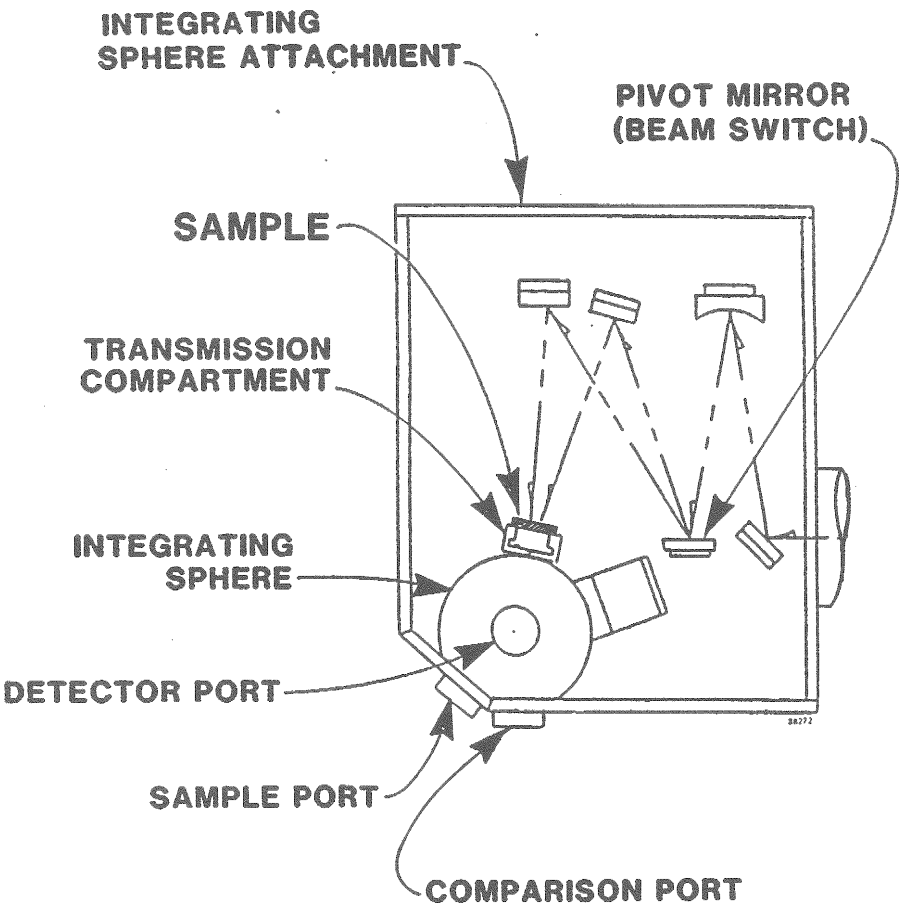


FIGURE 2-4. INTEGRATING SPHERE IN TRANSMISSION MODE.

In the wavelength range of interest (800 nm $\leq \lambda \leq$ 1300 nm), the index of refraction, n, varies only slightly. As a result, the constant σ is independent of wavelength, and depends only on the wafer structure and measurement geometry. The value of σ can be determined by noting that at 1300 nm, essentially no absorption occurs and T (1300 nm) = 1 - R (1300 nm). (These samples contained no heavily-doped regions, and Dash and Newman[10] give the absorption coefficient for lightly-doped Si at 1300 nm as $\ll 0.1\ cm^{-1}$.) From Equation 2.1, σ is given by

$$\sigma = \frac{T_m\ (1300\ nm)}{1 - R\ (1300\ nm)} \tag{2.2}$$

The measured transmission was corrected by dividing $T_m(\lambda)$ by σ for all λ. Figure 2-5 shows transmission data before and after the scatter correction for a typical textured sample.

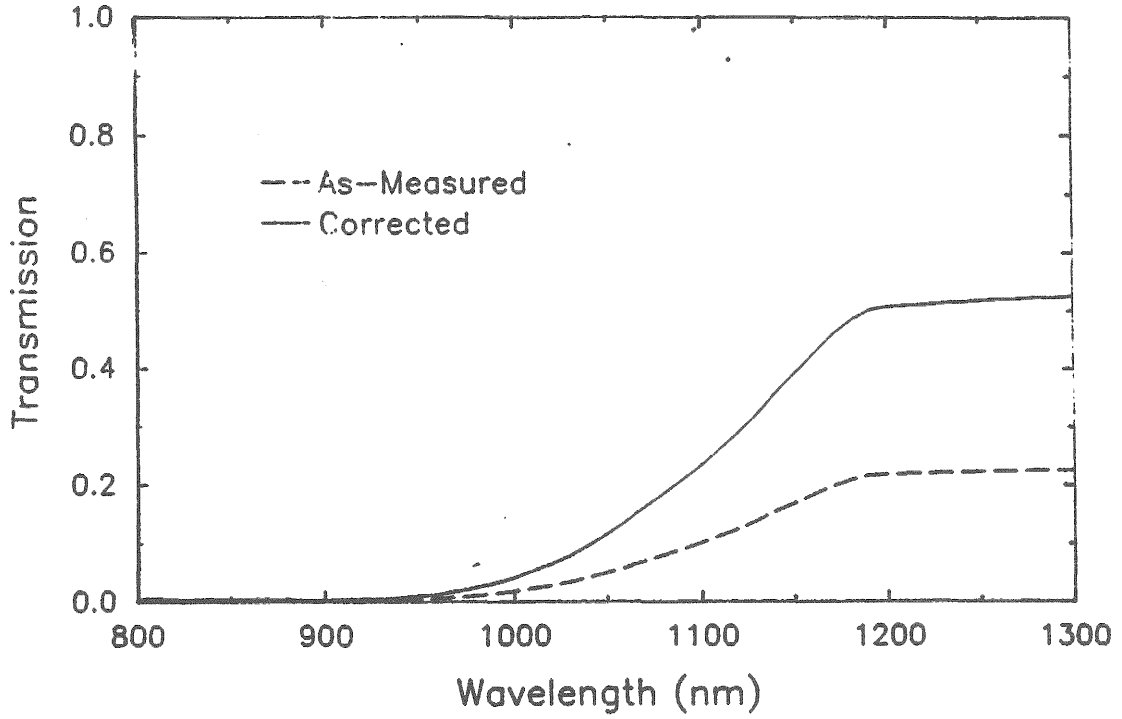


FIGURE 2-5. TRANSMISSION DATA BEFORE AND AFTER SCATTERING LOSS CORRECTION.

2.3.3.2 Photocurrent Calculation

The short-circuit current density J_{sc} is taken as the ultimate indicator of light-trapping effectiveness. Assuming that all carriers generated by the absorption of photons are converted to current, the maximum attainable J_{sc} can be calculated by integrating the product of the measured spectral absorption and the AM1.5 direct normal spectral irradiance. The external J_{sc} is then given by

$$J_{ext} = \frac{1}{hc} \int_0^{\infty} (1 - R - T)\ \lambda E_{\lambda}\ d\lambda \qquad (2.3)$$

where

h = Planck constant

c = Velocity of light in vacuum

λ = Wavelength of light

E = AM1.5 direct normal spectral irradiance at λ.(11)

Since tests were performed on samples with markedly different front-surface reflectance (polished vs. textured), it was found that correcting the calculated J_{sc} for front-surface losses provided for better comparison between samples. This corrected, internal J_{sc} is given by

$$J_{int} = \frac{1}{hc} \int_0^{\infty} \frac{(1 - R - T)}{(1 - R)}\ \lambda E_{\lambda}\ d\lambda. \qquad (2.4)$$

The results and analysis of the light-trapping measurements are presented in Section 2.4.

2.4 RESULTS OF LIGHT-TRAPPING EXPERIMENTS

The light-trapping samples were measured under three conditions: uncoated, with front antireflection coating but no back coating, and with both front AR and back metal coatings.

2.4.1 Reflectance and Transmission Results

2.4.1.1 Uncoated Samples

Figure 2-6 gives the absorption measured on samples of five different surface conditions (cross groove, parallel groove, textured front/polished back, textured both

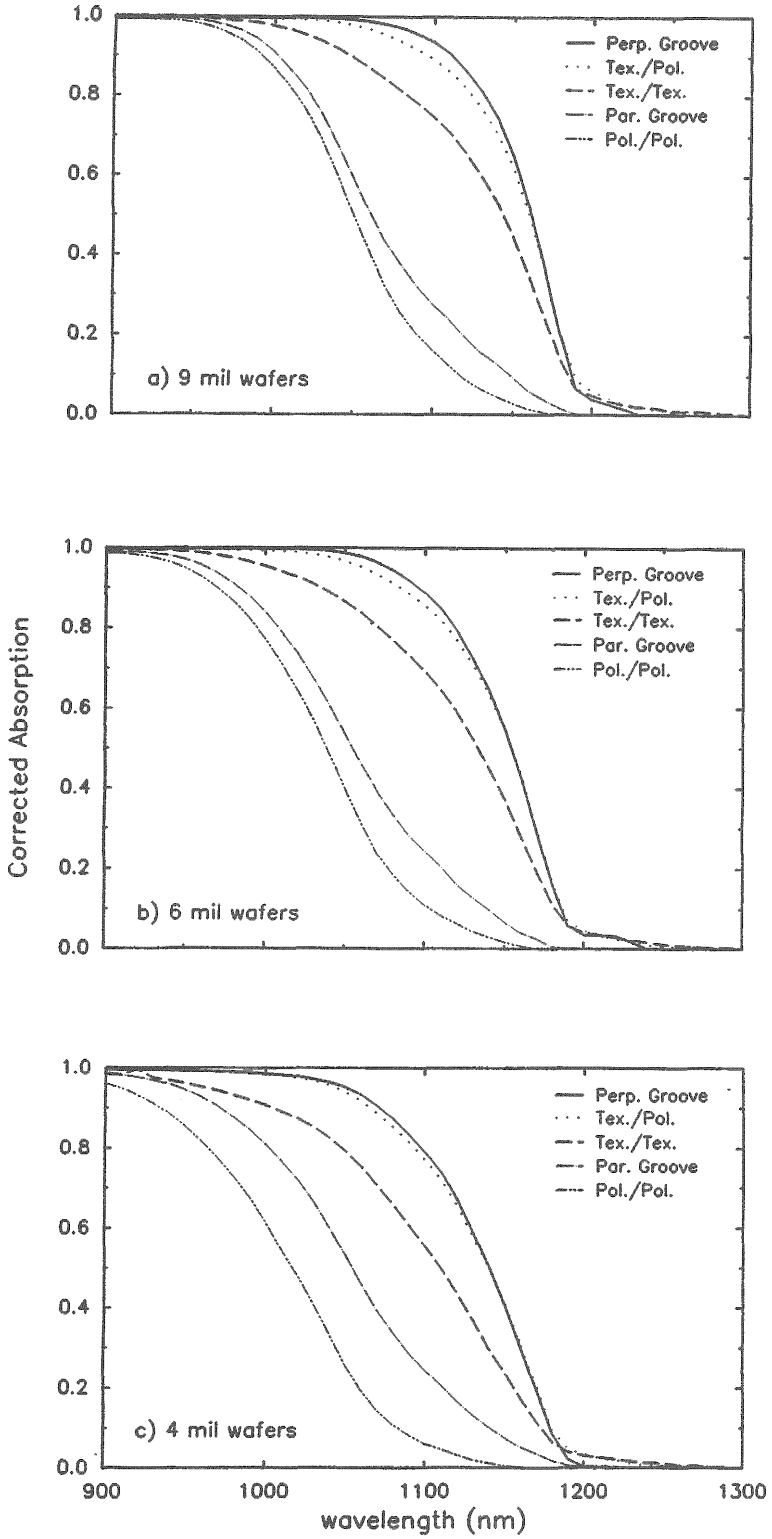


FIGURE 2-6. SPECTRAL ABSORPTION IN UNCOATED SILICON SAMPLES, CORRECTED FOR FRONT-SURFACE REFLECTION. a) 225 micron wafers, b) 150 micron wafers, c) 100 micron wafers.

sides, and polished both sides), and three different thicknesses (225, 150, and 100 microns). The quantity plotted here is (1-R-T)/(1-R), where R is the reflectance and T is the transmission; this gives an approximation to the light-trapping efficiency by correcting for light which is reflected from the front surface. The cross-groove samples show the greatest absorption, closely followed by the textured/polished samples. The parallel-groove samples show much less light trapping, as expected from geometrical considerations.

2.4.1.2 Coated samples

Figure 2-7 gives the absorption measured on the same samples after a standard antireflection coating was applied to the front surface. The coating consisted of 61 nm ZnS and 130 nm MgF_2 on the textured and grooved samples, and 70 nm ZnS and 107 nm MgF_2 on the polished samples. Since the front-surface reflectance is low, the measured reflectance includes a large component of back-reflected light which has escaped through the front, as well as light which never entered the wafer. Accordingly, we have plotted 1-R-T only; that should be a better approximation to the light-trapping efficiency. Qualitatively, the results are the same as without the coatings.

2.4.1.3 Coated Samples with Back-Surface Reflector

Finally, Figure 2-8 gives the measured reflectance of the same samples after coating with the back-surface mirror described in Section 2.2. Since the metal does not transmit light, the amount of light which was absorbed by the metal could not be measured, and so we have plotted only 1-R. The curves show a dip near 350 nm, which is due to front-surface reflectance. The striking difference between the cross-groove and parallel-groove samples remains, but the textured samples now show higher absorption at long wavelengths than the cross-groove samples.

The fact that the absorption in these samples does not approach zero at long wavelengths indicates that there is considerable absorption at the metal-silicon interface. The measured amount of absorption depends, clearly, on two factors: the actual reflection at the interface, and the number of passes which the light makes through the silicon (the degree of light trapping). Since both of these factors will depend on the structure, and since we are not able to measure them independently, the differences between the curves at 1300 nm cannot be directly related to the light-trapping efficiency of the structure.

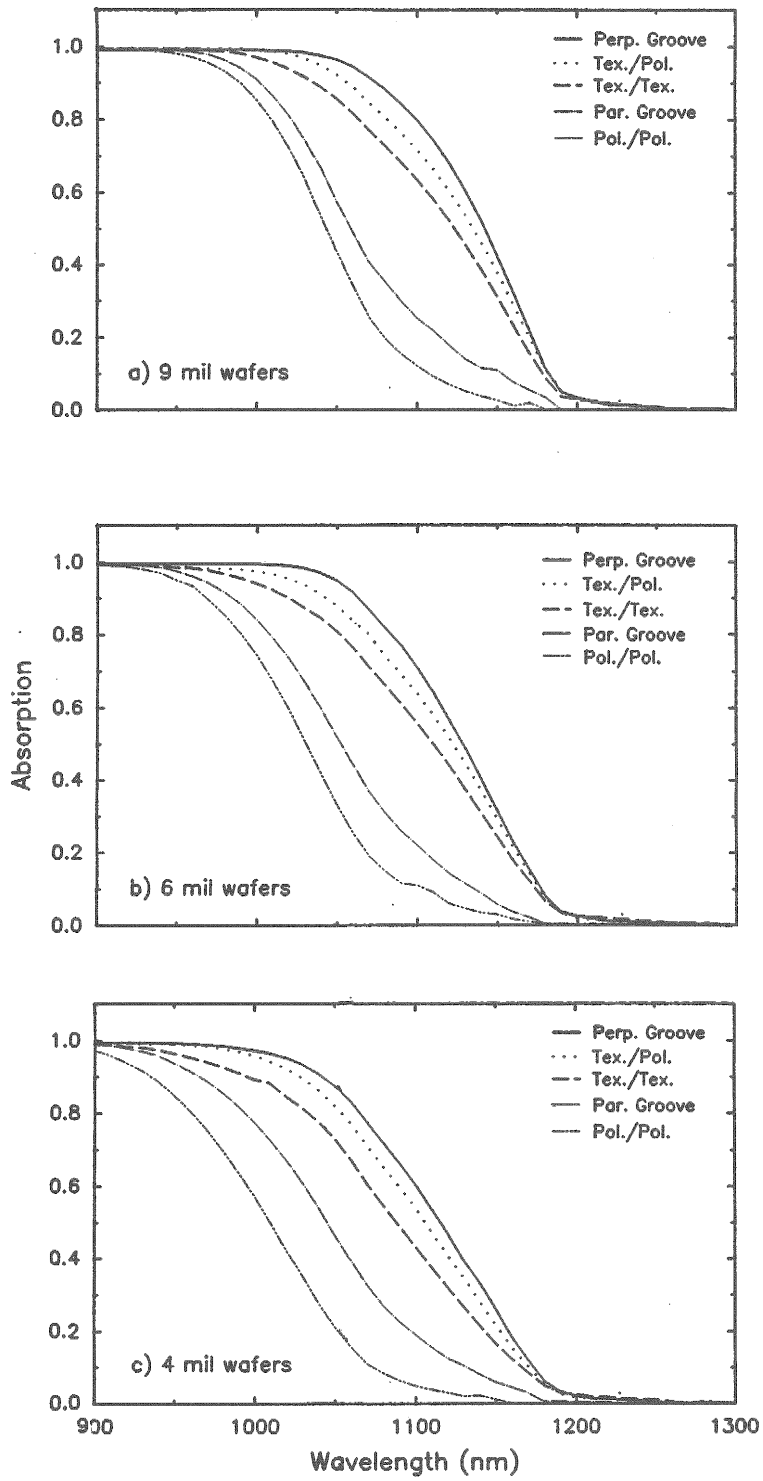


FIGURE 2-7. SPECTRAL ABSORPTION IN SILICON SAMPLES WITH ANTIREFLECTION COATING. a) 225 micron wafers, b) 150 micron wafers, c) 100 micron wafers.

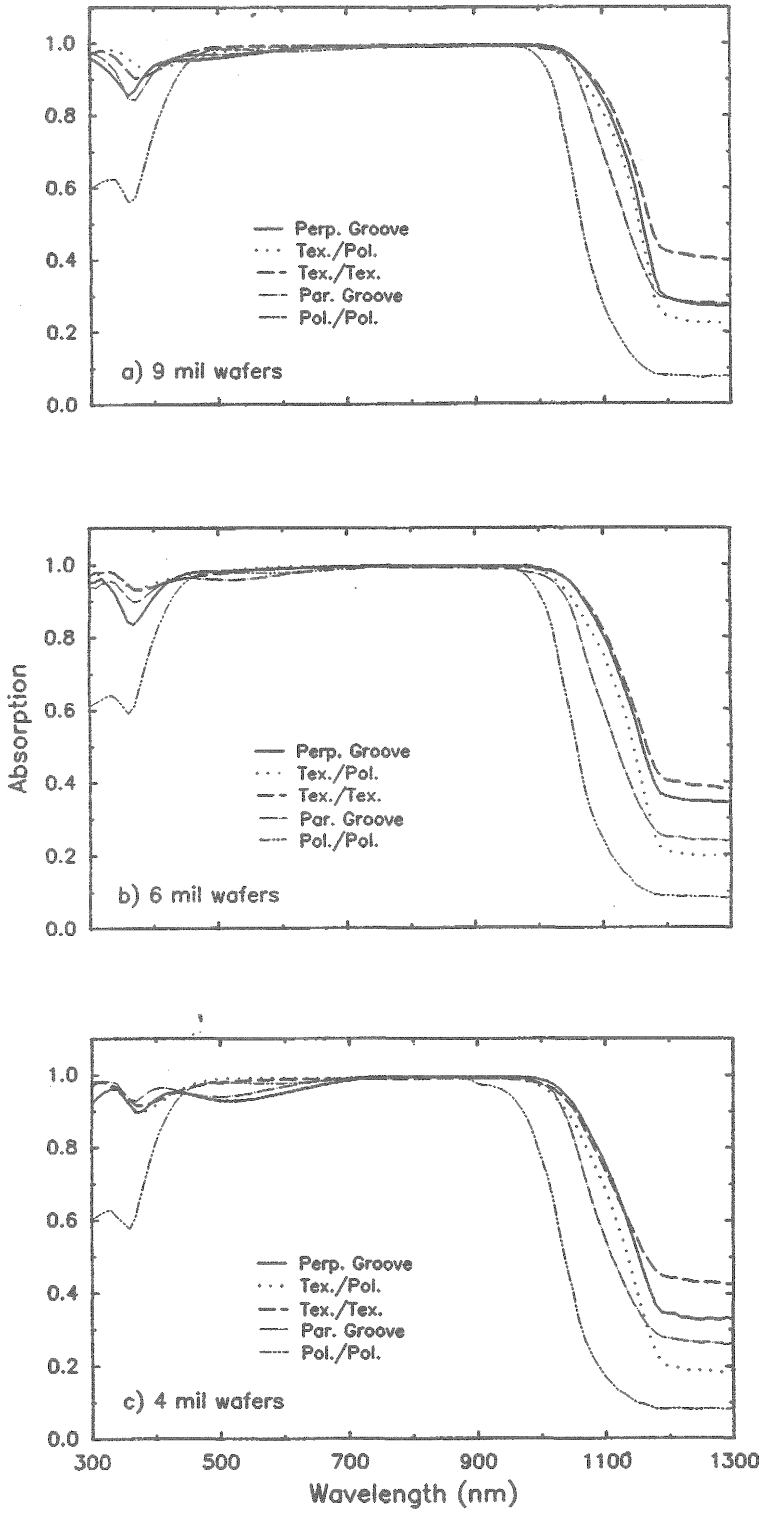


FIGURE 2-8. SPECTRAL ABSORPTION IN SILICON WAFERS WITH ANTIREFLECTION COATING AND BACK-SURFACE REFLECTOR. a) 225 micron wafers, b) 150 micron wafers, c) 100 micron wafers.

An approximate idea of the degree of light-trapping, however, can be extracted by observing the difference between the sub-bandgap reflectance (1300 nm) and the near-bandgap reflectance (1100 nm). If we assume that all the sub-bandgap absorption is associated with the back surface, we then have a measure of the relative magnitude of the back-surface absorption for each structure. If we compare the measured absorption at 1100 nm (where both bulk and surface absorption are present), we can estimate the relative amount of bulk absorption as well. For example, the cross-groove and double-side-textured samples are very close in absorption at 1100 nm, but from the data at 1300 nm it appears that the textured sample has more back-surface absorption. Therefore, we can conclude that the bulk absorption in the cross-groove structure is higher.

2.4.2 Integrated Current Results

These results are summarized in Figures 2-9, 2-10, and 2-11, which show the current generated in a hypothetical solar cell with each structure and no recombination or shadow loss. The current was calculated by convolving the standard AM1.5 direct solar spectrum with the curves shown in Figures 2-6, 2-7, and 2-8. It should be noted that the values of Figure 2-10 understate the actual current achievable in a solar cell because of the lack of a back-surface reflector, whereas the values of Figure 2-11 will overestimate the current slightly because of absorption by the metal. For comparison, the calculated absorption for the case of no light trapping (light passes once or twice through the cell thickness), and completely diffuse reflection (light passes through $2n^2$ or $4n^2$ times the cell thickness)[12,13] are shown in these three figures as dotted and dashed lines.

2.4.3 Discussion and Comparison with Calculations

Since a different spectrum and different wafer thicknesses were used for the theoretical calculations of Green and Campbell,[14] the J_{sc} results cannot be compared directly; however, the relative performance of the light-trapping structures can be compared.

For the configurations in Sections 2.4.1.1 and 2.4.1.2 (no back-surface reflector), one discrepancy is clear; the double-side-textured case shows clearly less absorption than predicted by Green and Campbell, whose calculations showed it to be better than the single side texture and very close in efficiency to the cross-groove case. The explanation

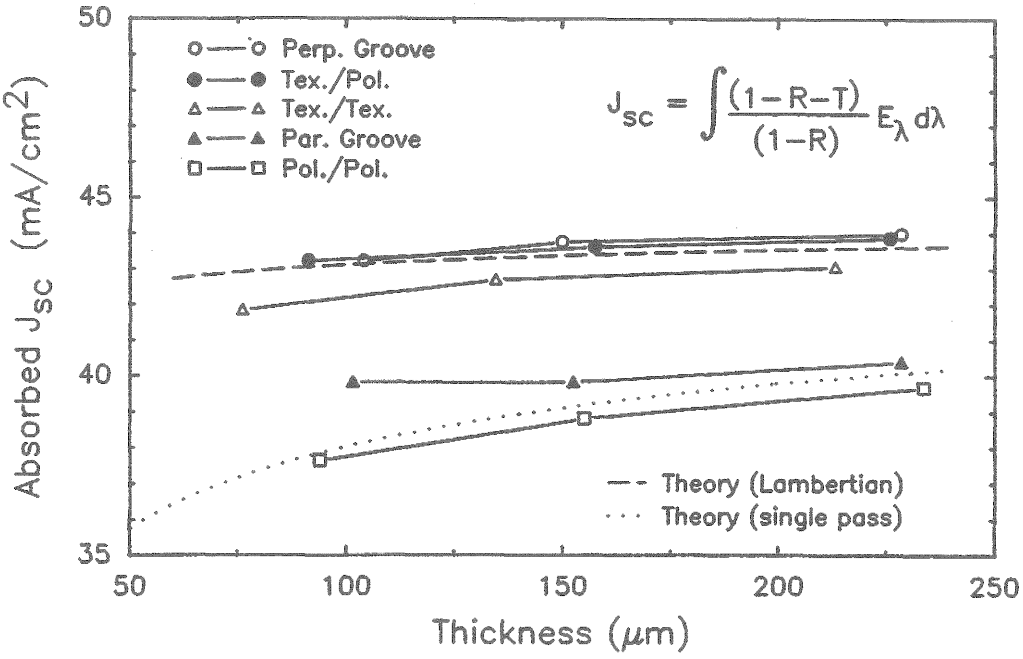


FIGURE 2-9. TOTAL ABSORBED CURRENT IN EACH OF THE SAMPLES FROM FIGURE 2-6.

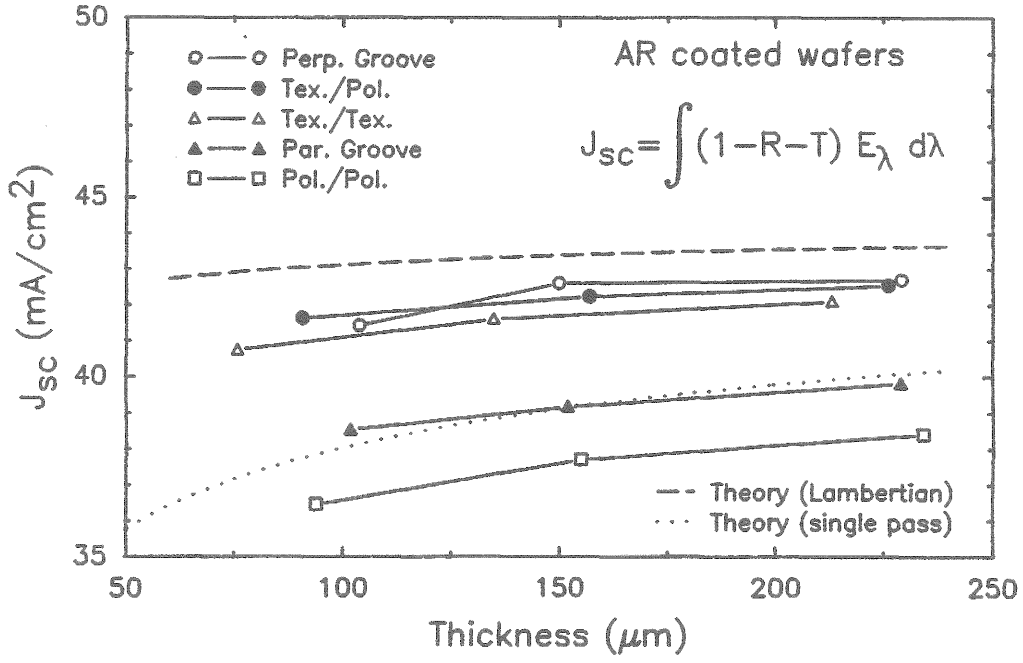


FIGURE 2-10. TOTAL ABSORBED CURRENT IN EACH OF THE SAMPLES FROM FIGURE 2-7. This is an underestimate of the solar cell current, since there is no back-surface reflector.

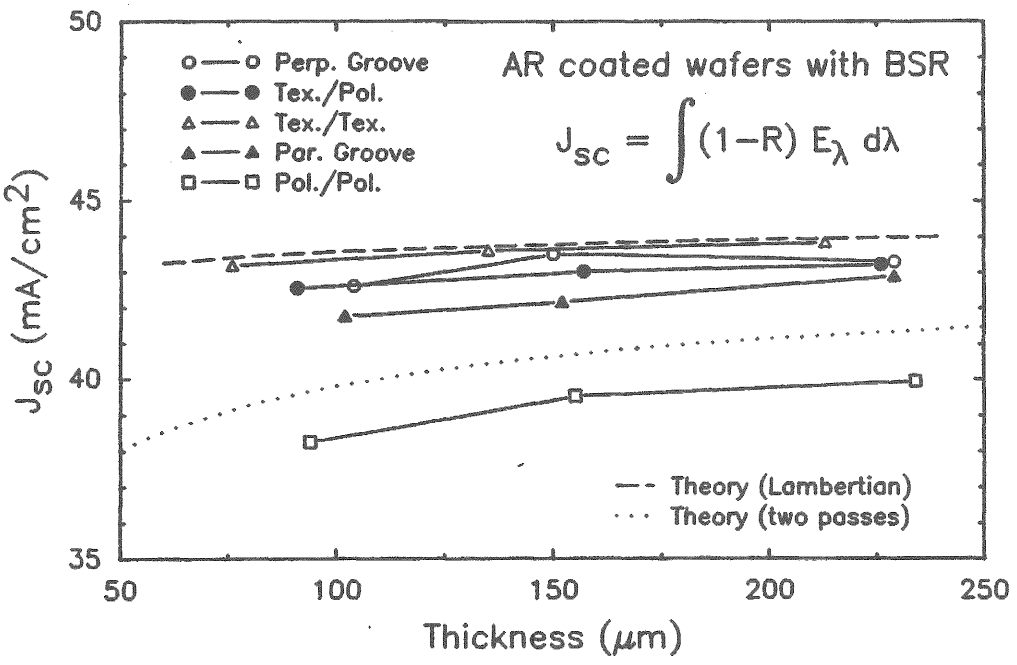


FIGURE 2-11. TOTAL ABSORBED CURRENT IN EACH OF THE SAMPLES FROM FIGURE 2-8. This is an overestimate of the solar cell current, because some light is absorbed by the metal.

presumably lies with the absence of the back-surface reflector. A significant fraction of the light incident on the double-side-textured wafer can escape from the back surface after one pass, instead of being trapped by total internal reflection. This is not the case for the single-side-texture or cross-groove cases. With the back-surface reflector, this light is trapped and the comparative advantage of the cross-groove cell is reduced. The polished wafers also showed proportionately lower absorption in these structures compared to the calculations; the same reason applies to them.

It is clear, however, that the cross-groove structure with the applied back-surface reflector shows lower total absorption than expected from theory; in fact, it is lower than that of the double-side-textured case. However, examination of Figure 2-8 shows that the absorption is higher even at 1300 nm, where absorption in the silicon is expected to be very small. These measurements have not given us enough data to correct for the absorption in the metal, but it is possible that the true difference in carrier generation is as small as that predicted in Ref. 14.

2.4.4 Reduction of Shadow Loss

Reflectance measurements were made on completed cells (also using the integrating sphere) to determine the extent of the reduction in effective shadow loss from the V-groove structure. The effective shadow loss is reduced by reflection of light from the grid line onto the adjacent non-metallized face of the groove, where it is absorbed and contributes to the photocurrent. In analyzing these data we made use of an "effective shadow loss" x', defined as:

$$1 - R_g = x\, A_m + (1-x')(1-R_b), \tag{2.5}$$

where R_g is the reflectance of the cell with grid lines, R_b is the reflectance of the same cell without grid lines, A_m is the optical absorption of the metal lines themselves, and x is the actual (geometric) shadow loss. The measured reflection R_g corresponds to:

$$R_g = x\, R_m\, R_s + (1-x)\, R_b + x\,(1-R_m-A_m), \tag{2.6}$$

where R_s is the reflectance of the second facet which the incident light strikes. R_m, which is the fraction of light incident on the metal which is reflected onto the active area, is given by:

$$R_m = (1 - x'/x)\,[(1 - R_b) / (1 - R_s)]. \tag{2.7}$$

Table 2-4 gives typical values of these quantities, measured at 600 nm on a grooved and a textured surface. Theoretical values of 0.017 for A_m and 0.345 for R_s were used; x was measured optically in a microscope.

TABLE 2-4. GRID LINE REFLECTANCE MEASUREMENTS.

	Grooved Wafer	Textured Wafer
Bare wafer reflectance, R_b	0.099	0.103
Reflectance with grid, R_g	0.151	0.158
Grid coverage, x	0.102	0.093
Effective shadow loss, x'	0.060	0.063
Fractional reduction, $1 - x'/x$	0.41	0.32
Metal-to-cell reflectance, R_m	0.564	0.438

It appears that the grooved structure has considerably reduced the reflection loss of the grooved cell. The reduction in this grooved sample is somewhat greater than that in the textured sample, despite the flat area on the grid line which appears from SEM micrographs to cover about one third of the metal area. Any further process development which allows the flat area to be reduced will therefore result in a corresponding decrease in the shadow loss.

SECTION 3
REDUCTION OF RECOMBINATION

As is the case with all high-efficiency p-i-n structures, these cells require a complex contact structure combined with surface passivation as complete as possible in order to give high efficiency. Although the fabrication of this structure was not completed under this contract, some work was done in that direction.

3.1 SURFACE PASSIVATION

An attempt was made to measure the surface recombination velocity in these cells by fitting the observed blue response to a theoretical model. This fitting was not able to give a precise value, only to establish an upper limit of 2×10^4 cm/sec. Figure 3-1 shows the internal quantum efficiency of a typical cell, along with values calculated from the theoretical model. The difference between zero surface recombination and 1.7×10^4 cm/sec is less than the experimental error in this case.

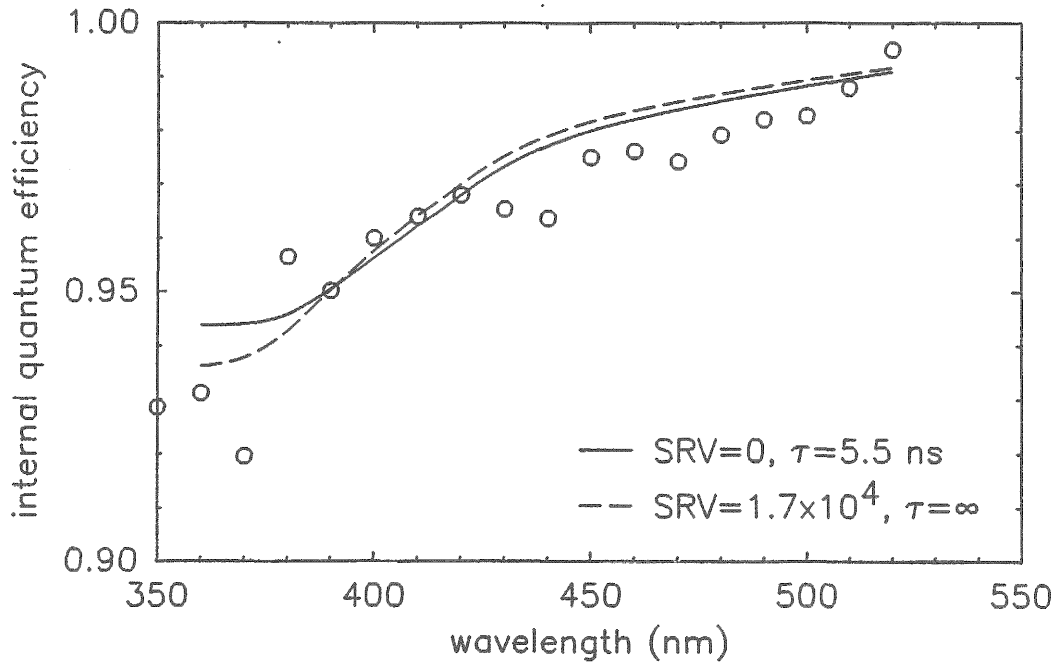


FIGURE 3-1. INTERNAL QUANTUM EFFICIENCY OF A REPRESENTATIVE CELL (#5096-17-10), COMPARED TO THEORETICAL MODELS. The measured recombination is too small to make an accurate measurement of the surface recombination velocity possible by this method.

The imprecision of the fit can be attributed to two reasons: first, the model assumes a uniform emitter and neglects the effect of the electric field produced by the doping gradient. This field reduces, in effect, the surface recombination velocity, and also changes the collection efficiency versus depth function. Second, it appears from the model that the recombination is dominated by the emitter itself, rather than the surface. That is, the surface recombination is low enough that it contributes only in a minor way to the loss of carriers generated by blue light, and, in consequence, the model cannot discriminate differences in surface recombination velocity as small as 10^3 cm/sec.

Increasing the junction depth would be expected to increase both the surface recombination and the emitter bulk recombination. If repeated with deeper junctions, these measurements might allow them to be separated more accurately, particularly if measurements with different junction depths could be compared.

3.2 JUNCTION DESIGN

The second element of recombination reduction is the reduction in the junction area. This proved to be crucial in the Stanford point-contact IBC cell and is expected to play a similar role in the bifacial structure employed here.

Theoretically, the ideal structure should be one like that shown in Figure 3-2, in which both the front and back contacts are made to small junction spots which cover a small fraction (on the order of 1%) of the cell area. While it did not prove possible to fabricate such a structure in this project, preliminary steps were taken in that direction.

3.2.1 Junction Under Busbar, Lot 5121.2

In one of the experiments, the effect of reducing the junction area was assessed by comparing the two structures shown in Figure 3-3. One group of cells had junction area extending over the entire cell, including the busbar, while in the other group, the junction was confined to the active area, and the material under the busbar was not implanted. Table 3-1 gives the results obtained for this comparison, which was carried out using grooved cells.

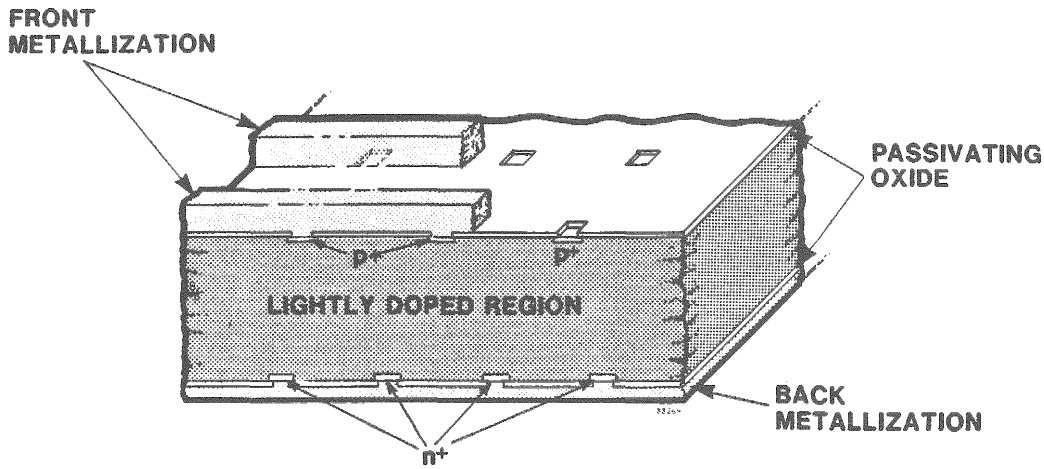


FIGURE 3-2. IDEAL BIFACIAL SOLAR CELL STRUCTURE. The p-type and n-type contact area are both kept very small, as in the case of the Stanford IBC cell.

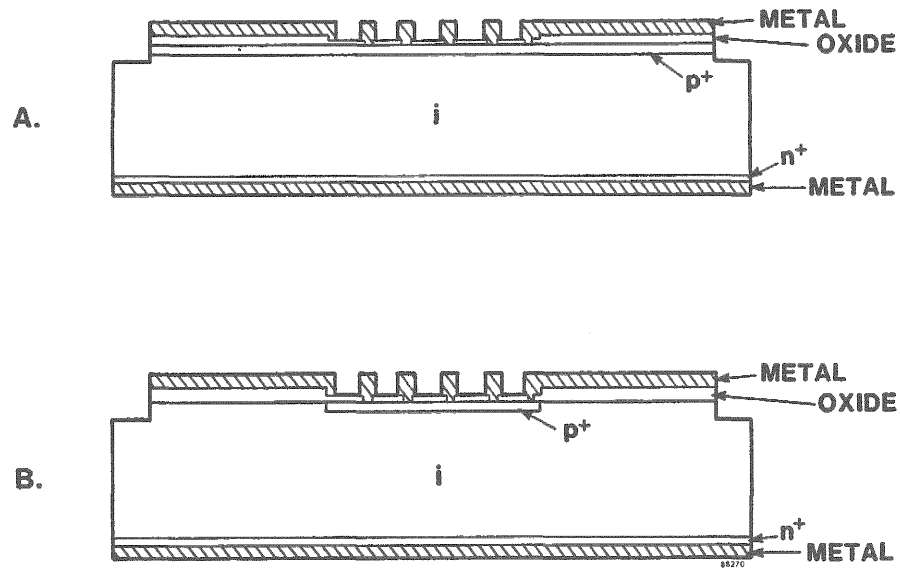


FIGURE 3-3. JUNCTION AREA REDUCTION INVESTIGATED IN THIS WORK. a) normal structure: the implanted area covers the entire cell, including the busbar area, b) reduced junction area: only the active area of the cell is implanted.

TABLE 3-1. EFFECT OF EMITTER AREA.
(Lot 5121.2)

Structure (see Fig. 3-3)	V_{oc} at 1 sun (mV)	V_{oc} at 5 suns (mV)
A (wafers 1-6)	515 ± 12	578 ± 18
B (wafers 7-12)	562 ± 8	610 ± 14

These results clearly show a lower dark current for the cells with smaller junction area. Furthermore, the difference persists up to at least 5 suns, despite the fact that the extra junction area under the busbar is connected to the cell contacts only through a relatively high-resistance current path. These results indicate that the relatively large junction area is the primary reason for the high saturation currents and low voltages seen here.

3.2.2 Reduced Back-Surface Contact Area

A similar design for the back surface was investigated as well. The structures shown in Figure 3-4 were compared, for both n-type and p-type back surfaces. Only the contact area was reduced in these experiments, not the actual junction area. Reduction of the ohmic contact area makes possible a reduction in saturation current similar to reducing the junction area by using a thin, electrically transparent, back-surface doped layer together with oxide passivation.

This experiment was carried out for both n-type and p-type back-surface layers, with two different doping levels. The high doping level ($\sim 2 \times 10^{19}$ cm^{-3}) was that normally used for metallized back surfaces, designed to provide a strong back-surface field to keep carriers away from the ohmic contact, and the lower doping level ($\sim 5 \times 10^{18}$ cm^{-3}) was designed to be transparent to minority carriers and provide low recombination when combined with a passivated surface. The results of this experiment are given in Table 3-2.

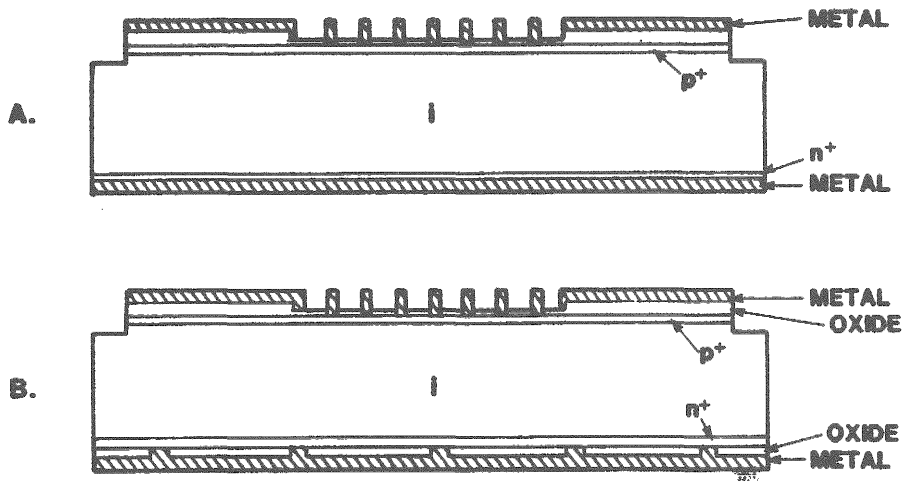


FIGURE 3-4. REDUCTION OF BACK-SURFACE CONTACT AREA. a) normal structure: the metal contacts the entire cell area, b) reduced contact structure: the metal contacts the cell on less than 1% of the total area.

TABLE 3-2. RESULTS OF BACK-SURFACE CONTACT EXPERIMENT. (Lots 5062 and 5096)

Back-Surface Type	Contact Area (%)	Doping	V_{oc} (mV)	Series Resistance (ohm-cm^2)
p	100	high	556 ± 6	0.2 ± 0.07
p	0.2	high	555 ± 4	2.8 ± 2.4
p	100	low	533 ± 6	0.17 ± 0.03
p	0.2	low	542 ± 8	1.8 ± 1.3
n	100	high	559 ± 21	1.2 ± 0.9
n	0.2	high	563 ± 14	1.0 ± 0.4
n	100	low	463 ± 35	6.2 ± 7.3
n	0.2	low	460 ± 40	11.3 ± 1.7

The series resistance given here is the total series resistance measured on the completed cell. Since the front grid structures are the same, we can expect that most of the variation is due to the back contact.

The reduction in the back-contact area led to significantly higher V_{oc} in only one case: the lightly-doped p-type surface. As expected, the contact area does not influence the V_{oc} in the heavily-doped cases, since the BSF layer is not transparent to carriers. The small differences seen are consistent with the results described in Section 3.2.1 which indicate that the saturation current is dominated by the front surface. Significant improvements could be expected if the front- and back-contact areas were reduced simultaneously.

We suspect that in many cases the high-series resistances seen here are attributable to irregularities in the etching of the small contact holes. We have since seen cases in which bubble formation apparently prevents an etchant from reaching the surface through a small opening in the photoresist. The large variation seen among the wafers bolsters this conclusion; values as low as 0.3 to 0.6 ohm-cm^2 have been measured for all the cases in Table 3-2 except the last. With some processing refinements, including the use of a wetting agent for example, these reduced-area contact structures could be made more reliably.

3.2.3 Emitter Recombination and Current Sublinearity

It is clear from the foregoing results that the front junction is the area of greatest recombination in the cells under this contract. Accordingly, structures such as those described in Figure 3-3 can be expected to show significant improvements over what has been achieved here.

This conclusion is strengthened by the recent work of Green, Zhao, and King,[15] showing that the emitter recombination is greatly enhanced in a high-injection cell at short-circuit and resulting in a sublinear increase in current with illumination level. Replacement of most of the emitter area with an effectively-passivated surface would presumably reduce this recombination as well.

3.3 CONTACT OPTIMIZATION

A number of experiments were carried out to determine the contact resistance of various metals on the emitter of these cells. Although earlier work[16] had shown a low-contact resistance with Al as the contact metal to a similar structure, the measurements here did not show the same results.

3.3.1 Contact Resistance versus Annealing Time Results

An experiment was done to measure the contact resistance of each of three metals: Ti, Al, and Cr, and to find the best annealing temperature for each. Three wafers with the standard emitter structure were prepared with transmission line patterns and coated with the contact metals. Each contact metal was covered by a layer of Pd and a thick layer of Ag before opening the evaporation chamber. Contact resistance was measured after evaporation and liftoff, and again after annealing at various temperatures. (Anneals were done for five minutes in a furnace tube under nitrogen.) Table 3-3 shows the results of this experiment.

TABLE 3-3. CONTACT RESISTANCE MEASUREMENTS.
(Lot 5153)
(values in 10^{-3} ohm cm^2)

Annealing Temperature (°C)	Contact Metal Cr	Ti	Al
no anneal	1.7-9.5	non-ohmic	non-ohmic
300	2.3-28	190	non-ohmic
350	8.2-13	51-240	non-ohmic
400	0.69-2.4	17-170	103-199

Contact resistance measurements were made difficult by adhesion problems which affected these wafers, accounting for the high variability. Furthermore, the higher values in the table (10^{-1} ohm cm^2) are not consistent with the series resistance measurements which were made on complete solar cells in the same run (Section 3.3.2); this casts doubt on the reliability of these results.

3.3.2 Lot 5153 - Effect of Different Metals

To continue these experiments, we fabricated cells using the same three metallization layers and compared their performance. Table 3-4 summarizes these results for the low-resistivity control cells.

TABLE 3-4. CELL RESULTS AS A FUNCTION OF METALLIZATION. (Lot 5153)

	1 sun		16 suns			
Contact Metal	V_{oc} (mV)	FF (%)	V_{oc} (mV)	FF (%)	Eff. (%)	Series Res. (ohm cm^2)
Ti (#15)	592 ± 1	72.8 ± 0.4	692	76.9	18.2*	0.147
Al (#18)	600 ± 2	72.8 ± 0.5	628	73.2	11.3	0.412
Cr (#19)	612 ± 1	79.9 ± 1.7	697	82.5	19.3*	0.062

*with antireflection coating

Clearly, the lowest resistance has been achieved with chromium contacts. However, measurements of other cells from this and other lots indicate that the low resistance is not yet reproducible under these conditions. In view of the low resistances achieved, and of the previous results which indicated that low resistance could be achieved with aluminum,[16] we may conclude that this problem could be solved with further refinement of cleaning, deposition, and annealing procedures.

SECTION 4
CELL FABRICATION

4.1 MASK DESIGN

A photomask set was designed for this project, taking into account the expected parameters of the cell. The design has one additional complication which is not found in a conventional polished or textured cell: the front grid lines must align with the V-grooves, placing some restrictions on the line spacing. Since other current research projects have used a 1.25 cm square cell, designed for 100 suns concentration, this same size was chosen for these cells. However, projections indicated that a slightly higher efficiency was possible with a smaller cell at higher concentration, so a 0.5 cm cell was designed as well, intended for a concentration near 500 suns.

Previous work had indicated that lines of 5 micron width and 5 micron height were possible on a polished surface. Although the possibility remained that this work could not be duplicated on a grooved surface, these values were used as a starting point.

A straightforward parallel-finger design was used, in which all the grid lines run in the same direction. While a slightly higher efficiency is possible with a symmetrical design in which all fingers lead to the nearest part of the busbar, comparing parallel-groove and perpendicular-groove structures in that case would require an additional mask and front-to-back alignment. The single-direction design was chosen for reasons of simplicity; the back of the wafer can be grooved using a full-area groove mask.

Preliminary experiments indicated that 15 micron wide grooves, which are 10 microns deep, were amenable to photolithography. Since the prospect of photolithography on larger grooves seemed unlikely (the unevenness of the resist depth creates serious problems), this was selected for our groove pattern. Calculations indicated that a grid spacing of 45 microns (one grid line every three grooves) was close to optimum for both cell sizes.

The grid line mask used for this program is shown in Figure 4-1. Cells with linewidths of 4, 5, and 6 microns were provided for each cell size. The cells are positioned to allow a maximum number (two large cells and three small cells) on a two-inch wafer. Transmission line patterns (for measurement of contact resistance) are included; this measurement can be done with grooves either parallel or perpendicular to the current flow, or with no grooves.

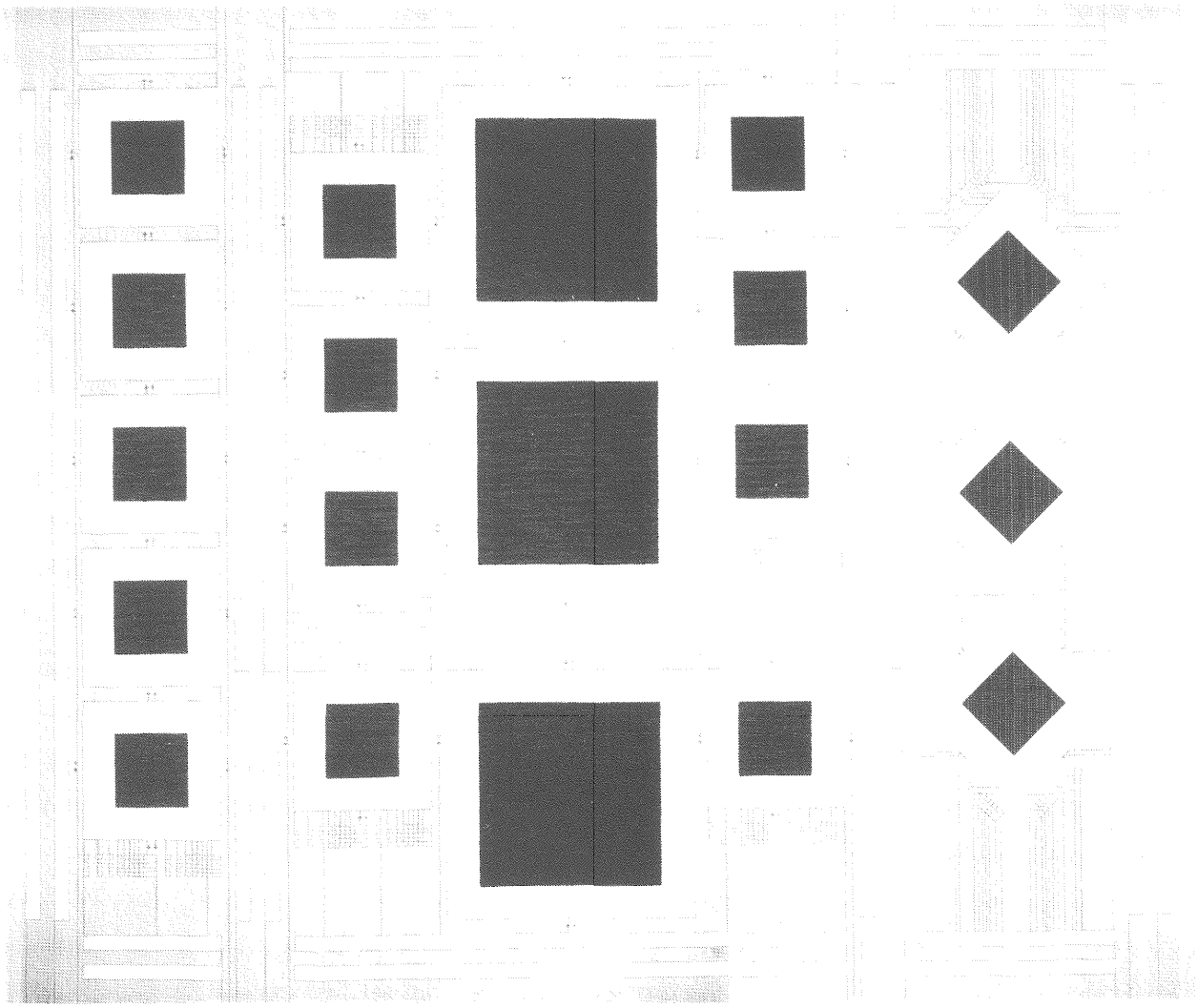


FIGURE 4-1. MASK DESIGN USED FOR THIS PROJECT. Two cells sizes, 0.5 cm and 1.25 cm, are provided with various line widths. Transmission line patterns are included as well.

The parameters used for the grid design, and the theoretical performance of the grid, are given in Table 4-1.

TABLE 4-1. GRID DESIGN PARAMETERS.

Property	0.25 cm^2 Cell	1.5625 cm^2 Cell
Cell Width (cm)	0.5	1.25
Cell Length (cm)	0.5	1.25
Concentration (suns)	500	120
1-Sun Active Area Current (mA/cm^2)	39.8	39.8
Voltage at Maximum Power (V)	0.766	0.729
Sheet Resistance (ohm/square)	150	150
Metal Resistivity (micro-ohm-cm)	2.0	2.0
Contact Resistance ($ohm-cm^2$)	10^{-5}	10^{-5}
Ideal Efficiency (no shadow or series resistance losses)	30.5%	29.0%
Grid Line Width (μm)	5	5
Fraction of Light striking grid line which is reflected onto the active area	0.80	0.80
Effective Grid Line Width (μm)	1.2	1.2
Grid Line Height (μm)	5	5
Grid Line Spacing (μm)	45	45
Shadow Loss (%)	2.7	2.7
Grid Line Resistance Loss (% of ideal cell output)	2.0	3.1
Sheet Resistance Loss (% of ideal cell output)	0.7	0.2
Effective Series Resistance (ohm)	0.0040	0.0032
Predicted Efficiency	28.8%	27.3%

4.2 PROCESS DEVELOPMENT

The cell design which optimizes light trapping utilizes a V-groove surface. Although Spire had experience in V-groove etching, the technology had not been applied to solar cells prior to this program. Cells with textured surfaces have been fabricated with pyramid heights of up to ten microns in previous work at Spire. Our experience in processing non-planar surfaces enabled us to develop a process for V-groove structures in a relatively short time.

Some of the concerns we had in the early development stages were V-groove profiles, ability to properly coat V-groove wafers (10 μm peak-to-valley height) with photoresist, alignment of the metal grid lines atop the narrow groove peaks, and metal-lift-off procedures for five-micron grid line height. Each of these areas presented different problems for processing; however, in order for the process to succeed, it was necessary that each step give consistent results. An outline of the process used to fabricate the V-grooved cells is shown in Table 4-2.

TABLE 4-2. CELL FABRICATION PROCESS OUTLINE.

1.	Thin Wafers to Desired Thickness
2.	Deposit Si_3N_4, Pattern and Etch V-grooves
3.	Deposit SiO_2 and Pattern for Junctions
4.	Ion Implant n^+ and p^+
5.	Anneal and Grow Passivating Oxide
6.	Pattern Resist for Metal Lift-off
7.	Metal Evaporation and Lift-off
8.	Sinter
9.	Deposit AR Coatings
10.	Dice
11.	Test

Processing related to V-groove structures will be discussed in this section. Development work required to fabricate V-groove solar cells, specifically steps 2, 6, and 7 in Table 4-2 will be detailed.

V-Groove Etch Development

V-shaped grooves can be etched in single-crystal silicon if the orientation is (100) normal to the surface. V-grooves will form if openings in an etch mask are aligned with the trace of the (111) plane in the (100) surface. The (111) plane can be referenced from the primary flat on a (100) wafer. A number of hydroxide etchants can be used including KOH, NaOH and NH_3OH. For this development effort KOH was used since Spire has had extensive experience with this etchant.

Silicon nitride (Si_3N_4) deposited by low-pressure chemical vapor deposition (LPCVD) was used as an etch mask. Spire does not have this capability in-house, so that wafers were sent to an outside vendor for coating. LPCVD Si_3N_4 is a high-quality nitride with a low pinhole density which etches slowly in KOH as compared to the etch rate of silicon. SiO_2 etches considerably faster than Si_3N_4, so it can only be used under certain conditions.

Wafers were coated with Si_3N_4 following thinning of the wafers. At this point the Si_3N_4 etch mask was patterned for the V-groove etch. A set of photolithographic etching masks was designed and purchased. The photomask for V-groove patterning consists of a series of parallel lines 5 μm wide with 15 μm center-to-center spacing. The pattern on the mask must be aligned to the flat of the wafer, which results in the 5 μm lines being parallel to the (111) plane.

Spire's photolithography lab utilizes a contact aligner, which puts the wafer and mask in intimate contact. The operator is allowed to move the wafer in order to align it to the mask. In this case the flat of the wafer is placed beneath the lines on the mask and rotated until the flat edge is parallel to the 5 μm mask lines. The mask pattern is transferred to the Si_3N_4 by exposing the resist to UV light, developing it and etching the Si_3N_4 in a plasma etcher. The result should be 5 μm wide Si_3N_4 lines which are parallel to the wafer flat.

Our first attempt at this alignment made us realize the difficulty of using the flat of a wafer, which we found to be lacking a clean straight edge. Another problem with this alignment was the mask pattern which consists of closely spaced lines. We realized that a separate line some distance away from the mask pattern would have allowed us to see the wafer flat without interference from the other lines on the mask. Our first two attempts at patterning the Si_3N_4 and etching the V-grooves resulted in what appeared to be an early success. The grooves were nicely formed with plateaus at the top of the grooves between 1-2 μm wide. For reduction of reflectance losses, it is important that the plateau on the groove tops should be as narrow as possible. Figure 4-2 shows the groove profile after our first attempt.

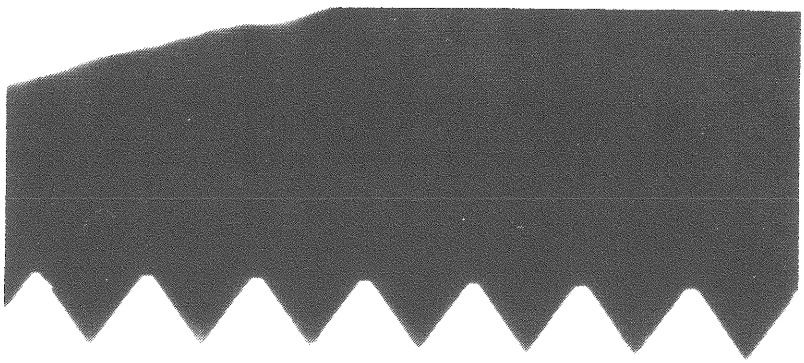


FIGURE 4-2. V-GROOVE PROFILE, 90 MINUTE ETCH IN KOH, FLAT AREA ON GROOVE PEAKS ABOUT 2 μm WIDE (1000X MAGNIFICATION).

We assumed that the difficult alignment was the cause of the wider than desirable flat tops on the V-groove. We tried various techniques to remove this difficulty, such as cleaving the wafer parallel to the flat in hopes that this would result in a clean straight edge, and we also attempted to improve the optics on the contact aligner. In spite of these efforts the alignment was still challenging.

Once a process had been developed to form V-grooves, sample preparation began for light-trapping structures; see Section 2. A total of 18 wafers was prepared for V-groove etching. Some were to have grooves on one side only and others on both sides. We thought that this number of wafers would demonstrate whether we could consistently align the wafer to the mask properly. As the wafers were etching in the KOH solution,

it was observed that some wafers were etching at a faster rate than others, and some seemed to stall in the etch. The result of this was V-grooves with non-uniform profiles; the width of the flat tops varied from 1 μm to 5 μm. The wide variation in plateau width was a real concern. In order to develop a photo process for metal lift-off we needed to consistently etch V-grooves with plateaus of 1 μm or less. Various possibilities existed which might explain the non-uniform etching, such as incomplete etching of the etch mask, non-uniform temperature or agitation of the etching solution, or misalignment of the wafer to the mask pattern. Figure 4-3 shows groove profiles of various wafers etched at the same time. The variation in the width of the flat tops on the grooves can easily be seen.

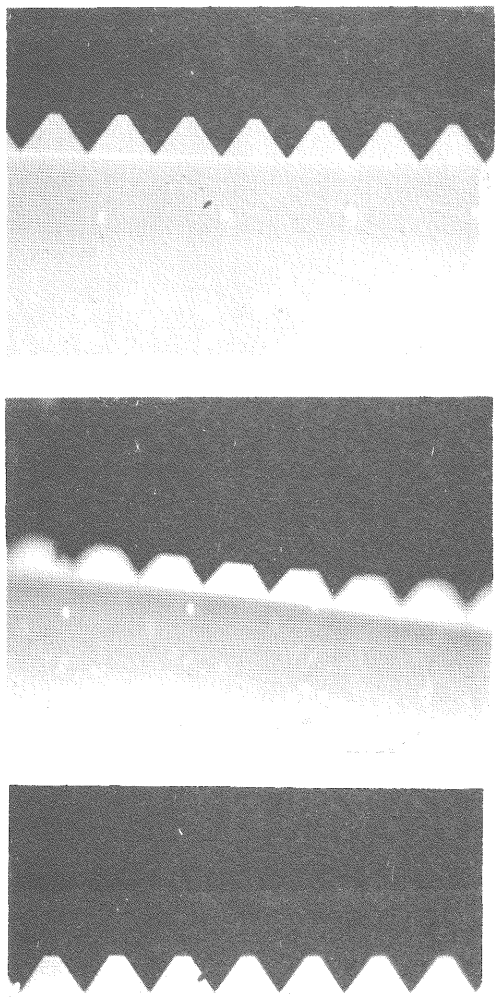


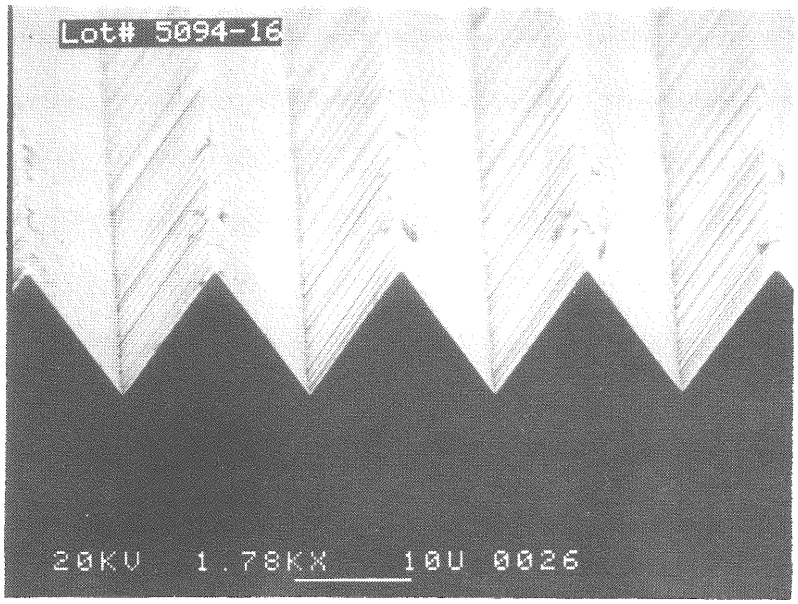
FIGURE 4-3. NON-UNIFORM GROOVE PLATEAUS ON WAFERS ETCHED IN BATCH MODE.

It was evident that the V-groove etch process needed further development since the groove peaks were not as narrow as 1 μm and were not uniform from wafer to wafer. A thorough investigation into the cause of non-uniform groove profiles revealed a somewhat surprising result. Misalignment of the pattern to the wafer was suspected as the cause; this suspicion turned out to be correct. However, it was not exactly as we had suspected. It was thought that wafers with poor groove profiles were not properly aligned to the flat. As it turned out the opposite was true. It was discovered that wafers which were aligned perfectly would stall in the KOH etchant, while wafers slightly misaligned would etch nearly perfect (plateau <1 μm) V-grooves. It is believed that unless there is some misalignment, the etchant is unable to undercut the Si_3N_4 etch mask which is necessary to form narrow-topped V-grooves. The slight misalignment apparently exposes the (100) planes near the Si_3N_4 lines, allowing the etch to undercut the Si_3N_4. If the etch is terminated at the proper time the groove tops will be less than a micron wide. It has been observed that the etch time is critical; that is, if the etch is allowed to continue once the Si_3N_4 lines are completely undercut the V-grooves rapidly erode. Once this requirement of misalignment was realized a new batch of wafers went through the V-groove process, all intentionally misaligned by approximately one degree off the wafer flat. The result was uniform V-grooves on all wafers. Figure 4-4 shows SEM photographs of V-grooves etched after a controlled misalignment. Figure 4-5 shows a photograph of a sample which had V-grooves etched on both sides parallel to each other. A side benefit of the misalignment requirement was less difficulty in the wafer-to-mask alignment. It is somewhat easier to slighty misalign a pattern to the wafer flat than to perfectly align it.

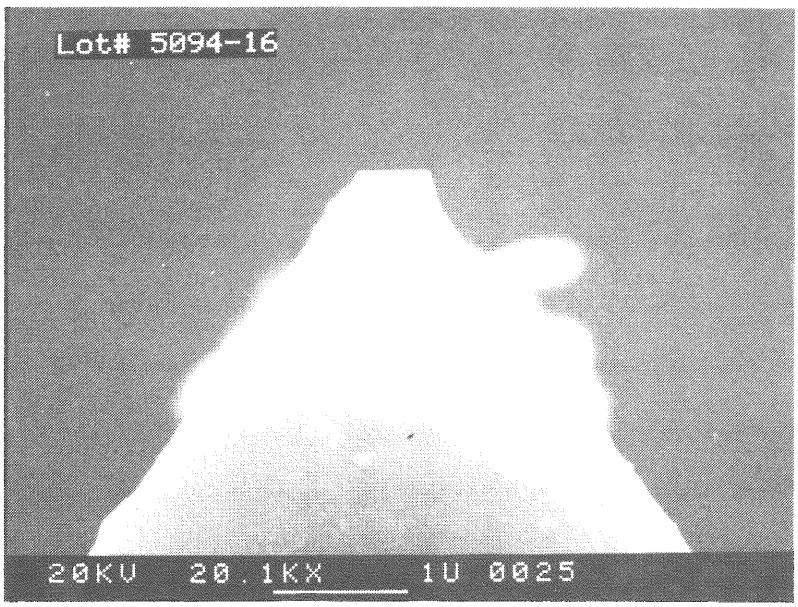
The results of the second batch etching of wafers to form V-grooves gave us confidence that we could consistently etch V-grooves with plateaus of less than one micron.

Pattern Resist for Lift-Off

Following the successful completion of V-groove etch development, work began to pattern photoresist on a V-groove surface in preparation for metal evaporation. This was the second major development area in terms of processing for this cell design. Spire had previously been successful at patterning resist on a textured surface with pyramids up to



A.



B.

FIGURE 4-4. SEM PHOTOGRAPHS OF V-GROOVE PROFILE WITH INTENTIONAL MISALIGNMENT. (a) Series of V-grooves, (b) Single V-groove profile.

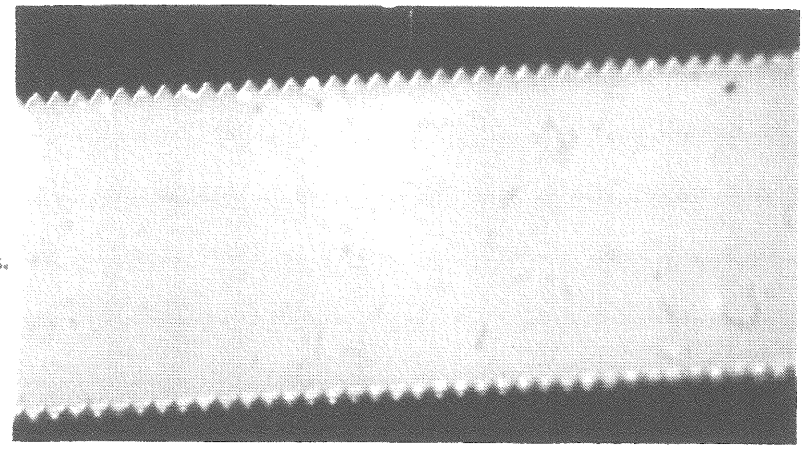


FIGURE 4-5. PHOTOGRAPH OF WAFER WITH V-GROOVES ETCHED ON FRONT AND BACK OF WAFER PARALLEL TO EACH OTHER.

10 microns in height. This prior experience on coating nonplanar surfaces with photoresist resulted in considerably less development time than otherwise may have been required.

The successful development of V-grooves uniform from wafer to wafer with narrow plateaus simplified this second development effort. As a first step in developing this process we needed to identify a photoresist which could planarize the V-groove surface. Spire uses various photoresists which result in resist thicknesses of 1 to 6 μm. A number of wafers which had V-grooved surfaces were spin coated at 4000 rpm with different photoresists. These samples were then taken to a scanning electron microscope where they were cleaved perpendicular to the V-grooves and examined for surface planarity. Three resist types were tried. Two did not planarize the surface, but the third resist (AZ4620) worked nicely. The AZ4620 photoresist normally results in a film thickness of 5 or 6 microns on a polished surface. This same resist was also successful on textured surfaces. Figure 4-6 is a photograph of this resist applied to a V-groove surface. Three groove tops can be seen four microns below the resist surface. This result was very encouraging since a planarized surface minimizes problems in a photolithography process. Figure 4-7 shows a different resist type (AZ1370) which was unable to planarize the V-groove surface.

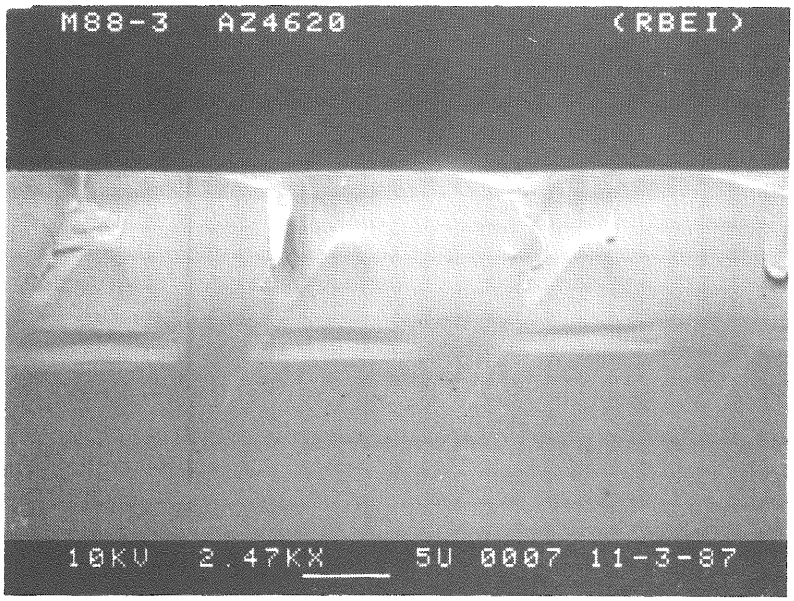


FIGURE 4-6. SCANNING ELECTRON MICROSCOPE PHOTOGRAPH SHOWING AZ4620 PHOTORESIST PLANARIZING V-GROOVE SURFACE.

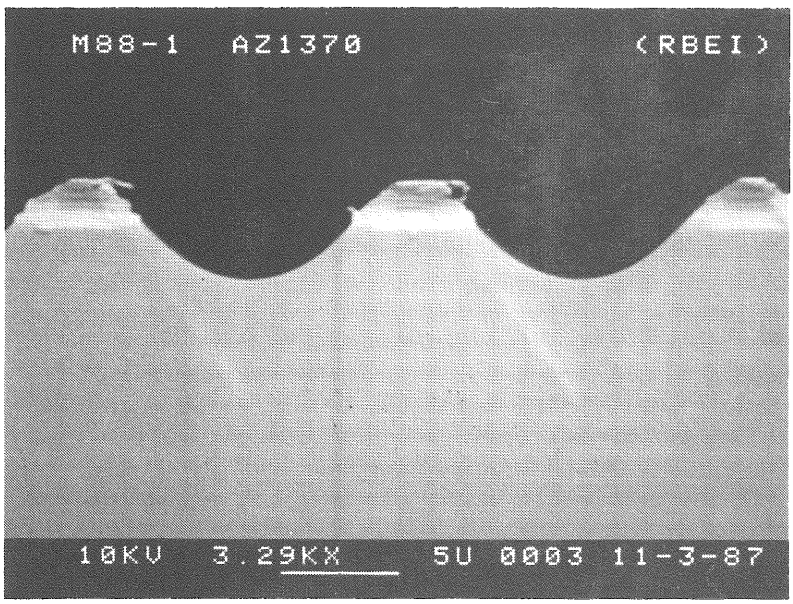


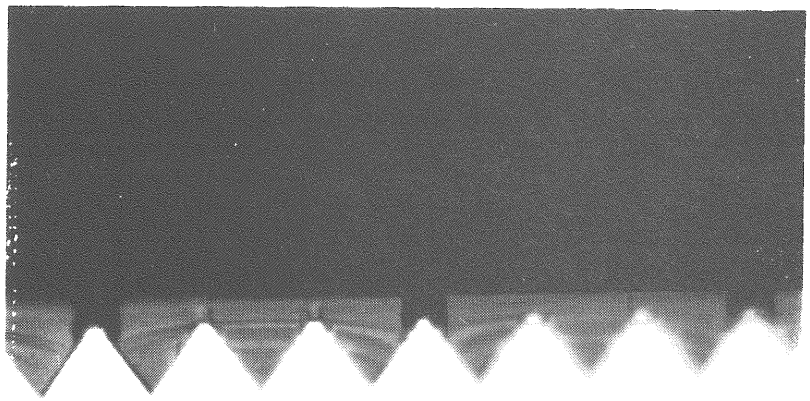
FIGURE 4-7. SCANNING ELECTRON MICROSCOPE PHOTOGRAPH SHOWING AZ1370 PHOTORESIST. This resist unable to planarize the V-groove surface.

After a resist was selected which could planarize the surface, the development effort was directed towards patterning the resist with the new photomask. The mask set included a metal grid mask which had linewidths of 3, 4, and 5 microns. In order to maintain these linewidths, the exposure and develop times are critical and must be monitored carefully. A reverse image process is employed here which results in negative slopes of the resist walls, facilitating metal lift-off. During this part of the development, it was found that another alignment problem would require attention. The alignment of the metal grid photomask (level 3) to the V-groove surface is dependent on the alignment marks from the V-groove photomask (level 1). Due to the V-groove etch, the alignment marks on the wafer were distorted. This resulted in some error when aligning level 3 to level 1. Even a slight misalignment resulted in the grid line openings in the resist being offset from the groove peaks. If the misalignment is severe then the resist depth is more than can be developed and the grid lines will fall off during the lift-off. Due to these factors we had to insure that this alignment could be done with accuracy. After some effort, we were able to protect the Si_3N_4 etch mask in the alignment area; this helped to preserve the original shape of the alignment mark. Although still a difficult alignment, with practice near-perfect alignment of the metal grid to the V-groove structure was achieved regularly. Figure 4-8 shows two wafers after resist patterning; one shows near-perfect alignment and the other shows slight misalignment. At this stage of the photo development, it was time to attempt a metal evaporation and lift-off.

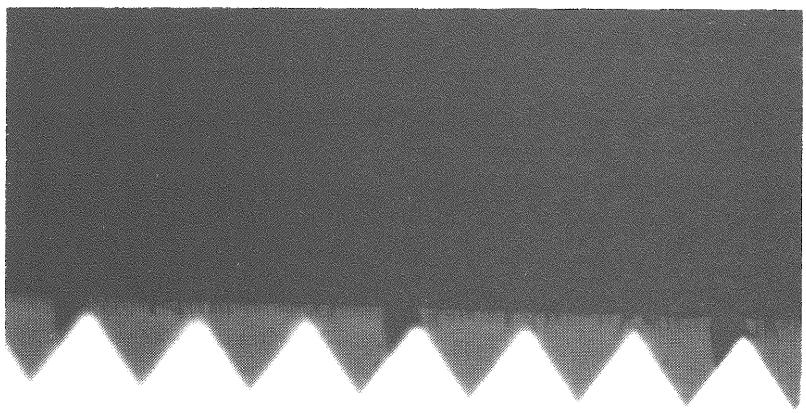
Metal Evaporation and Lift-Off

The cell design called for a metal thickness of four microns for the grid lines. Four micron metal lift-offs are done routinely at Spire on polished and textured surfaces; this same process was applied to the V-groove structures. During metal evaporation the wafers are placed normal to the evaporation source resulting in a highly directional deposition. This prevents bridging of the two metal layers on the resist and on the silicon surface and facilitates an easy lift-off.

Following the photo development, we attempted the metal evaporation and lift-off process on some wafers. The initial attempt was only partially successful. The metal lift-off did work; however, some of the metal grid separated from the wafer as well.



A.



B.

FIGURE 4-8. PHOTOGRAPHS OF V-GROOVE WAFERS WITH RESIST PATTERNED FOR METAL GRID LINES. (a) Good Alignment, (b) Slight misalignment.

The cause of this loss of grid metal was attributed to the misalignment problem discussed under photo development. Figure 4-9 shows the problem rather clearly. The lower layer in the photo shows a trough which is the grid line opening in the resist. This opening is misaligned from the groove peak. Since the resist depth increases as the misalignment worsens, the resist is not fully developed and metal is not in contact with silicon, therefore when the resist is dissolved in a solvent the grid line falls off. The solution to this problem is to accurately align the metal grid pattern to the V-groove surface.

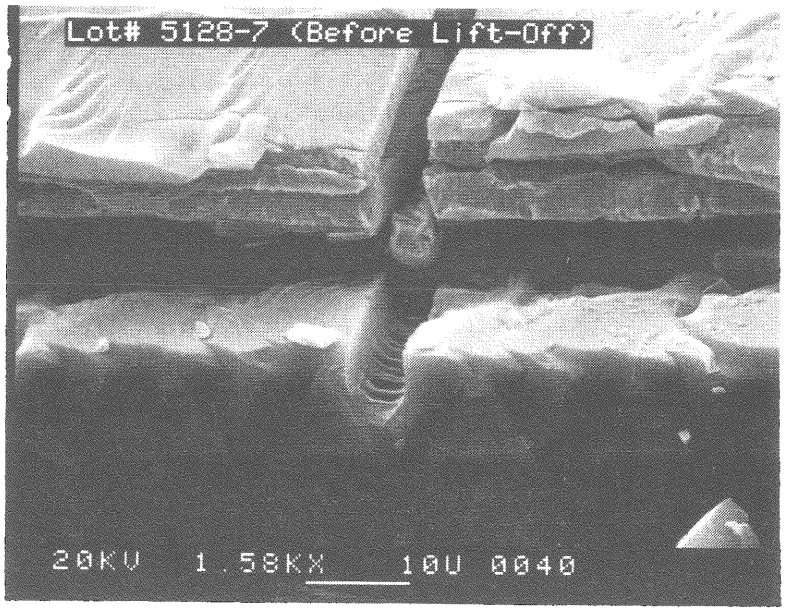
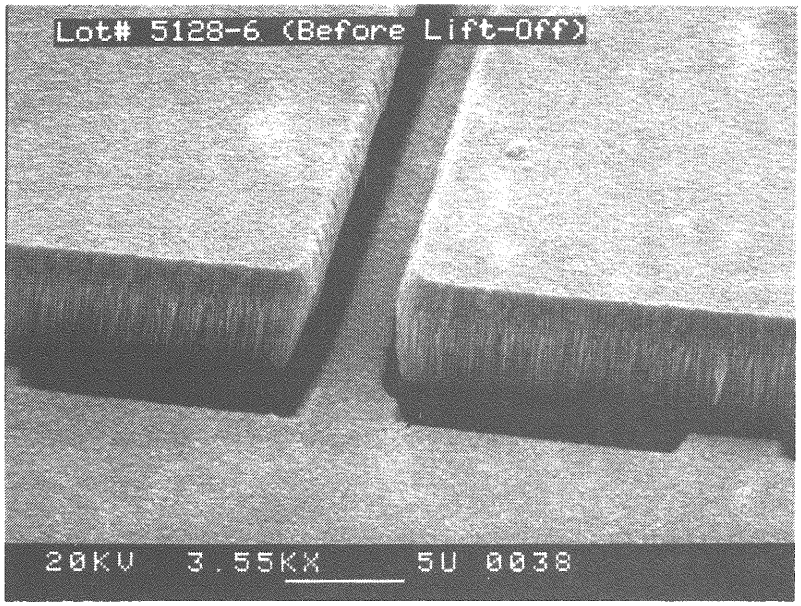
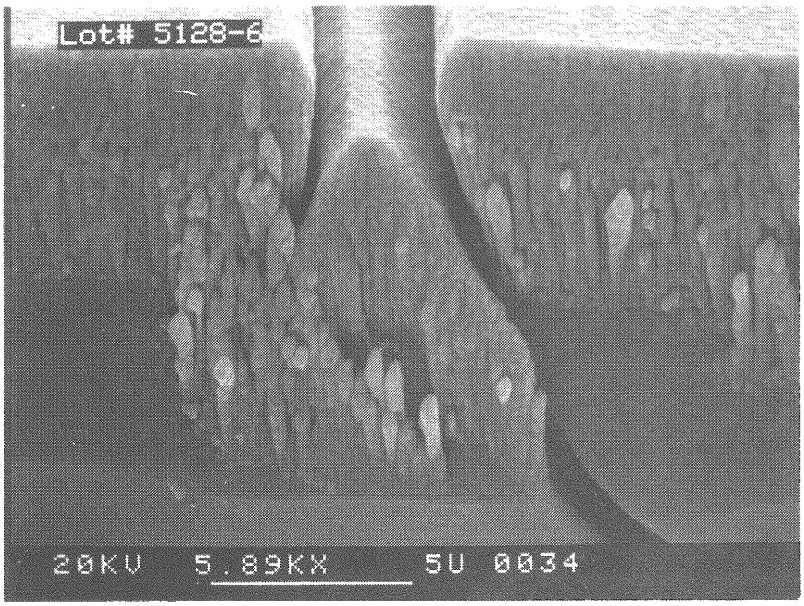


FIGURE 4-9. SCANNING ELECTRON MICROSCOPE PHOTOGRAPH SHOWING RESULT OF POOR ALIGNMENT (see trough in lower layer). Grid line opening in photoresist missed groove peak (to the left) resulting in grid line loss.

In the second attempt the process was successful. The alignment was carefully done during the photo process resulting in grid line openings in the resist centered over the V-groove peaks. Metal was evaporated onto these wafers followed by lift-off. Figure 4-10 shows two SEM photographs of wafers with metal prior to lift-off. They show a clear separation between grid line metal and field metal. There is a height difference because the field metal rests on photoresist. If there were no separation between the two metal layers (metal bridging) the field metal would not lift-off due to the connection to the grid line.



A.



B.

FIGURE 4-10. PHOTOGRAPHS OF V-GROOVE WAFERS AFTER METAL EVAPORATION, BEFORE METAL LIFT-OFF. Separation of metal layers allows for easy lift-off.

Once the metal lift-off process was completed, samples were cleaved in preparation for SEM examination. Results were very good. Grid lines rested on the top of every third peak, approximately four microns in height and three microns wide. Figure 4-11 shows a cleaved sample with a grid line atop the V-groove. Figure 4-12 shows same sample as in Figure 4-11 at a lower magnification; note the grid line on every third peak. The results of this second attempt achieved the goal of the development effort. We had reached the point where we were ready to fabricate functional V-groove solar cells. This concluded Phase I of process development; Phase II was cell fabrication. The effort would now be to integrate processing unique to V-groove structures into our high-efficiency cell process. Cell fabrication will be discussed in the following section.

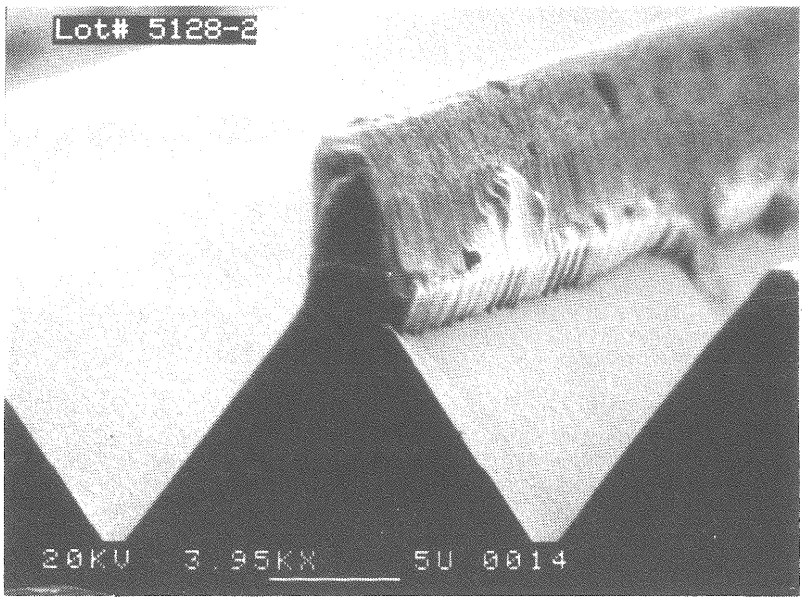


FIGURE 4-11. SEM PHOTOGRAPH OF SAMPLE WITH METAL GRID LINE ATOP V-GROOVE.

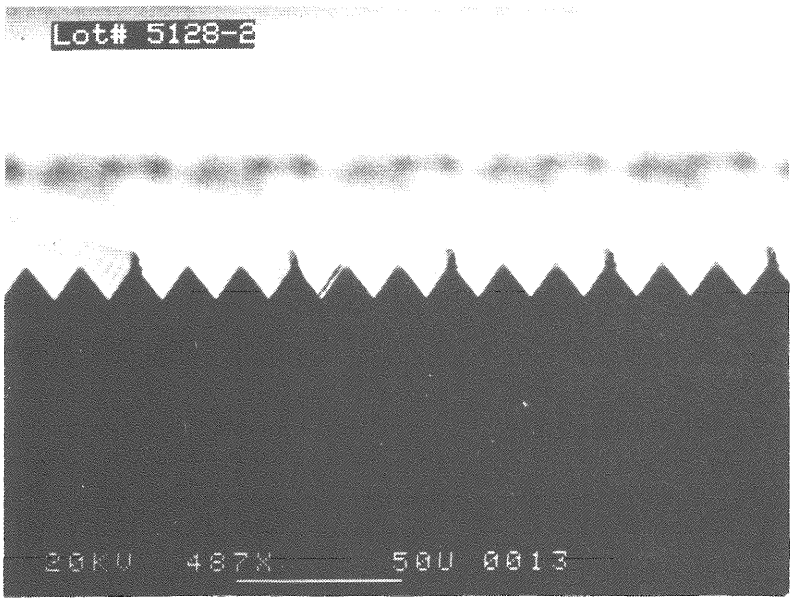


FIGURE 4-12. PHOTOGRAPH OF SAMPLE IN FIGURE 4-10 SHOWING METAL GRID LINES ON EVERY THIRD V-GROOVE.

4.3 CELL FABRICATION

Seventeen wafer lots were processed during this program. These lots were processed under three objectives: process development, light-trapping samples, and cell runs. Light-trapping samples were completed in the first few months, development runs continued midway through the program, and cell runs were processed throughout the program.

Since considerable process development was required before V-groove solar cells could be fabricated, it was decided to process concentrator cells with an existing process. Two lots of non-grooved cells were processed early in the program. This allowed us to evaluate the high-resistivity silicon which was purchased for this program, as well as our silicon processing for high lifetime. One group each of p-i-n (Lot 5062) and n-i-p (Lot #5129) cells (polished surfaces) were fabricated and tested. These lots consisted of both low-(0.15 ohm-cm) and high-(100 ohm-cm) resistivity silicon. Cell results for both lots will be discussed in the next section.

Process development eventually reached a point where fabrication of functional V-groove cells was required. For this purpose an abbreviated high-efficiency process was used. This first wafer lot of V-groove cells (Lot 5132) consisted of full-thickness wafers and did not utilize an implant mask for junction formation or an oxide for bus metal isolation. The processing of this lot went quite well considering it was the first of this type. When completed, cells were tested at Spire and then sent to Sandia for concentration testing; these results will be presented in the following section. The successful completion of this lot without any difficulty concluded initial process development for V-groove solar cells. As other cell lots were processed in this program, processing inconsistencies were corrected and some minor improvements were made. This type of development continued throughout the program.

Other V-groove cell lots followed the initial lot. Lot 5121 was the first run to go through the high-efficiency process. With each new lot, we incorporated a new element of our high-efficiency process including the thinning of wafers. As early cell results were analyzed, we suspected a lifetime problem with the silicon. To determine if it was a processing related problem, wafer lots were started to investigate lifetime degradation in various areas of the process. Lot 5129 was intended to investigate the possibility

of contamination from the SiO_2. In this lot, which consisted of polished cells, three different systems were used to deposit SiO_2 on wafers. This allowed us to compare the SiO_2 quality and determine that the SiO_2 from two of the systems were satisfactory and that the other system resulted in slightly lower cell efficiencies. A second lot (Lot 5138) investigated the cooling rate of our post implant anneal cycle. Lot 5138 was annealed in two groups, one group had the normal 4°C/min ramp down, the second group was ramped down at 1°C/min. The result of this investigation indicated a slightly higher average open circuit voltage for the slower cooling rate. The difference was too small to be considered conclusive.

Lot 5147 was a lot of thin V-groove concentrator cells which went through the high-efficiency process, except that no SiO_2 isolation was used. When front metal contacts were evaporated on this lot, different contact metals were tried in an effort to minimize contact resistance. Chromium and titanium were used; titanium is our standard contact metal. Aluminum was also used as a contact metal on a group of wafers from another lot, so that we could compare contact resistance from the three metals. Results of contact resistance measurements are discussed in Section 3.3.

The last cell lot of this program was Lot 5153 and consisted of low- and high-resistivity silicon. Half of the wafers used SiO_2 for bus metal isolation. Different contact metals were again tried in an effort to minimize contact resistance. The processing of V-grooved cells continuously improved as cells were fabricated during the program. Further improvements could surely be made if this work were to continue. In the timeframe we were working in, the results were quite good from a cell fabrication point-of-view. Although cell efficiencies were not as high as we had hoped, functional V-groove cells were fabricated which had respectable efficiencies. The following section will discuss these results in detail.

4.4 SOLAR CELL RESULTS

This section gives the measurement results on the solar cells made in this work. The first subsection, which tabulates the data, is followed by a summary which discusses the loss mechanisms and implications for design and fabrication. In the data tables of this section, average values are listed, with standard deviations in parentheses. When no standard deviations are present, only one cell was measured.

4.4.1 Cell Data

This section describes the most important lots of cells and the cell performance results obtained from them. V_{oc}, J_{sc}, fill factor, and efficiency were measured with a Spectrolab X25 solar simulator adjusted to AM1.5 direct conditions with a reference cell calibrated at SERI. Cell temperature for all measurements was maintained at 25°C.

Concentration measurements up to 20 suns were taken with the same equipment, assuming linearity of current with intensity; in some cases low-resistivity cells were measured as well to provide a check on the linearity. Representative cells from each lot were sent to Sandia for concentration measurements; those results are reported in Section 4.4.2.

Series resistance was extracted from dark I-V and I_{sc}-V_{oc} measurements; the difference in voltage between these two curves at the same current level I was taken as $I \times R_s$. J_0, the reverse saturation current, was extracted from the I_{sc}-V_{oc} curves as well when possible; however, in many cases the slope of the curve was not close to kT/q at one sun.

Quantum efficiency measurements were made using a monochromator from 300 to 1100 nm. For polished cells, spectral response and reflectance were measured simultaneously; for textured and grooved cells, spectral response was measured and corrected to internal quantum efficiency using reflection curves measured on representative cells with an integrating sphere. Diffusion lengths were extracted from the quantum efficiency data by the method of Stokes and Chu.[17]

Contact and sheet resistances were measured using transmission line patterns on the same wafers as the cells.

I_{sc}-V_{oc} data were analyzed to separate the two saturation current components. A curve-fitting algorithm was used to model the J_{sc} as

$$J_{sc} = J_{01}\exp(qV_{oc}/kT) + J_{02}\exp(qV_{oc}/2kT) + J_{03}\exp(qV_{oc}/n_3kT), \qquad 4.1$$

with four parameters, J_{01}, J_{02}, J_{03}, and n_3.

Assuming the cell is operating under high injection, J_{01} should correspond to the recombination at the surfaces or within the heavily-doped regions, and J_{02} to the recombination in the bulk and at the edges.

Considering the lightly doped region to be characterized by equal electron and hole concentrations and assuming that the applied voltage is equal to the difference in the quasi-fermi levels, we should have

$$J_{02} = qWn_i(1/2t + PS/A), \qquad 4.2$$

where W is the device width, t the carrier lifetime, S the surface recombination velocity at the cell edge, P the perimeter, and A the area.

4.4.1.1 Baseline Cells (n-i-p) (Lot 5062)

This group consisted of polished-surface n-i-p concentrator cells. These cells were made from 100 ohm-cm n-type material, with an n-type implant on the front and a p-type implant on the back. Technically, these are front-surface field cells with the junction on the back, but under high injection the distinction becomes less important. Both normal thickness (9 mil) and thin (1.5-3 mil) cells were made. Cell performance measurements (at one sun, without AR coating) are shown in Table 4-3. (Each entry represents the average of several cells with the standard deviation shown in parentheses.)

TABLE 4-3. n-i-p BASELINE CELLS.
(Lot 5062 - before AR coating)

Back Implant Dose	Back Dot Contact	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF	Efficiency
		wafers 25-28 (9 mil)			
High	No	0.556(0.006)	24.8(0.6)	0.693(0.012)	9.5(0.3)
High	Yes	0.555(0.004)	25.2(0.1)	0.571(0.065)	8.0(1.0)
Low	No	0.533(0.006)	22.3(1.4)	0.675(0.005)	8.0(0.7)
Low	Yes	0.542(0.008)	24.2(0.4)	0.686(0.014)	9.0(0.4)
		wafers 1-20 (thin)			
High	No	0.553(0.008)	22.5(0.4)	0.680(0.021)	8.5(0.3)
High	Yes	0.549(0.002)	23.4(0.3)	0.688(0.004)	8.9(0.1)
Low	No	0.529(0.004)	22.4(0.1)	0.654(0.052)	7.8(0.7)

The high-implant dose, which was intended to create an effective back-surface field for the metallized surface, was 5×10^{15} ions cm^{-2} at 50 keV; the low dose, which was meant to create a thin, electrically transparent layer for the passivated surface, was 5×10^{14} ions cm^{-2} at 5 keV. The reduced-area back contact was made through 10 micron squares on a 380 micron triangular grid, for a total contact area of approximately 0.1%.

Table 4-4 shows further results from the same cells. It was found, as discussed in Section 3.2.2, that some of the cells with reduced contact area (dot contacts) on the back showed high-series resistance, although some did not.

TABLE 4-4. FURTHER RESULTS FROM n-i-p CELLS.
(Lot 5062)

Back Implant Dose	Back Dot Contact	J_{o1} (pA/cm^2)	J_{o2} (nA/cm^2)	Series Res. (ohm-cm^2)	qe @ 1100 nm
		wafers 25-28 (9 mil)			
High	No	3.43(0.41)	220(29)	0.19(0.09)	0.257(0.011)
High	Yes	5.24(0.66)	187(100)	4.01(2.06)	0.324(0.009)
Low	No	3.33(1.01)	596(119)	0.15(0.01)	0.237(0.038)
Low	Yes	6 (1.6)	257(31)	0.56(0.06)	0.306(0.017)
		wafers 1-20 (thin)			
High	No	1.20(0.30)	490(82.5)	0.21(0.04)	0.076(0.005)
High	Yes *	2.22	352	0.37	0.088
Low	No *	4.53	618	0.21	0.074
Low	Yes *	11.3	234	3.14	

*Only one wafer was completed in this category, so no standard deviation could be determined.

As can be seen from this table, J_{02} does not appear to depend on the cell thickness. This presumably indicates that there is another component independent of the bulk which dominates this component.

The spectral response of these cells appears quite encouraging. (See Figure 4-13). The internal quantum efficiency is close to unity throughout the ultraviolet and visible range. A small increase in the long-wavelength response is seen with the presence of the back dot contacts. Although the infrared response is low (since there is no light-trapping), calculations show that the diffusion length is at least twice the cell thickness. Furthermore, low-resistivity control cells made at the same time show the expected diffusion lengths (150-170 microns). Interestingly, a few cells showed very low quantum efficiency at all wavelengths, although their J_{sc}'s were normal.

After AR coating, the cells were remeasured at one sun and at concentration; selected data are shown in Table 4-5.

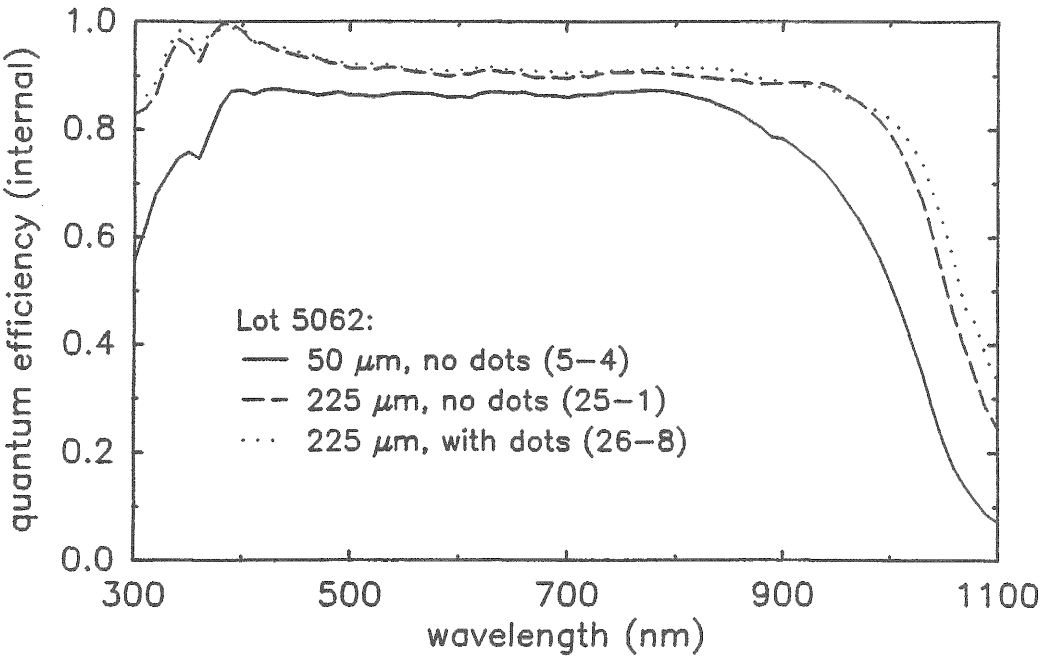


FIGURE 4-13. SPECTRAL RESPONSE OF BASELINE n-i-p CELLS (Lot 50662). Since these cells are polished, they show no light-trapping, but there is still a small effect of the back-surface contact area.

TABLE 4-5. CONCENTRATION RESULTS FROM n-i-p CELLS.
(Lot 5062 - after AR coating)

Suns	V_{oc} (mV)	I_{sc} (mA)	FF	Eff. (%)
High dose, no dots, 51 microns thick (Sandia measurement)				
1.0 (0.0)	566 (3)	10.9 (0.01)	0.695 (0.003	13.5 (0.0)
4.1 (0.0)	622 (4)	44.5 (0.71)	0.746 (0.002)	15.9 (0.1)
20.4 (0.1)	670 (2)	222.5 (2.12)	0.776 (0.005)	17.8 (0.2)
97.9 (1.4)	710 (1)	1067.0 (15.6)	0.774 (0.001)	18.9 (0.1)
187.7 (1.9)	725 (1)	2045.5 (21.9)	0.757 (0.004)	18.8 (0.1)
High dose, no dots, 229 microns thick (Sandia measurement)				
1.0	564	11.52	0.704	14.4
3.9	619	45.	0.754	17.0
18.0	664	207.	0.746	18.0
100.2	712	1155.	0.597	15.4
High dose, no dots, 381 microns thick (Spire measurement)				
1.0 (0.0)	485 (95)	9.86 (0.06)	0.613 (0.046)	9.4 (2.4)
5.1 (0.1)	621 (20)	50.50 (0.50)	0.589 (0.143)	11.4 (3.0)
21.6 (0.3)	680 (3)	212.50 (1.50)	0.682 (0.071)	14.4 (1.5)

Figure 4-14 shows the data measured at Sandia on one of the thin cells without the dot contact. It is clear that the voltage is approaching ideal behavior at high concentrations, but that the fill factor remains low due to series resistance. Sublinearity of current (not shown in the above table) is considerable as well.

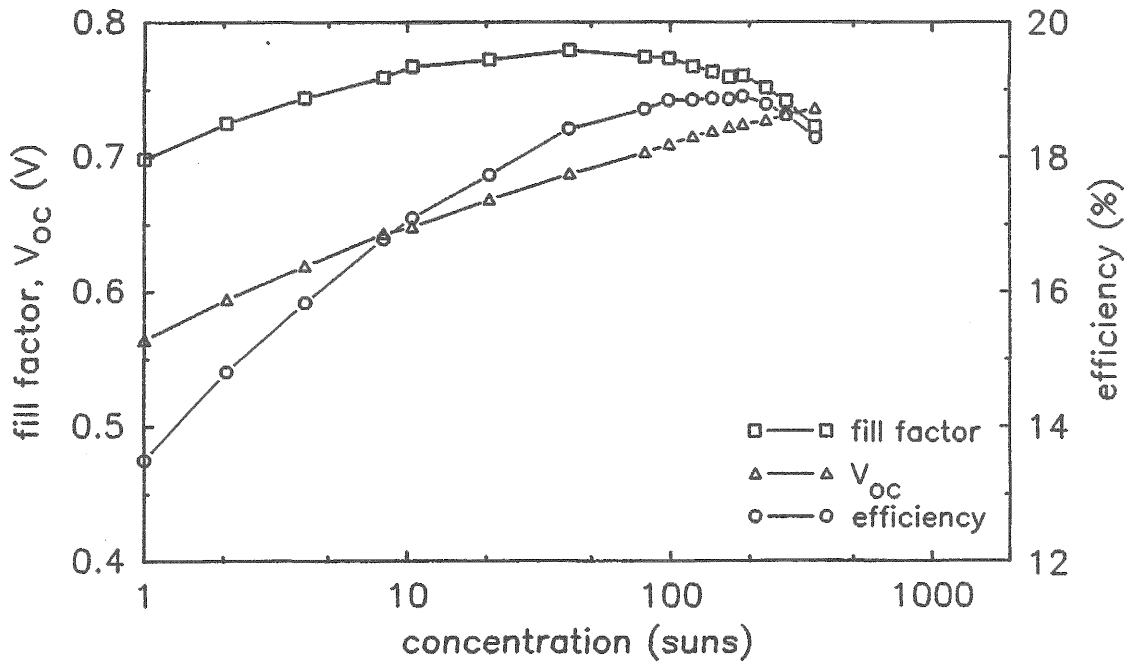


FIGURE 4-14. CONCENTRATION MEASUREMENTS OF BASELINE n-i-p CELL (Cell 5062-9-5). The cell thickness is 50 microns, and the back contact is full area.

4.4.1.2 Baseline Cells (p-i-n) (Lot 5096)

This group of polished-surface cells had a p-i-n structure, allowing useful comparison with the n-i-p cells above. Cell results (without antireflection coating) are given in Table 4-6.

TABLE 4-6. p-i-n CELL PERFORMANCE.
(Lot 5096 - before AR coating)

Back Implant Dose	Back Dot Contact	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF	Efficiency
		Wafers 1-8 (2 mil)			
High	No	0.551 (0.023)	24.0 (0.4)	0.640 (0.061)	8.5 (1.2)
High	Yes	0.555 (0.008)	24.5 (0.4)	0.691 (0.025)	9.4 (0.5)
Low	No	0.488 (0.021)	22.8 (1.0)	0.571 (0.121)	6.4 (1.7)
Low	Yes	0.458 (0.028)	17.0 (4.2)	0.200 (0.028)	1.4 (0.8)
		Wafers 9-16 (4 mil)			
High	No	0.565 (0.017)	25.2 (0.2)	0.703 (0.014)	10.0 (0.4)
High	Yes	0.568 (0.014)	25.1 (0.1)	0.671 (0.023)	9.6 (0.5)
Low	No	0.434 (0.023)	22.4 (2.0)	0.323 (0.078)	3.3 (1.2)
Low	Yes	0.462 (0.046)	22.3 (1.7)	0.255 (0.045)	2.4 (1.1)
		Wafers 17-20 (9 mil)			
High	No	0.571 (0.005)	26.5 (0.2)	0.691 (0.015)	10.5 (0.2)
High	Yes	0.133 (0.008)	21.8 (0.8)	0.303 (0.005)	0.9 (0.1)
Low	No	0.466 (0.005)	23.9 (0.3)	0.638 (0.013)	7.1 (0.3)
Low	Yes	0.450 (0.007)	22.5 (1.0)	0.286 (0.029)	2.9 (0.4)
		Wafers 21-24 (15 mil low-resistivity)			
High	No	0.429	23.5	0.503	5.1
High	Yes	0.386	23.9	0.436	4.0
Low	No	0.326	21.4	0.556	3.9
Low	Yes	0.306	18.0	0.258	1.4

The relatively high dark current which was seen in the n-i-p cells is present here as well. Despite this, some conclusions can still be drawn: first, the low-dose back implant (which in this case was 10^{15} cm^{-2} of phosphorus ions at 5 keV) results in a higher dark current than the high dose (5×10^{15} cm^{-2} at 50 keV). This was expected in the case of the full-area back contact, since the low-dose layer is transparent to minority carriers. In the case of the dot contact, calculations predict a lower saturation current for the low dose.

After some of these cells were completed with their final coating, more detailed measurements were made. (See Table 4-7.) Concentration measurements (Figure 4-15) show a relatively rapid decrease of fill factor with concentration level, and the I-V measurements confirm that the series resistance is high. As explained in Section 4.4.2.2, we attribute this primarily to the contacts.

TABLE 4-7. FURTHER RESULTS - POLISHED p-i-n CONCENTRATORS. (Lot 5096)

Back Implant Dose	Back Dot Contact	Series Res. (ohm-cm^2)	qe @ 1100 nm
		Wafers 1-8 (2 mil)	
High	No	1.59 (1.13)	0.091 (0.036)
High	Yes	0.98	0.126 (0.028)
Low	No	1.57 (1.24)	0.076 (0.013)
Low	Yes		0.113
		Wafers 9-16 (4 mil)	
High	No	1.27 (0.73)	0.151 (0.039)
High	Yes	0.97 (0.58)	0.160 (0.030)
Low	No	13.18 (7.11)	0.078 (0.022)
Low	Yes	13.08	0.092
		Wafers 17-20 (9 mil)	
High	No	0.66 (0.25)	0.207 (0.010)
High	Yes		
Low	No		
Low	Yes	9.62	0.078

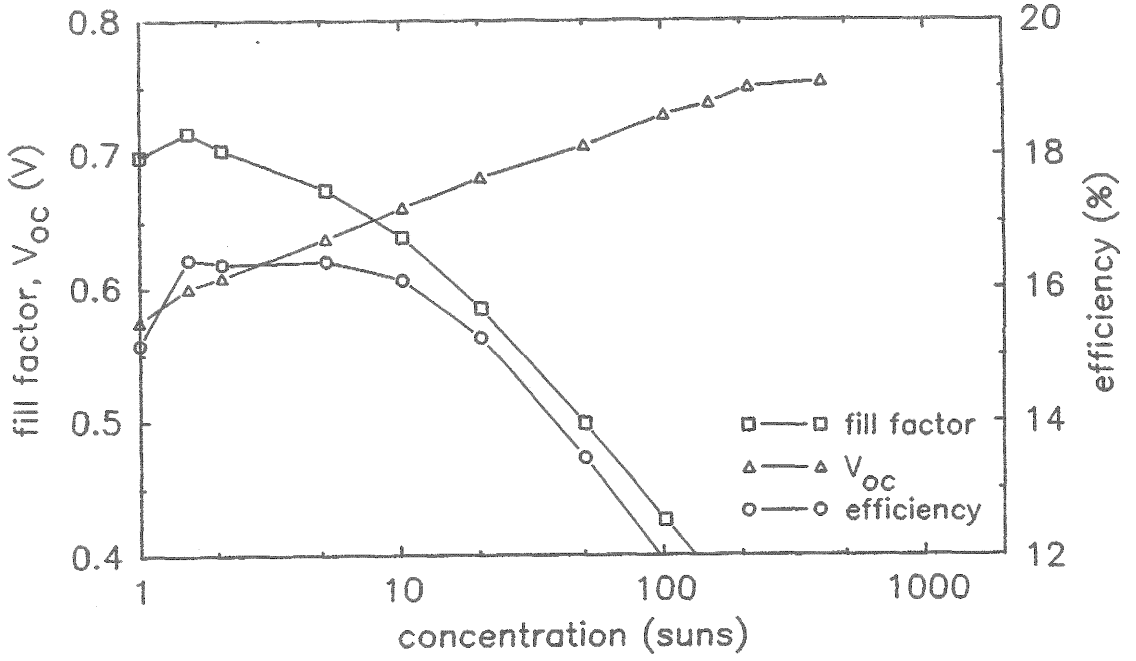


FIGURE 4-15. CONCENTRATION MEASUREMENTS OF BASELINE p-i-n CELLS (cell #5096-17-9). The cell thickness is 225 microns, and the back contact is full area. The high-series resistance is apparent.

As in the previous group, spectral response measurements show the expected high-quantum efficiency, although the low dose back implant results in much lower red response due to a higher surface recombination velocity (Figure 4-16). From these results, it does not appear that the bulk lifetime in these concentrator cells is low; we suspect that the low voltages result from recombination at the edges or surfaces. (See Section 4.4.2.3.)

Spreading resistance measurements were made of the front and back layers from this lot, to verify that the implantation process is yielding the expected doping concentrations. The results (Figure 4-17) are well in agreement with previous work.[18]

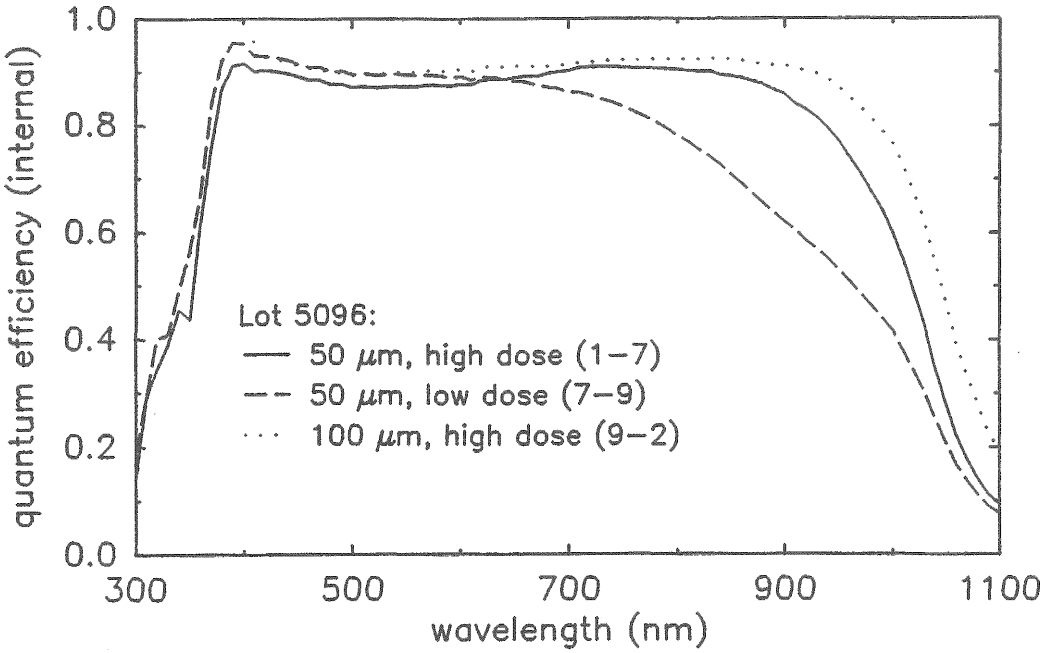


FIGURE 4-16. SPECTRAL RESPONSE OF BASELINE p-i-n CELLS (lot 5096). The low implant dose clearly results in a high back surface recombination velocity.

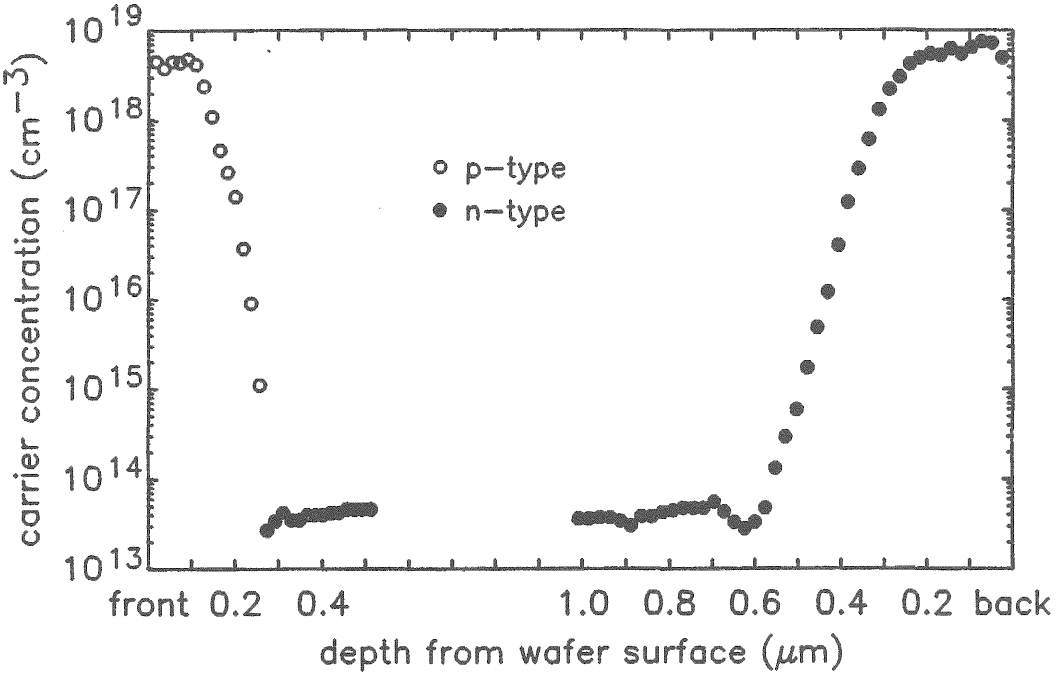


FIGURE 4-17. SPREADING RESISTANCE ANALYSIS OF p-i-n CELLS. The boron-implanted front surface has a junction depth of about 0.25 microns and a peak concentration of about 5×10^{18} cm^{-3}. The phosphorus BSR is 0.6 microns deep and has a peak concentration of 8×10^{18} cm^{-3}.

4.4.1.3 One-sun Cells (Lots 5129 and 5138)

A number of one-sun p-i-n cells were processed in an attempt to further clarify the recombination mechanisms at work. The same 100 ohm-cm n-type silicon was used as the starting material for these cells. First, to test the possibility that frozen-in defects from the thermal anneal are responsible, an experiment was done to compare cells which were cooled from the anneal temperature at the normal rate (4°C/min) with cells cooled at a slower rate (1°C/min). The results are given in Table 4-8.

TABLE 4-8. EFFECT OF COOLING RATE ON ONE-SUN CELLS.
(Lot 5138 - after AR coating)

	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (%)
Slow Cooled (3-4)	621 (2)	37.86 (0.15)	0.738 (0.003)	17.36 (0.07)
Control (1-2)	617 (1)	37.80 (0.19)	0.739 (0.004)	17.23 (0.09)

Although the slowly-cooled cells show slightly higher V_{oc} than the controls, the difference is not statistically significant.

Second, we investigated the possibility that some impurity from the deposited oxide (which is used to insulate the bus area from the wafer) was diffusing into the silicon. Cells were made using deposited oxide from different processes and compared to controls made without deposited oxide. Results are shown in Table 4-9.

TABLE 4-9. EFFECT OF DEPOSITED OXIDE.
(Lot 5129)

Type of Oxide	V_{oc} (mV)	Fill Factor	J_{01} (pA/cm^2)
None	602	0.714	1.2
CVD (Silox)	616	0.739	1.1
CVD (Pyrox)	611	0.732	1.1
Evaporated	545	0.671	11.

The same experiment was also done using longer anneals to exaggerate the effects of any impurity diffusion. The results were essentially the same; it appears that there is no loss of lifetime associated with the oxide deposition except in the case of evaporated oxide.

4.4.1.4 Polished-Surface Concentrators (Lot 5153)

To further clarify the role of the oxide in passivating the busbar and the active area, and to find the best structure for the busbar area, polished concentrator cells were made with five different structures as shown in Figure 4-18. In two groups, no deposited oxide was used: the first group has the busbar and active area passivated with the thin thermal oxide, and the second group has only the active area passivated; the busbar is in contact with the silicon. The third group uses a CVD oxide deposited after the anneal (over the thermal oxide) and the last two use a CVD oxide deposited and patterned before the thermal oxide was grown. (The last two differ only in the etching process used to fabricate the structure.) All of these cells were of the p-i-n type. Low-resistivity (p-n) controls were made as well. Results from the high-resistivity cells are shown in Table 4-10. Cells from group B (the only group without oxide under the busbar) suffered from severe shunting and could not be measured accurately.

TABLE 4-10. RESULTS FOR DIFFERENT BUSBAR STRUCTURES.
(Lot 5153 - 0.25 cm^2 cells - no AR coating)

Structure (See Fig. 4-18)	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (%)	q.e. @ 1000 nm
A	576 (4)	25.03 (0.61)	0.692 (0.034)	10.0 (0.4)	
C	584 (3)	28.31 (0.65)	0.721 (0.004)	11.9 (0.3)	0.894
D	581 (3)	25.14 (0.81)	0.721 (0.004)	10.5 (0.4)	0.928
E	587 (3)	25.18 (0.62)	0.724 (0.008)	10.7 (0.3)	0.877

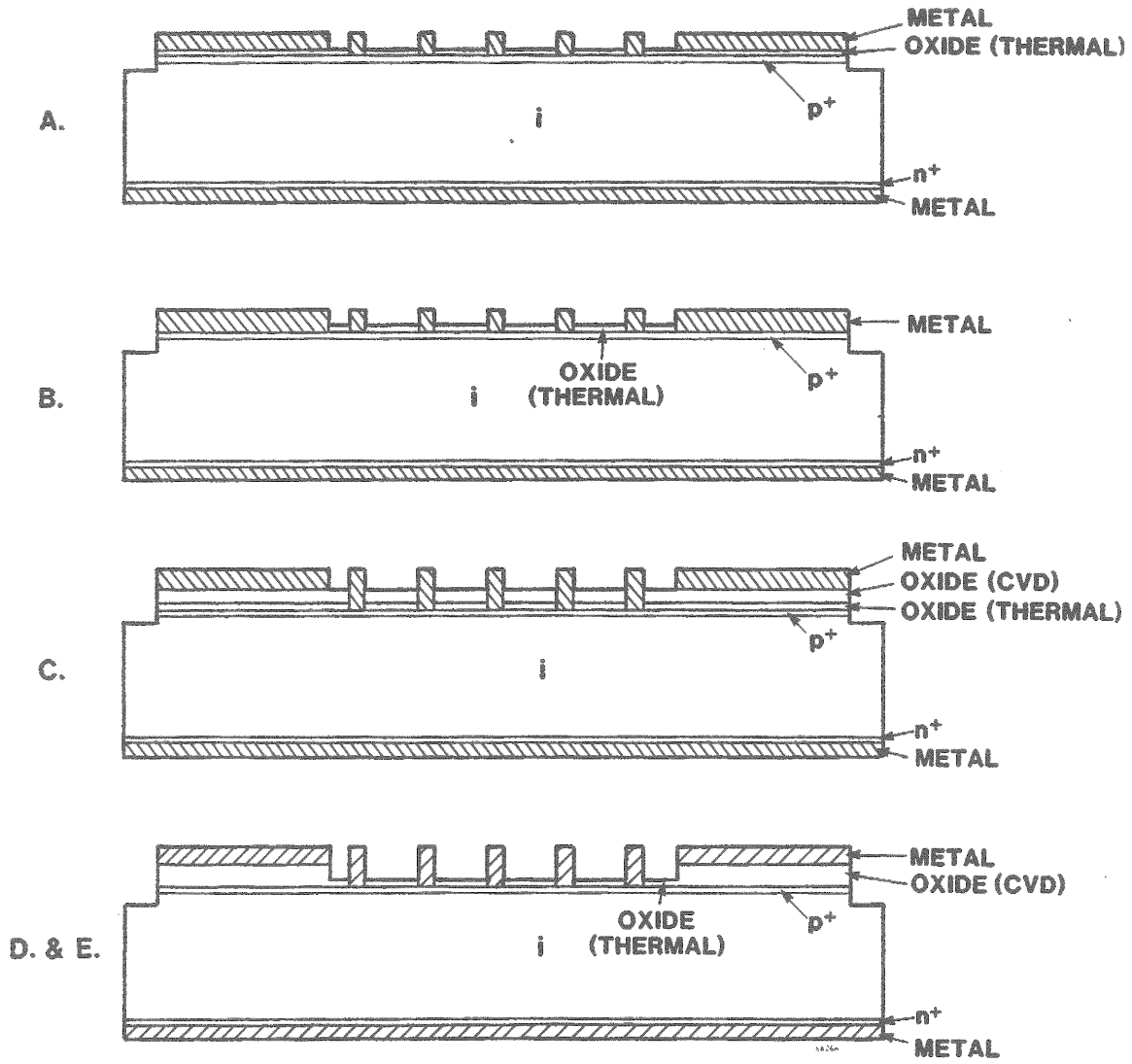


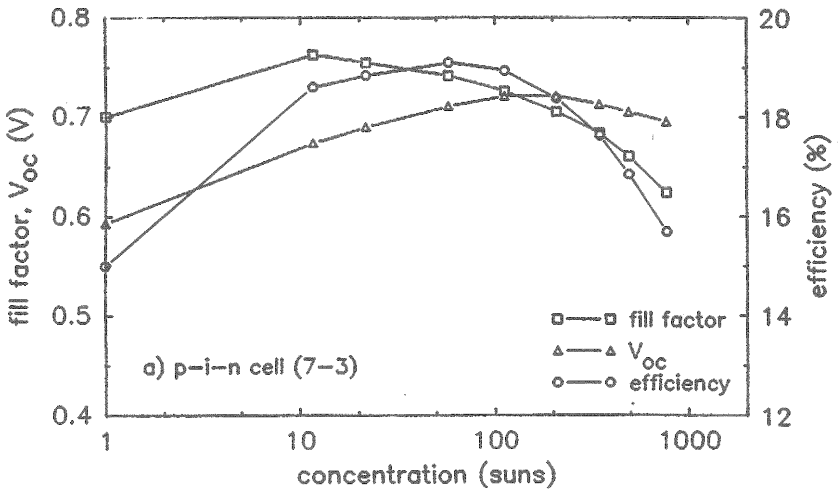
FIGURE 4-18. PASSIVATION STRUCTURES INVESTIGATED IN LOT 5153. a) thin thermal oxide covers the active area and the silicon under the busbar, b) thin thermal oxide covers the active area only, c) deposited oxide covers the active area and the busbar area, d & e) deposited oxide covers the busbar area; thermal oxide covers the active area.

From these results we can conclude, first, that the CVD oxide is not acting as an impurity source to degrade the base lifetime, since the cells without deposited oxide do not show better performance. Second, from the blue response results, we can see that the surface passivation afforded by the thermal oxidation of the surface after CVD oxide deposition appears to be equal to that obtained by oxidation of a bare surface.

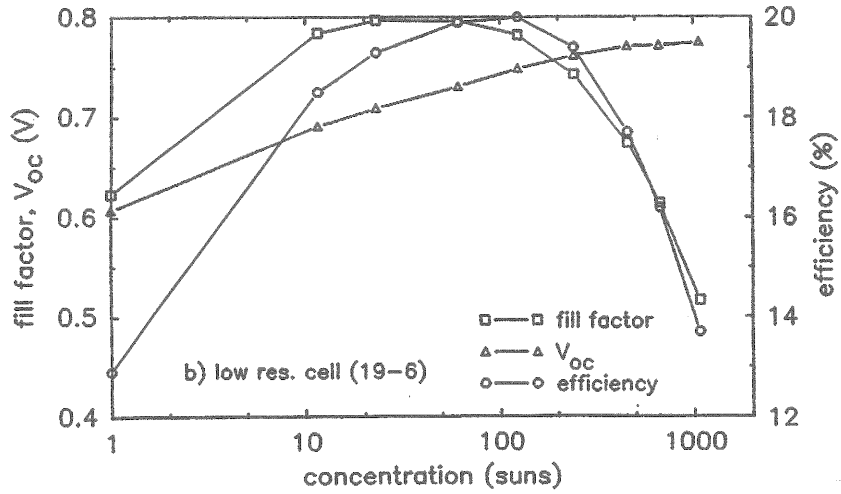
The above results are from the small (0.25 cm^2) cells. Larger (1.56 cm^2) cells were made as well; these show open-circuit voltages consistently higher by 14 to 23 mV. Considering that the larger cells have a higher ratio of active area to total area than the small cells (0.54 vs 0.28), this seems to indicate that the implanted area under the busbar, although effectively insulated from the busbar itself, still contributes to the recombination current. Table 4-11 and Figure 4-19 show the results from these cells at concentration, and, as expected, the effect of the cell size decreases as the I-V curve becomes more nearly ideal.

TABLE 4-11. CONCENTRATION RESULTS.
(Lot 5153 - after AR coating)

Cell #	Area (cm^2)	Suns	V_{OC} (mV)	J_{SC} (mA/cm^2)	Fill Factor	Eff. (%)
7-2	1.56	1.00	613	35.6	0.769	16.8
(Spire		2.40	634	85.4	0.780	17.6
Measurement)		4.17	648	148.5	0.782	18.0
		8.57	667	305.1	0.775	18.4
		18.17	682	646.9	0.754	18.3
7-7	0.25	1.00	598	36.0	0.720	15.5
(Spire		2.03	619	73.1	0.751	16.7
Measurement)		4.97	647	178.9	0.760	17.7
		9.23	665	332.3	0.767	18.4
		15.56	679	560.2	0.740	18.1
19-6	0.25	1.00	607	34.2	0.623	12.9
(Sandia		11.59	691	196.	0.784	18.5
Measurement)		22.96	709	784.	0.797	19.3
		61.01	731	2084.	0.796	19.9
		124.25	749	4244.	0.782	20.0
		241.57	762	8252.	0.743	19.4
		456.26	771	15584.	0.674	17.7
		1070.03	775	36552.	0.516	13.7



A.



B.

FIGURE 4-19. CONCENTRATION MEASUREMENTS ON LOT 5153. a) high-resistivity p-i-n cell, b) low-resistivity control cell.

4.4.1.5 Grooved Cells (Lot 5132)

The first group of V-grooved concentrator cells were p-i-n structures, 225 microns thick. Cross-groove, parallel-groove, and polished back surfaces were included; the front surfaces were all grooved. An 0.5 cm pattern, designed for 500 suns, and a 1.25 cm pattern, designed for 120 suns, were used.

Lines of 3, 4, and 5 micron nominal width and 4 micron height were used; the lines are positioned at the tops of the grooves, as discussed in Section 4.1.

Table 4-12 gives the AM1.5 performance of these cells. The high currents show that the light-trapping structures and the reduction in shadow loss are effective. However, the cross-groove cells show lower currents than the others. Spectral response (Figure 4-20) shows that the polished back surface and the parallel-groove structure each result in slightly better trapping of red light than in the cross-groove cells. However, the difference is small, and since only one wafer was measured, this cannot be considered conclusive.

There is still considerable variation in the open-circuit voltages and fill factors of these cells. I_{sc}-V_{oc} curves (a typical example is shown in Figure 4-21) show that the unexplained recombination which we saw in our baseline concentrators is still present, though it has been reduced. As in Section 4.4.1.4., the larger cells have a higher V_{oc}; since the baseline cells also were small and had a large busbar area, the results also indicate that the busbar area may be the source of the additional saturation current.

Concentration measurements, made at Sandia and Spire, are shown in Table 4-13 and Figure 4-22. The behavior of the V_{oc} and fill factor is somewhat as expected, but considerable nonlinearity is seen in the short-circuit current as a function of illumination intensity. We evaluated this nonlinearity according to the procedure described in Ref. 15, and achieved good agreement between theory and experiment using the emitter saturation current as an adjustable parameter. (The value of emitter saturation current which yielded the best agreement was 1.8×10^{-12} A/cm^2) (Figure 4-23). According to the equations of Ref. 15, therefore, we may expect that reduction in the cell thickness and in the junction area would reduce this nonlinearity to acceptable levels.

TABLE 4-12. V-GROOVE CONCENTRATOR CELLS.
(Lot 5132 - after AR coating)

Cell #	Back Grooves	Area (cm^2)	Avg. V_{oc} (mV)	Avg. J_{sc} (mA/cm^2)	Avg. FF	Avg. Eff. (%)	Highest Eff. (%)
			- 5 micron grid lines -				
2a (1 cell)	Cross	1.56	532	35.1	0.726	13.6	13.6
3-4a (2 cells)	Parallel	1.56	545 (14)	36.15 (0.07)	0.722 (0.042)	14.3 (1.2)	15.1
5-8a (4 cells)	Polished	1.56	561 (3)	35.73 (1.28)	0.676 (0.079)	13.5 (1.6)	15.1
4h (1 cell)	Parallel	0.25	529	36.7	0.719	14.0	14.0
5c,7h (2 cells)	Polished	0.25	533 (1)	37.65 (0.92)	0.713 (0.006)	14.3 (0.3)	14.5
			- 4 micron grid lines -				
5-8dg (3 cells)	Polished	0.25	533 (2)	38.73 (1.50)	0.706 (0.007)	14.6 (0.6)	15.1
			- 3 micron grid lines -				
2b (1 cell)	Cross	1.56	524	34.1	0.711	12.7	12.7
3-4b (2 cells)	Parallel	1.56	551 (14)	37.65 (0.21)	0.737 (0.009)	15.3 (0.5)	15.6
5-8b (4 cells)	Polished	1.56	564 (5)	37.52 (0.81)	0.634 (0.106)	13.4 (2.1)	15.2
5e (1 cell)	Polished	0.25	535	39.3	0.716	15.0	15.0

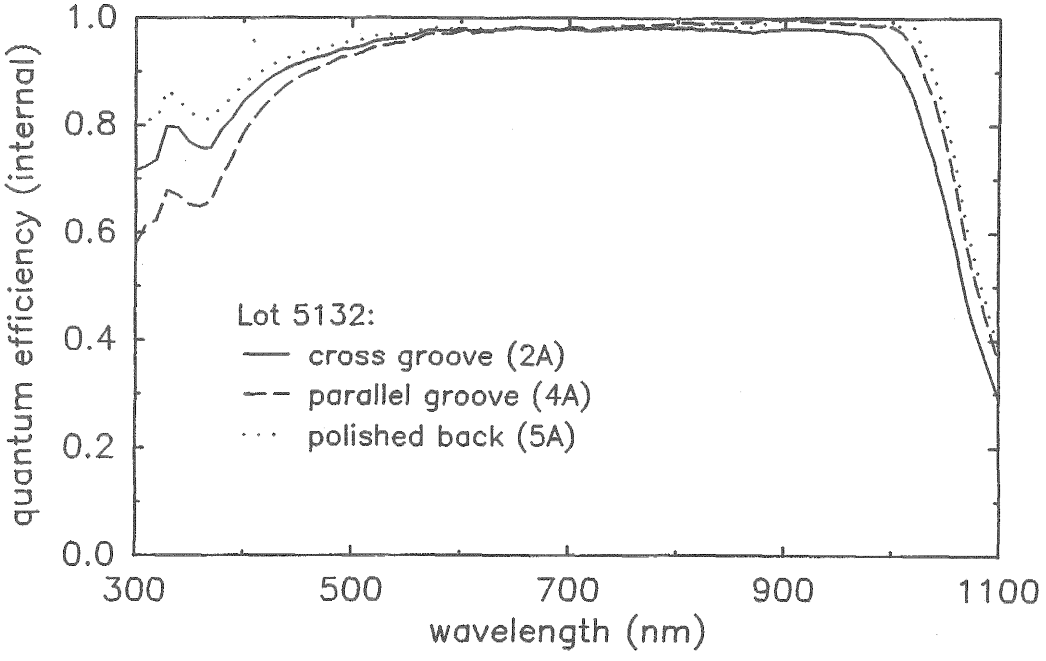


FIGURE 4-20. QUANTUM EFFICIENCY OF GROOVED CELLS, COMPARING CROSS GROOVE, PARALLEL GROOVE, AND POLISHED BACK STRUCTURES. (Lot 5132).

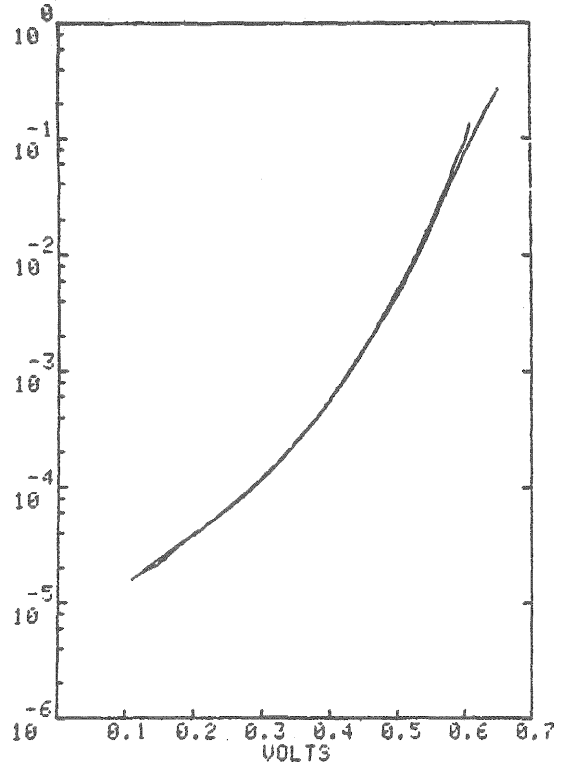


FIGURE 4-21. I_{SC}-V_{OC} CURVE OF A GROOVED CONCENTRATOR CELL.

TABLE 4-13. CONCENTRATOR MEASUREMENTS OF GROOVED CELLS.
(Lot 5132 - after AR coating)
(Sandia measurements - corrected for nonlinearity)

Cell #	Area (cm^2)	Suns	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (%)
5E	0.25	1.00	539	39.8	0.724	15.5
(polished		11.14	617	432.	0.752	18.0
back)		23.07	636	872.	0.753	18.1
		62.01	661	2256.	0.749	18.0
		96.69	671	3336.	0.747	17.3
		139.51	681	4560.	0.744	16.6
		217.51	690	6600.	0.738	15.5
		546.88	706	13496.	0.704	12.3
		1030.44	713	20204.	0.664	9.3
5B	1.56	1.00	573	39.3	0.762	17.1
(polished		11.14	640	405.	0.762	17.7
back)		23.07	657	822.	0.751	17.6
		62.01	680	2135.	0.719	16.8
		96.69	690	3147.	0.693	15.6
		139.51	696	4313.	0.670	14.4
4B	1.56	1.00	564	38.2	0.767	16.5
(parallel		11.14	632	398.	0.754	17.0
grooves)		23.07	649	801.	0.743	16.7
		62.01	672	2068.	0.715	16.0
		96.69	683	3016.	0.698	14.9
		139.51	691	4132.	0.679	13.9

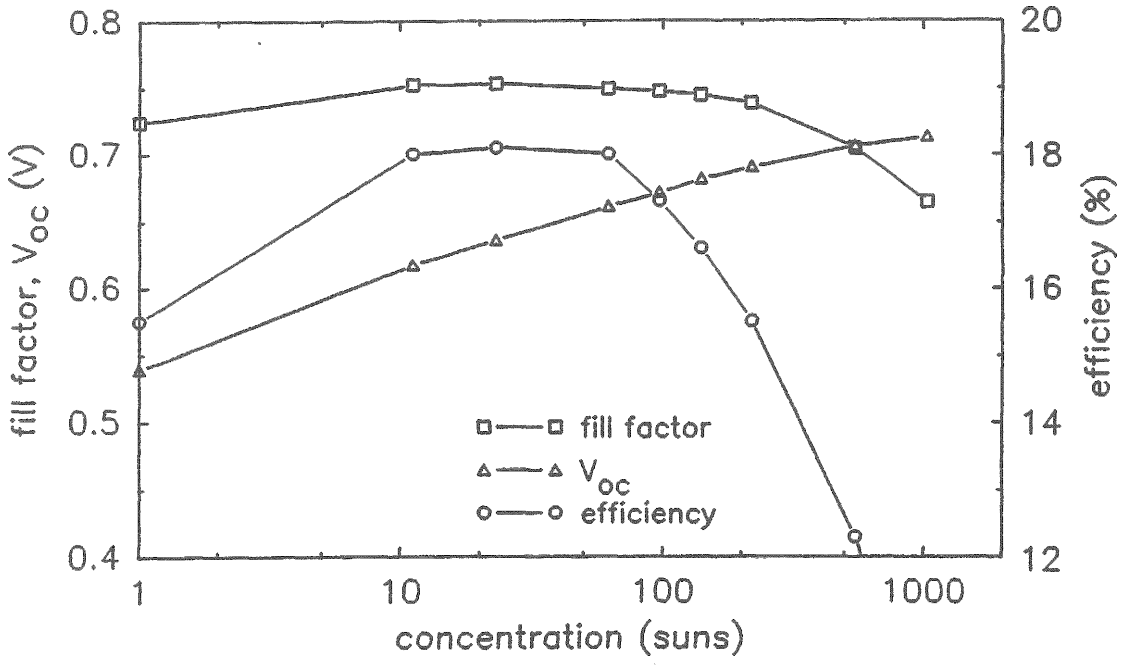


FIGURE 4-22. CONCENTRATION MEASUREMENTS OF GROOVED CELLS (Cell #5132-5E). The efficiency data are corrected for current sublinearity.

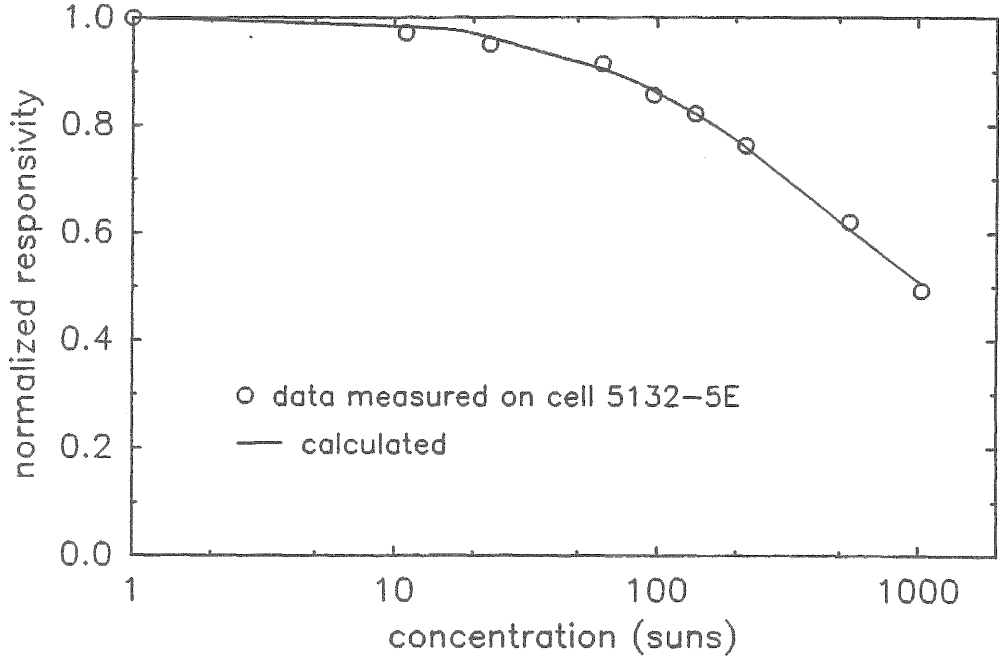


FIGURE 4-23. SUBLINEAR CURRENT RESPONSE OF CELL 5132-5E. The experimental data fit the equations of Ref. 15 using an emitter saturation current of 1.8 pA/cm^2 and a bulk lifetime of 1 ms. The ambipolar diffusivity of 28.25 cm^2/s and the Auger coefficient of 1.66 x 10^{-30} cm^2/s were taken from Ref. 15.

4.4.1.6 Grooved Cells With Reduced Junction Area (Lot 5121)

In the next lot, the junction under the busbar was eliminated, as discussed in Section 3.2.1. Table 4-14 shows the cell results by category; cross groove, parallel groove, and polished cells were made.

TABLE 4-14. GROOVED CONCENTRATOR CELLS.
(Lot 5121 - before AR coating)

Structure (See Figure 3-3)	Surface	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (%)	q.e. @ 1100 nm
		- 0.25 cm^2 cells -				
A (#1-3)	Cross Groove	519 (18)	33.05 (0.55)	0.675 (0.032)	11.6 (0.9)	0.155 (0.008)
A (#4-6)	Par. Groove	502 (11)	33.30 (0.78)	0.676 (0.027)	11.3 (0.5)	0.171 (0.023)
A (#21)	Polished	489 (7)	24.24 (0.67)	0.643 (0.017)	7.6 (0.4)	
B (#7-9)	Cross Groove	558 (11)	33.36 (0.74)	0.679 (0.027)	12.6 (0.7)	0.263 (0.074)
B (#10-12)	Par. Groove	549 (8)	32.84 (1.28)	0.651 (0.065)	11.7 (1.1)	0.207 (0.010)
B (#22)	Polished	524 (9)	24.40 (0.39)	0.597 (0.012)	7.6 (0.2)	
		- 1.5625 cm^2 cells -				
A (#1-3)	Cross Groove	528 (6)	32.50 (0.30)	0.630 (0.004)	10.8 (0.3)	
A (#4-6)	Par. Groove	515 (11)	32.93 (0.29)	0.678 (0.028)	11.5 (0.6)	
A (#21)	Polished	500 (9)	23.85 (0.55)	0.599 (0.076)	7.1 (0.9)	
B (#7-9)	Cross Groove	564 (8)	32.80 (0.17)	0.688 (0.023)	12.7 (0.5)	
B (#10-12)	Par. Groove	551 (10)	32.08 (0.43)	0.676 (0.021)	11.9 (0.3)	
B (#22)	Polished	539 (13)	24.10 (0.60)	0.602 (0.004)	7.8	

Comparing the voltages from the different sizes of cells, it is clear that the cells with reduced junction area ("B") show not only higher V_{oc}s in general, but also less difference between the small cells and the large cells. The remaining difference may be due to edge effects.

The quantum efficiency measurements show an interesting result as well. As expected from thick cells, no significant difference was seen in the red response between the cross-groove and parallel-groove cells in general. However, with the exception of one cross-groove wafer (#8), all of these cells show lower-than-expected red response (Figure 4-24). Analysis indicates a low diffusion length (100-300 microns), much lower than was observed in the previous lots. The wafers with the reduced area implantation ("B") seem to show somewhat less degradation in general, but only #8 has a lifetime as long as expected from this material. Since the lifetimes were not measured before or during processing, the source of the degradation cannot be identified conclusively.

Concentration measurements of these cells show a very high and non-ohmic series resistance, which we attribute to the front contacts.

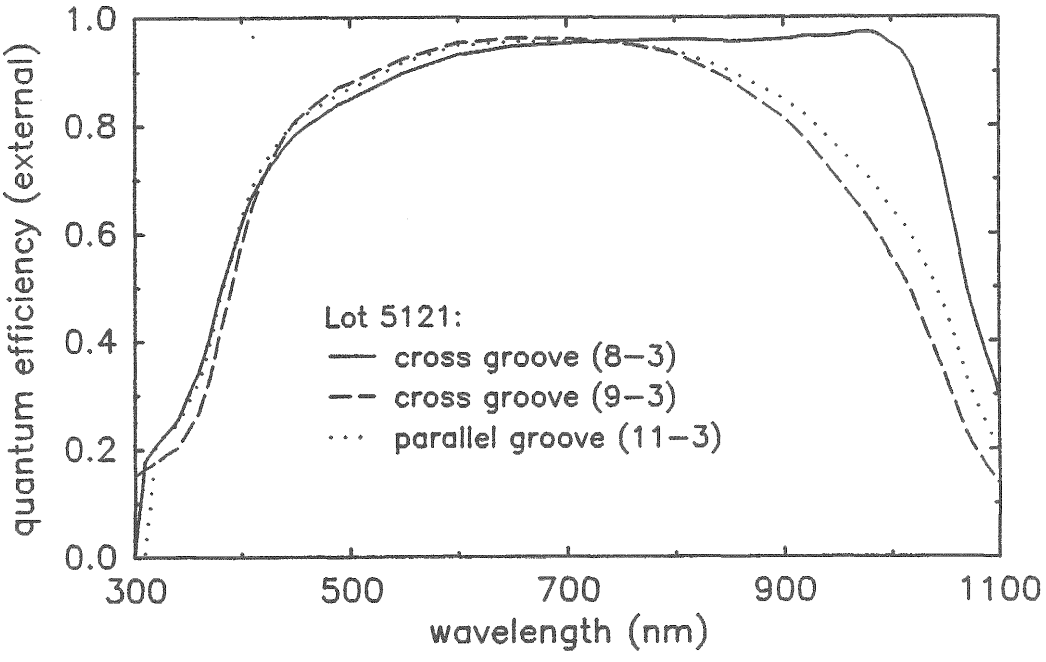


FIGURE 4-24. QUANTUM EFFICIENCIES OF GROOVED CELLS FROM LOT 5121. All wafers except #8 show lower-than-expected diffusion length.

4.4.1.7 Thin Grooved Cells (Lot 5147)

The final group of cells compared cross-groove, parallel-groove, and polished structures for both 200 micron and 100 micron cells. Although some 50 micron polished cells were made, the 50 micron grooved wafers proved to be too fragile for processing. Cell data are given in Table 4-15.

TABLE 4-15. THIN GROOVED CELLS.
(Lot 5147 - before AR coating)

Thickness (microns)	Surface	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (%)	q.e. @ 1100 nm
		- 0.25 cm^2 cells -				
100 (#9-11)	Cross Groove	555 (10)	31.20 (1.55)	0.661 (0.045)	11.5 (1.2)	0.093
100 (#12-14)	Par. Groove	564	33.60	0.674	12.8	0.122
100 (#15)	Polished	551 (11)	22.68 (0.38)	0.655 (0.025)	8.2 (0.5)	
225 (#17)	Cross Groove	522 (19)	31.70 (1.42)	0.600 (0.067)	10.0 (1.5)	0.281
225 (#18)	Par. Groove	458 (14)	28.74 (0.88)	0.643 (0.023)	8.5 (0.)	0.031
225 (#19)	Polished	521 (22)	24.24 (0.39)	0.638 (0.006)	8.0 (0.4)	0.000
		- 1.56 cm^2 cells -				
50 (#7)	Polished	550	21.70	0.640	7.6	0.034
100 (#9-11)	Cross Groove	575 (3)	29.75 (0.55)	0.642 (0.101)	10.9 (1.6)	0.094
100 (#15)	Polished	572 (4)	22.50 (0.20)	0.708 (0.001)	9.1 (0.0)	0.051
225 (#17)	Cross Groove	542 (9)	29.15 (0.95)	0.533 (0.128)	8.5 (2.4)	0.201
225 (#18)	Par. Groove	478 (10)	27.90 (0.60)	0.662 (0.008)	8.8 (0.5)	0.042
225 (#19)	Polished	545 (11)	23.85 (0.25)	0.686 (0.002)	8.9 (0.1)	0.099

Figure 4-25 shows the quantum efficiency measured on four of these cells. For the 225 micron thick case, a large difference in red response is seen between the cross-groove and parallel-groove wafers, but there is only one wafer in each of these categories, and no corresponding difference is seen in the thinner cells. Lifetime degradation is apparent for both of the 225 micron cells. These data must be considered inconclusive.

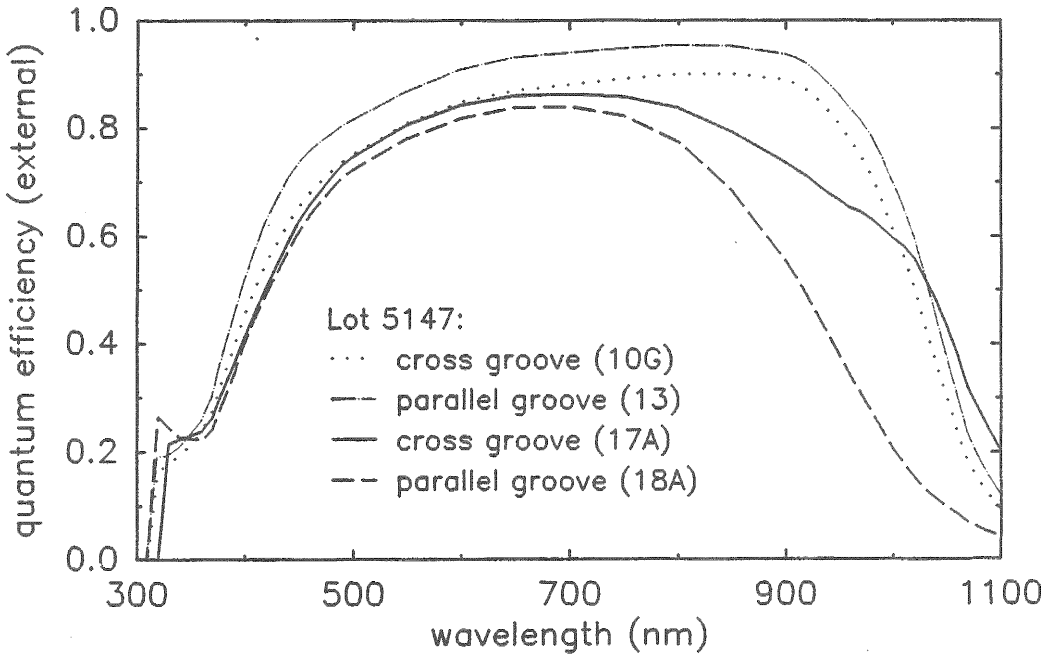


FIGURE 4-25. QUANTUM EFFICIENCIES OF GROOVED CELLS FROM LOT 5147. The upper two curves (10G and 13) are 100 micron thick cells; the other two (17A and 18A) are 225 micron thick cells. Although #17 and #18 show a considerable difference between the parallel-groove and cross-groove structures, variation in lifetime could explain the results as well.

Current-voltage measurements show high-series resistance in these cells as well. Concentration measurements on selected cells (Table 4-16) confirm that the fill factor does not increase at 20 suns, except for the thin polished cell.

TABLE 4-16. CONCENTRATION MEASUREMENTS ON THIN-GROOVED CELLS.
(Lot 5147 - 0.25 cm^2 cells)
(Grooved cells are AR coated; polished cells are not)

Cell #		Suns	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill Factor	Eff. (%)
10-g	(4 mil cross)	1.00	553	34.6	0.676	12.9
		18.85	629	652.1	0.631	13.7
13	(4 mil par.)	1.00	566	36.0	0.676	13.8
		19.44	636	699.9	0.505	11.6
15-c	(4 mil pol.)	1.00	571	22.9	0.676	8.8
		20.16	668	462.1	0.762	11.7
17-d	(9 mil cross)	1.00	550	35.3	0.686	13.3
		19.97	659	705.5	0.647	15.1
18-c	(9 mil par.)	1.00	484	32.3	0.666	10.4
		20.28	621	655.5	0.568	11.4
19-c	(9 mil pol.)	1.00	518	24.7	0.627	8.0
		19.83	616	490.2	0.559	8.5

4.4.2 Cell Data Summary

From the foregoing data, it appears that, despite the optical measurements which seem to confirm the theoretical advantages of the cross groove structure, we have not conclusively demonstrated the predicted increase in light-generated current in an actual solar cell. The predicted increase is small (on the order of 1%) and has apparently been masked by differences in bulk carrier lifetime and in BSR effectiveness. However, the work done here has demonstrated that the basic cross-groove structure can be fabricated, and has suggested ways in which it can be improved toward its theoretical efficiency limit.

4.4.2.1 Bulk Lifetime

Examination of the spectral response curves of this section shows that the carrier lifetime of the cells made here varies considerably. Experiments have eliminated the deposited oxide and the furnace cooling rate as possible causes. Since the lower lifetimes seem to be associated with grooved cells, it is possible that the nitride deposition, which is done at high temperature, has a detrimental effect, although the correlation is not exact. Further work, using in-process lifetime measuring techniques[19,20] could identify and correct the problem.

4.4.2.2 Series Resistance

Considerable series resistance, which at times appears to be non-ohmic, has degraded the efficiency of these cells, particularly at concentration. We attribute this problem primarily to the p-type front contact, which is made to a relatively lightly-doped ($<10^{19}$ cm^{-3}) material. Although a few cells were made in which a low series resistance was seen, the result could not be reproduced reliably, and experiments to optimize the metal and the contact anneal were unsuccessful. However, we know that low-resistance contacts can be made, by increasing the dopant concentration under the metal if not by simpler means, and so this problem does not represent a barrier to further development of this cell structure.

4.4.2.3 Recombination Components

To achieve high efficiency with this cell structure, a number of sources of recombination must be considered and eliminated. Bulk recombination can be made quite low, as we have seen; the bulk presents no new problems which are not already seen with the IBC structure.[21]

Recombination in the emitter, which is responsible for current sublinearity as well as low V_{oc}, must be addressed by reducing the emitter area. We have clearly shown that cells in which the emitter extends under the busbar have greater recombination than cells in which the emitter covers only the active area; although the series resistance theoretically should separate the extra emitter area from the active cell and make this difference less important at concentration, the effect is still significant.

With one-sun cells, high efficiencies (20%) have been achieved with emitters covering the full active area.[18,22] The higher current levels and additional metal coverage which is needed for a concentrator cell argues in favor of reducing the emitter area further, to make the point-contact structure described in Figure 3-2.

SECTION 5
SUMMARY AND CONCLUSIONS

1) The cross-grooved structure has been experimentally found to have superior light-trapping properties compared to other structures including combinations of pyramid-etched, V-grooved, and specular surfaces. The next-best structure, which is only slightly inferior, was the combination of pyramid-etched front and specular back surfaces. For a 100-micron thickness, the cross-grooved structure absorbs extra light corresponding to a 15% short-circuit current increase over a polished wafer.

2) In addition to its light-trapping effectiveness, the cross-grooved cell exhibits reduced grid line obscuration losses, because light striking the metallized grooves is reflected onto the active cell area. Measurements showed that despite a 1-micron flat spot on top of the groove, more than 50% of the light striking the grid lines is collected.

3) A fabrication process was developed for producing silicon concentrator cells with the cross-grooved structure. High short-circuit current densities, 39.8 mA/cm^2, were measured for V-grooved concentrator cells with 7% grid coverage.

4) As part of the process development, low-resistivity concentrator cells with 20% efficiency at 124 suns were produced. These cells did not incorporate light-trapping.

5) The best p-i-n cross-grooved concentrator cells had an efficiency of 18% at 23 suns. The cells were limited by sublinearity of the short-circuit current and by poor ohmic contacts.

6) The major loss in the present cross-grooved cells is recombination in the full-area emitter layer. The emitter dark current limits V_{oc}, and also causes the short-circuit current sublinearity. To reduce this loss, the area of the junction must be reduced.

7) For future work, better control of minority-carrier lifetime during processing and more reproducible ohmic contacts are needed.

8) Good processing yields were obtained for wafers thinned to 100 microns or greater. At 50 microns, however, breakage during handling was a major problem. The V-grooves, approximately 10 microns deep on each side of the wafer and aligned on cleavage planes, degrade the mechanical strength of the wafer. Even such thin cells could potentially be processed using membrane-etching techniques developed in a previous Sandia project. In this process some of the silicon wafer remains at its original thickness while the cell areas are thinned.

9) Although future work remains to solve the fabrication problems, we believe the cross-grooved cell is a viable approach toward the limit-efficiency silicon concentrator cell.

SECTION 6
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