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CADMIUM SULFIDE/COPPER SULFIDE HETEROJUNCTION CELL RESEARCH

Quarterly Technical Progress Report for October 1—December 31, 1979

By
John A. Thornton

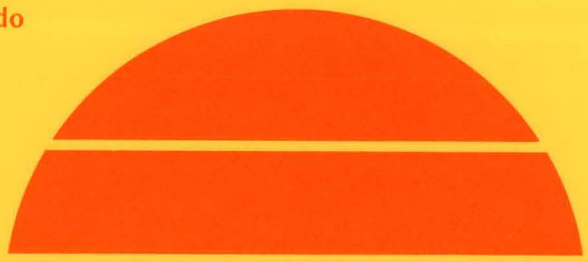
February 28, 1980

Work Performed Under Contract No. EG-77-C-01-4042

Telic Corporation
Santa Monica, California

and

Solar Energy Research Institute
Golden, Colorado



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Quarterly Technical Progress Report

Period: October 1, 1979 - December 31, 1979

By John A. Thornton

Telic Corporation
1631 Colorado Ave
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February 28, 1980

Work Performed Under Contract No. XJ-9-8033-2

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ABSTRACT

This report covers the work performed for the approximate period October 1, 1979, to December 31, 1979.

Extensive modifications to the multi-source deposition apparatus, including the installation of a larger vacuum chamber on the existing pumping system, have been completed. The new chamber provides improved inter-source shielding, an improved substrate mounting and heating system, and a vacuum interlock for introducing substrates.

The investigation of CdS resistivity control by In doping has been continued. It has been established that the resistivity of CdS coatings deposited from an In doped target by reactive sputtering in an Ar - H_2S working gas is very sensitive to the H_2S injection rate. Thus coatings varying in resistivity from 10^3 Ω-cm to 10^{-1} Ω-cm were deposited from a target doped with 1 at. percent In as the H_2S injection rate was varied by only 25%. Microprobe analysis confirmed that the In content in the coatings was identical to that in the target. The resistivity variations are believed to result from variations in the Cd vacancy level and the associated vacancy acceptor compensation of the In donors.

The sputter-deposited solar cells fabricated thusfar are characterized by a low short circuit current. Cell current-voltage characteristics and capacitance-voltage measurements under solar illumination indicate that the cause is a poor junction collection efficiency due primarily to a low junction electric field in the heat-treated cells.

1. PROJECT DESCRIPTION

The program objective is to investigate and evaluate the application of cylindrical-post magnetron reactive sputtering for the production of solar cell quality thin films of CdS/Cu_2S for large-scale terrestrial photovoltaic energy conversion. The reactive sputtering process is being investigated at Telic Corporation. The coating and device characterization is being done at the Lockheed Palo Alto Research Laboratory.[1,2]

The Telic portion of the program includes the following tasks.

Task 1: Deposition Process Development

This task calls for modification of the deposition equipment and procedures to overcome deficiencies that were identified during the previous program.[3] The modifications include: (1) reconfiguring the cathode shielding to remove foreign surfaces from the proximity of the cathodes and the substrates; (2) installing a vacuum interlock so that substrates can be inserted without exposing cathode and shield surfaces to the atmosphere; and (3) redesigning the substrate holder to provide better substrate temperature control and more rapid substrate cooling. The task also includes an investigation of the use of rf-reactive sputtering as a means for achieving higher deposition rates with the absence of arcing.

Task 2: $Cd_xZn_{1-x}S$, CdS Deposition Studies

This task concentrates on gaining improved control over the deposition of the specific semiconductor layers required for the cells. In the case of the CdS or $Cd_xZn_{1-x}S$ layer, the emphasis is on controlling the coating resistivity, either by In doping or by achieving off-stoichiometry deposits through the use of special deposition techniques or post-deposition heat treatment. In the case of the Cu_2S, the emphasis is on gaining control of the properties of Cu_xS deposited over CdS layers. (In the previous program the specific properties of the Cu_2S had been investigated in detail only for coatings deposited on glass substrates[3]).

Task 3: Device-Material Parameter Optimization

Throughout all stages of the program solar-cell structures will be deposited and their performance evaluated as photovoltaic devices.

This report is organized with respect to the progress made during the third quarter on each of the program tasks.

2. DEPOSITION PROCESS DEVELOPMENT (Task 1)

The emphasis during this quarter was on completion of the apparatus modifications. The specific objectives of the apparatus modifications were to:

1) Reconfigure cathode shielding to reduce the shield surface area adjacent to the sputtering sources and substrates.
2) Install a vacuum interlock so that substrates can be inserted without exposing the cathode and shield surfaces to the atmosphere.
3) Redesign the substrate holder to permit rapid cooling of the substrates following the CdS and prior to the Cu_2S depositions.
4) Install a movable mask to restrict Cu_2S deposition at the cell edge.

The design of the modified apparatus was described in the first quarterly report.[4] The modification involved fabricating and mounting a larger vacuum chamber and magnetic field coil system on the pumping stand. (The pumping stand is the same one that was used for the previous apparatus.) The modified apparatus is shown in Fig. 1. The vacuum chamber and magnetic coil system are shown schematically in Fig. 2. The magnetic field coils are located in the annular space between a nonmagnetic (Type 304) stainless steel vacuum chamber wall and a carbon steel outer cylinder. The chamber top and bottom plates are also fabricated from carbon steel. Thus the field coils are enclosed within a shell of magnetic material which is made thick enough so that it is not saturated by the magnetic flux. With this configuration a magnetic field that is uniform in magnitude and direction can be produced within the vacuum enclosure by the short solenoidal coil system. Magnetic field lines pass through the chamber and then return via the shunt path in the steel as indicated in Fig. 2. The coil system is connected electrically into three coil sets so that the currents can be independently controlled. This adjustment permits the effects of perturbations, such as the holes in the top plate where the

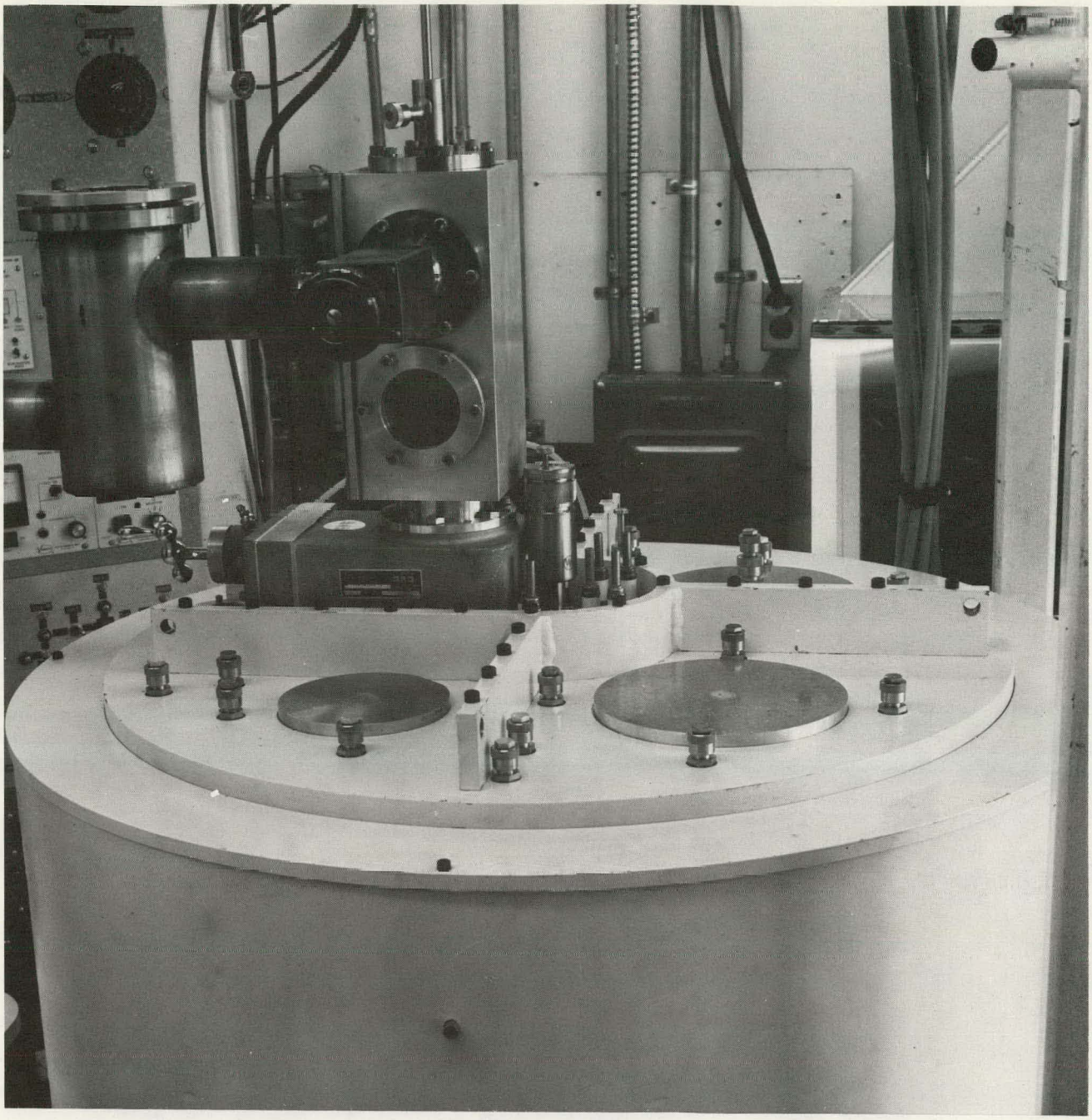

FIG. 1 Photograph showing modified deposition apparatus. The vacuum interlock can be seen at the left.

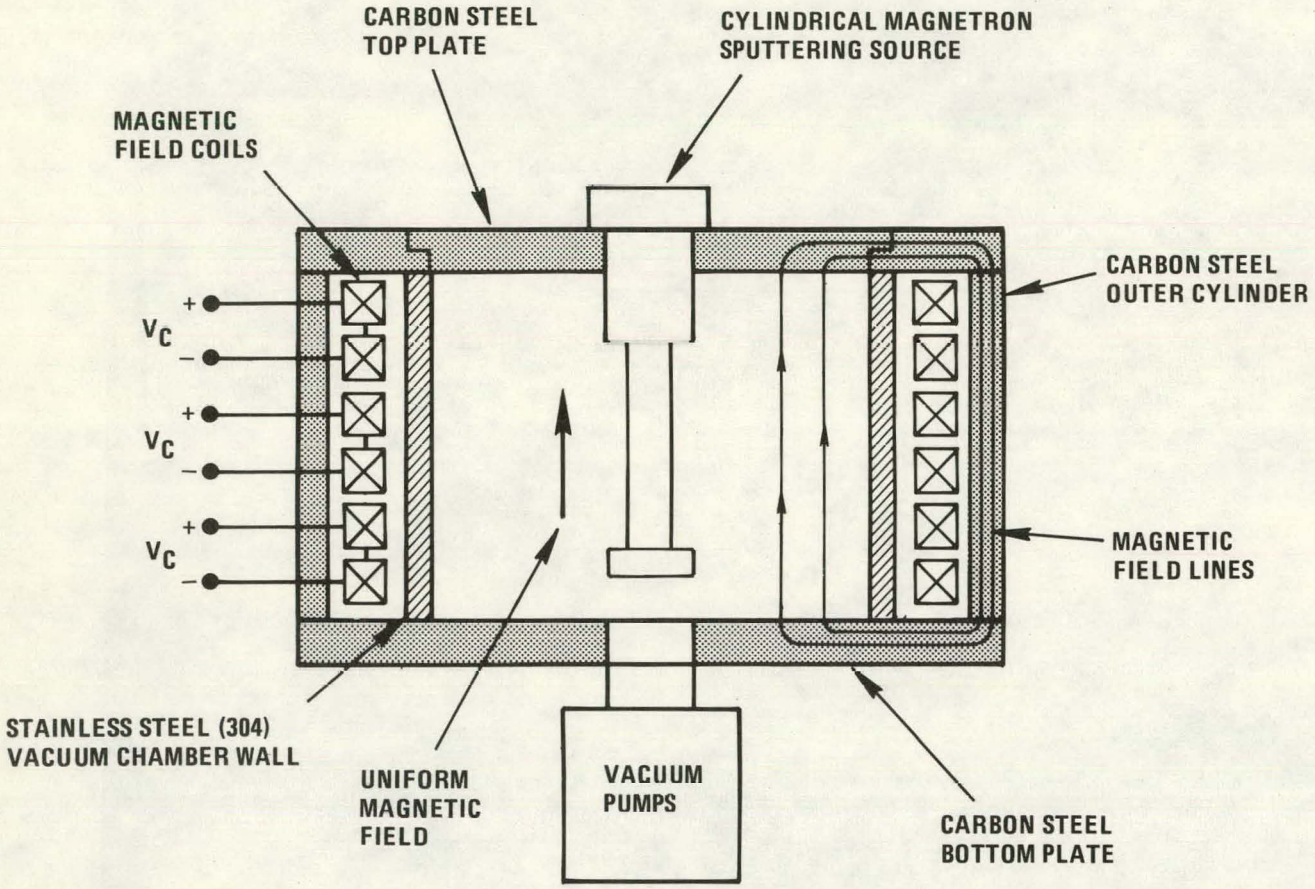

FIG. 2 Schematic illustration of chamber magnetic field coil system.

cathodes are inserted, to be compensated for. Magnetic probe measurements at the cathode mounting positions have been used to measure the magnetic field strengths and to verify that the uniformity is adequate for operating the cylindrical-post magnetron sputtering sources.

A series of shields partition the coating chamber into four compartments within which the individual magnetron sputtering sources are located, as shown in Fig. 3. The shields are located much farther from the sputtering sources than in the previous apparatus, and have provisions for water cooling (first objective listed above).

Substrates are loaded into a stainless steel frame of low thermal mass and placed on a loading rod within the vacuum interlock which is located on the top of the chamber (second objective). See Fig. 4. After the interlock chamber is evacuated, the rod is used to lower the substrate frame through a 2-inch gate valve and onto a carrousel type mounting frame, as shown in Fig. 5. The carrousel frame permits the substrates to be rotated and passed into the four different coating positions. Fixed substrate heaters are located behind the carrousel at each of the coating positions. The carrousel has a low thermal mass, so that the substrates can be quickly cooled by rotating them away from a substrate heater to a cooling position (third objective).

Dummy glass substrates with imbedded thermocouples are mounted on the carrousel, adjacent to the deposition substrates, in holders identical to the ones used for the deposition substrates. These thermocouples are calibrated against similar thermocouple-containing-plates, which were placed at the deposition positions during heater tests. They will be used to estimate the substrate temperatures during deposition. (This is the same procedure that was used with the previous apparatus). The carrousel and substrate holder are shown in Fig. 6. The lower two substrate positions mount the plates which contain the reference thermocouples.

Rotational pass-throughs are located adjacent to each of the coating positions to permit the installation of auxiliary shields (fourth objective).

All the basic elements of the modified apparatus (substrate heaters, substrate loading mechanism, etc.) have been tested. Shakedown deposition tests

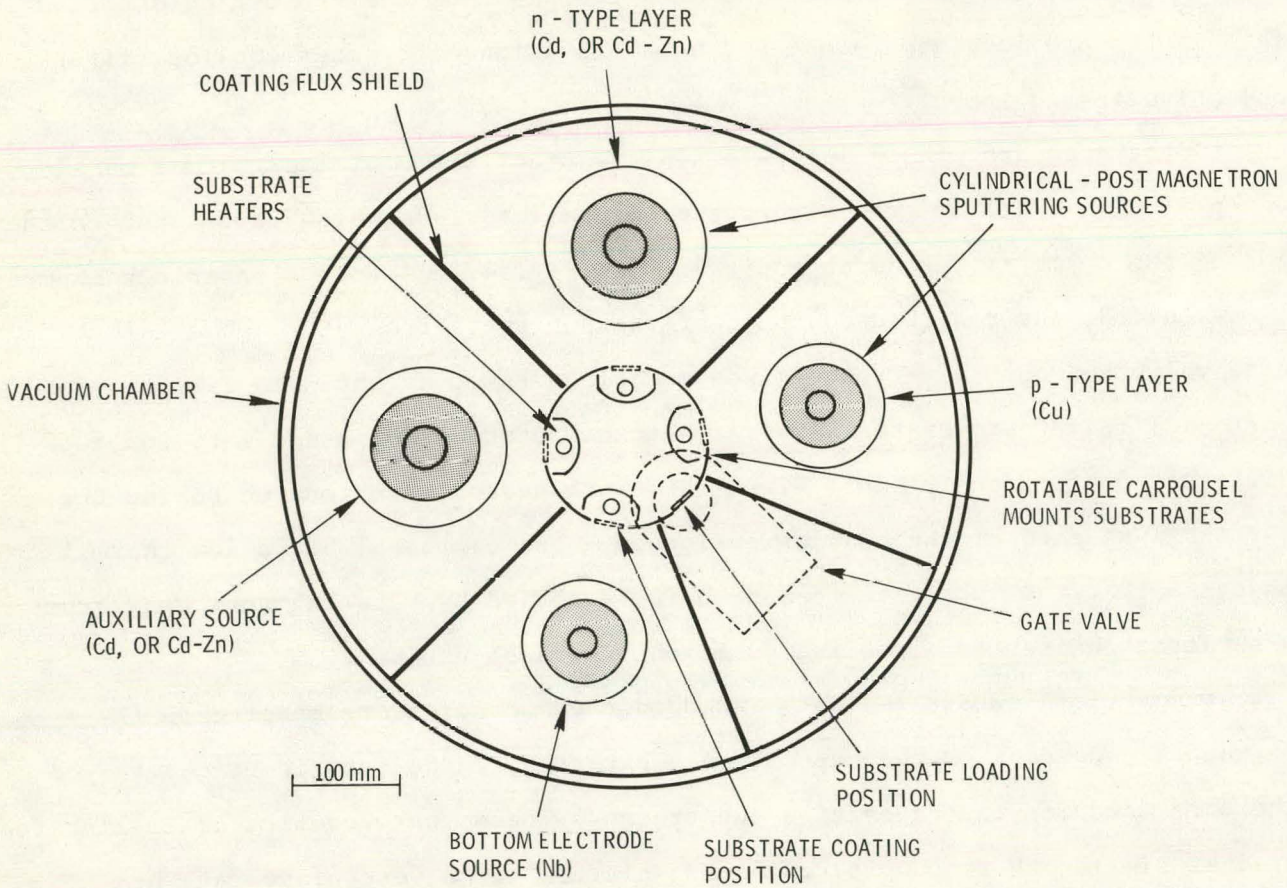

FIG. 3 Schematic diagram of modified multi-source deposition apparatus.

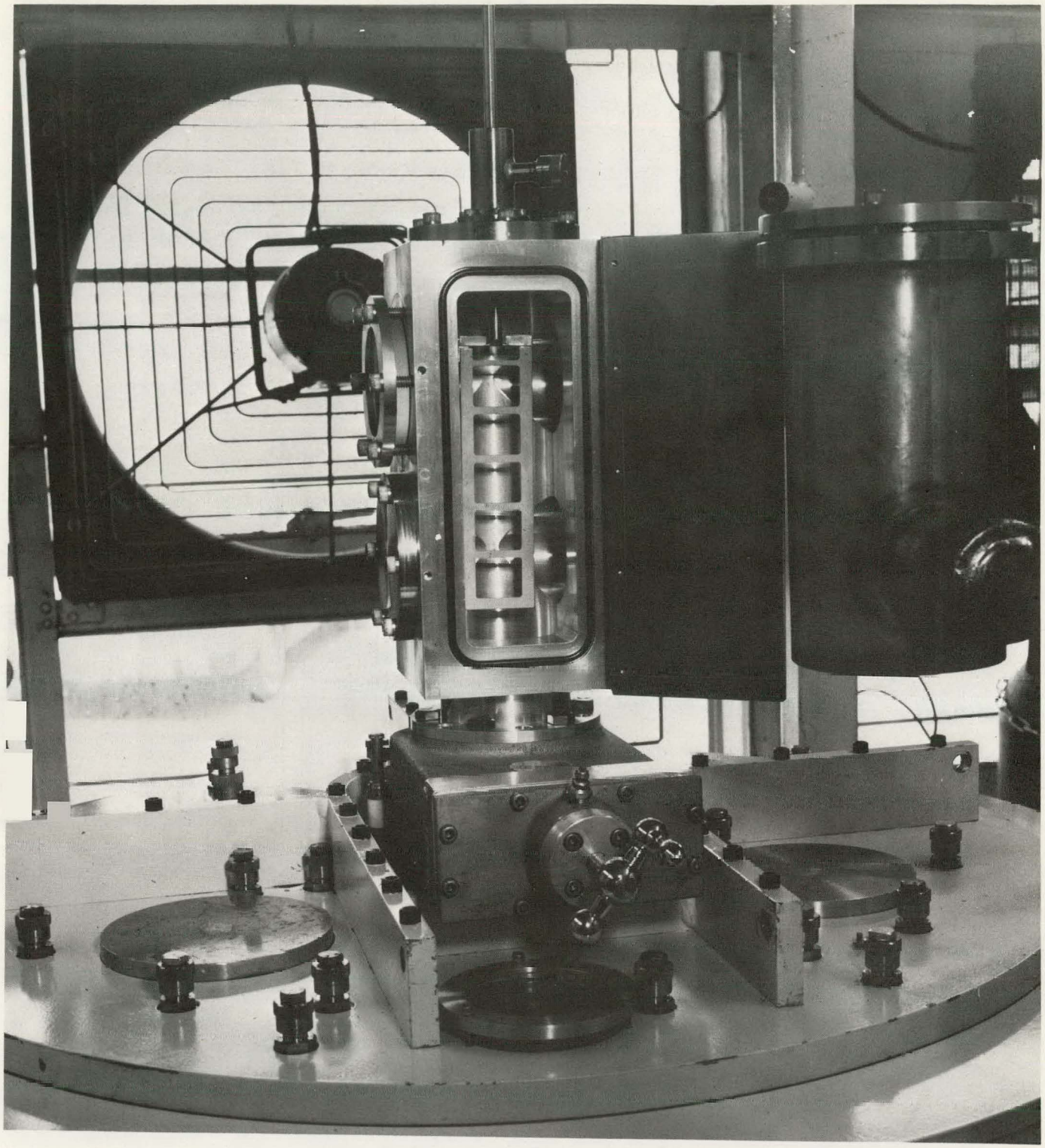

FIG. 4 Photograph of substrate loading interlock.

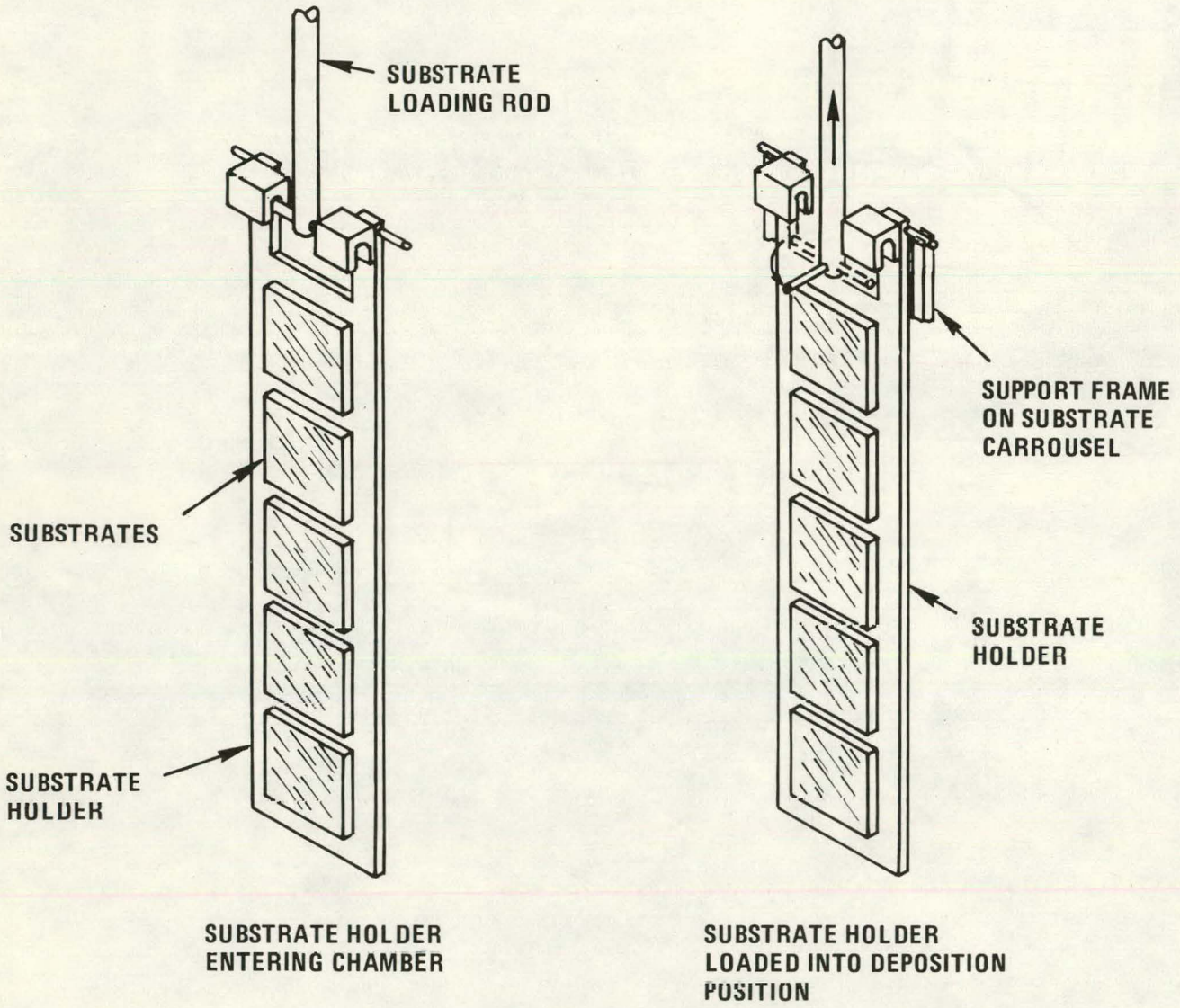

FIG. 5 Schematic illustration of substrate loading procedure.

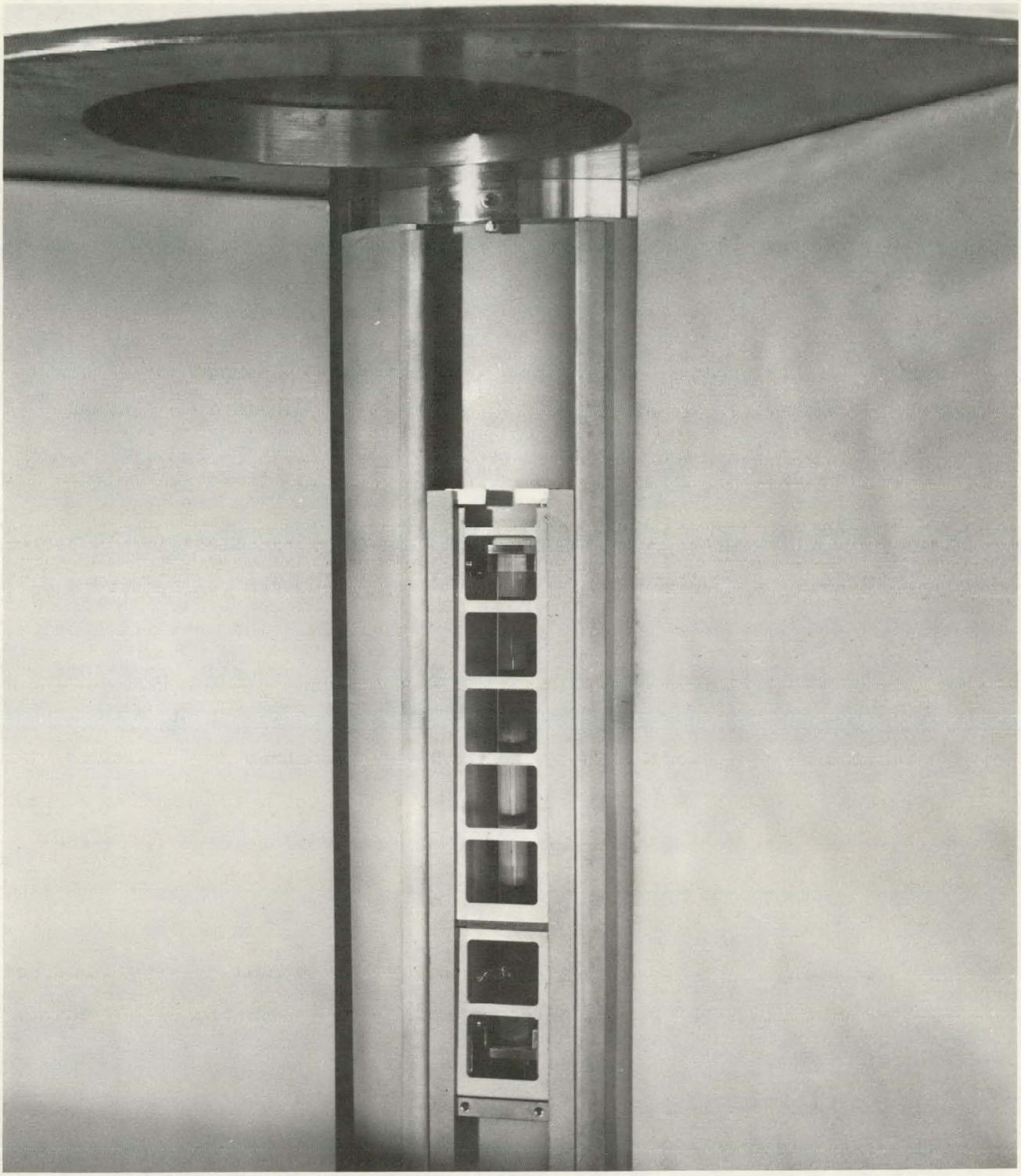

FIG. 6 Photograph with chamber lid raised showing carrousel type substrate holder.

are now beginning.

A new dc power supply with an improved arc suppression circuit has been designed and fabricated, in an independent Telic-sponsored project, for use on the program. Preliminary tests during Cd-H_2S reactive sputtering indicate that the power supply is effective in suppressing arcs.

3. CdS, $Cd_xZn_{1-x}S$ AND Cu_2S DEPOSITION (Task 2)

3.1 Resistivity Control by Doping

Figure 7 shows the resistivity versus substrate temperature for CdS coatings deposited by reactive sputtering from undoped Cd targets and from targets doped with 0.1 and with 1 at. percent In. The undoped and 1 at. percent data were reported previously;[5] the 0.1 at. percent data are new. The coatings were approximately 150 nm thick and were deposited onto glass substrates having pre-deposited Nb diagnostic electrodes that permitted resistivity and electron mobility measurements in the plane of the film. The mobilities of the 1 at. percent In coatings were measured and found to be about 10 $cm^2/V\text{-}sec$. The carrier concentrations were about $7x10^{18}$ cm^{-3}, indicating that about 3.5% of the In atoms contributed electrons to the conduction band.[5]

Figure 8 shows the resistivity and electron mobility versus indium content for reactively sputtered CdS coatings which were doped by co-deposition from a separate In source during the previous program.[3] The In content was determined from microprobe measurements. The figure is plotted from data given in Figure 13 of Ref. 6. The resistivity of the coatings deposited using the doped cathodes (Fig. 7) is seen to be consistent with data obtained by Cd and In co-deposition (Fig. 8).

3.2 Role of Cadmium Vacancies

In CdS crystals S vacancies and Cd interstitials form donor levels, while Cd vacancies form acceptor levels. The donor levels are relatively close to the conduction band ($\sim$0.2 eV).[7] By contrast, the Cd vacancy levels are much farther from the valence band.* Consequently, CdS tends to be an n-type semi-

* It has been suggested that neutral cadmium vacancies are stabilized by the formation of bonds between adjacent sulfur atoms.[7] These bonds are weakened or destroyed by the addition of electrons. Thus, the addition of an electron to a neutral Cd vacancy level involves considerable energy. Accordingly, the vacancy acceptors form deep levels far from the valence band.

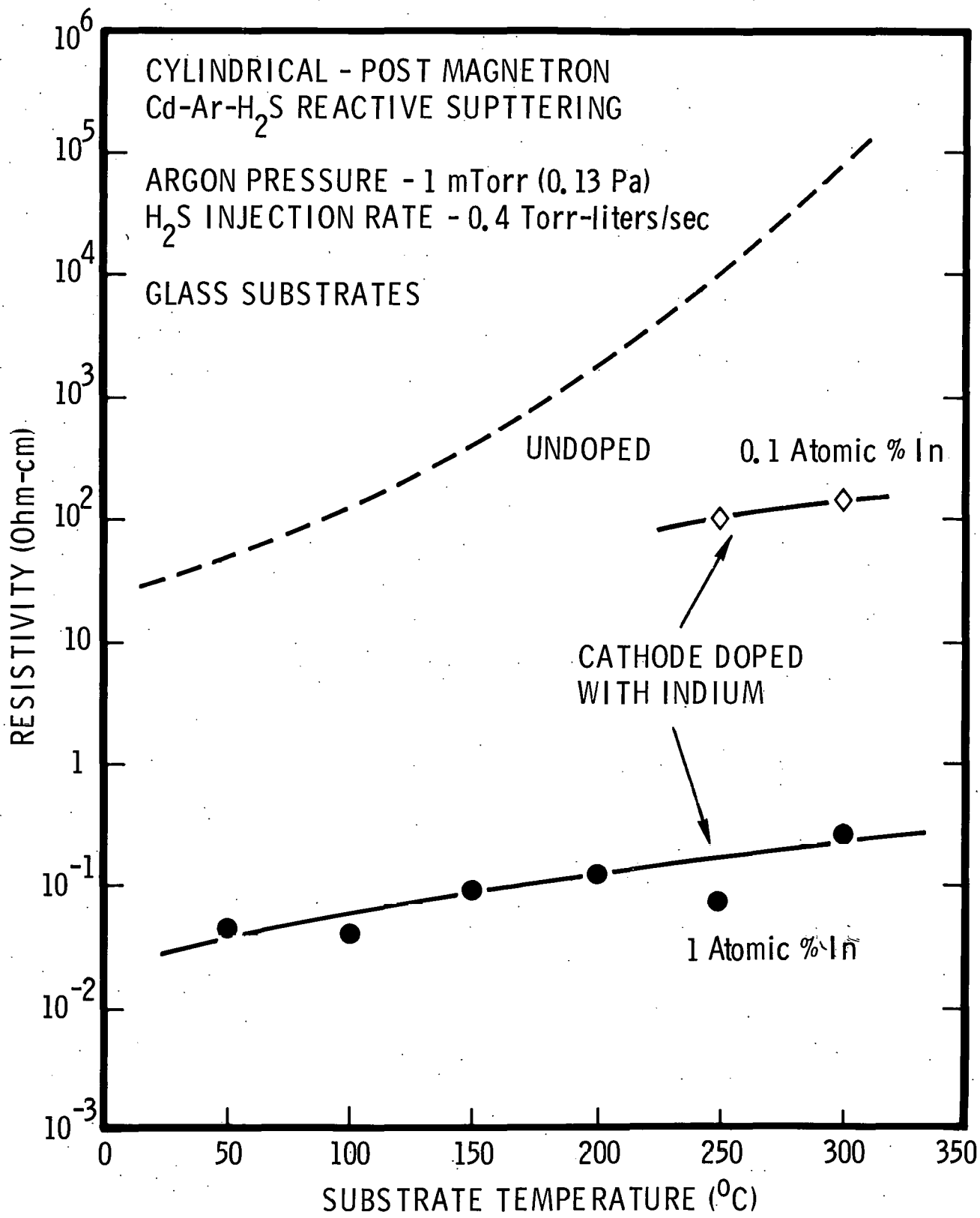

FIG. 7 Resistivity versus substrate temperature for reactively sputtered CdS coatings.

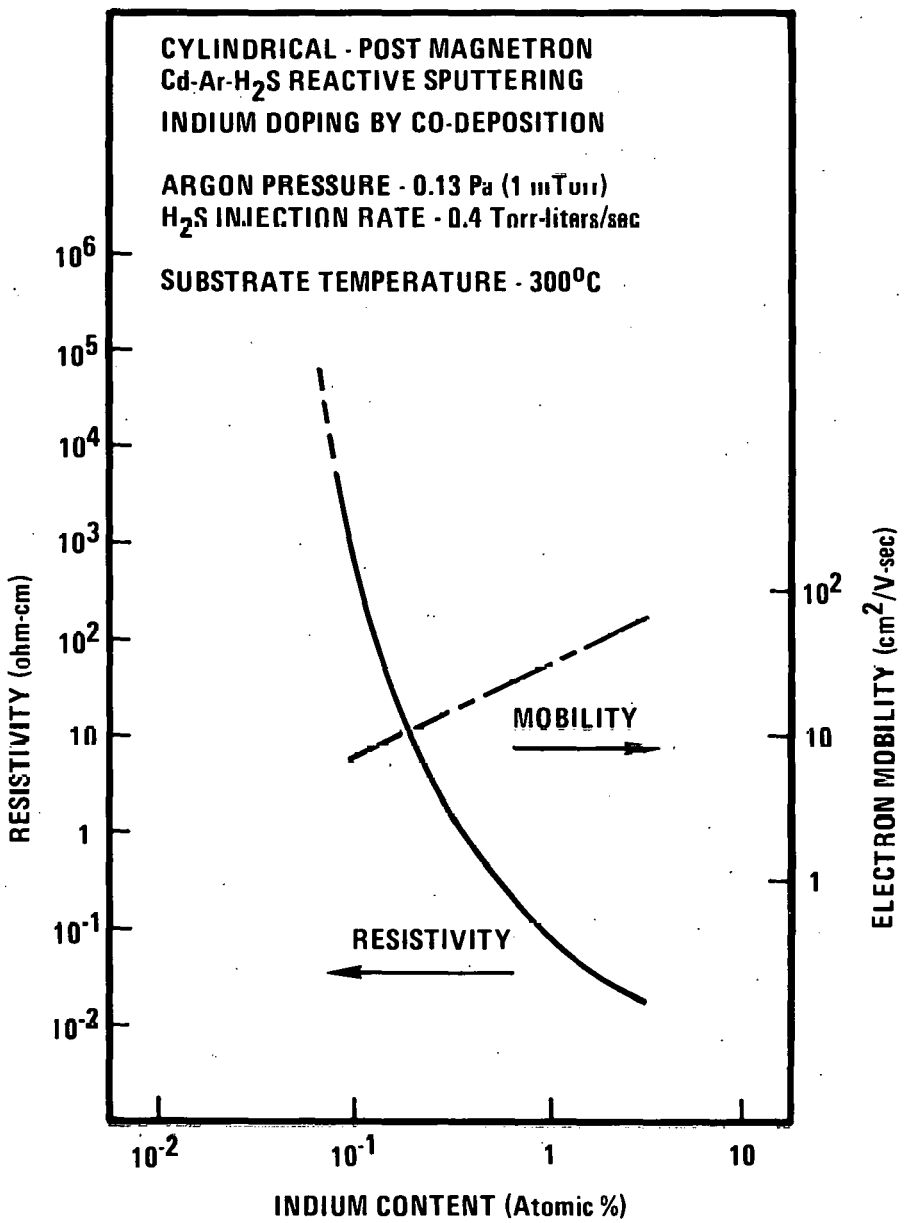

FIG. 8 Resistivity of reactively sputtered CdS versus indium content. Data from Ref. 6.

conductor.

Indium doping atoms on Cd sites form donors in the CdS crystal. The In_{Cd} donor level is close to the conduction band, so that ionization is always complete.[7] However, if the energy which can be recovered by transferring an electron from the In donor to the Cd vacancy acceptor level is larger than the energy required for Cd vacancy formation, then it is energetically favorable for the crystal to form Cd vacancies which compensate the incorporated In donors.[8] The probability for self-compensation becomes high in large-bandgap materials,[8] such as the highly ionic II-VI compound semiconductors.[9]

Thus, in order to obtain a high conductivity in both undoped and doped CdS, it is necessary that the Cd vacancy level be minimized.[10] Equilibrium calculations[7] and experimental observations[11] confirm that a high Cd vapor pressure over a CdS crystal minimizes Cd vacancy formation and enhances the effectiveness of In doping. Woodbury prepared In doped CdS samples by diffusing In into the crystals.[11] Samples were prepared with In levels ranging from about 10^{17} cm^{-3} to very degenerate cases having In contents of about 10^{20} cm^{-3}. Carrier concentrations were much lower than the doping levels (e.g., doping level of 10^{20} cm^{-3} yielded carrier concentration of $8x10^{17}$ cm^{-3}), unless the samples were fired in Cd vapor for a few hours at a relatively high temperature (800°C). With this type of treatment a 1:1 correspondence was obtained between the In content, as determined spectroscopically, and the room temperature carrier concentration, for carrier concentrations ranging from 10^{20} cm^{-3} down to the donor impurity level of about 10^{17} cm^{-3}.

Experimental evidence of the Cd vacancy effects described above have been seen in the reactively sputtered coatings. Figure 9, from our previous work,[3] shows the dependence of the deposition rate on the H_2S injection rate and substrate temperature for cylindrical magnetron reactive sputtering of Cd in H_2S. At high H_2S injection rates (A) the deposition rate is limited by the available Cd flux. At low injection rates (B) the sulfur flux is rate-limiting. The deposition rates decrease with increasing substrate temperature because of the reduced sticking coefficients. The coatings in Figs. 7 and 8 were deposited just to the left of the knee (point C) of the curve in Fig. 9; i.e.,

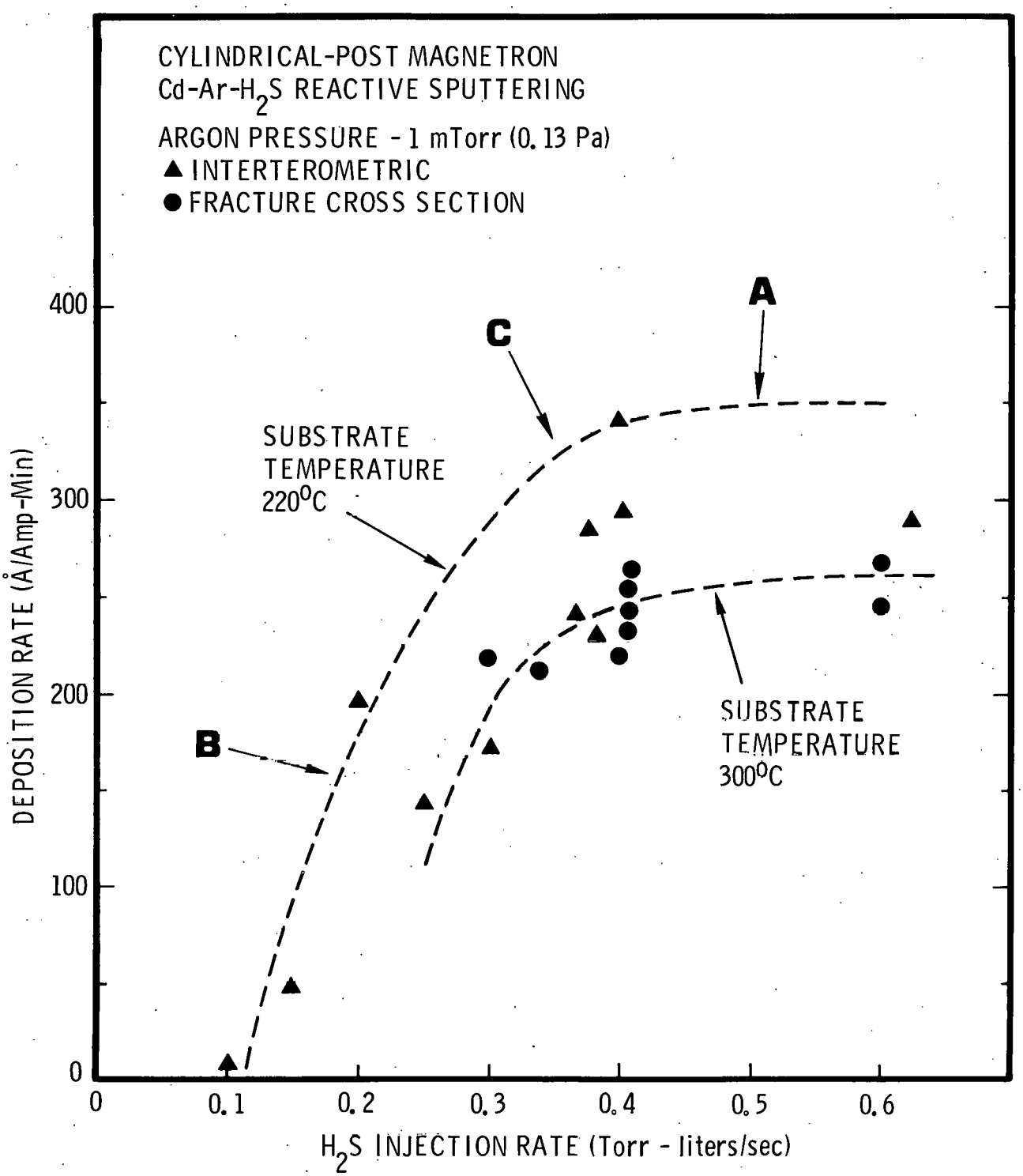

FIG. 9 Dependence of CdS deposition rate on H_2S injection rate and substrate temperature during cylindrical magnetron reactive sputtering. From Ref. 3

in the Cd-rich, S-deficient region where the Cd vacancy level might be expected to be reduced. Figure 10 shows the resistivity versus H_2S injection rate for doped and undoped CdS coatings deposited at a fixed substrate temperature of 250°C. The doping is seen to rapidly increase in effectiveness as the H_2S injection rate is reduced sufficiently to pass into the range (B in Fig. 9) where the H_2S flux and not the Cd flux is rate-limiting in the deposition process. Microprobe measurements for the 1 at. percent In case confirmed that the high resistivity coatings deposited at large H_2S injection rates did indeed contain the 1 at. percent of In. The resistivity of the undoped material is also seen to be reduced by about an order of magnitude as the H_2S injection rate is decreased. Additional work is required to determine the reason for the apparent "lower limit" to the resistivities that were obtained under sulfur-deficient conditions using the undoped and 0.1 at. percent In targets.

The use of pulsed H_2S injection to reduce the Cd vacancy level and therefore the resistivity of coatings deposited with an undoped cathode was described in Ref. 5. This method successfully reduced the resistivity of undoped CdS from 10^4 to 10^3 Ω-cm; i.e., by an amount identical to that associated with a reduction in the steady state H_2S injection rate as shown in Fig. 10. The pulsed method was also used with the cathode doped with 1 at. percent of In. Low resistivity (10^{-1} Ω-cm) coatings were obtained for average H_2S injection rates that would have yielded high resistivity (10^3 Ω-cm) coatings under steady state injection. This indicates that the pulsed injection method is in fact effective in reducing the Cd vacancy level.

3.3 Cu_2S Deposition Studies

Both doped and undoped CdS coatings deposited by reactive sputtering were sent to the University of Delaware Institute of Energy Conversion, where arrangements have been made to have Cu_2S layers deposited by the conventional $CuCl_2$ solution ion exchange process.[12] These coatings will be used as a basis for comparing sputtered and ion exchange deposited Cu_2S layers. These coatings will also permit a comparision between evaporated and sputtered CdS layers in terms of their influence on the Cu_2S layers that form by the ion exchange process.

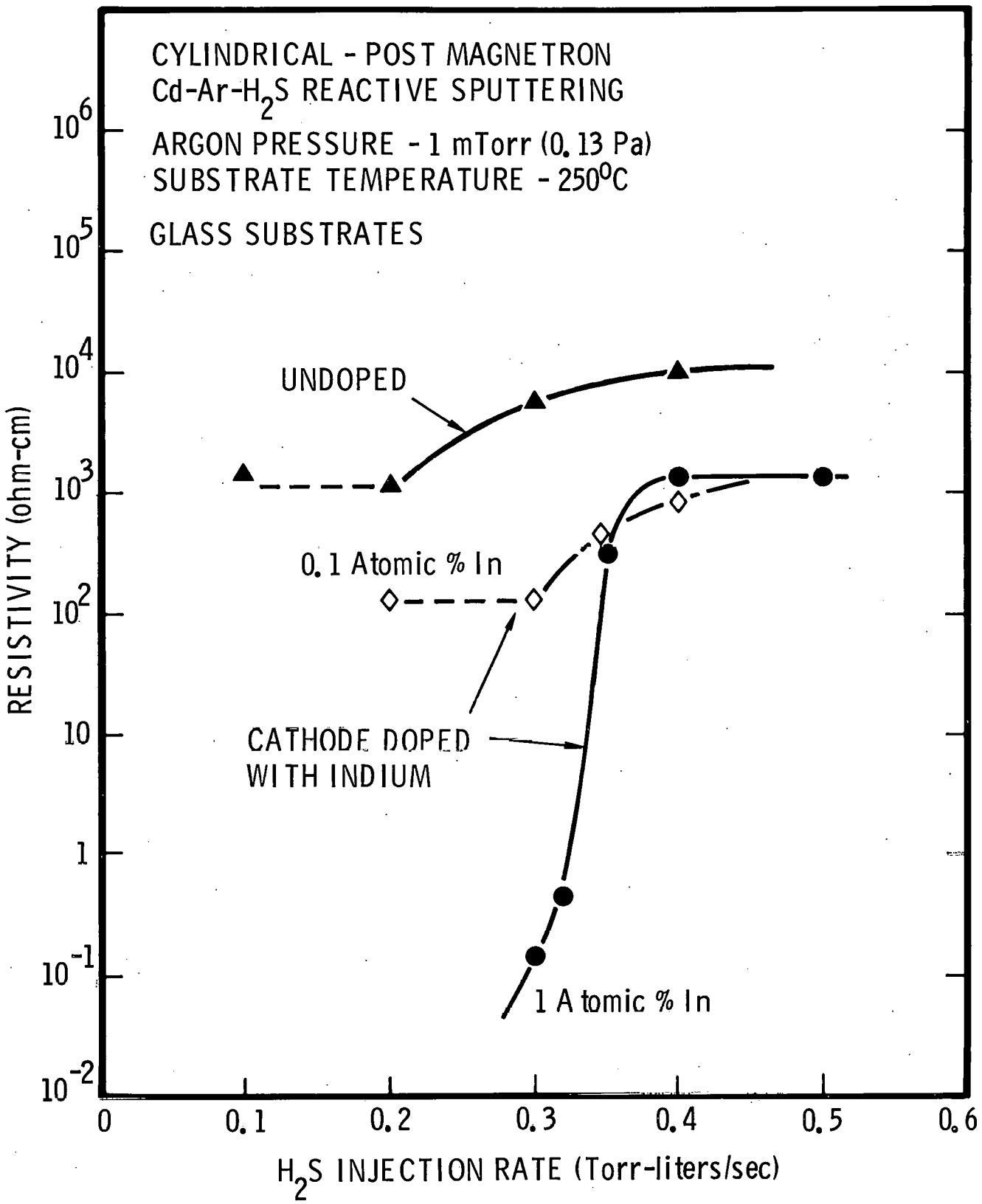

FIG. 10 Resistivity versus H_2S injection rate for reactively sputtered CdS coatings.

A first task in the shakedown of the modified apparatus will be to explore the systematics of Cu_xS deposition. As noted previously,[5] it is expected that the modified apparatus will be particularly important in improving the control of the Cu_2S deposition. When the shakedown of the Cu_2S deposition in the modified appparatus is complete, Cu_2S coatings will be deposited onto (CdZn)S coatings which were prepared by evaporation at the Institute for Energy Conversion. These heterojunctions will then be returned to IEC, where cells will be fabricated to evaluate the sputtered Cu_2S.

4. DEVICE-MATERIAL PARAMETER OPTIMIZATION (Task 3)

The cells fabricated during the third quarter were of the general form shown in Fig. 11. The substrates are 7059 glass plates 25 mm x 25 mm x 1.2 mm. The rear electrode is a 100 nm thick Nb layer which was deposited in a separate chamber. These precoated substrates were then stored and used as required in the multi-source chamber (old configuration) where sets of three cells were formed at one time. The reactively sputtered CdS layers were typically 3 to 6 μm thick. The CdS consisted of either a uniformly doped layer, with 0.1 at. percent In, or a composite n^+/n layer such as the one shown in Fig. 11. The composite layers were formed by sputtering in sequence from doped (1 at. percent In) and undoped cathodes. The thickness of the undoped region adjacent to the junction was varied between 0.1 and 0.5 μm thick. The highly doped material (0.1 Ω-cm) extended from this region to the rear electrode. The substrate temperature during CdS deposition was 250°C. The reactively sputtered Cu_2S layers were about 150 nm thick. They were deposited at a substrate temperature of 150°C. The Au top grid electrodes were applied in a separate chamber by sputter deposition using a mechanical mask. The grid consists of 31 lines 0.05 mm wide and 1 μm thick, spaced on 0.75 mm centers. The bus bars that connect the lines are not being deposited at the present time.

Cell uniformity was tested at Lockheed by independently examining the current-voltage characteristics of the individual grid lines. During our early attempts at cell fabrication, a problem of pinhole shorts at the grid electrodes was encountered.[4] Improved handling and storage procedures for the pre-metallized substrates has greatly reduced this problem so that cells with no shorts among

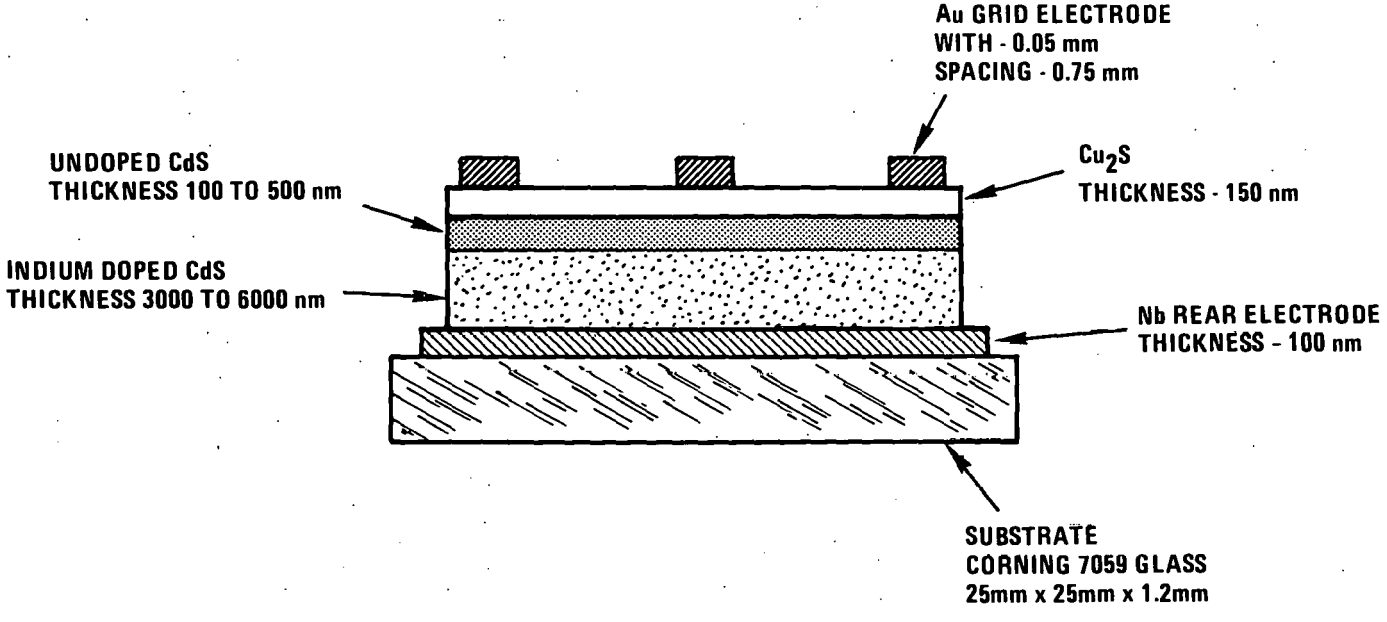

FIG. 11 General configuration of sputter-deposited solar cells fabricated during the third quarter.

the 31 grid lines are not uncommon at the present time. Furthermore, in contrast to the earlier cells, virtually all the cells now being deposited exhibit a photovoltaic effect in their as-deposited state. Thus a concentrated effort on device optimization is now beginning.

Table I summarizes the performance of some of the cells (824, 825, 917 and 920), with composite n^+/n CdS structures (type shown in Fig. 11) and 0.50 μm thick undoped layers, that were subjected to extensive testing during the third quarter.[16] The performance of one of the best cells (653) deposited on the present program[5] (using pulsed H_2S injection method) is shown for comparison, along with that for a high performance planar CdS cell fabricated at the Institute of Energy Conversion.[13] The IEC cell should probably be considered as a "nearly planar" cell, since a slight etch of the CdS is used prior to the deposition of the Cu_2S (by CuCl evaporation and ion exchange reaction). The estimated optimum performance of a truly planar cell is also shown for comparison. The estimate is based on: (1) top grid electrode system with 90% transmission, (2) Cu_2S layer thickness of 0.15 μm, (3) Mulder's single crystal Cu_2S optical data,[15] (4) zero recombination on the Cu_2S front surface, (5) total reflection at the Nb rear electrode, (6) a Cu_2S minority carrier diffusion length of 0.1 μm, (7) a fill factor of 0.8 (arbitrarily selected), and (8) an open circuit voltage of 0.54V (assumed). See Fig. 36 of Ref. 3.

The difference between the short circuit currents in the IEC cell and the idealized planar cell is believed to be indicative of the light trapping which occurs in the IEC cell because of the slight surface texture which is built into these cells. The sputtered cells have a very planar structure because of the smooth glass starting substrate and the absence of an etch step between and CdS and Cu_2S depositions. This is apparent in the intense CdS and Cu_2S interference pattern which has been observed in the sputter-deposited cells.[16] Therefore an assessment of the performance of the sputter-deposited cells can probably best be made by comparing their performance with that of the idealized planar cell. Picking $J_{sc} \sim 3$ mA/cm^2, $V_{oc} \sim 0.4$V, and FF$\sim$0.4 as being representative of the best sputtered cells, we conclude that:

TABLE I

PERFORMANCE OF SELECTED SOLAR CELLS

Cell	J_{sc}* (mA/cm^2)	V_{oc} (V)	FF	(%)
Cells having composite CdS structure shown in Fig. 11 with 0.5 μm thick undoped CdS layer.				
824	3.7	~0.3	--	--
825	2.1	~0.3	--	--
917	2.5	0.33	~0.3	~0.25
920	2.7	0.28	~0.3	~0.23
Cell deposited using pulsed H_2S injection method (see Ref. 5)				
653	3.5	0.43	0.41	0.58
Institute of Energy Conversion planar cell with evaporated CdS. Cu_2S deposited by dry process after slight each. (From Ref. 13)	21	0.54	0.72	8
Estimated optimum performance for planar cell with L_n = 0.1 μm. (see Ref. 14)	15.5	0.54	0.8	6.5

* Based on illumination intensity of 100 mA/cm^2.

J_{sc} for sputtered cell is ~20% of planar cell goal,

V_{oc} for sputtered cell is ~75% of planar cell goal,

FF for sputtered cell is ~50% of planar cell goal.

It is clear that the primary problem with the sputter-deposited cells is the low short circuit current. The second most serious problem is the low fill factor.

There are three factors that can cause a low J_{sc}:

1) Failure to absorb radiation and produce photocarriers because of a low absorptivity in the Cu_2S.
2) Failure of the photocarriers to reach the junction because of a high front surface recombination velocity or a low minority carrier diffusion length in the Cu_2S.
3) Failure of the photocarriers to pass over the p/n junction because of interface recombination.

Measurements of the short circuit current spectral response for cell 824 indicate that all of the photocurrent is generated within the Cu_xS layer.[16] This is consistent with previous work[17] which showed that the absorption characteristics of Cu_2S layers deposited using cylindrical magnetrons are equivalent to those reported for chalcocite, and with that of other workers who have fabricated cells with efficiencies of several percent using sputter deposited Cu_2S layers on single crystal and evaporated CdS.[18,19] These observations imply that the problem is at the p/n junction. Neglecting shunt currents, one can write

$$J_{sc} \sim J_L \eta_c \quad , \qquad (1)$$

where J_L is the light-generated current reaching the junction from the Cu_2S and η_c is the junction collection efficiency.[20] If we use a J_{sc} of 3 mA/cm^2 for the sputter-deposited cells, and assume that the $J_L \sim 15$ mA/cm^2 (ideal planar cell), we obtain $\eta_c \sim 0.2$ from Eq (1). Collection efficiencies for high performance evaporated cells are about 0.95. The J_L for the sputter-deposited cells is undoubedly a little less than 15 mA/cm^2. However, it is clear that the primary problem with the sputter-deposited cells is the low junction collection efficiency, which is perhaps about 0.25.

According to the theory of field-aided collection,[20] one has

$$\eta_c = \frac{E_o}{S_I/\mu + E_o} \quad , \tag{2}$$

where S_I is the interface recombination velocity for interface states created by the Cu_2S/CdS lattice mismatch, μ is the electron mobility in CdS, and E_o is the electric field strength at the junction.

For a uniform doping level the junction field is given by

$$E_o = \frac{2(V_D - V)}{W} \quad , \tag{3}$$

where V_D is the diffusion potential, V is the external junction voltage, and W is the depletion layer width. The depletion layer width can be written as

$$W = \left(\frac{2\epsilon\epsilon_o(V_D - V)}{q\, N_D^*} \right)^{1/2} \quad , \tag{4}$$

where q is the electronic charge, ϵ_o is the dielectric constant of free space, ϵ is the relative dielectric constant of CdS ($\epsilon \sim 10$) and N_D^* is the effective donor dopant density (assumed uniform).

The low values of η_c for the sputtered cells imply that $E_o << S_I/\mu$. When eqs. 1 through 4 are combined, one obtains the following relationship for small and negative bias V, in the limit of $E_o << S_I/\mu$.

$$J = J_L \frac{\mu}{S_I} \left(\frac{2q\, N_D^*\, V_D}{\epsilon\epsilon_o} \right)^{1/2} \left(1 - \frac{V}{V_D} \right)^{1/2} \quad , \tag{5}$$

The J^2 vs V dependence implied by Eq (5) has been confirmed for cells 653 and 917 in the low and negative bias regime.[16] These measurements therefore support the conclusion that most of the photocurrent reaches the junction and that $E_o << S_I/\mu$.

A more complete picture of the electric field at the junction, and its influence on the short curcuit current, is provided by capacitance versus voltage studies made at the Institute of Energy Conversion on cells with

evaporated CdS layers and at Lockheed for the sputter-deposited cells.[16] Table II compares depletion layer widths deduced from these capacitance measurements for cells in their as-fabricated state, after heat treatment and during subsequent exposure to solar illumination. The as-deposited depletion layer thicknesses are consistent with predictions made using Eq (4) and measured donor densities. The sputtered cell data is for cells with the composite n^+/n structure shown in Fig. 11. The depletion layer implied by the capacitance measurements corresponds, as would be expected, to the width of the undoped layer and therefore confirms the control which was maintained during the deposition. During heat treatment the depletion layer widths increased in both cases and, in the sputtering case, extended beyond the thickness of the cell. The significant observation is that under solar illumination the depletion layer width in the evaporated cells decreased by approximately an order of magnitude, while in the sputtered cells it did not.

Using $W = 0.2\,\mu m$ and $V_D = 0.8V$ for the evaporated cells yields $E_o = 8\times10^4$ V/cm. Recent estimates for high performance evaporated cells places S_I/μ in the range from 1.3×10^3 to 4.5×10^3 V/cm.[21] Using $S_I/\mu = 3\times10^3$ V/cm, we obtain $\eta_c = 0.96$ for the evaporated cells using Eq (2). The I^2 vs V plots indicate that the diffusion potentials for the sputtered cells are a little less than 0.8V.[16] Using $V_D = 0.5V$ and $W = 3\,\mu m$ for the sputtered cell yields $E_o = 3.3\times10^3$ V/cm. This electric field, along with $\eta_c \sim 0.25$, implies that S_I/μ 1.3×10^4 V/cm, a value that is three to four times larger than the values for the evaporated cells. The higher S_I/μ in the sputtered cell may be due to a greater degree of disorder on the surface of the sputtered CdS (no etch is used to place the junction within the CdS).

The above analysis can be summarized as follows:

1) The major reason for the poor efficiency of the sputter-deposited cells is a poor junction collection efficiency, which results from a low electric field and an elevated S_I/μ.

2) A major difference between the cells fabricated using evaporated CdS and those fabricated thusfar by sputtering at Telic is that the depletion layer width in the sputtered cells does not decrease significantly under solar illumination.

TABLE II

DEPLETION LAYER WIDTHS

	Evaporated CdS Wet process Cu_2S Inst. Energy Conv.	Sputtered CdS Sputtered Cu_2S Telic/Lockheed
As deposted	$\sim 0.1\ \mu m$	$\sim 0.5\ \mu m$
After heat treatment	$\sim 10\ \mu m$	$\sim 5.2\ \mu m$
Under solar illumination	$\sim 0.17\ \mu m$	$\sim 3.0\ \mu m$

The low electric field is particularly important. The dependence of η_c on E_o and S_I/μ is shown in Fig. 12. The range of S_I/μ observed for evaporated cells is indicated by the shading. Note that if the electric field in the sputtered cells were increased to a value comparable to the evaporated cells ($E_o = 8 \times 10^4$ V/cm), then η_c for the sputtered cells would be about 0.9, with no improvement in S_I/μ.

The generally accepted model for junction formation in the evaporated cells is that the heat treatment causes Cu acceptors to diffuse into the CdS junction region. The compensating effect of these acceptors causes the space charge region to increase in width. However, under illumination the space charge region shrinks by an order of magnitude because of trapping of photo-generated holes by the Cu acceptors.[20]

The explanation for the failure of the depletion layer width to decrease under illumination in the sputter-deposited cells may be related to an enhanced Cu diffusion into CdS when In doping is present. Enhanced diffusion of In and Cd into CdS containing In has been measured.[7,22,23] The usual explanation is that charge neutrality requires that one Cd vacancy be present in the crystal lattice for every two In atoms, and that these vacancies promote those diffusion processes which occur via a vacancy mechanism. The copper diffusion into CdS is expected to proceed by a vacancy mechanism. Therefore, for a given heat treatment, it is possible that much more Cu passes into the In-doped sputtered coatings than passes into the undoped evaporated cells. Different heat treatment procedures are undoubtedly required for In-doped cells. The use of In is not considered to present a fundamental problem in itself. Cells having efficiencies of 6% were fabricated on the Clevite program using evaporated CdS layers doped with In.[24]

It is planned that tailored CdS-In doping profiles and cell heat treatments will be used to control the width of the depletion layer and therefore the junction electric field strength. Elemental analysis (Auger and SIMS), with depth profiling, will be used to determine the Cd, In and Cu distribution in the CdS junction region. Post-deposition heat treatments will be used in an attempt to reduce the disorder on the surface of the sputter-deposited CdS before depositing the Cu_2S.

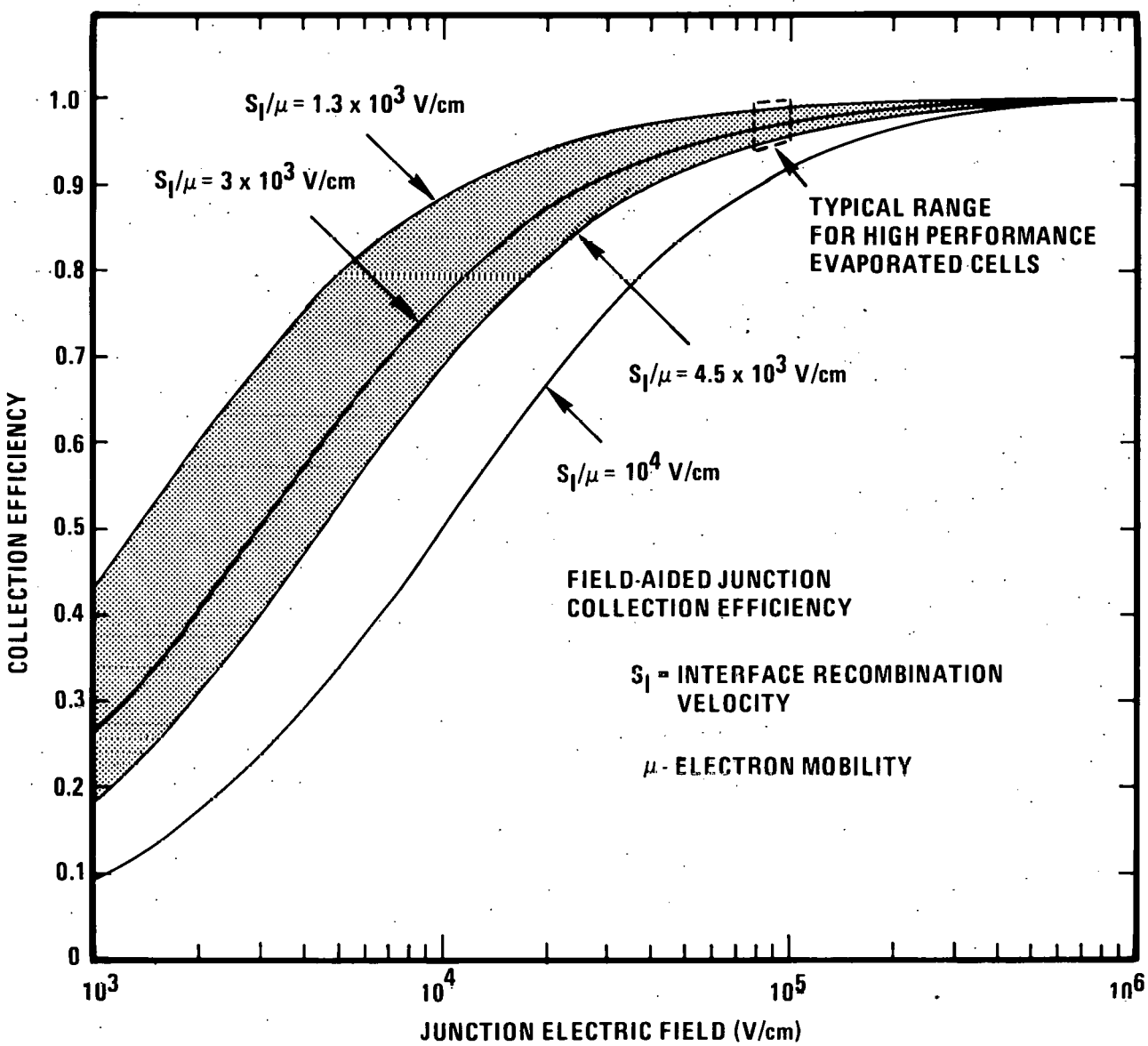

FIG. 12 Dependence of η_c on E_o for various values of S_I/μ. Range of S_I/μ observed for evaporated cells[22] are indicated by the shaded region.

5. SUMMARY STATUS

Progress has been made on all of the research tasks during this reporting period.

Installation of the modified deposition apparatus with its improved substrate mounting, shielding and vacuum interlock (Task 1) is virtually complete. Shakedown tests are beginning. Cu_xS deposition will be examined first. It is anticipated that the modified apparatus will permit significant improvements in the control and reproducibility of the Cu_xS reactive sputtering process.

Additional work has been done on controlling the CdS resistivity through In doping (Task 2). Resistivities of the order of 10^2 Ω-cm have been achieved for coatings deposited using a target doped with 0.1 at. percent In. The importance of precisely controlling the H_2S injection rate when depositing CdS coatings by means of reactive sputtering using an In doped target has been established. The requirement for controlling the H_2S injection rate apparently results from the necessity for minimizing the Cd vacancy level, because of the effectiveness of these vacancy acceptors in compensating the In donors.

Considerable progress has been made in improving the general quality of the sputter-deposited cells (Task 3). The number of pin hole shorts which are present in the Au gridded cells has been greatly reduced and it is not uncommon to now form cells with no flaws among the 31 grid lines. Furthermore, virtually all the cells now being deposited exhibit an easily discernible photovoltaic effect in their as-deposited state. Accordingly, a concentrated effort on device processing is now beginning.

The sputter-deposited cells fabricated thusfar have been characterized by low short circuit currents. Cell current-voltage characteristics, and capacitance measurements of the depletion layer thicknesses, reveal that the major cause of the low short circuit current is a poor junction collection efficiency, due primarily to a low electric field at the junction. A major difference between the cells fabricated by sputtering thusfar and the high performance evaporated cells is that the post-heat treatment depletion layers in the sputtered cells do not undergo the large decrease in width on exposure to solar radiation that is characteristic of the evaporated cells. Future work will

examine the use of tailored CdS-In doping profiles and cell heat treatments to control the depletion layer widths and thereby the junction electric field strengths. Elemental analysis with depth profiling will be used to determine the Cd, In and Cu distribution on the CdS side of the junction.

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