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Seventh Workshop on The Role of Impurities and Defects in Silicon Device Processing

Extended Abstracts and Papers

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Workshop Chairman: B.L. Sopori

Program Committee:
R. Sinton, T. Tan, J. Kalejs, J. Gee, L. Jastrzebski, T. Saitoh, B. Sopori

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, Colorado 80401-3393
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Seventh Workshop on The Role of Impurities and Defects in Silicon Device Processing

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Poster Papers

R&D Issues for Crystalline Silicon to Support GW/Yr. Goal by the Year 2010

Bhushan Sopori
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

The demand for photovoltaic (PV) energy has been increasing at a rapid pace during the last few years. The silicon technology is continuing to meet this need with improved solar cell/module efficiency and cost. It is expected that this demand will continue to grow, and that by the year 2010 it will exceed 1GW/yr. Other factors such as the "Million Solar Roofs" Program, if successful, can further enhance this demand. To date, nearly 90% of the PV demand is satisfied by crystalline silicon technology, with the balance using a-Si and other thin-film technologies. Although it is expected that newer technologies such as CIS and CdTe will be launched into commercial production, silicon is expected to continue to have a dominant role. This is based on the fact that the price for silicon modules has already come down, and further cost reductions, approaching $2/W, are being contemplated. Increased productions that can raise the factory output levels to 25 MW/yr. can further reduce the module cost to $1.78/W.

Clearly, silicon is facing challenges, both on the absolute terms of lowering the module costs and with the advent of potentially lower-cost thin film technologies. There are concerns as to how Si can meet these challenges, continue as the leading technology in the future, and meet the heavy demands in the future. The flip side of this argument is that the newer technologies have to compete with the performance, reliability, and cost of crystalline silicon technologies.

The previous workshops have addressed some issues on high demands and cost reduction by improving the cell performance and the cell cost. This workshop is aimed at raising the awareness of these issues and initiating planning activities. At the outset, a workshop on the role of impurities and defects in silicon device processing may appear out of place for discussion of such issues. However, because a major impact on the production can occur precisely by improving the material quality and fabrication procedures, this workshop is a valuable opportunity to address these issues. Some of these issues are related to:

- Silicon feedstock: availability/cost/quality
- Improved material quality through improved crystal growth, and post-growth gettering and defect passivation
- Further understanding the performance-limiting factors and the approaches to resolve them
- The use (handling, device processing, encapsulation) of thinner wafers
- Higher efficiency device fabrication
- Higher throughput processes
- "PV" oriented equipment
- Monitoring techniques

In addition to current "wafer-based" devices, it is expected that a major effort will be devoted to the development of thin silicon solar cells. New understanding of the mechanisms of nucleation and growth, grain enhancement processes, thin film stress control, low-temperature gettering, and defect passivation are all a testament to the success of this emerging approach.

* There are additional issues related to module fabrication, and system design and development, that will not be directly discussed in this workshop.

A Study of the Manufacture at 500 MWp p.a. of Crystalline Silicon Photovoltaic Modules

T.M. Bruton (BP Solar), G. Luthardt, K.D. Rasch, K. Roy (ASE), I.A. Dorrity, B. Garrard, L. Teale (Crystalox), J. Alonso, U. Ugalde (IES-UPM), K. Declerq, J. Nijs, J. Slufcik (IMEC), A. Räuber, W. Wettling (FhG-ISE), A. Vallêra (ICAT)

In the framework of the EU programme APAS a study was performed by eight companies and research institutions with the task to determine if 500 MWp per year could be successfully manufactured using crystalline silicon technology. The result of the study showed that module costs of 1 ECU/Wp using multicristalline wafers with screen printed contacts are achievable. Further extension of the ribbon silicon technology by the EFG process could lower costs further to 0.7 ECU/Wp. It was confirmed that it is market size which is a key driver in cost reduction.

Annual production of silicon PV modules is presently around 60 MWp p.a. This is very small compared to the market for PV demanded by such schemes as „PV power for the world", the ALTENER study and the Madrid Conference on a „Renewable Energy Strategy for Europe" where an annual production rate of 500 MWp to 1 GWp was required. This study was a multi-institution study carried out under the APAS programme of the European Commission [1] to determine if manufacture at the scale of 500 MWp p.a. is possible with crystalline silicon technology. The study also examined the potential to reduce the costs by increased volume with the target of 1 ECU/Wp for factory gate module costs.

The silicon PV module manufacturing process can be sub-divided into five stages:

(1) Feedstock production, (2) crystallisation, (3) wafering, (4) solar cell processing and (5) module fabrication. A group was appointed to study each of these stages as a task.

Approximate calculations of product costs were carried out at the task level but the detailed costing was done by the IES group in Madrid using a commercially available computer costing package, STAMPP (task 6). Here a population weighted and over several European countries averaged labor rate of 14.4 ECU/hr was used which included all social costs.

(1) Concerning the silicon feedstock it was assumed that the demand of 5000 tons p.a. should be provided by a new production facility that is producing silicon only for PV applications. After investigating several other technical paths it was concluded that a somewhat relaxed Siemens process could be used for this feedstock fabrication and that the polysilicon costs would be about 20 ECU/kg, a number which is higher than todays feedstock price which is based on „heads and tails" of the microelectronic industry.

(2) Three possible options to convert the silicon feedstock into a crystalline form appropriate for wafer production were taken into account in the study: (i) directional solidification of multicrystalline ingots (DS), (ii) Czochralski growth of monocrystalline boules (CZ) and (iii) direct crystallization as silicon foil (EFG). For each method costs were evaluated together with producers assuming the most advanced technique available.

(3) Wafering was assumed to be performed by multiwire saws (MWS) with little technological improvement above present day practice. Wafer dimensions were assumed as 125x 125x 0.2 mm^3 and the kerf loss as 230 μm.

(4) Five solar cell processing schemes were considered in the study:

- Screen printing solar cells [2] which is the predominant present day manufacturing process (SP). This is the assumed process also for EFG material although the exact process details of the present EFG solar cell process are confidential.
- Laser grooving of buried grid (LGBG) cells. This is a high-efficiency process which has been in operation at BP Solar España since 1991 [3].
- MIS contacting to diffused solar cells which is developed at ASE and which has demonstrated reproducibly high-efficiency solar cells [4].
- A simplified localized back surface field (LBSF) process for solar cells. The LBSF process which is similar to the PERL process of UNSW, (the world record holding process) has demonstrated near world record efficiencies with float zone wafers at Fraunhofer ISE [5].

It was necessary to set solar cell efficiencies and wafer size and thickness giving full consideration to data inputs from wafering and module fabrication studies. Table 1 shows the efficiencies for the various technologies as assumed for the cost calculations.

Table 1. Assumed efficiencies versus wafer type and size for different cell processing technologies.

Cell Technology	125x125 mm^2, mono	125x125 mm^2, multi	150x150 mm^2, multi
Screen printed	16	15	14
LGBG	18	16	16
MIS-Diffused	17	15	13
EFG	n/a	14.4	n/a
LBSF	20	n/a	n/a

(5) Two module technologies were investigated in the study:

- Reflow soldering for the tabbing process and vacuum lamination using EVA, (S/L)
- Ultrasonic welding for the tabbing process and resin in-fill between glass plates, (USW/RF).

Two high capacity highly automated module lines were assumed for this task.

(6) For the detailed cost calculations seven alternative scenarios have been costed [6]. They are summarized in Table 2.

Table 2. Scenarios for costing of different crystalline silicon manufacturing technologies. The abbreviations used are explained in the above text.

Process	Crystallization	Wafering	Solar Cell Proc.	Module Assemb.
Scenario 1	DS	MWS	SP	S/L
Scenario 2	CZ	MWS	SP	S/L
Scenario 3	CZ	MWS	LGBG	S/L
Scenario 4	CZ	MWS	MIS	S/L
Scenario 5	CZ	MWS	MIS	USW/RF
Scenario 6	CZ	MWS	LBSF	S/L
Scenario 7	EFG	n/a	SP	S/L

The costs as specified for the five processing tasks are given in Table 3.

Table 3. Factory cost in ECU/Wp for different crystalline manufacturing scenarios at 500 MWp p.a. manufacture by process step.

Process	Crystalliz.	Wafering	Solar Cell	Module assembly	Module power(Wp)	Cost ECU/Wp
Scenario 1	0.28	0.22	0.11	0.30	86.9	0.91
Scenario 2	0.62	0.21	0.12	0.31	85.6	1.25
Scenario 3	0.55	0.18	0.14	0.28	96.3	1.15
Scenario 4	0.59	0.21	0.18	0.30	90.9	1.28
Scenario 5	0.59	0.21	0.18	0.36	90.9	1.34
Scenario 6	0.50	0.18	0.83	0.27	107.0	1.78
Scenario 7	0.28	0	0.11	0.32	81.5	0.71

In Table 4 the cost for the seven scenarios are specified with respect to the main cost categories as labour, materials, maintenance, depreciation and overhead. All costs are given in ECU/Wp.

Table 4. Factory cost in ECU/Wp for different manufacturing scenarios broken down into the main cost categories at 500 MWp p.a. manufacture.

Process	Labour	Materials	Maintenan.	Depreciat.	Overhead	Cost ECU/Wp
Scenario 1	0.10	0.66	0.03	0.07	0.05	0.91
Scenario 2	0.13	0.85	0.07	0.12	0.07	1.25
Scenario 3	0.13	0.78	0.06	0.12	0.06	1.15
Scenario 4	0.13	0.88	0.09	0.17	0.06	1.28
Scenario 5	0.13	0.88	0.09	0.17	0.07	1.34
Scenario 6	0.32	0.94	0.14	0.27	0.11	1.78
Scenario 7	0.13	0.40	0.04	0.07	0.07	0.71

These results show that the avoidance of the wafering step in the EFG process produces the lowest module cost. The well proven route for screen printed cells on wafers made by directional solidification and wire sawing gives the next lowest cost and is at 0.91 ECU/Wp below the 1 ECU/Wp target. The technology improvements required to achieve this scenario are modest and all the individual parameters of ingot size, wafer thickness and cell efficiencies have been demonstrated. All the processes based on CZ wafers show higher costs because of the high wafer cost. However it can be seen that the LGBG process, with the highest efficiency, produces the lowest cost on monocrystalline wafers.

The other new processes require further improvement to be cost effective and the study has shown which areas must be addressed to achieve cost competitiveness. In particular the LBSF process which demands by far the highest labour and investment costs in this study is not optimized and requires more detailed study and process experience to fully specify the lowest cost production route. The balance of systems benefit of very high efficiency should also be noted.

The study has shown, subject to appropriate investment, that there are no barriers to achieving 500 MWp p.a. production of photovoltaic modules using crystalline silicon. Costs below or near 1 ECU/Wp are projected for a number of crystalline silicon manufacturing technologies. Investment costs are in the region of 1 ECU/Wp of installed production capacity and around 3000 jobs would be created in a 500 MWp p.a. manufacturing plant.

This study has clearly confirmed the widely held view that by increasing the market size, the prize of PV modules will fall. Indeed the study shows that it is market size which is one of the most significant factors in achieving cost reduction.

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Addresses of the participants of the study

T.M. Bruton
BP Solar International
PO Box 191
Sunburry on Thames
Middlesex TW16 7XA, UK

G. Luthardt, K.D. Rasch, K. Roy
ASE GmbH
Industriestraße 13
D-63755 Alzenau, Germany

I.A. Dorrity, B. Garrard, L. Teale
Crystalox Ltd.
1 Limborough Rd.
Wantage, Oxon OX12 9AJ, UK

J. Alonso, U. Ugalde
Instituto Energia Solar
E.T.S.I. de Telecomunicaciones
Ciudad Universitaria
E-28040 Madrid, Spain

K. Declerq, J. Nijs, J. Slufcik
IMEC
Kapeldreef 75
B-3001 Leuven, Belgium

A. Räuber, W. Wettling
Fraunhofer Institute for Solar Energy Systems
Oltmannsstrasse 5
D-79100 Freiburg, Germany

A. Vallêra
ICAT
Univ. de Lisboa
Edif C1, Campo Grande
P-1700 Lisboa, Portugal

Grown-In Defects in FZ and CZ Silicon Crystals

Takao ABE
Isobe R&D Center, Shin - Etsu Handotai
2-13-1 Isobe, Annaka - Shi, Gunma - ken 379-01

ABSTRACT

Six silicon ingots of different diameters (200, 150, 125, 100, 75 and 50 mm) were grown from a single crystal puller under identical crucible and growth conditions. Each crystal included a region containing a junction between high and low growth rates. The distributions of SEP (Secco etch pit) defects and FP (flow pattern) defects were observed using longitudinal cut surfaces (110) along the growth direction <100>. Only the SEP defects were observed in the 50 mm crystal, and this was in the region in and around the time of slow growth rate. For the 75 and 100 mm crystals, a similar but smaller region of SEP defects was seen in the area of low growth rate. However, FP defects were also observed in the high growth rate regions of these crystals. For the crystals of 125 mm diameter and larger, both defects were found coexisting throughout the crystals. An effect on the defect density is still seen when the crystal growth was slowed. The behavior of the SEP and FP defects are exactly the same as that of A and D defects in FZ crystals, respectively. From the results presented here, it is confirmed that the species of intrinsic point defects is determined not by growth rate, but by the thermal gradient at the growth interface in CZ crystal growth. This has been demonstrated in the past for FZ crystal growth.

INTRODUCTION

As integrated circuits such as D-RAMs go to finer design rules, smaller grown-in defects have an opportunity to affect the device performance. Therefore, since traditional IG (internal gettering) treatment [1] may not be enough, a high temperature hydrogen annealing has been proposed for denuding [2]. Moreover, epitaxial wafers which can be made free of grown-in defects have been used for high performance microprocessors and may be used in the future D-RAM generations. Finally, as the age of 300 mm wafers comes, it is anticipated that SOI may be utilized for all advanced devices. The behavior of grown-in defects during the bonded SOI process has been recently reported [3].

On the other hand, concerning R-OSF (ring like distributed oxidation induced stacking faults) the generation and annihilation conditions have been clearly demonstrated by Dornberger et al [4]. The nuclei of these stacking faults come from one of the grown-in defects discussed in this paper. However, with regard to COP (crystal originated particle) [5] and FP defects, the generation mechanism has not been discussed. The GOI (gate oxide integrity) clearly depends on the density of FP defects [6] but little has been reported (except one paper [7]) showing FP defects to affect the real device characteristics. This may be true due to the fact that actual device processes include a high temperature oxidation before the gate oxidation. Annihilation of the FP defects in such a process has been demonstrated by Yamagishi et al. [6]. It should be remembered, however, that if processing temperatures are reduced in the future, a serious effect from the FP defects may result.

Whereas the FP defects are associated with excess vacancies, it is shown in this paper that the SEP defects arise from secondary defects formed by excess silicon interstitials. The SEP defects may, therefore, be more important than the FP defects. Many researchers tend to connect the growth rate of the crystal with the formation of grown-in defects, but it is shown here that this concept is not true and the Voronkov theory [8] is not complete.

EXPERIMENTS

A conventional CZ furnace was charged with 70 kg and used for pulling 6 different diameter silicon crystals (200, 150, 125, 100, 75 and 50 mm). First, the 200 mm crystal was grown and then poly crystal with the same weight as the 200 mm crystal was recharged into the puller. This process was repeated as crystals of progressively smaller diameters were grown. The crystals used here are summarized in Table 1.

Diameter (mm)	200	150	125	100	75	50
Weight (kg)	39.3	18.6	12.4	8.0	4.6	2.5

Table 1 Crystal weights (= recharged weights) of each diameter crystal.

Each crystal was grown to about 30 cm in length. The growth rate through most of the crystal was fixed at 1.0 mm / min. At the middle of the crystal (approximately 15 cm position) the growth rate was suddenly changed to 0.2 mm / min and held for 30 min (6 mm in length). To avoid the diameter increasing as the growth rate was decreased, the input power was changed just prior to slowing the growth (to add 14% for 200 mm and 2.5% for 50 mm). Before returning to the 1.0 mm / min growth rate, the input power was decreased. Seed rotation was 15 rpm and the crucible was counter - rotated at 1.5 rpm.

The crystals are <100> orientation and p type 10 - 20 Ωcm. Each crystal was cut perpendicularly to growth direction with the length of 15 cm as including the low growth rate region at center and then cut longitudinally to growth direction with (110) surface. Each wafer was polished with 700 μm in thickness. These wafers were deposited vertically in Secco etch solution for 1 hr. to observe the SEP and FP defects. In order to observe the R-OSF distribution and the growth interface shape which was influenced by low growth rate, these wafers were annealed at 1100 C, 1 hr in wet oxygen and observed by conventional x-ray diffraction topography. The distributions of oxygen and carbon concentration were measured along the growth direction centerlines by IR absorption using the measurement area of 4 mm in diameter. For the analysis of the defect distributions a wafer lifetime (WLT) method was applied using SEMILAB WT-85. In the FP defect annihilation experiment, PROTECH RTPF-850 as a rapid thermal annealer was used.

RESULTS

Figure 1 shows the x-ray topographs of the wafers annealed for the R-OSF observations, but contrast of R-OSF was not clearly seen. The temperature fluctuations induced by the operation at low growth rates caused the noted diameter changes in all cases. The growth interfaces as revealed by oxygen striations are varied by the low growth rate, but much less so for the larger diameter.

Figure 2 shows dark-field photographs using oblique lights after Secco etching. Macroscopic distributions of etch pits can been seen. In Fig. 2 (a) the 50 mm wafer is shown. There is a wide area before and after the low-growth section where SEP are generated. A part of this area was delineated by Nomalski optical microscopy and is shown in Fig. 3 (a). Various etch pits of different shapes and sizes are seen. The area before and after the slow growth shows SEP defects. Next, in Fig. 2 (b), the 100 mm wafer is seen. The area before and after the slow growth shows only SEP defects similar to the 50 mm sample, but in the outer high growth regions, FP and SEP defects are noted. The size of the core pit of the FP defect is extremely small compared to the SEP defects as seen in Fig. 3 (a). Neverthless the size and density of the FP defects are small, we can easily observe their distributions as shown in Fig. 2 (b) owing to the extending flow patterns. The 200 mm wafer is shown in Fig. 2 (c). Here the effect of the slow growth on defect generation is only seen in the peripheral region. As can be seen in Fig. 3 (c), the defect area consists of both SEP and FP defects.

Figure 1 shows a sketch with the three types of defect regions superimposed : mainly

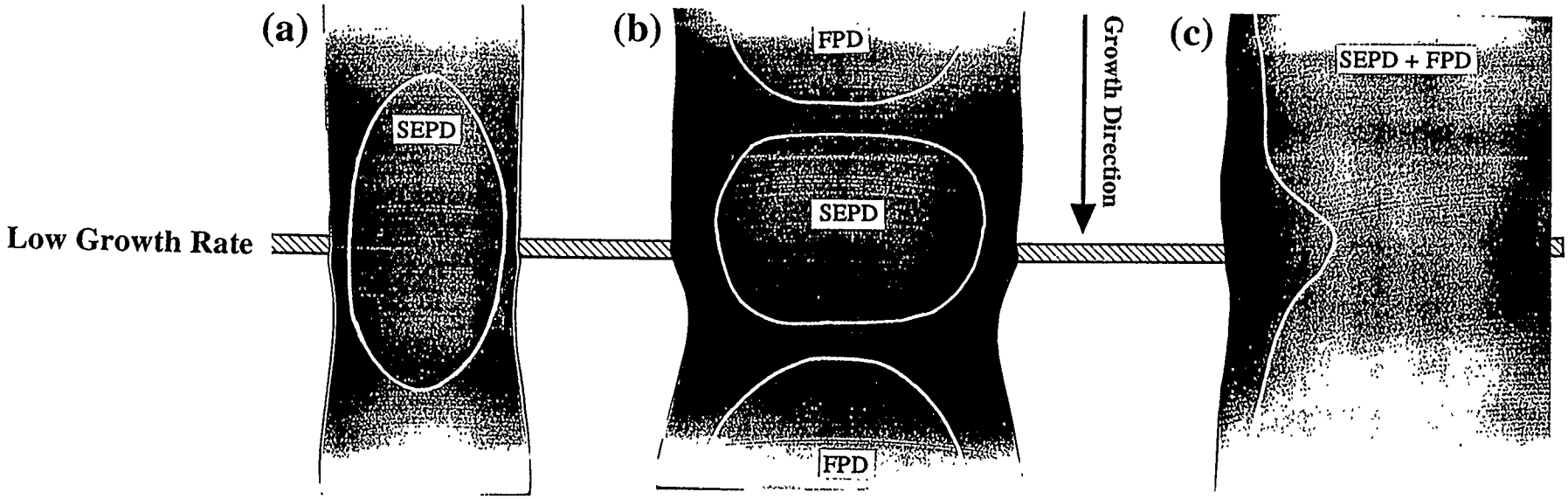

Fig. 1. X-ray topographs of the longitudinal cut wafers with 50 mm (a), 100 mm (b) and 200 mm in diameter (c) annealed with 1100 C, 2hrs in wet. White lines showing the SEP and FP defect regions are superimposed by sketching from the dark field photographs as seen in Fig. 2.

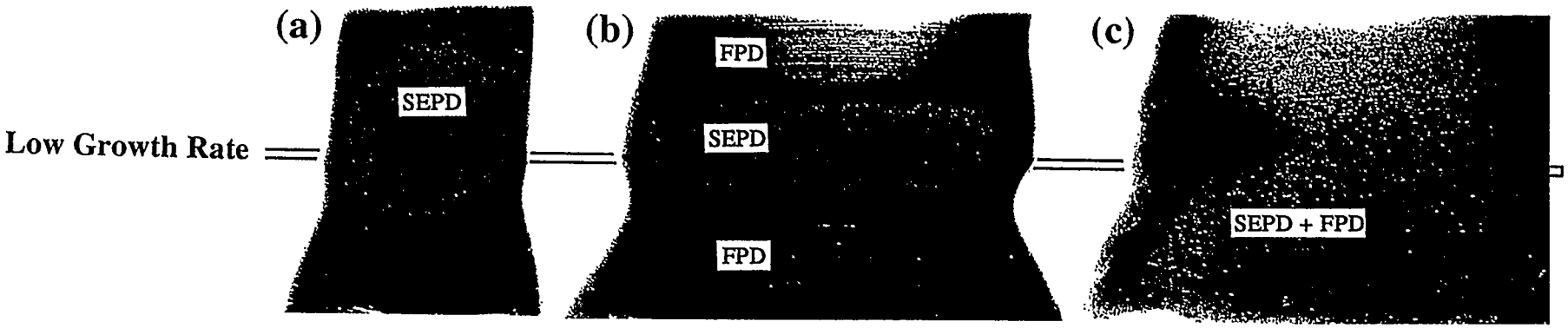

Fig. 2. Dark field photographs. 50mm (a), 100mm (b) and 200mm wafers in diameter (c).

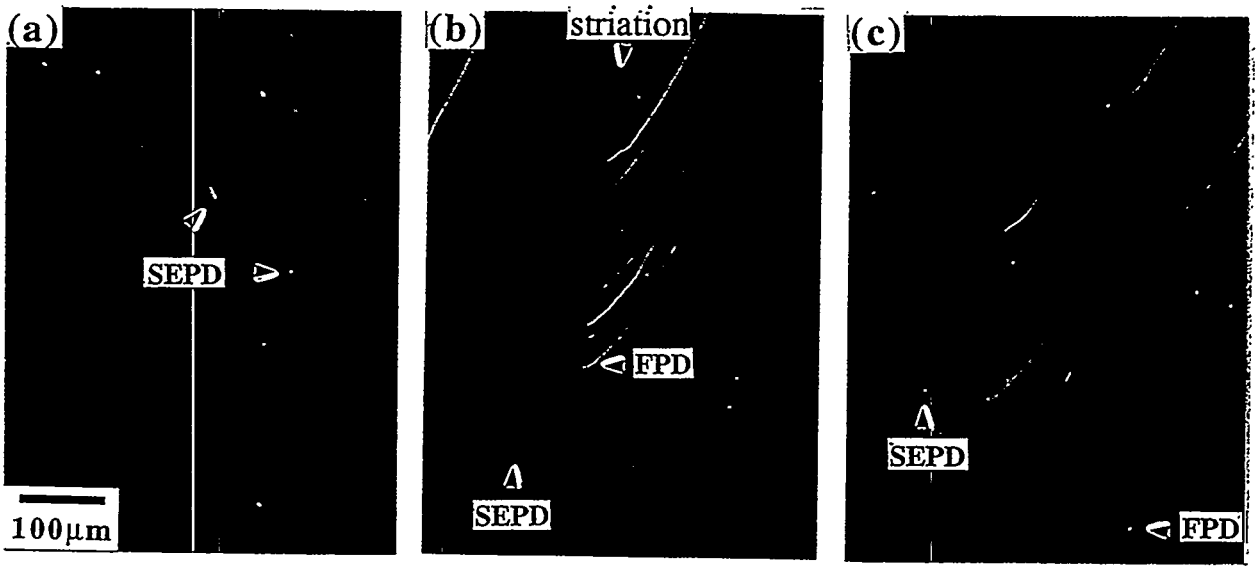

Fig. 3. Microphotographs (a), (b) and (c) which are obtained in center area in Fig. 1 (a) the upper area of Fig. 1 (b) and the middle area of Fig. 1 (c), respectively.

SEP, mainly FP on growth striations, and a combination of FP and SEP. The SEP are the main defects for small diameter crystals, while FP defects increase with larger diameters until finally the mixed defects form. Figure 4 (a) and (b) give an analysis of the density of SEP and FP defects along the growth direction centerlines for the 50, 100 and 200 mm wafers. The counting volumes of each defect are 0.1 mm x 5 mm x 24.4 μm for the SEP and 1.0 mm x 5 mm x 24.4 μm for the FP defects, respectively. These distributions are not always in accord with the pattern distributions of Fig. 2. This is because Fig. 2 gives a macroscopic view and Fig. 4 is created by counting densities in limited small areas. As seen in Fig. 3 (b), the FP defects are located along growth striations and the SEP defects distribute uniformly. In Fig. 3 (c), both SEP and FP defects are observed randomly. From Figs. 4 (a) and (b), it can be understood that as the crystal diameter increases, the SEP defects decrease and the FP defects increase.

Figure 5 shows a WLT distribution corresponding to Figs. 2 (a), (b) and (c) on the as polished surfaces. The SEP defect regions in Figs. 4 (a) and (b) have the lower WLT compared to the other region where is the lower density of the SEP. The values of the WLT in the mixed region of SEP and FP defects in Fig. 2 (b) do not show any reduction. This may be due to the lower densities of SEP defects. It is noted that the WLT in the periphery of the SEP defect regions in Figs. 2 (a) decreases clearly. This can be related to the peak densities indicated by p in Fig. 4 (a).

Along the so-called R-OSF band in Fig. 4 (c), several points with the low values of WLT are seen. They are probably related to nuclei of the R-OSF and they are generated as the results of interaction with the strong growth striations. In the area after the slow growth rate where is free of the strong growth striation no such contrast is seen.

The outer boundaries of the SEP defect regions in Figs. 1, 2 amd 4 coincide to the regions of the lowest WLT values in Fig. 5. These boundary regions probably became to the R-OSF bands when these wafers are annealed at 1100C, 1hr in wet oxygen.

The distributions of oxygen concentrations along the growth direction centerlines are shown in Fig. 6. Carbon concentrations ranged from 0.05 ~ 0.12 ppma for all wafers. Due to the slow rotation of the crucible, the oxygen content was not high even for the 200 mm case. For the small diameters, it was extremely low. An anomalous oxygen distribution was seen in the low growth rate region, and will be discussed elsewhere.

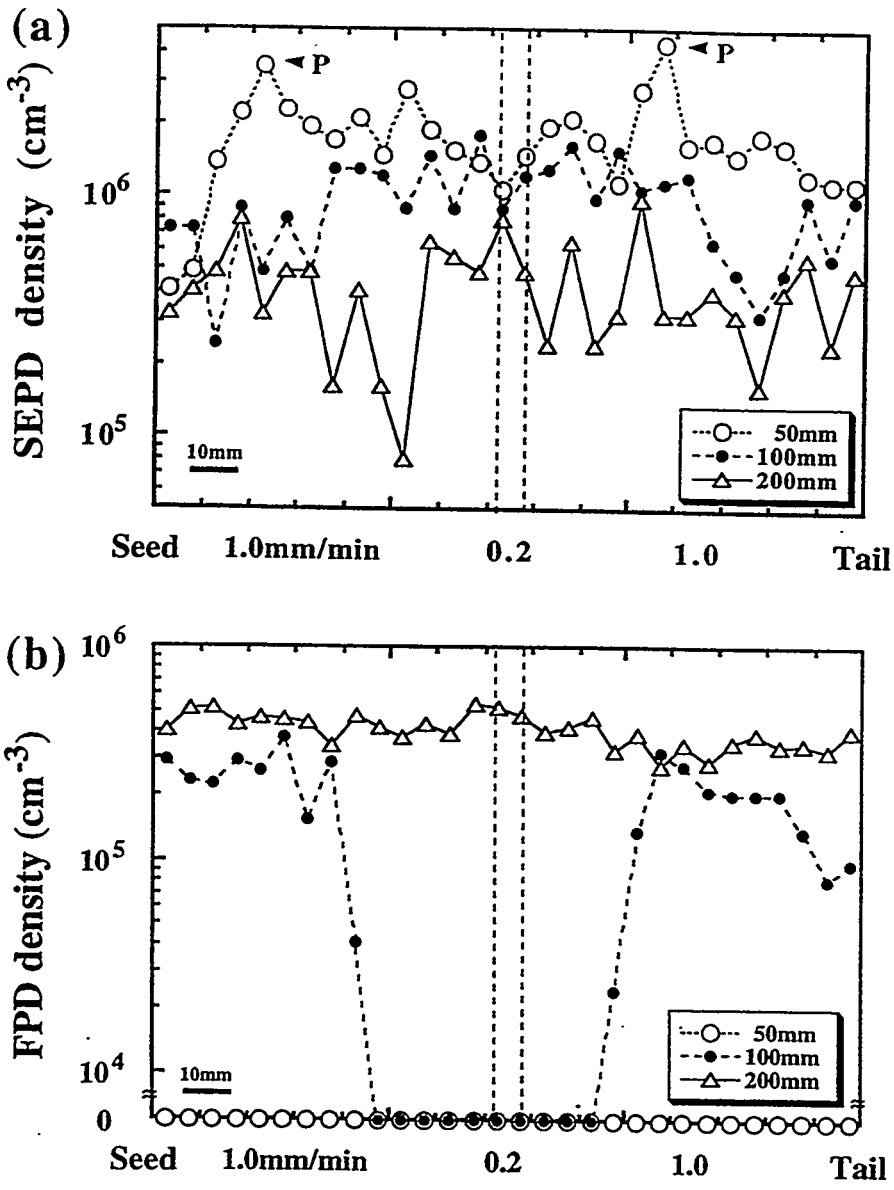

Fig. 4. Density distributions of the SEP (a) and FP (b) defects measured along growth direction on center line.

DISCUSSION

Habu et al [9,10,11] first formulated the behavior of secondary defects induced by intrinsic point defects such as the R-OSF [12] and the AOP [13] (anomalous oxygen precipitation) during CZ crystal growth. They postulated the main species of the intrinsic point defects at growth interface. However, from our experimental results [12,13,14,15], we have reported that there is no universal equilibrium concentration of intrinsic point defects during growth as far as the thermal gradient exists. The predominant point defects, whether excess silicon interstitials or vacancies at the growth interface are determined by the growth condition. This relation was first proposed by Voronkov [8] based on the experimental result obtained by Roksnouer et al. [16]. Recently, Dornberger et al [4] demonstrated that Voronkov's theory clearly agree with their experimental results. When $V/G > Ccrit = 1.3 \times 10^{-3}$ cm^2 min^{-1} K^{-1}, the FP defects generate. On the other hand, when $V/G < Ccrit$, large defects believed to

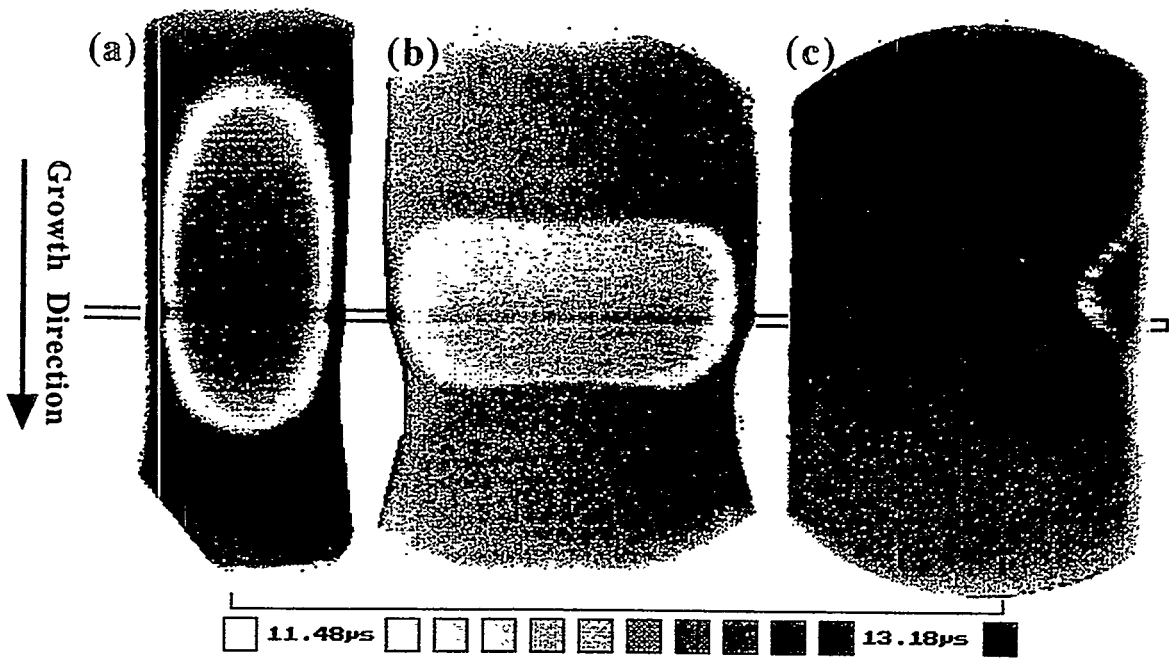

Fig. 5. Wafer lifetime maps. 50mm (a), 100mm (b) and 200mm wafers in diameter (c). Relative WLT values are represented by different levels of darkness.

be SEP appear. (V is the growth rate and G is the thermal gradient at growth interface.) However, the V / G relationships only explain that higher growth rate is necessary to compensate for larger thermal gradients and the thermal gradients in large diameter crystals are small compared to the smaller sized crystals.

They did not measure the actual thermal gradients of the growing crystal but employed the theoretical calculation values simulated using the commercially available finite element code FEMAG which include the effects of the shapes of growth furnaces and crystal diameters. The effect of growth rate on thermal gradient was ignored. The higher growth rate on the same diameter introduces the smaller thermal gradient as shown in our experimental results in the FZ crystal growth. The thermal gradient should be a reverse function of the growth rate.

Moreover, if the Voronkov's relation is kept even when the growth rate is zero, excess interstitials should be generated independently of the thermal gradient. However, when a crystal is heated with uniform temperature distribution, the vacancy rich crystal will be realized. It can be said that vacancy is predominant in equilibrium state of silicon in terms of the thermal gradient (when G = 0). On the other hand, heating with a strong thermal gradient brings about excess interstitials as shown in the experimental results by Roksnoeur et al. [16]. They demonstrated that the D defect region changes into the A defect region by *in situ* annealing after growth.

We have proposed that the principal parameter determining whether excess silicon interstitials or excess vacancies is only the thermal gradient G based on results using FZ crystals [14]. In this paper based on CZ crystals, it is again proposed that growth rate is not a controlling parameter.

In these experiments, the growth conditions such as the crystal puller configuration, the initial melt level and especially the growth rate are the same for the 6 crystals of diameters from 50 to 200 mm in diameter. Nevertheless, the FP defects do not generate in the 50 mm crystal at the growth rate of 1.0 mm / min. When the growth rate is reduced to 0.2 mm / min, as seen in Figs. 1 (a), 2 (a), and 4 (a), a high density of SEP appear not only in the low growth region, but also in the sections before and after this part. Such extraordinary effects have been previously reported for FZ crystals [14,15], the fundamental reason for this phenomenon is not fully understood, but we have proposed that the high thermal gradient

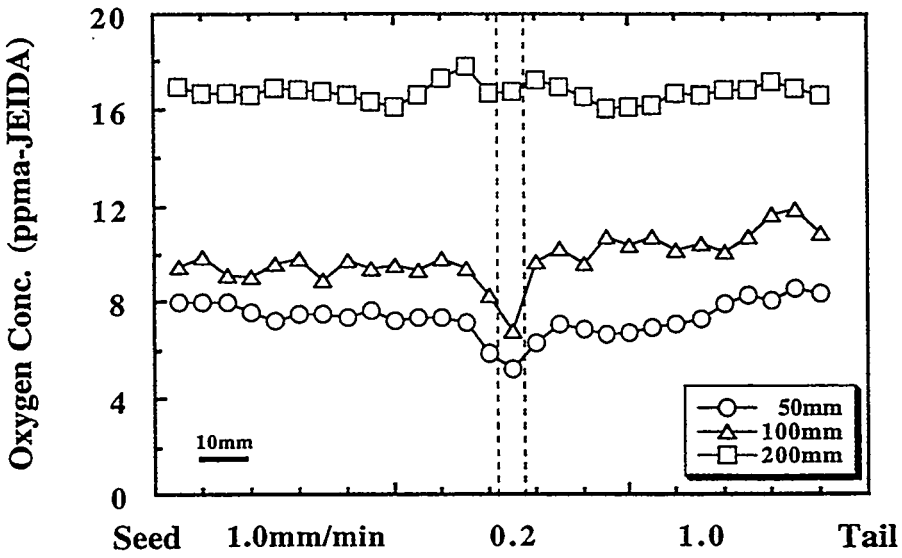

Fig. 6. Oxygen concentration distributions along growth direction.

effect extends to the region of the material already grown and continues after the growth rate is restored.

In the 75 and 100 mm crystals grown at 1.0 mm / min, FP defects spread across the whole area except the periphery. However in the low growth section (0.2 mm / min, 30 min) and adjacent areas the FP defects disappear. On the contrary, SEP defects emerge. This fact is exactly the same phenomenon [15] which one of the authors has reported in FZ crystals. There the D defect region changes into an A defect region by stopping the growth of a 40 mm diameter crystal for 2 min. Therefore, it is reasonable to conclude that the origin of the SEP defects is the same as that of the A defects and the origin of the FP defects is the same as that of the D defects in FZ crystals.

For the CZ crystals greater than 125 mm in diameter, the effect of the low growth rate does not show so clearly the replacing of FP defects with SEP defects. This indicates that in the larger crystals, the thermal gradient is relatively small and the heat capacity is large enough to minimize the effect of the low growth rate. However, from the previous discussions, the parameter controlling whether excess interstitials or vacancies is predominant at the growth interfaces is the thermal gradient and not the growth rate. Different lattice strains are induced which allow for excess silicon interstitials or vacancies.

Using the same growth conditions for different diameter crystal brings about differences in melt convection and evaporation of oxygen from the melt. Hence, the oxygen concentration varied widely. However, the behavior of the SEP and FP defects is consistent and independent of the oxygen concentration. Therefore, it appears that the interaction between intrinsic point defects themselves is dominant, rather than the interaction between the intrinsic point defects and oxygen atoms. In the larger crystals, both the SEP and FP defects are mixed in the same regions. There are two possibilities to explain the intrinsic point defect interaction. One is the idea that the interaction between the same kind of defect (interstitials or vacancies) is stronger than the interaction between interstitials and vacancies. (If vacancies interacts with interstitials they are annihilated as they combine.) The second explanation is that the reaction temperatures are different. For instance, the reaction temperature for excess self interstitials may be higher than that for excess vacancies ; possibly over 1200 C for excess interstitials and under 1200 C for excess vacancies as previously reported for FZ crystals [15].

Previously, it has been noted that the FP defect density has a direct relationship with GOI [6]. So crystals having a lower density of FP have been required. These were created by using an after-heater during the crystal growth process.

However, as the density of FP defects decrease, their size increases. A solution which

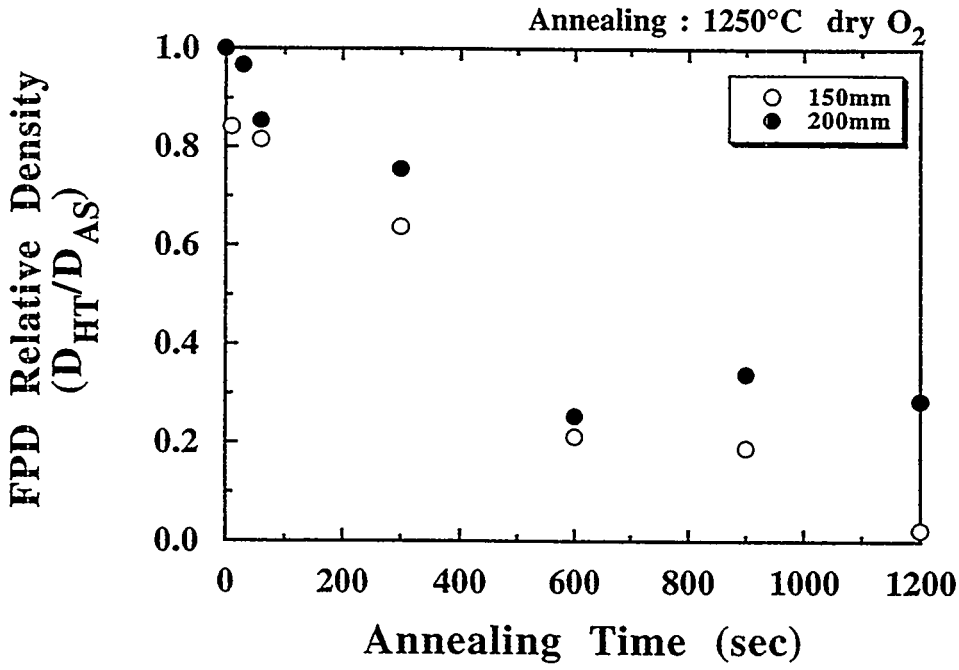

Fig. 7. Annihilation rate of the FP defects normalized with densities in as-grown state on different crystal diameter.

provides a smaller density of larger and more stable defects is not desirable for future device characteristics. Figure 7 shows the results of an annihilation experiment on FP defects using a RTA. The FP defects annihilate quickly when the specimens are thin, as in a wafer. The annealing temperature used was 1250 C in an ambient of dry oxygen. The process was ramped up and down from and to room temperature in 20 sec. Two crystals were examined : one was 150 mm in diameter with a relatively high growth rate of 1.18 mm / min and the other was 200 mm grown at 0.8 mm / min. It can be seen that the FP defects of higher density disappear faster than those of lower density. This may be due to the defects being of a bigger size.

In the future, for crystals of 300 mm and larger, the sizes of FP and SEP defects are expected to be large. In order to prevent these defects, the authors propose that as fast a growth rate as possible be used even though there would be an increase in the density of the FP defects.

CONCLUSION

When crystals of different diameters are grown from the same growth condition at both high and low growth rates, the SEP defects are generate in the low growth region and the regions adjacent to it in the smaller crystals. In the rest of the high growth regions FP defects appear except near the periphery. For larger crystals, the effect of the low growth rate is small but still exists in the periphery. Both types of defects appear together. From the analogy with FZ crystals, the SEP defects relate to excess silicon interstitials similar to the A defects, and the FP defects are associated with excess vacancies as are the D defects in FZ material. The oxygen in CZ crystals does not significantly disturb the formation of either defect. Finally, it may be concluded that the essential parameter determining the species of intrinsic point defects at the growth interface is not the growth rate, but the thermal gradient. From the viewpoint of perfect crystals, the properties of FP defects are understood to some extent. However, the SEP defects may be more harmful to devices of the future and more fundamental analysis is needed on them.

ACKNOWLEDGEMENT

The authors deeply thank Y. Yamagishi group (SEH R&D) for growing crystals, Y. Nakazato group (Nagano Denshi) for wafering process and S. Ushio group (SEH R&D) for x - ray topographs and IR measurements.

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ORIGINS AND REDUCTION OF DISLOCATIONS IN SEMICONDUCTING CRYSTALS

S. Mahajan

Department of Materials Science and Engineering

Carnegie Mellon University

Pittsburgh, PA 15213-3890

ABSTRACT

The supersaturation of point defects occurs in the melt-grown crystals during the cool down. To reduce the supersaturation, the point defects cluster together to form embryonic dislocation sources. In the presence of thermal gradient-induced stresses, these dislocations multiply. Thus, the perfection of the crystal is impaired.

Two approaches have been used to reduce the density of dislocations. First, by binding the point defects with some impurities so that they cannot cluster together to form dislocation sources. Both electronic and size interactions between the point defects and the impurities may be important for this purpose. Second, to strengthen the crystals by the addition of suitable impurities so that the probability of thermal gradient-induced slip is reduced. Examples of the two approaches will be presented.

1. INTRODUCTION

That dislocations have deleterious effects on the performance and reliability of the minority carrier devices, such as solar cells, light emitters, photoelectrons, etc., is well documented. Ishida and Kamejima (1979) have shown that dark line defects observed in the degraded regions of GaAlAs/GaAs double heterostructure laser diodes originate from existing dislocations. Dutt et al. (1981) have demonstrated that dislocations and stacking faults in GaAlAs layers, grown on poorly prepared GaAs surfaces, have a marked effect o the performance of light emitting devices.

Meier et al. (1985) have examined in influence of dislocations on the minority carrier diffusion length and the efficiency of silicon solar cells. They have seen that the increase in the density of dislocations lowers the minority carrier diffusion length. This decrease is in turn reflected in the reduced efficiency of the solar cells.

Beam et al. (1990) have shown that during homoepitaxy all the substrate dislocations intersecting the surface are replicated into an epitaxial layer. This observation implies that substrates having low dislocation densities are essential for the growth of high quality epitaxial layers.

It is clear from the above discussion that substrates with low dislocation density are required for reliable minority carrier devices. To achieve this objective, an understanding of the origins of dislocations in as-grown crystals is essential. Then, some schemes must be designed to reduce the density of dislocations. These topics are briefly covered in the present paper.

2. ORIGINS OF DISLOCATIONS IN CRYSTALS GROWN FROM THE MELT

The introduction of dislocations during the seeded growth from the melt could result from three different sources. First, dislocations present in seed crystals could propagate into a growing crystals. Second, the supersaturation of point defects could occur during cool down. This supersaturation could be reduced by the clustering of point defects into dislocation loops. Third, dislocation loops in the growing crystal could multiply under the influence of thermal gradient-induced stresses. Since it is possible to grow using dislocated seeds crystals having high perfection, the seed quality does not appear to influence the quality of as-grown crystals (Mahajan et al. 1981). In addition, the incorporation of a necking procedure during growth can also reduce the effects of the seed quality.

During growth, the non-equilibrium concentrations of point defects are incorporated into the crystals. The free energies of the crystals, crystallizing in the diamond cubic and zinc-blende structures, can be lowered if the excess point defects cluster into embryonic faulted loops on {111} planes. These loops grow by the absorption of either interstitials or vacancies. When the loops each a critical size, they undergo unfaulting, resulting in perfect dislocation loops. Such loops have been seen in float zone silicon crystals (Föll and Kolbesen 1975, Petroff and de Kock 1975, 1976).

The nucleation of the faulted loops occurs preferentially on dopant atoms and their clusters because of the strain energy considerations.

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Therefore, the distribution of the loops would tend to follow that of the dopant atoms, i.e., impurity striations. This effect is illustrated in Fig. 1 that shows the distribution of loops in a longitudinal section of a dislocation-free float zone silicon crystal as revealed by x-ray topography (de Kock 1980).

Fig. 1. X-ray topograph of a longitudinal section of a dislocation-free float zone silicon crystal revealing lithium-decorated A swirl defects.

To form faulted loops, two {111} layers of either interstitials or vacancies must be added to the crystal. The situation is a bit more complicated in the case of the III-V crystals. In this case, one of the layers contains group III defect species, whereas group V defect species reside in the second layer.

If thermal gradient-induced stresses are low, the critical resolved shear stress of the crystal may not be exceeded during the cool down. Its ramification is that the crystal will only contain dislocation loops discussed above. As a result, it will be of high quality and will be macroscopically dislocation-free. However, if the critical resolved shear stress is exceeded, then the loops can act as dislocation sources, multiplication occurs by glide

and the dislocation density increases. Since slip occurs on {111} planes of the diamond cubic and zinc-blende structures, the etch pits due glide-induced dislocations are aligned along specific crystallographic directions on a given plane. This effect is illustrated in Fig. 2 that shows the alignment of etch pits along the [110] direction of a (001) InP wafer that is highly dislocated (Mahajan 1989).

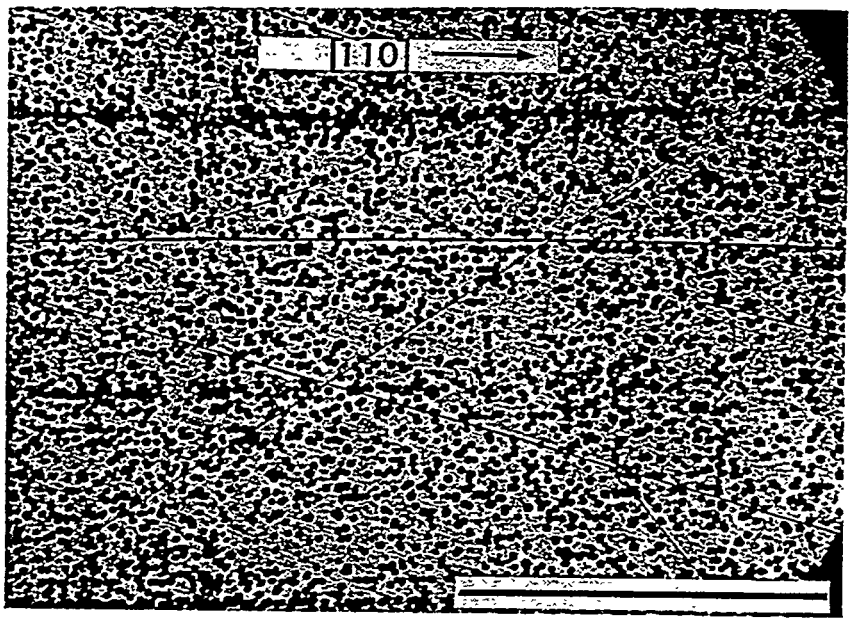

Fig. 2. Typical dislocation etch pit distribution observed on a (001) slice of highly dislocated S-doped InP wafer. Marker represents 0.1mm.

The thermal gradient-induced stresses are the major source of dislocations in II-VI and III-V crystals because they are softer materials. This is elegantly demonstrated in the study of Jordan et al. (1980). In Fig. 3 (left), a photomicrograph obtained from a {001} tellurium-doped GaAs wafer is shown. The key features of the observed dislocation distribution are: (i) its

four fold symmetry, (ii) maximum density at the <100> edges, (iii) minimum density midway between the center and <110> edge, and (iv) intermediate densities at the center and the <110> edges. Jordan et al. (1980) have rationalized the results of Fig. 3 (left) in terms of slip caused by thermal gradient induced stresses. The computed dislocation density contour lines are shown in Fig. 3 (right). It is remarkable that their analysis can predict the salient features of the observed dislocation distribution.

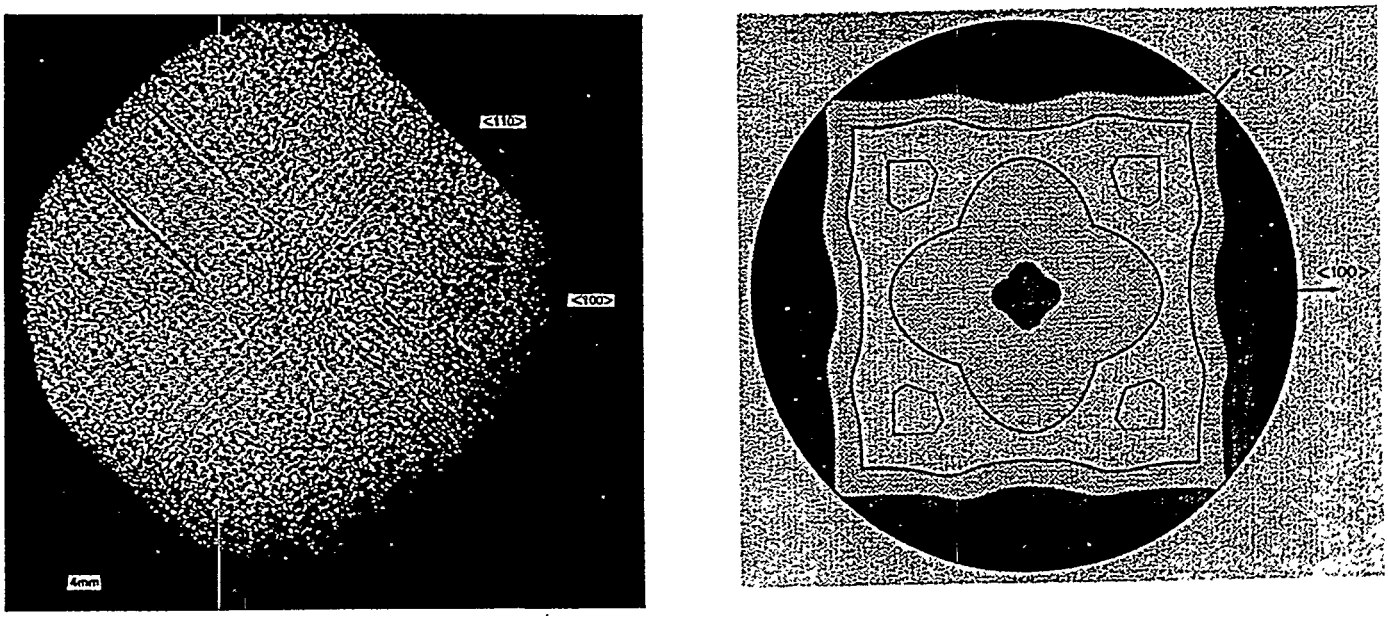

Fig. 3. (left) Photomacrograph obtained from a KOH etched {100} GaAs wafer. The crystal was cut close to the top end of a Te-doped boule grown by the liquid encapsulated Czochralski technique. (right) Constant dislocation density contour lines for the top wafer were obtained from a boule grown along the <100> direction.

3. REDUCTION OF DISLOCATION DENSITIES

Two approaches have been used to produce crystals with lower dislocation densities. In one of the schemes, point defects are prevented from clustering by binding them with suitable impurities so that embryonic dislocation sources do not form. In the second approach, crystals are strengthened by the addition of suitable impurities. This reduces the probability of thermal gradient-induced slip.

de Kock et al. (1979) have investigated the influence of different dopants on the formation of microdefects, i.e., embryonic dislocation sources, in macroscopically dislocation-free Czocharalski silicon crystals. The density of the microdefects is reduced for certain dopants. These results can only be understood if it is invoked that there is binding between the point defects and the dopant atoms. The interaction appears to be electronic in nature and does not depend on the size of the dopant atom.

The efficacy of zinc in reducing the dislocation density in InP crystals is considerably higher than that in the case of GaAs. Tucker and Hooper (1975) have suggested that the zinc atoms form complexes with the vacancies and thus prevent them from clustering into microdefects. On the other hand, the complexes may not develop in GaAs, leading to diclocation sources that can multiply under the influence of thermal gradient-induced stresses. It can also be argued that the above results cannot be explained on the basis of the size differentials between the dopant and host lattice atoms.

The above results imply that point defect-dopant interactions are electronic in nature. Therefore, to select suitable impurities for controlling the dislocation density, information on the electronic properties of the point defects in the host lattice is important.

A number of workers have shown that the perfection of InP crystals, grown by the liquid encapsulated Czochralski technique can be substantially improved by heavy doping (Seki et al. 1976, 1978 and Cockayne et al. 1983). High doping could affect the density of dislocations in two ways. First as discussed previously, the impurities could interact with the point defects and thus present them from clustering into potential dislocation sources. Second, hardening of the lattice by the impurities reduces the probability of introducing dislocations by thermal-gradient-induced stresses. Ehrenreich and Hirth (1985) visualize that when some of the Ga atoms on the group III sublattice in GaAs are replaced by In, five-atom $InAs_4$ tetrahedral units are produced within the matrix. The volume of the $InAs_4$ unit is larger than that of the $GaAs_4$ unit because the In-As bond is longer than the Ga-As bond. The strain field associated with the $InAs_4$ unit interacts strongly with glide dislocations, leading to strengthening of the GaAs lattice by the addition of In. Ehrenreich and Hirth believe that this solid solution strengthening is responsible for the reduction of dislocation density observed in LEC grown In-substituted GaAs. Extending the Ehrenreich-Hirth approach to S- and Te-doped InP and neglecting the charge transfer-induced size effects, it can be argued that Te should be more potent than S in reducing the dislocation

density. This assessment is not borne out by the experimental observations (Seki et al. 1976, 1978). It is reckoned that in the case of the isoelectronic impurities, the size differentials between the impurities and the host lattice atoms may be responsible for reducing the dislocation density, whereas the point defect-impurity interactions along with the size effects could improve the crystal perfection in the case of electrically active impurities.

In summary there are two sources for the introduction of dislocations in as-grown semiconductor crystals: (i) point defects, and (ii) thermal gradient-induced stresses. The influence of the stresses can be reduced substantially by the addition of suitable impurities to the crystals. These impurities either bind the point defects and prevent them from clustering into embryonic dislocation sources or strengthen the lattice by introducing strain centers in the host lattices.

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The Role of Dislocations and Associated Defects in Determining Minority Carrier Lifetime

Lionel C. Kimerling
Department of Materials Science and Engineering
Massachusetts Institute of Technology
Cambridge, MA 02139

The electrical activity of dislocations as recombination centers is manifested in three primary ways: 1) the intrinsic activity of imperfect bonds on the dislocation line; 2) the activity of point defect debris associated with dislocation glide; and 3) the activity of precipitates and impurity atmospheres in the vicinity of the dislocation line.

The intrinsic activity of imperfect dislocation bonds depends largely on the kink site density, because the dislocation core dissociates and reconstructs to minimize the density of dangling bonds. For typical silicon materials that have been plastically deformed, N_T (cm^{-3}) ~ 10^6 N_d (cm^{-2}), where N_T is the density of recombination centers and N_d is the dislocation density. Figure 1 shows the data that enable this conclusion.

The point defect debris are created by cross slip in concentrations that can be x10 higher than the intrinsic electrical activity. These defects disappear upon annealing at temperatures of 900C or higher. Figure 2 shows evidence of this behavior.

Precipitates act as short circuits in solar cells. Impurity atmospheres enhance the recombination velocity in the dislocation core region. However, dislocations getter metallic impurities from the bulk of the active region. Therefore, dislocations, like grain boundaries, can play a beneficial role when present in controlled numbers. One must engineer the spatial distribution in a way that minimizes the detrimental effect on open circuit voltage.

The energy level structure for intrinsic activity is shown in Figure 3, as observed by several measurement methods. The Fermi level is pinned to produce p-type conduction in heavily dislocated regions.

The accumulation of charge in the vicinity of the dislocation core induce band bending as shown in Figure 4. This band bending enhances the capture cross section for minority carriers. It also gives rise to an occupation dependent recombination rate. This, recombination proceeds at a slower rate at high injection levels.

The observations listed above have been reported for SiGe alloys and misfit dislocations produced by heterostructure growth. Hence, they are considered to be generic to dislocations in silicon materials systems.

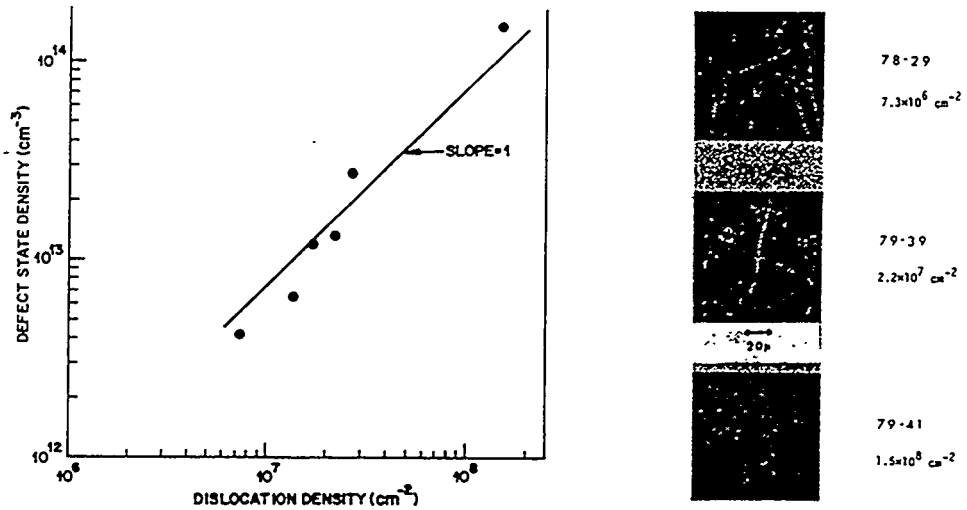

Figure 1 - Defect state concentration as a function of local dislocation density under the Schottky barrier in samples. (EBIC micrographs of samples are also shown).

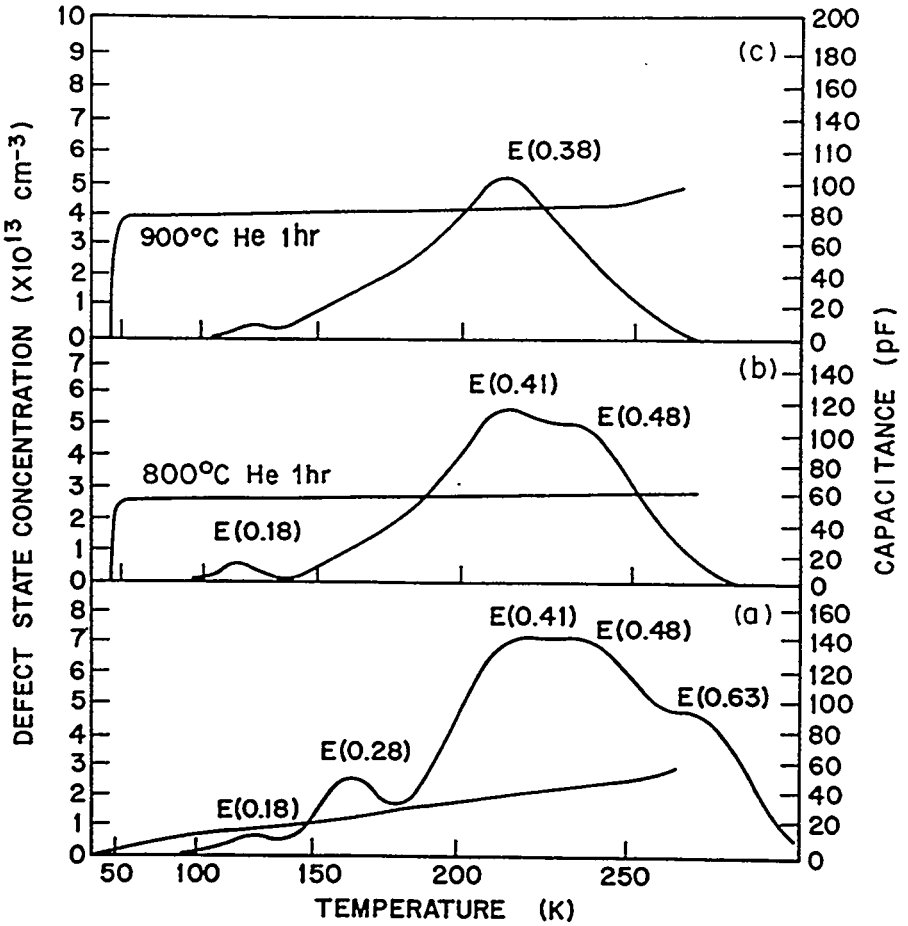

Fig. 2. (a) Defect spectrum produced by deformation at $T = 770°C$, $\epsilon = 5\%$; annealing at 700°C 1 hr caused little change in the original spectra after deformation. (b) and (c) Stability of the defect spectrum shown after annealing for 1 hr at temperatures shown. The smooth featureless line represents junction capacitance; F.Z. silicon, $n = 3 \times 10^{15}$ cm^{-3}, $\tau_t = 6$ ms.

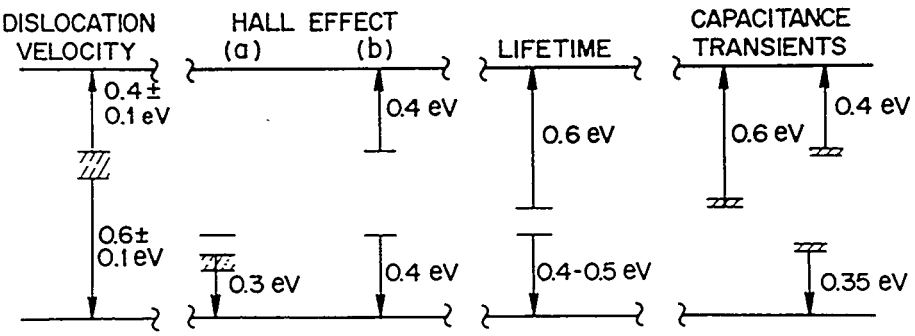

Fig. 3 . Schematic comparison of dislocation levels in silicon obtained from a variety of experimental determinations.

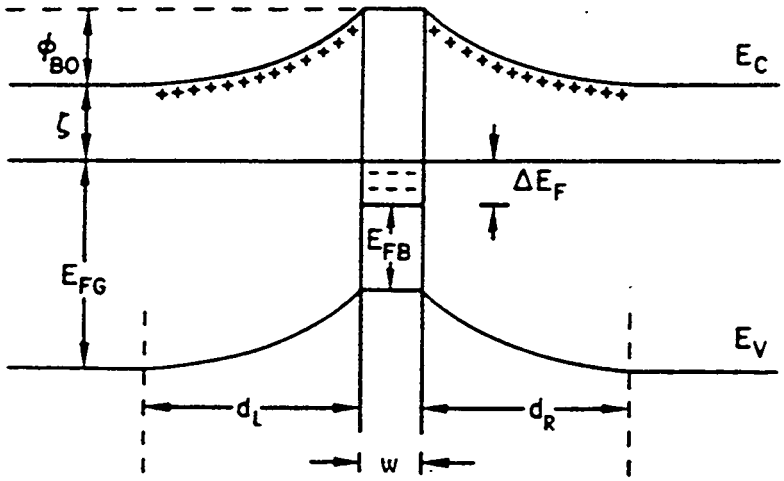

Fig. 4. Energy band diagram for two grains and boundary region. Value E_{FB} is the neutral Fermi level of the boundary before charge transfer from the grains. (From Seager

Transition metals and lifetime in PV silicon

A.A.Istratov, E.R.Weber.

Department of Materials Science and Mineral Engineering,
University of California at Berkeley,
577 Evans Hall, Berkeley CA 94720-1760, USA
e-mail: weber@socrates.berkeley.edu

Introduction.

One of the most important and critical parameters of photovoltaic (PV) silicon is the diffusion length (lifetime) of minority charge carriers. This parameter determines the effectiveness of solar cells and is significantly lower in PV silicon than in CZ and FZ silicon. In this paper, we discuss the role of precipitates and agglomerates of transition metals in the reduction of lifetime in PV silicon.

Transition metals form electrically active levels in the bandgap and can act as minority carrier recombination sites, decreasing the lifetime. CZ silicon manufacturers routinely use minority carrier diffusion length measurement (for example, SPV) as indication of the level of contamination by transition metals. The first studies of the effect of transition metals on solar cell efficiency made on CZ silicon, revealed that the critical contamination level, which leads to a substantial decrease in solar cell efficiency, is individual for each metal. The frequently cited results of Hopkins *et al*[1,2] are presented in Fig.1. It is interesting to note that, according to Ref.1,2, the most critical metals for CZ solar cell performance are Ti, V, Cr and Al, which have a deleterious effect in concentrations 10^{11}-10^{12} cm^{-3}. On the contrary, Fe, Co, Ni and Cu, which can be easily incorporated into the volume of the wafer during any heat treatment and are considered the chief metal contaminants in the semiconductor industry are (according to Ref.1,2) tolerable in CZ solar cells in concentrations up to 10^{14}-10^{16} cm^{-3}.

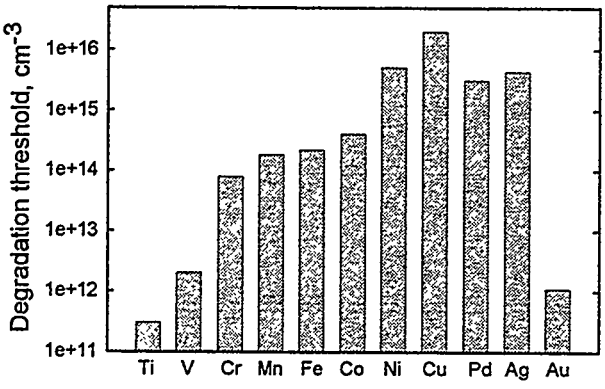

Fig.1. Threshold impurity concentrations for CZ solar cell performance reductions (after Hopkins and Rohatgi[2])

Numerous gettering techniques have been developed to decrease the concentration of metals in the critical areas of the wafer. They are based on creation of artificially formed precipitation sites (i.e., oxygen precipitates or dislocations) or regions with elevated solubility of impurities (backside aluminum layer) in non-critical areas of the wafer. The experiments, made on FZ and CZ material have shown that the diffusion length, drastically decreased after intentional iron contamination, could be restored by a gettering procedure (Fig.2, FZ,CZ). This means that the interstitially dissolved metals could be gettered almost completely. However, the same gettering procedure was found much less efficient on low-cost PV material (Fig.2, EFG).

Gettering by precipitation can be analyzed by measuring the precipitation rate, as demonstrated by Gilles[3,4]. The determination of the density of precipitation sites from iron precipitation kinetics is based on Ham's law[5,6], from which it follows that the precipitation rate is proportional to the density of precipitation sites. Using this approach for various silicon solar cell materials (including FZ, CZ, MCZ, EFG, SOPLIN)[7,8,9,10], it was revealed that the precipitation rate of iron was proportional to the as-grown minority

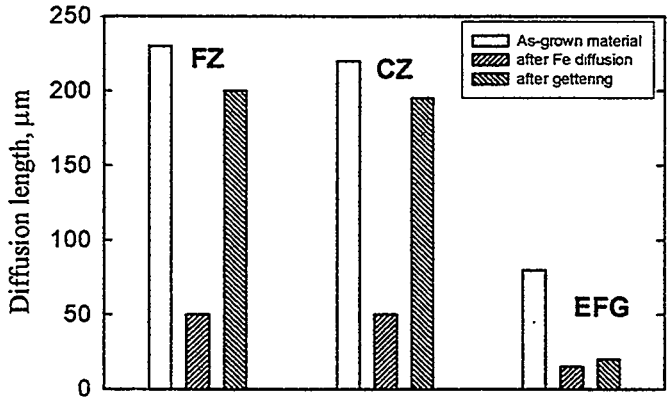

Fig.2. Dependence of minority carrier diffusion length in as-grown sample, after iron diffusion and after phosphorus-diffusion gettering for three types of material: float zone (FZ), Chochralski-grown (CZ) and edge-defined film-fed grown silicon for solar cells (Ref.8).

carrier lifetime and inversely proportional to the square of the diffusion length (Fig.3). In other words, in materials with low initial diffusion length iron precipitated very quickly, indicating that the materials with a low lifetime contained a higher concentration of precipitation sites[7,8,9,10].

Structural investigations of grains with low diffusion length revealed that they contained high densities of dislocations and intragranular defects. The nature of the latter type of defect is still being investigated. In a recent paper by M.Werner[11] several types of microdefects were reported. In particular, she reported spherical particles and planar defects lying in {111} planes. The size of the defects was below 100 nm. They might contain (or even consist of) precipitated transition metals. The last premise is confirmed by spatially resolved X-ray fluorescence data[12,11], which indicated that the grains of as-grown multicrystalline silicon with low initial diffusion lengths and high density of precipitation sites contained agglomerations of Fe, Cr and Co in significant concentrations (Cu concentration could not be measured since the sensitivity of the setup to copper was too low). Agglomerates of metals were found both on dislocations and in virtually dislocation-free regions[12].

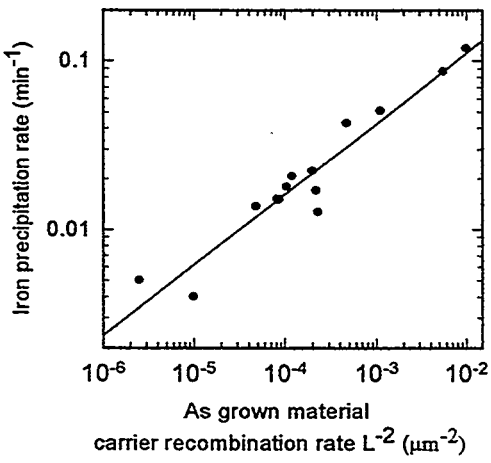

Fig.3. Dependence of iron precipitation rate on lifetime of minority charge carriers in as-grown semiconductor. The data were obtain on different types of materials: FZ, CZ, MCZ, EFG, SOPLIN.

It is clear that extended defects (including clusters of microdefects, dislocations and grain boundaries) are the main culprits of the low diffusion length in PV silicon. Most transition metals in the dissolved state do not represent significant trouble since they can easily be gettered. However, they readily precipitate on lattice defects. The decrease of the diffusion length due to contamination of extended defects was found to be at least 4 to 5 times higher than it would be just due to the presence of metals in the interstitial state[13]. Unfortunately, gettering becomes inefficient if the metals have precipitated on microdefects and dislocations[14]. One of the factors hindering effective gettering of precipitated metals is dissolution of precipitates. If the binding energy of metals to defects is high, they can not be dissolved within a reasonable amount of time at normal gettering temperatures. PV material can be improved either by finding better gettering treatments (which includes both

development of advanced temperature treatments and new methods to create gettering sinks), or by development of passivation techniques which can reduce the recombination activity of these clusters. This requires a good deal of knowledge of the properties of precipitated (agglomerated) transition metals. Whereas most 3d metals which can be quenched into the interstitial state are fairly well studied, the morphology of their precipitates and the nature of their recombination activity is generally rather poorly understood. This paper provides a review of the literature data reported on the structure and recombination activity of Cu, Ni, Co and Fe precipitates. The most recent experimental data, obtained by the authors, are presented as separate papers at this conference. It is shown that when these metals form small precipitates, they may have significant influence on minority carrier lifetime, even if their local concentration is about 10^{12}-10^{13} cm^{-3}, which is indeed much lower than the estimate of Ref.1,2 (Fig.1).

Properties and recombination activity of copper precipitates.

The process of Cu precipitation is determined by the cooling rate, amount of copper present and already existing defects. The effect of cooling rate was explored by several authors (see, for example, Ref. [15] and references therein). In the absence of other extended defects, for very slow cooling rates, copper outdiffuses from the bulk of the sample and creates surface defects. For the medium range (air cooling, 1 to 25 K/s), copper forms colonies of precipitates in the near surface regions[16,17,18]. For the fast cooling rate (quench, >100 K/s) it precipitates in the bulk[19,20].

Copper precipitate colonies can be detected by preferential etching of Cu-diffused wafers, which leads to the formation of large star-shaped etch pits in the regions, containing Cu precipitates[18]. Various TEM investigations (Refs.[18,21,22]) revealed that the size of precipitate colonies can range between 0.5 and 80 μm, and they protrude up to 40 μm into the bulk of a Si wafer. The colonies consist of small particles forming planar arrangements parallel to Si {110} and sometimes {001} planes. The colonies are usually bounded by edge-type dislocation loops. The diameter of the particles varies between about 7 nm (even values as low as 1 nm were reported[23]) in the vicinity of the dislocation loops and 20 nm for precipitates at least 50 nm away from the bounding dislocation. Copper-based colonies show high recombination activity - Correia *et al*[24] recorded EBIC contrast as high as 93% on a colony. The model of growth of planar precipitate colonies by a repeated nucleation process on climbing edge dislocations has been proposed by Nes *et al*[17,22,25] based on a mechanism described by Silcock *et al*[26].

Copper usually decorates extended defects. The precipitation of copper was reported along dislocations[27,28,29,30], on stacking faults[31,32,33,24,34,35], on punched-out dislocations around oxygen precipitates and oxygen-induced stacking faults[36,37,38,39,33], grain boundaries[40,23,21,41] or on implantation induced cavities[42,43,44,45]. If several kinds of extended defects are present in the sample, copper may decorate one of them preferentially, depending on the cooling rate. As shown by Shen *et al*[39,30,46], in slowly cooled samples, Cu develops precipitate colonies in the region away from Frank partials and does not decorate them even on an atomic scale. Cu colonies originate from punched-out dislocation loops although they are much lower in density and smaller in size than Frank partials. At the same time, a high density of Cu precipitates was observed on Frank partials when samples were cooled fast.

After fast quench, copper forms precipitates in the bulk of silicon in the form of thin platelets, lying mainly in the {111} planes. The size of the platelets depends on the cooling rate[19,47] and usually ranges between 20 and 600 nm. In all cases, the platelets are surrounded by strong deformation fields. The atomic structure of the precipitates is not clear. M.Seibt reported[19] that after fast quench copper forms copper-silicide islands, which are surrounded by thin extended defects, similar to stacking faults. The earliest stages of copper precipitation investigated so far are characterized by platelets with a thickness of only two or three lattice planes[48,65]. Larger and thicker precipitates, which were not surrounded by stacking faults, were reported in Ref. 47.

The equilibrium phase diagrams of the binary Cu-Si system show no silicon-rich silicides[49,50,51,52]. The structure and composition of Cu-Si particles is still being discussed. As the metal rich silicide Cu_3Si is in equilibrium with Si below the eutectic temperature of 850^{0}C (Ref. 51), it is commonly accepted that the chemical composition of copper silicide is Cu_3Si. This composition is supported by energy dispersive X-ray analysis, which showed that the particles consist of copper and silicon only and the copper content is larger than 72 at. % (Ref. 23). On the basis of electron-diffraction patterns the crystal structure of copper silicide was suggested to be b.c.c. β[53,23,47,22], f.c.c.[54], diamond cubic[54], η-Cu_3Si[27,38,55], or orthorhombic η"-Cu_3Si[18,56]. The last structure is the most commonly accepted.

It was suggested by El Kajbaji *et al*[47], that the important factor controlling the morphology of the precipitates is the stored elastic energy. The elastic stress originates from the difference in unit-cell volumes of the silicon lattice and Ci_3Si platelet. η"-Cu_3Si has a relatively large molecular volume (volume for one silicon atom) of 46 A^3 (compared to the molecular volume of silicon of 20 A^3)[57], which means that for every silicon atom consumed, approximately 1.3 silicon interstitials should be emitted. If the excess interstitials can be absorbed rapidly either by dislocations or at grain boundaries, the stress will be relaxed and the precipitates will be spherical. This is what is observed at relatively slow cooling rates, especially near the surface, at grain boundaries or along dislocations. If silicon interstitials cannot be absorbed, as in regions of perfect crystal, or if the cooling rate is too fast, or under conditions of overall excess of self-interstitials due to oxidation, the elastic stresses cannot relax and favor the growth of a platelet. The stress can partly be relaxed, forming dislocation loops and stacking faults around the precipitates.

The electrical activity of dislocations and boundaries, contaminated with copper, was studied in several papers[21,58,59,60,61,62]. As a rule, one peak appears in the DLTS spectrum of n-Si at a temperature of about 200 K[63,64,20]. A copper-related DLTS peak with similar temperature position was reported by Broniatowski *et al*[21,60] and by Hamet *et al*[61] for twinned boundaries. Hammet[61] reported that the width and position of the peak depended on annealing conditions and cooling rate. The broadening of the DLTS peak[21,58] and EBIC-results[59] indicated that there was not a single level but a set of closely spaced levels or a defect band due to copper. These results were supported by results of M.Grieβ[20], who established that the width of the DLTS peak depended on the diameter and structure of precipitates. This broadened peak seems to be the most important level due to precipitated copper in silicon. However, since the parameters of such broad peaks cannot be determined using the traditional Arrhenius plot, there is as yet no reliable data on the parameters of this defect.

The width of the peak becomes extremely wide after very fast quench[65]. Variations of the DLTS rate window and the filling pulse length showed that this was a single peak due to one extended defect, forming a band-like state in the upper half of the bandgap. The position of the defect band depended on the cooling rate. For the fast cooling rates (about 2000 K/s), the band was estimated to be approximately between E_c-0.15 eV and E_c-0.40 eV. In the case of more complicated thermal treatment, consisting of several steps, a complicated spectrum consisting of several peaks and a broad band between 90 K and 200 K was registered[61]. The last result shows that the copper-precipitate-related defect band, which can be formed by fast quench, may also appear after slow cool. This possibility also follows from the paper of Correia *et al.*[24]. He detected the formation of related platelets, lying in (111) planes with the diameter of about 12 nm after copper diffusion followed by slow cool. The structure of these platelets and the existence of strong electric fields indicate that they are similar to precipitates obtained after a fast quench.

The recombination activity of copper precipitates was shown to be significantly higher than that of interstitial copper[66]. The diffusion length, limited solely by interstitial copper in concentration of about 10^{15} cm^3 was estimated to be about 110 μm in p-type silicon. However, diffusion length was similarly limited by copper in concentrations of only 10^{12} cm^{-3}, if it formed platelets of the same size as after quench in 10% NaOH[66]. The low recombination activity of interstitial copper corresponds well with the expectation that the interstitial copper level should be close to the conduction band and that it should be a

shallow donor. Usually, one expects an active recombination center to be a deep level close to the mid-gap rather than a shallow level. Since copper-related extended defects form a band not far from the middle of the bandgap, they should provide an excellent recombination channel for minority carriers.

Properties and recombination activity of nickel precipitates.

As with copper, nickel can not be kept at interstitial sites at room temperature and precipitates during or immediately after the quench. For nickel, the silicide in equilibrium with silicon is $NiSi_2$ which has the cubic CaF_2 structure and can be visualized as an f.c.c. lattice with nickel atoms at the origin and silicon atoms at $\pm a/4[111]$. Since the lattice parameter of $NiSi_2$ differs from that of silicon by less than 0.4%, the volume change associated with nickel precipitation is small.

Fast quench of nickel diffused FZ silicon leads to the formation of platelets consisting of only two {111}-planes of $NiSi_2$. The diameter of these platelets varies between 20 nm and 0.9 μm depending on the quenching rate and the initial concentration of interstitial nickel[67]. The atomic structure of the precipitates was established from TEM measurements[67]. In agreement with a model proposed earlier[68] for $NiSi_2$-Si{111} Schottky barrier junctions, the precipitate-matrix interface was found to be built up by Si-Si bonds, leaving nickel in sevenfold coordination. The formation of $NiSi_2$ platelets involves a displacement of (a/4)<111> in the silicon lattice. This shift is compensated by a dislocation at the border of the particle[67].

The DLTS spectra of n-type silicon samples revealed a band-like state with the estimated position of the band between E_c-0.4 and E_c-0.6 eV[69]. Since the position of the defect band was even closer to the middle of the bandgap than that of Cu_3Si, one can expect from $NiSi_2$ precipitates a comparable (if not higher) recombination activity.

The recombination activity of $NiSi_2$ precipitates was studied experimentally by M.Kittler *et al*[70,71]. Nickel was diffused into FZ Si at 1050°C (which corresponds to the solubility of 5×10^{17} cm^{-3}, Ref.[72]). After quenching, the samples were annealed for 20 min in the range 500-800°C. After this treatment, hexagonal nickel-silicide platelets with diameter of about 250 nm and thickness about 15 nm were formed. Their density was about 10^9 cm^{-3}. The diffusion length depended slightly on the temperature of the ripening heat treatment and varied between 7.2 and 12.3 μm[70]. The precipitates showed large EBIC contrasts (about 40%), which were tentatively explained by existence of space-charge regions around the particles[71].

The recombination activity of interstitial and precipitated nickel cannot yet be compared because there are no experimental data on limitations in diffusion length due to interstitial nickel.

Properties and recombination activity of cobalt precipitates.

Cobalt is the lightest of the fast-diffusing 3d transition metals. Unintentional cobalt contamination is very rarely found in samples after processing. The solubility of cobalt is lower than that of copper and nickel and is close to the solubility of iron and manganese[72]. During cooling of the sample from high temperature, cobalt precipitates completely. Cobalt forms silicides which exhibit a decreasing metal content with increasing temperatures: CoSi between 375°C and 500°C and $CoSi_2$ at temperatures above 550°C[50]. The structure of $CoSi_2$ is similar to that of $NiSi_2$ (Ref.[73,74]). Similar to nickel, cobalt can be bound to cavities[75] and twin boundaries[76].

To the best of our knowledge, very little is known about the electrical activity of cobalt precipitates. This is primarily due to the relatively low solubility of cobalt and low density of cobalt precipitates after the quench. Because of the almost complete precipitation of cobalt, the correlation of the residual electrically-active defects to defined defect structures is questionable. Though several investigators reported deep levels due to cobalt[77,78,79,80,81,82], the nature of these levels is still uncertain.

Properties and recombination activity of iron precipitates

Interstitial iron forms, together with manganese and chromium, a group of moderately-fast diffusing transition metals. As a consequence, iron can be quenched at interstitial sites even after moderately fast cooling. After a short storage at room temperature, it forms electrically active complexes with shallow acceptors (B, Al, In). Iron precipitates during slow cooling of the sample from diffusion temperatures or during subsequent annealing performed at lower temperatures. For iron, the silicides in equilibrium with the silicon are α-$FeSi_2$ and β-$FeSi_2$ above and below 915^0C, respectively. Both modifications have been found experimentally[83,84]. Iron silicide is known[85] to have cubic structure with tetragonal symmetry for α-$FeSi_2$ and orthorhombic symmetry for β-$FeSi_2$. The volume of the unit cell of iron silicide is less than that of silicon and the precipitation of iron requires absorption of silicon self-interstitials (approximately 0.11 self-interstitials per precipitated iron atom[48]). Since iron and copper precipitation are associated with volume changes of opposite sign, co-precipitation should be effective for strain reduction[48].

The precipitation of iron on grain boundaries[86,87] and dislocations[88], leading to the increase of the recombination activity of these defects were reported. Unlike Cu and Ni, moderately diffusing iron requires slow cooling to precipitate at a grain boundary[87]. Iron precipitates easily on oxygen-related bulk stacking faults[89] and on Frank-type partial dislocations[90], significantly enhancing the EBIC contrast.

The recombination activity of precipitated iron was studied by Hieslmair et al[91]. It was shown that the lowest diffusion length was obtained after the diffusion of iron and quench, when iron forms FeB pairs. This value increased during precipitation and then slightly decreased again. The final diffusion length, obtained after precipitation, was 15 to 40% higher than in the beginning of the precipitation. The nature of the decrease of the diffusion length at the end of precipitation is still unclear. One of the possible explanations can be Ostwald ripening, occurring as the precipitation nears completion, which could eliminate many of the smaller precipitates, making larger precipitates more active. However, this still needs to be investigated. The initial (after quench and formation of FeB pairs) and final (after the precipitation is complete) diffusion lengths are close, demonstrating that iron is nearly equally dangerous to the lifetime in both the interstitial and precipitated states, which confirms the data reported earlier[92].

Discussion

PV silicon contains a significant density of grown-in dislocations and microdefects, which indeed provide efficient and stable sinks for transition metals. The enhancement of the recombination activity of grain boundaries and dislocations in silicon by precipitates of copper, iron and nickel is a well-known phenomenon. As-grown grain boundaries are often reported to be electrically inactive[93], which is confirmed by theoretical calculations[94,95,96] and TEM data[97], showing that most of the clean and reconstructed grain boundaries do not have energy states in the forbidden gap. The impurities precipitated at extended defects introduce deep levels[98] in the forbidden gap and act therefore as recombination centers[99] for minority carriers. Numerous EBIC data[100,101,41] confirmed the increase in recombination activity of boundaries and dislocations after Cu, Fe, Ni contamination. Besides recombination through well-defined deep levels, there might be enhanced recombination at metal decorated interfaces similar to surface recombination.

The other type of transition-metals-related defects, which may be deleterious to the performance of solar cells, are micro-precipitates of metals, formed in the bulk. Fundamental studies, performed on FZ silicon showed that micro-precipitates, forming a defect-related band in the bandgap, may substantially enhance the recombination activity of precipitated metals. Though the formation of micro-precipitates in FZ silicon usually requires fast quench, some experimental data (particularly obtained for copper) indicate that micro-precipitates may also appear in slowly cooled samples. The existence of dislocations, boundaries or lattice defects seems to favor their formation. It can be argued that, at least in the case of

copper, these extended defects provide effective sinks for silicon self-interstitials, formed during the growth of copper-silicide, thus decreasing the potential barrier for precipitation.

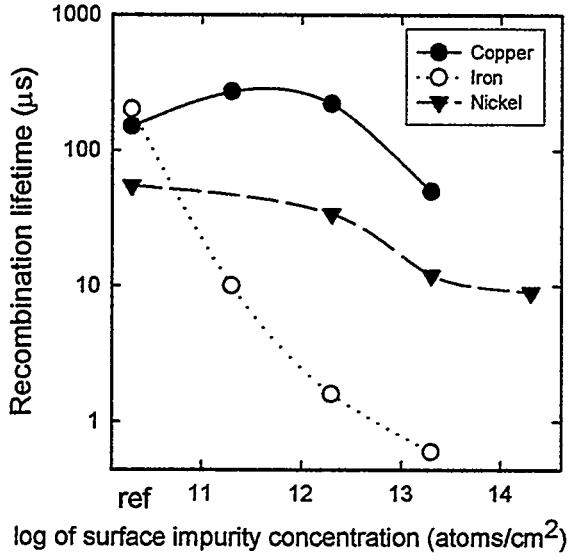

Fig.3. The dependence of recombination lifetime on contamination level (after Naito *et al*[102]).

The influence of contamination by transition metals on lifetime in PV, CZ and FZ silicon was investigated in numerous papers. Naito and Nakashizu[102] compared recombination lifetime of CZ samples after contamination of the samples by spin-coating method and following heat treatment (Fig.3). This figure clearly demonstrates that iron is the most dangerous impurity in the bulk of silicon. This is due to strong recombination activity of interstitial iron and FeB pairs[103] and is in line with the conclusion of R.Falster *et al*[104] that the FeB pair is the dominant recombination center in current p-type as-grown CZ material. High-quality CZ material does not offer enough precipitation sites for copper and, if contamination level and the degree of supersaturation are relatively low, copper remains dissolve interstitially or forms complexes with other impurities. Since the recombination activity of interstitial copper is very low, it influences the recombination lifetime only if contamination exceeds 10^{12} cm^{-2}, which is in a good agreement with our own estimates[66] and with the experimental data of M.Miyazaki[105].

The recombination activity of metal-silicide-precipitates, which are the main impurity type in PV silicon, is either comparable, or significantly higher than that of interstitial metals. For copper, it depends on the morphology of the precipitates. If the precipitates are small and form a wide defect band, their recombination activity can be one-two orders of magnitude higher than that of interstitial copper. For iron, the diffusion length after precipitation is slightly higher than before precipitation. For nickel, there is no experimental data for the recombination activity of the interstitial Ni and comparison of recombination on interstitial and precipitated nickel is not possible. However, since it also forms a defect-related band, one may assume that, as with copper, the recombination activity of nickel is enhanced by precipitation. Since the apparent amplitude of the defect-band-related DLTS signal is much lower than the real defect concentration, it can partly explain why it is difficult to measure by DLTS deep levels responsible for lifetime degradation in PV silicon.

Conclusions

The recombination activity of transition metals (especially Cu, Ni) may be substantially enhanced after formation of precipitates in the bulk or at the existing extended defects. In the case of Cu and Ni the formation of precipitates is followed by the formation of a defect-related band in the bandgap. The nature of this band is not completely understood. This band seems to be much more favorable to the recombination of minority charge carriers than the states of individual interstitial atoms. It was also argued[71] that electrostatic effects (attraction of minority charge carriers by space-charge region around the precipitates) may enhance recombination. Another recombination mechanism, suggested in this review, is the surface recombination at the interface between silicides and silicon. The understanding of the

morphology and electrical properties of precipitates of transition metals in silicon is of crucial importance to increase the efficiency of solar cells manufactured from cost-efficient PV material.

Acknowledgments

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Oxygen Precipitation in Polycrystalline Ingot and Ribbon Solar Silicon

H. J. Möller, Li Long, S. Riedel, M. Rinio, D. Yang
Institute for Experimental Physics, TU Bergakademie Freiberg, Silbermannstr. 1, 09599 Freiberg, Germany

M. Werner
Max-Plank Institute of Microstructure Physics, Weinberg 2, 06120 Halle, Germany

1. Introduction

Multicrystalline silicon grown by directional solidification and polycrystalline RGS silicon are low cost materials for photovoltaic applications. The properties of solar cells made from these materials are mainly determined by dislocations, grain boundaries and intragrain defects such as impurities, small clusters of atoms or precipitates. Because of the use of quartz and graphite parts in both processes oxygen and carbon are the main impurities but are introduced in different quantities. The concentrations are generally higher in ribbon material and are close to the solubility limits.

Oxygen is known to affect the conversion efficiency of solar cells. Both for Cz - and multicrystalline silicon an improvement of the solar cell performance as well as a degradation has been reported [1, 2]. Oxygen can form a variety of defects that affect the electrical behavior differently. Clusters of a few oxygen atoms and various sizes and crystal structures are observed for larger SiO_2 precipitates. Well known defects are the Thermal Donors which are clusters of a few oxygen atoms and the New Donors that have been connected with SiO_2 precipitates [3]. In addition, oxygen can precipitate at grain boundaries and dislocations and change their electrical behavior.

The defects can also have an impact on the diffusion length, the mechanical strength and on the properties of the pn - junction if they are large enough to penetrate the space charge region [4]. Furthermore, oxygen precipitates are efficient gettering sites and can reduce the efficiency of the phosphorous and / or aluminum gettering steps during solar cell processing. The evolution of the oxygen defects depends very much on the thermal history of the material and every thermal step between crystal growth and solar cell process has to be considered.

In this paper results are summarized that demonstrate the important role of oxygen - induced defects in multicrystalline ingot and RGS ribbon silicon. Furthermore, in a systematic study the oxygen precipitation in polycrystalline silicon is investigated under definite conditions. In addition, a numerical program has been developed that allows one to simulate the precipitation process and to determine the size and density distribution of the precipitates for any thermal treatment. The numerical results are compared with experimental investigations on mc - and RGS silicon that has been processed under various conditions. The aim of this approach is to predict the size and density of oxygen - induced defects for any sequence of thermal treatments that a material experiences.

2. Multicrystalline ingot silicon

2.1 Selective etching of microdefects

Microprecipitates can be detected in mono- and multicrystalline silicon by selective etching. Figure 1 shows a typical example where in addition to the large etch pits from dislocations shallow pits occur. Repeated etching after the removal of a thin surface layer shows that the defects are small precipitates. They occur both in as grown ingot silicon from various suppliers, in RGS ribbon silicon, and in CVD and LPE thin films deposited on multicrystalline silicon substrates [5]. The density of the shallow etch pits varies between 10^5 to 10^8 cm^{-2}. It has been found, however, that more microdefects become visible if the surfaces are chemomechanically polished with alkaline slurries before the etching step. We assume that both size and decoration of the precipitates during polishing determine if a shallow etch pit is formed.

The TEM investigations that shall be presented in the following chapters show that at least a part of the shallow etch pits are due to oxygen microprecipitates. This assumption is also supported by the fact that

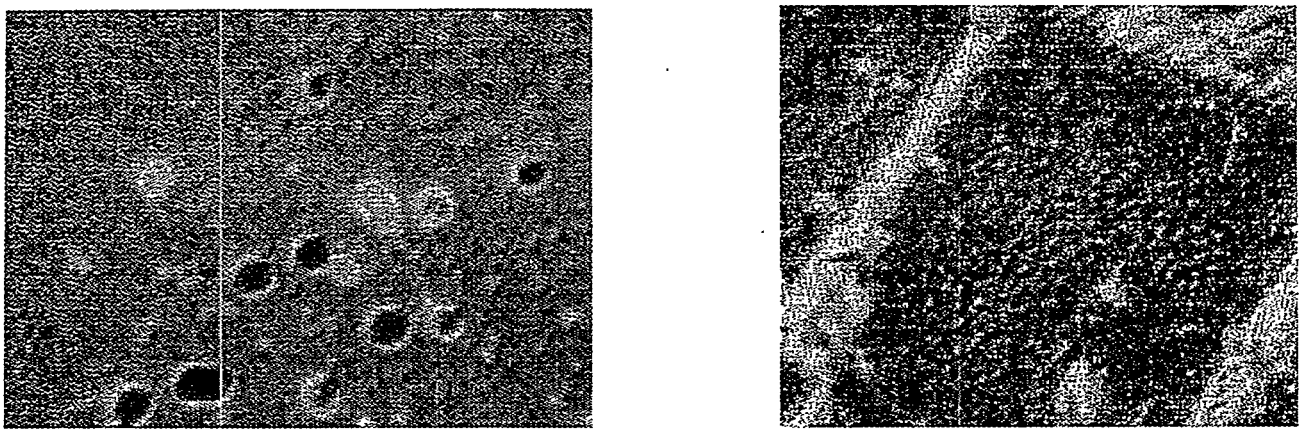
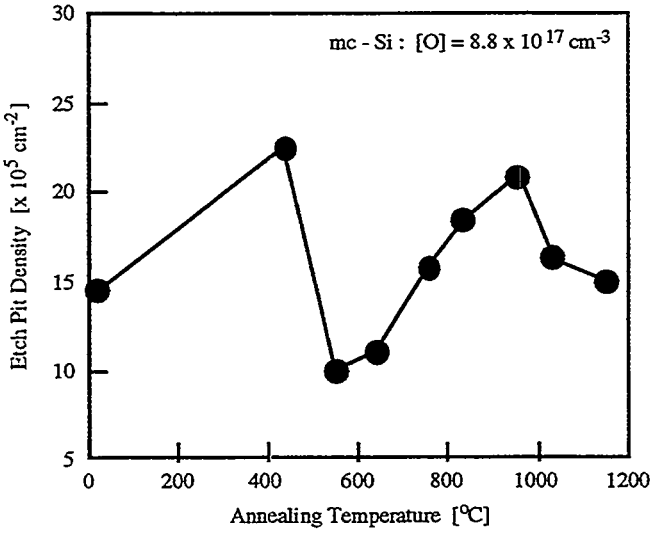


Figure 1 Shallow etch pits of microdefects in multicrystalline (left) and RGS ribbon silicon after chemomechanical polishing and selective etching. Large etch pits are dislocations. (1 cm ≡ 8 m).



the density of the etch pits increases after annealing particularly in the temperature range between 700 - 900°C when most of the oxygen precipitates as will be shown later (figure 2). The defects that are responsible for the second increase at lower temperatures has not been identified yet but may also be due to oxygen - related precipitates. So far it is not possible to determine the density of oxygen precipitates exactly from etch pit investigations but within an order of magnitude the results agree with the densities determined from TEM investigations (table 1).

Figure 2 Density of shallow etch pits as a function of the annealing temperature after precipitation of oxygen.

Table 1

Density of microdefects as determined by TEM and selective etching for as-grown and annealed specimens.

Sample	TEM defect density [cm^{-2}]	Etch pit density [cm^{-2}]
as-grown	3×10^6	6×10^6
as-grown	$< 10^4$	0
950°C	3×10^8	-
1050°C	1×10^6	2×10^6

2.2 Annealing experiments and FTIR results

The oxygen concentrations in multicrystalline silicon ingots vary between 1 - 20 ppma, in RGS ribbon silicon between 20 to 40 ppma which is close to the solubility limit. The tendency to precipitate is thus high particularly in the RGS material. During crystal growth and solar cell processing the material experiences several high temperature annealing treatments. The temperature regime around 800 - 1050 °C is particularly important for the diffusion of phosphorous to form the p-n junction. The oxygen concentrations are comparable to Cz - silicon where the oxygen precipitation has been thoroughly investigated [6]. Therefore the question arises whether oxygen in polycrystalline silicon shows a similar behavior.

The annealing behavior of oxygen was studied by FTIR spectroscopy in multicrystalline silicon specimens with various initial oxygen and low carbon concentrations (below the detection limit of 5×10^{15} cm^{-3}). The first results showed that the previous thermal history of the specimens had an influence on the annealing behavior. Therefore the specimens were preannealed at 1260 °C for 1 hour which turned out to be sufficient to eliminate any previously formed nucleation centers that are responsible for an enhanced precipitation of oxygen. The specimens were annealed then at different temperatures between 2 to 24 hours.

Some results are summarized in figure 3. The main result is that the interstitial oxygen concentration decreases between 750 - 1050 °C. The corresponding FTIR spectra confirm the formation of the SiO_2 phase. In addition, stacking faults are observed by etching at 1050 °C. Below the oxygen concentration of about 2×10^{17} cm^{-3} precipitation does not occur anymore.

The comparison of the results with Cz - silicon of the same oxygen concentration (and no carbon) shows essentially the same precipitation behavior after preannealing below 1050 °C. Therefore it appears that the presence of dislocations and grain boundaries in mc - silicon has no influence on the precipitation process below that temperature. However, the FTIR spectra also show that above 1050 °C the SiO_2 precipitate line at 1224 cm^{-1} disappears again. Above this temperature the oxygen diffuses fast enough to reach the dislocations which have a mean distance of 10 m. This indicates that oxygen prefers to precipitate at dislocations then which does not produce a signal in the FTIR spectrum. The TEM results for RGS silicon presented later confirm this.

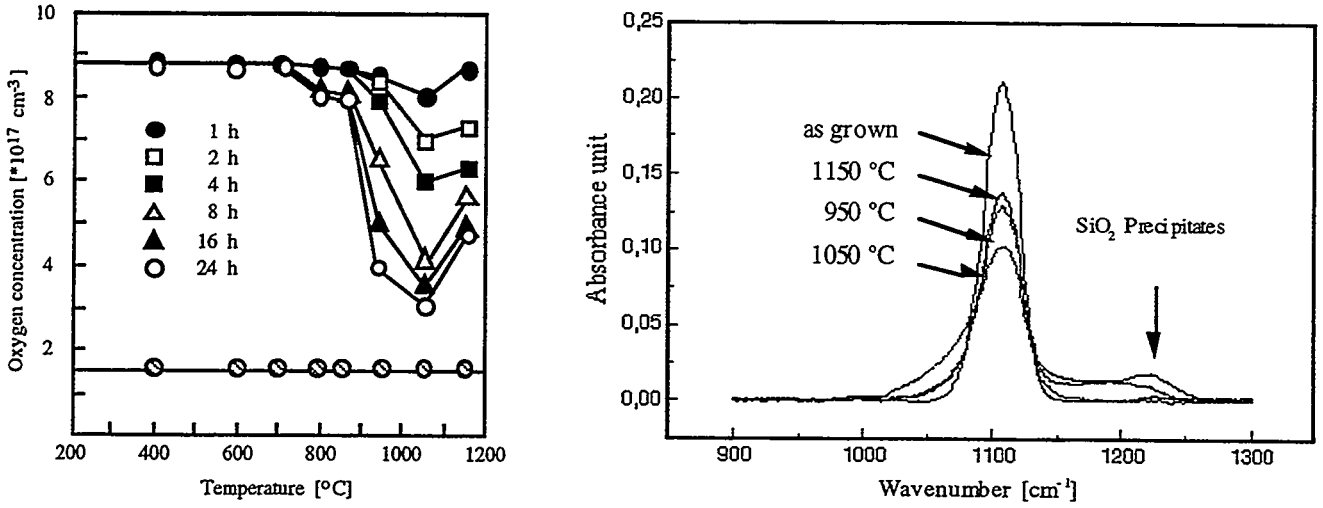


Figure 3 Concentration of interstitial oxygen in multicrystalline silicon after annealing at different temperatures (a, left). Specimens are pre-annealed at 1260°C for 1 hour. Corresponding FTIR absorbance spectrum showing the interstitial oxygen and SiO_2 precipitate lines (b).

2.3 TEM investigations

TEM investigations of the same specimens were performed to study the structure of the microprecipitates in the as-grown and annealed specimens. The following types of precipitates are observed : spherical (figure 4) and platelike defects (figure 5 and 6). Lattice images confirm the amorphous structure of the spherical defects that are typical for SiO_2 precipitates. For the platelike defects several different types occur : a single platelet on (111) planes (figure 5a) or several parallel plates connected to each other. In addition, HREM imaging shows (111) platelets with a thickness of one or two atomic layers. They contain an extra (111) lattice plane which suggests that they may be extrinsic stacking fault. The nature of the platelike defects in general is not clear. Whether they are platelike amorphous SiO_2 precipitates and / or extrinsic stacking faults could not be determined yet.

Both spherical and platelike defects occur already in the as-grown multicrystalline material. The densities increase however after annealing around 900°C. Above 1050°C only the platelike precipitates are observed. In the same temperature regime the 1224 cm^{-1} absorbance line in the FTIR spectra disappears. As discussed in the previous section we assume that most of the oxygen diffuses now to dislocations and precipitates there. Table 1 summarizes the results for the densities in as-grown and annealed specimens.

Since the TEM study has not been completed for all annealing conditions a comprehensive comparison with Cz - silicon is not yet possible. However, apart from the multi-platelet defects similar types of oxygen precipitates and oxygen related defects are also observed in annealed Cz - silicon.

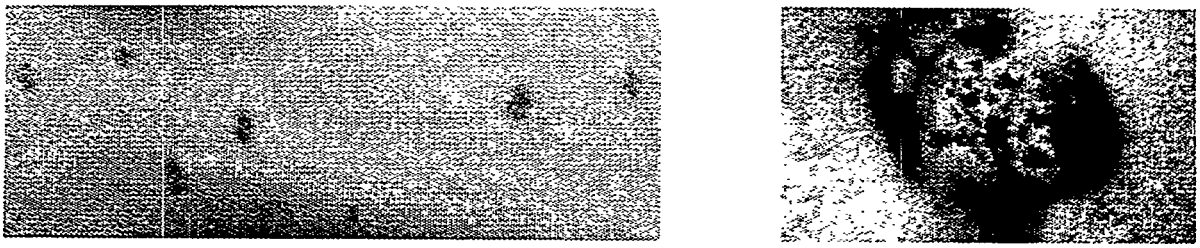


Figure 4 TEM micrograph of spherical precipitates that occur both in as-grown and annealed multicrystalline silicon (e.g. here at 950°C for 24 hours).

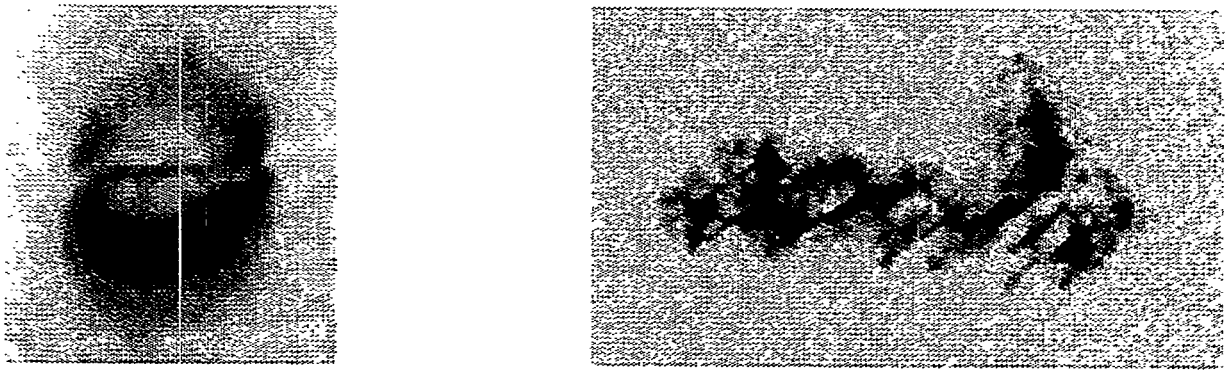


Figure 5 TEM micrograph of a platelike precipitate (left) and a multi-platelet defect.

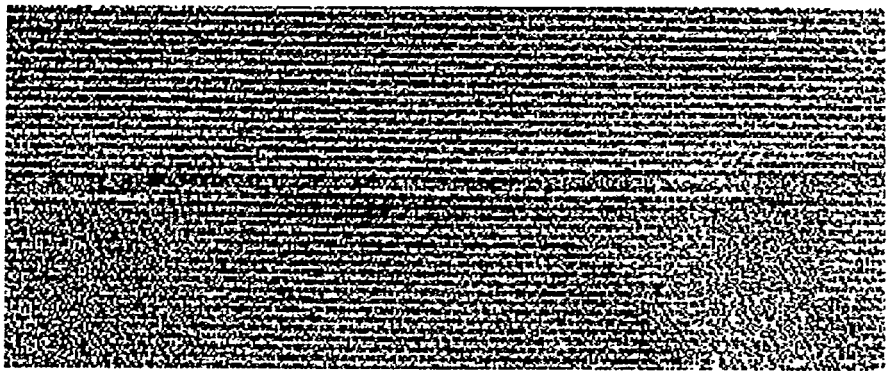


Figure 6 HREM micrograph of a thin platelike defect on a (111) plane. The defect consists of an extra (111) plane .

2.4 Decoration of dislocations

The FTIR and TEM results show that oxygen segregates or precipitates at dislocations if there is sufficient time for diffusion. One can assume however that even for shorter times or lower temperatures some of the oxygen in the vicinity will diffuse to the dislocations and decorate them. As a result dislocations may have different recombination behavior depending on the degree of decoration in different parts of the wafer.

Since a large number of dislocations has to be analyzed locally to investigate this hypothesis quantitatively we applied the LBIC method with a high spatial resolution. In regions of higher dislocation densities the short circuit current is mainly determined by the local recombination behavior of the dislocations. A typical example is shown figure 7 where the dislocation density varies over two decades. The dislocation density in the area under investigation was determined by etching and the etch pits automatically counted by an image processing system. Both the LBIC and optical image are correlated to each other with an accuracy of about 5 m.

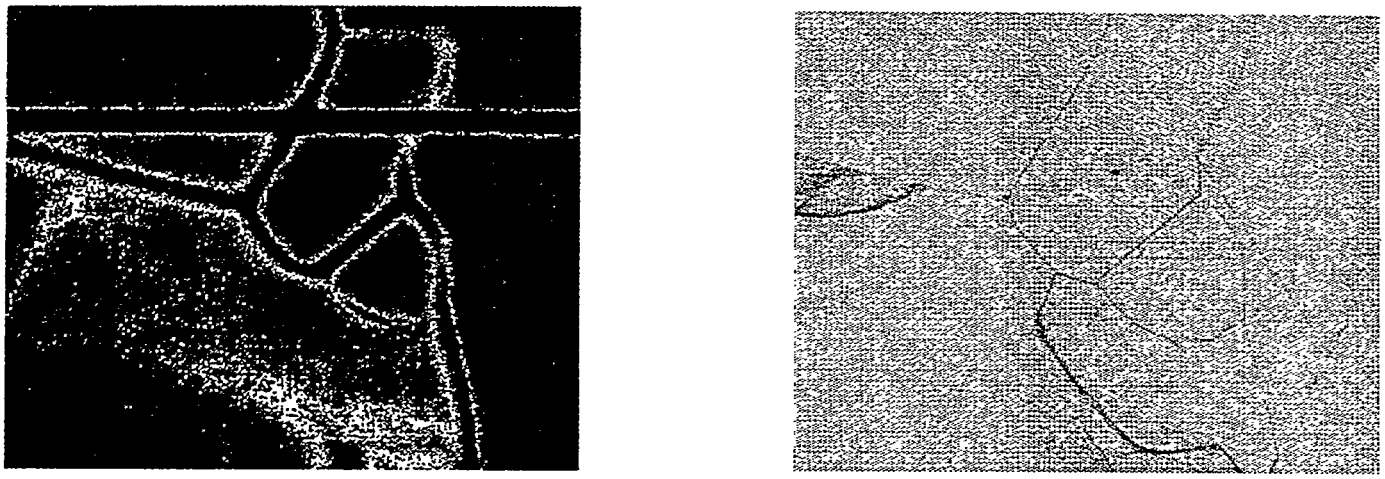


Figure 7 LBIC topogram of an area with varying dislocation density (left). The etched surface of the same area is shown on the right. The dislocations densities are determined by counting the etch pits (not visible here at this magnification) and are correlated with the local light beam induced current.

The results for two different areas are shown in figure 8 where the short circuit current is depicted as a function of the dislocation density. In both cases the current saturates below a dislocation density of about 10^5 cm^{-2} which indicates that for lower densities the dislocations are not the recombination limiting defects any more. For dislocation densities above about 5 x 10^6 cm^{-2} the etch pits begin to overlap which limits the accurate determination of the density.

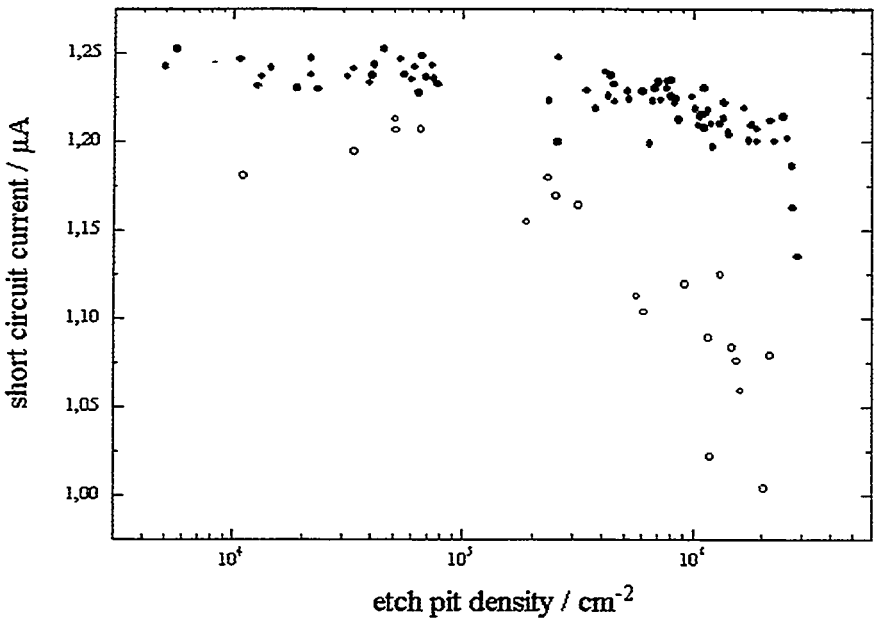


Figure 8 Short circuit current as a function of the dislocation density in two different regions of the same wafer.

The important result, however, is that the recombination behavior of the dislocations in both regions differs. We assume that this is due to a different degree of contamination. Since the TEM investigation of the dislocations in mc - silicon did not reveal any differences in the dislocation structure one must assume that only very small amounts of impurities are responsible. In view of the result that oxygen tends to segregate at dislocations particular at higher temperatures we assume that this element also plays a role here. Possibly metallic impurities have to be considered as well.

3. RGS ribbon silicon

Compared to polycrystalline ingot silicon RGS ribbons have a very different microstructure. The grain size varies between 200 - 500 µm and the dislocation density from 10^5 to 10^7 cm^{-2}. This is due to the faster solidification and a shorter growth time. The ribbons solidify within a few seconds. In addition, the impurity levels are generally higher, in particular the concentrations of oxygen and carbon are close to the solubility limits. Nonetheless, efficiencies of 10% have been reached recently with short circuit currents of 19 mA/cm^2 (without AR coating) that are comparable to multicrystalline solar cells. The main reason for the lower efficiencies is a reduced open circuit voltage which indicates loss mechanisms in the pn - junction of the solar cell. The investigations focused therefore on defects in the space charge region of fabricated solar cells.

3.1 LBIC investigations

LBIC topograms show a rather uniform distribution of the short circuit current in the entire cell. Due to the smaller grain sizes a high spatial resolution is required to identify areas of higher recombination. An example is shown in figure 8 where the enlarged area is measured with a lateral resolution of 6 µm. The comparison with the defect structure on the etched surface reveals that the dark areas mainly correspond to grain boundaries. This is in contrast to multicrystalline ingot silicon where areas of low recombination current are generally due to higher dislocation densities. Although under different processing conditions the distribution and number of recombination active grain boundaries can vary considerably they are generally more dominating compared to mc - ingot silicon.

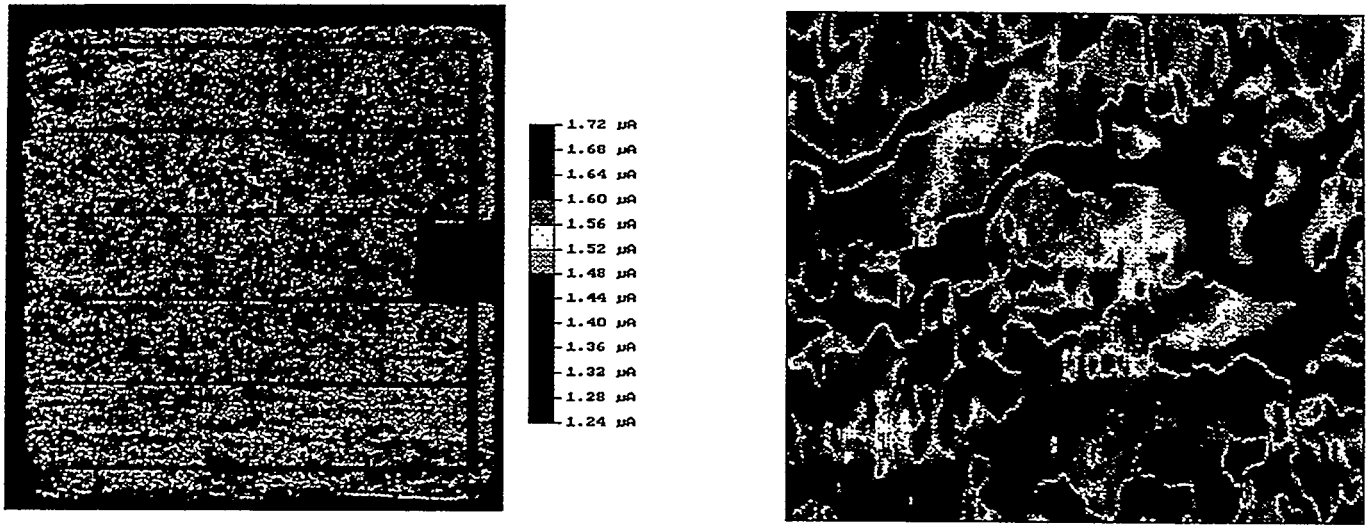


Figure 8 LBIC topogram of a 5 x 5 cm^2 RGS solar cell (left). An enlarged region measured with a spatial resolution of 6 m is shown on the right. Dark areas are regions of high recombination and low current and are caused by contaminated grain boundaries.

3.2 TEM investigations

The TEM investigations of the ribbon material show the following distribution of SiO_2 precipitates. In the bulk region spherical, amorphous precipitates are observed but no platelike defects as in ingot silicon. In addition SiC precipitates occur probably because of the high carbon concentrations in the material. The size of all defects varies between 20 - 50 nm and the typical densities of the bulk precipitates are between 10^{11} and 10^{12} cm^{-3} (see table 2). This also corresponds to the densities that are obtained from the etch pit investigations. In addition to the bulk defects precipitation also occurs at grain boundaries and dislocations. Typical examples are shown in figure 9. The strong recombination of grain boundaries as observed in the LBIC topograms is thus due to a heavy contamination with SiO_2 and SiC precipitates.

These extended defects also penetrate the space charge region of the solar cells. It is thus likely to assume that these defects are responsible for the lower open circuit voltage of RGS solar cells because they may provide a conducting path through the pn - junction. SiO_2 and SiC precipitates are, however, not necessarily conductive therefore we assume that a contamination with metallic impurities is also required. During the formation of the pn - junction metallic impurities are particularly gettered into the emitter and space charge region which may explain the activation of the extended defects in this area. Systematic variations of processing parameters seem to support this assumptions but a conclusive proof is still lacking.

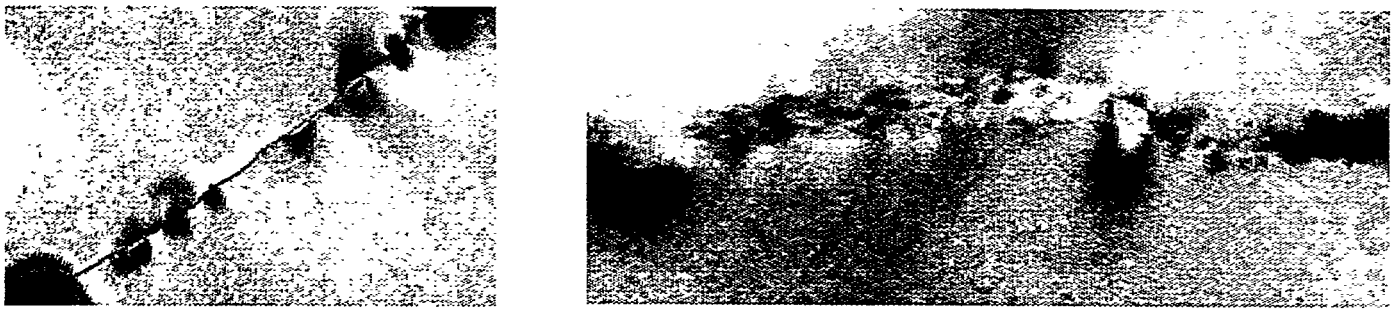


Figure 9 TEM images of SiO_2 and SiC precipitates at grain boundaries (left) and dislocations (right) in RGS ribbon solar cells.

4. Numerical simulation of the oxygen precipitation

The experimental results demonstrate that the distribution of oxygen and SiO_2 precipitates depends very much on the processing conditions. Because of the impact on the device performance it is desirable to know the modifications of oxygen which occur for a given sequence of thermal processes. In recent years much progress has been made in the theoretical description and numerical simulation of the oxygen precipitation in Cz - silicon [7-11]. The precipitation process consists of two steps : nucleation and growth. More recent theories take into account both factors which allow one to simulate the precipitate size distribution in addition to the loss of interstitial oxygen [9-11]. Based on one of the latter models the following simulations are performed.

4.1 Theoretical description

The simulation is based on a theoretical model used by Schrems [11]. The precipitation process is described by a particle size distribution function f (n, t) which depends on the number n of oxygen atoms in the precipitate and the time t. The growth of a precipitate containing n atoms is described by chemical rate equations of the following type

$$\frac{\partial f(n)}{\partial t} = g(n-1)f(n-1) - (d(n)+g(n))f(n) + d(n+1)f(n+1)$$

with the growth rate g(n,t) and the dissolution rate d(n,t). The condition for particle conservation determines the equation for n = 1. If n is large enough (n > 20 in our calculation) the equations can be approximated by a Focker - Planck type system

$$\frac{\partial f(n)}{\partial t} = -\frac{\partial I(n)}{\partial t} \qquad \text{with} \qquad I(n,t) = -B\frac{\partial f(nt)}{\partial n} + A f(n,t)$$

$$B(n,t) = \frac{1}{2}[g(n,t) + d(n,t)] \qquad A(n,t) = g(n,t) - d(n,t) - \frac{\partial B(n,t)}{\partial n}$$

The growth rate g (n, t) and the dissolution rate d (n, t) are given by

$$g(n,t) = k_{react}\ C_o^{if} \qquad d(n,t) = k_{react}\ C_o^{if,eq} \qquad \text{with} \qquad k_{react} = 4\pi r^2 \frac{D_o}{\delta} \exp\left(\frac{-\Delta G}{kT}\right)$$

$$\Delta G = G(n+1) - G(n) \qquad G(n) = -nkT\ln\left(\frac{C}{C_o^{eq}}\right) + 4\pi r^2 \alpha\,(1+(\frac{\varsigma}{n})^{1/3})$$

where C_o^{if} and $C_o^{if,eq}$ are the non-equilibrium and equilibrium concentrations of O_i at the precipitate - matrix interface, respectively. $G(n)$ is the Gibbs free energy that yields the chemical driving force for precipitation. In addition, certain boundary conditions are required. For the simulation the following parameters are used : the parameter $\zeta = 0.22$ [11] and the interfacial energy $\alpha = 0.48$ J / m^2 [12]. The equilibrium concentration and the diffusion coefficient for oxygen are taken from reference [13] :

$$C_o^{eq} = 9\times10^{22}\ \exp(-1.52eV/kT) \quad [cm^{-3}] \qquad D_o^{eq} = 0.13\ \exp(-2.52\ eV/kT) \quad [cm^2/s]$$

4.2 Numerical results

The simulation allows one to monitor the evolution of the precipitation process as a function of time. Two example shall be discussed. In the first case the oxygen precipitation in mc - silicon is simulated for the

same conditions that have been used in the experimental investigations. A uniform oxygen concentration at the beginning is assumed. The calculated size distribution for a 1050°C and 24 hours anneal is shown in figure 10a. The precipitated oxygen mainly occurs in clusters with about 10^8 atoms which corresponds to a precipitate size of about 20 nm assuming a spherical shape. This is indeed observed by the TEM investigations. The remaining interstitial oxygen is shown in figure 10b as a function of time and compared with the experimental results. The agreement is quite well except for the temperature 1050°C where less oxygen has precipitated than calculated. This may be due to the fact that in this temperature range precipitation occurs mainly at dislocations. The simulation of this process may require different parameters that are not known.

The second simulation is performed for the RGS process which is much faster and consists of several temperature steps. The initial oxygen concentration is 2×10^{18} cm^{-3}. Figure 11a shows the size distribution function at two different times. Due to the high oxygen concentration the precipitation occurs quite rapidly within a short period of time. The remaining interstitial oxygen is shown in figure 11b. The mean size and the density of the SiO_2 precipitates obtained from the simulation are given in table 2 and compared with the TEM results. The agreement in this and other case that cannot be presented here is quite good. However, there are still not sufficient experimental data available for a comprehensive comparison with the simulation. In particular it is not yet possible to study the influence of carbon on the precipitation process.

Table 2
Measured and calculated sizes and densities of SiO_2 precipitates in RGS ribbon silicon.

	Size [nm]	Density [cm^{-3}]	O_i [cm^{-3}]
RGS cell	20 - 50	4.9×10^{11}	6×10^{17}
Simulation	22	5.9×10^{11}	4×10^{17}

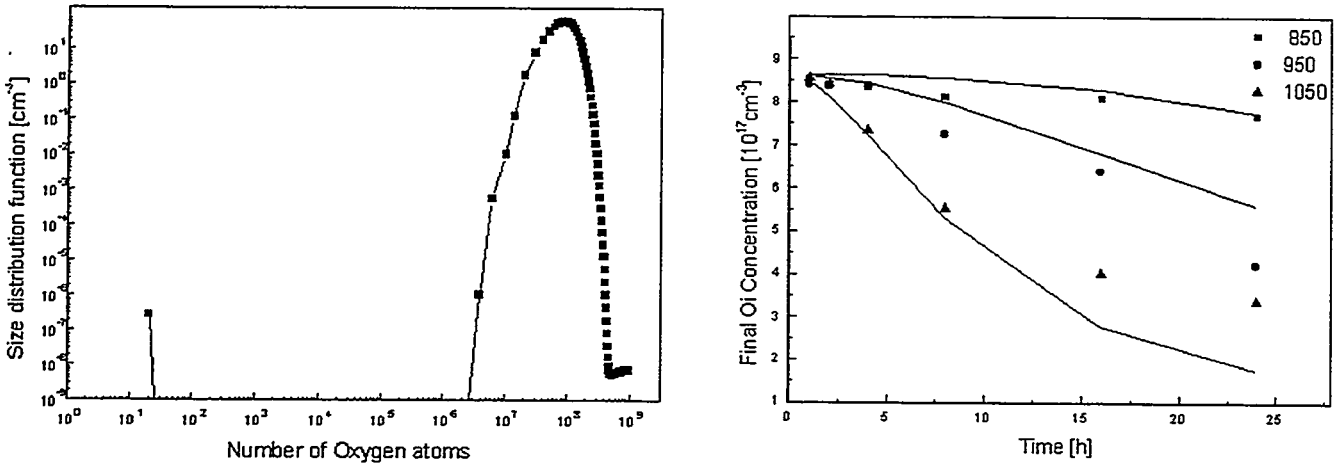


Figure 10 The size distribution function as function of the number of the precipitated oxygen atoms for a 24h anneal at 1050°C for mc-Si (left). The total interstitial oxygen concentration as a function of the annealing time and comparison with experimental results (right).

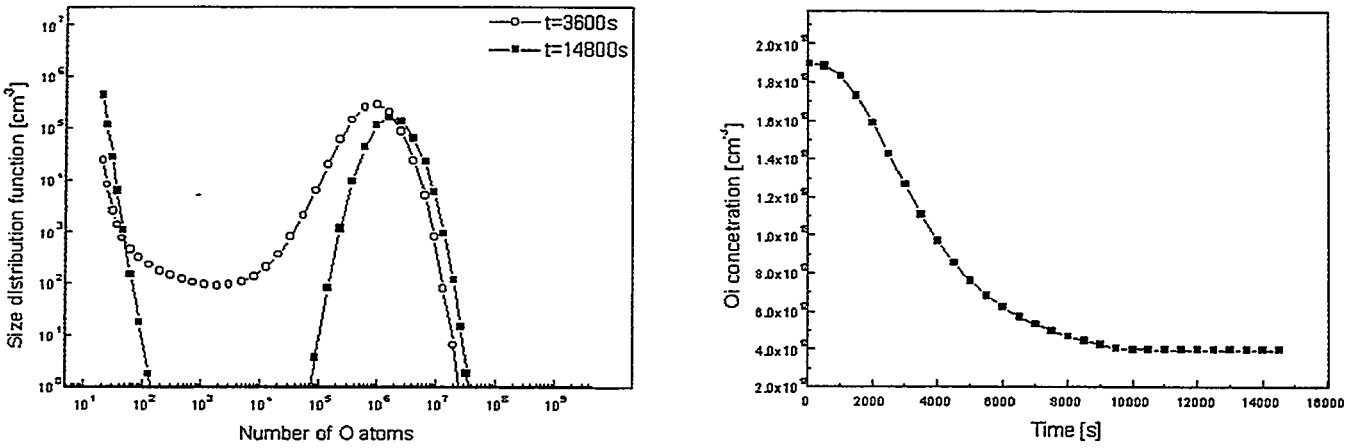


Figure 11 The size distribution as a function of the number of the precipitated oxygen atoms for the RGS process (left). The total interstitial oxygen concentration as a function of the annealing time (right).

The results have been used already to modify the RGS processing sequences in such a way that different precipitate distributions were obtained. Solar cells from these materials indeed show that this has an impact on the device performance.

5. Summary

The oxygen precipitation can be an important factor in polycrystalline solar cells made from ingot and RGS ribbon silicon. In this report it has been shown that the distribution and size of the precipitates depends considerable on the thermal history of the material. The bulk precipitation is comparable to Cz - silicon, however, higher carbon concentrations, dislocations and grain boundaries that are not present in monocrystalline material can have a significant impact on the precipitation process in particular temperature ranges. The ramifications of the various types of precipitates and decorated extended defects on the device performance are not completely analyzed yet, but there is substantial evidence that these defects have to be taken into account. It could also been shown that numerical simulations are already sufficiently accurate now to support the development of the polycrystalline material and to improve the crystal growth as well as the solar cell processes.

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ANALYSIS OF IRON PRECIPITATION IN SILICON USING MINORITY CARRIER LIFETIME MEASUREMENT

Worth B. Henley and Deepak A. Ramappa
Center for Microelectronics Research, University of South Florida, Tampa, Florida

Abstract

Temperature dependent iron precipitation in float-zone grown silicon wafers has been experimentally investigated. Results of iron precipitation experiments over a wide thermal process temperature range and time are presented. Precipitation of iron in silicon was analyzed by a quantitative assessment of change in interstitial iron using a surface photo voltage minority carrier lifetime analysis technique. Contamination levels of iron in the range 10^{11} to 10^{13} atoms/cm^3 are investigated. It is concluded that maximum iron precipitation occurs in the temperature range of 500°C to 600°C. Iron precipitation is rapid in this region where more than 90% of the interstitial iron precipitates in a period of 30 minutes.

Introduction

Metallic transition elements are prevalent contaminants in Si which can degrade device performance either by forming metal silicides or/and by acting as recombination centers. Iron is one of the primary heavy metal impurities in silicon. Commonly reported sources of iron contamination include ion implanters, contaminated chemicals, and wafer handling tools. Iron diffuses rapidly through the silicon matrix by interstitial diffusion. Because of the high diffusivity (approximately 10^{-6} cm^2/s at 900°C)[1] iron contaminates introduced from the wafer surface during thermal processing diffuse throughout the bulk of the wafer. The steep, retrograde temperature dependence of iron solubility in Si[1] results in supersaturation during wafer cooling from high process temperatures. This supersaturation is responsible for localized precipitation.

Iron plays an important role in the decoration of defects in silicon.[2-5] This can be very detrimental to device region of the wafer, as strain fields and process induced defects can localize the Fe impurities in this sensitive area.[6] It is well accepted that iron contamination degrades gate oxide integrity and decreases yield as devices are scaled to sub-micron dimensions.[7] Unprecipitated iron remains as the interstitial deep level impurity Fe_i or as Fe-B pairs in p-type silicon. It reduces minority carrier lifetime and increases diffused junction leakage.

Generally for contamination levels of practical concern, at temperatures below 800°C the Fe-Si system is metastable and thermodynamically favors iron-silicide precipitation. The iron solubility limit in silicon at 500°C is about $2x10^7$ atoms/cm^3. Since the best commercially available wafers today typically contain $5x10^9$ atoms/cm^3 of iron, the fact that iron supersaturation and precipitation can occur are a matter of general concern to the technologist.

The tendency for iron precipitation to occur is influenced by the amount of time for nucleation and embryo growth before the lower silicide reaction (formation) temperature is reached. This is illustrated in Figure 1, which shows the temperature cycle of a typical anneal or

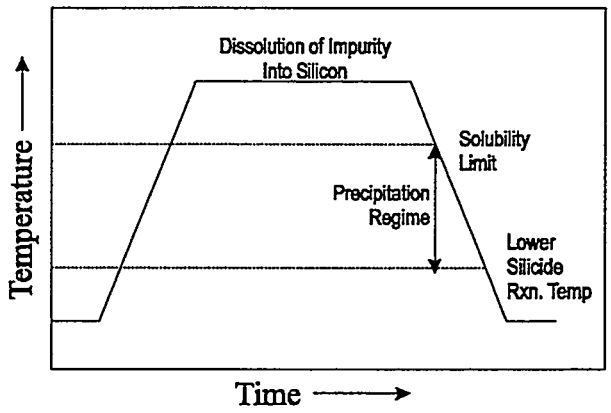


Figure 1: Typical silicon IC fabrication thermal cycle showing where precipitation is most likely to occur.

oxidation process. Previously reported lower silicide temperatures vary between 300°C and 500°C.[8-9] Iron-silicide ($FeSi_2$) precipitation favors heterogeneous nucleation.[10] This can be useful for some internal gettering procedures as oxygen precipitates may serve as favored precipitating sites. It has also been shown that the internally gettered iron is often not the precipitate phase.[11] Redissolution of the $FeSi_2$ phase or release of gettered atomic iron[11] remains hazardous to the surface device area.

Fe precipitation in Si has been previously studied in highly contaminated silicon [10^{14} to 10^{16} Fe atoms/cm^3] [10,12-15] and in the lower temperature range of 100°C to 300°C.[8,16] In this paper we present an experiment which quantitatively evaluates Fe precipitation in lightly contaminated Si [10^{11} to 10^{13} Fe atoms/cm^3]. Low oxygen content float zone (FZ) grown silicon crystals were used in experimentation, so as to avoid the uncertainties introduced by O_2 precipitation and the consequent gettering uncertainties. Precipitation over the entire temperature range of 300°C to 900°C over different process times have been experimentally evaluated.

To analyze precipitation of iron in silicon, quantitative interstitial iron (Fe_i) concentration measurements, were performed using the technique of surface photo voltage (SPV) minority carrier lifetime analysis. The SPV method has very good sensitivity in detecting low concentrations of bulk Fe_i in the silicon wafer.[7] Interstitial Fe concentrations are measured before and after a precipitation anneal. Any decrease in Fe_i is assumed to be due to formation of the $FeSi_2$ precipitate phase. This change in interstitial Fe (ΔFe_i) is used to analyze the iron precipitation quantitatively with respect to time and temperature. A characteristic relationship between the precipitating iron and annealing time over the entire process temperature range is deduced.

Experiment

The experiment can be broadly analyzed in two stages. First iron was diffused from a surface source into the wafer, to obtain a stable and uniform Fe_i concentration in the wafer. Following the in-diffusion, the iron rich surface region was chemically removed and various anneals were performed. Iron precipitation was monitored by comparing the change in interstitial iron after the thermal anneal process.

The experimentation was performed using 3 inch, 1-2 Ω-cm, P-type FZ grown <100> wafers [Wacker-Chemitronic]. Starting wafer background iron concentration was determined to be $4x10^{10}$ atoms/cm^3. The samples were cleaned in the order HF--SC1--HF--SC2--HF, where the HF was diluted with water in the ratio 1:50. SC1 was a 1:2:10 solution mixture of ammonium hydroxide, hydrogen peroxide and water heated to a temperature 65°C. SC2 was a 1:1:5 solution mixture of hydrochloric acid, hydrogen peroxide and water maintained at 65°C. The background level of iron contamination from the starting wafers, cleaning procedure and subsequent furnace processing was established to be about 6×10^{10} atoms/cm^3 at 900°C. Thus the wafer processing procedure introduced about 2×10^{10} atoms/cm^3 of Fe_i into the samples. This is typical after a high temperature thermal process.

Selected samples were intentionally doped with iron by immersion in a 100 ppm solution of ferric chloride ($FeCl_3$) for 10 minutes and then nitrogen blow-dried. To obtain a target Fe_i concentration of $2x10^{13}$ atoms/cm^3 a diffusion temperature of 900°C was used according to Fe solubility data.[1,15] The wafers were slowly ramped up to minimize lattice deformation and were diffused for 40 minutes in a nitrogen ambient. After the in-diffusion heat treatment the samples were quench cooled by blowing cool nitrogen vapors onto the surface during withdrawal from the furnace. Other techniques and materials of quench cooling such as oil immersion, di-ethylene glycol, and water were evaluated but dismissed as they caused significant amount of thermally induced lattice damage, which disrupted minority carrier lifetime measurements. The nitrogen cooling cooled the sample down from 900°C to room temperature in about 2 minutes. Such rapid cooling was performed to prevent any unwanted precipitation and to ensure most of the iron remained in an interstitial state.

The surface of the samples were chemically etched to remove any Fe rich areas on the surface. The etchant was a concentrated reagent mixture of nitric acid(HNO_3), glacial acetic acid(CH_3COOH) and hydrofluoric acid(HF) in the ratio 6:1:1[Dash etch [17]]. They were etched for 3 minutes, to remove a surface layer of about 60 μm.

Interstitial iron concentration (Fe_i) and the change in Fe_i was monitored using a surface photo voltage (SPV) minority carrier lifetime analysis technique. The SPV method is an analytical technique for the measurement of minority carrier diffusion length and thus lifetime of carriers in semiconductors. It provides a fast, non-contact, non-invasive measurement. Iron concentration was determined from the lifetime measurements using well known Fe-B pairing relationships[18,19,22] outlined below. The iron concentration measurement was made at 10 points across the wafer and care was taken to measure the same sites on the sample.

For the precipitation studies the measured samples were annealed for different times and temperatures. The specimens were annealed in a nitrogen ambient, over the temperature range of 300°C to 900°C, for times of 5 to 90 minutes. All the experimental specimens were cooled at a similar rate to keep the cooling rate constraint as a non-variant. Quantitative measurement of Fe_i of each sample, was performed by the SPV technique. By comparing the pre-anneal interstitial iron concentration to that following the anneal, the precipitated fraction was easily calculated.

Results

The amount of Fe diffused into the silicon wafer from the surface contamination was chiefly a function of the drive-in temperature and independent of the drive-in duration for a drive-in time of greater than 15 minutes. Since both the drive-in and anneal were performed in nitrogen ambients, oxide growth was avoided and thus prevented Fe out diffusing into the oxide.[7] For the 900°C drive-in temperature used here, the described intentional contamination procedure routinely yielded silicon wafers with approximately $2x10^{13}$ atoms/cm^3 interstitial iron concentration in agreement with solubility considerations.[1] Wafer mapping showed the iron concentration uniformity to be to be ±10%.

Non-contaminated control Si wafer samples processed with the Fe doped wafers showed some degradation in diffusion length following the thermal drive-in process. This was most likely due to the rapid quenching from the 900°C process resulting in a thermally induced native defect structure. Typical diffusion lengths and the corresponding Fe_i concentrations measured on the iron doped Si samples are shown in Table 1. The Fe_i concentrations of all the iron contaminated samples, averaged around $2.7x10^{13}$ Fe atoms/cm^3. Iron concentration on the non contaminated control samples was typically 6×10^{10} atoms/cm^3.

Table I. Typical minority carrier diffusion lengths and interstitial iron concentrations measured on clean and iron doped silicon after annealing and quench cooling.

Sample	Diffusion Length (μm)	Fe_i Concentration (atoms/cm^3)
Fe doped	44.2	2.7×10^{13}
Uncontaminated wafer	112.4	6×10^{10}

The precipitation anneal experiments showed the change in post anneal interstitial iron concentration to be highly dependent upon the annealing temperature and time. Figure 2 clearly shows that significant precipitation occurs over the temperature range of 400°C to 800°C. The greatest loss of interstitial iron was seen in the range of 500°C to 600°C. Our ability to discern changes in interstitial iron was limited to about the 10^{11} atoms/cm^3 range due to the background wafer defect structure effects on the SPV measured carrier lifetime. Thus, we have been unable to clearly asses what occurs beyond the 90 minute annealing. It is evident that significant precipitation can occur in the 500°C to 600°C process regime. A loss of more than two orders of magnitude in interstitial iron is noted. Above a temperature of 800°C, precipitation is much reduced and redissolution of pre-existing precipitates or release of some previously gettered iron is observed which can result in an increase in the final Fe_i concentration.

Figure 3 further illustrates the time/temperature precipitation tendencies of the iron-silicon system. Here the dramatic effect of the process temperature is seen clearly. For temperatures above 700°C, there is less effective solute supersaturation and the chemical thermodynamics still support the combined presence of both interstitial iron and the precipitate phase. Indeed, as mentioned above, our work shows that at temperatures exceeding 900°C, precipitate redissolution can occur. This finding was confirmed by subjecting heavily precipitated samples to a 900°C

Generation and Influence of Deep Levels in N_2 Diffused Si

Yukio Takano and Katsunori Kakumoto

Department of Materials Science and Technology, Science University of Tokyo,
2641 Yamazaki, Noda-shi, Chiba 278, Japan

Abstract

N_2 related deep levels are found in n-type and p-type CZ- and FZ-Si annealed in N_2 and then quenched to room temperature. The activation energy and capture cross section of the deep level are Ec-0.5 eV and 7.6×10^{-16} cm^2 in n-type Si and Ev+0.55 eV and 10^{-15} cm^2 in p-type Si, respectively. Depth profiles of the deep level density show that of the complementary error function. Diffusion coefficient estimated by the profiles agrees well with that of N_2 in Si. The deep level is decreased by injecting interstitial Si from the interface between a growing SiO_2 film and a Si crystal. It is strongly suggested that the deep levels are caused by N_2-vacancy complexes.

The energy level of the deep level is located near the middle of the band gap, therefore it is likely that the deep levels act as recombination centers. We show the experimental results that the lifetime is decreased by the N_2 related deep levels.

1. Introduction

N_2 gas is widely used in Si device fabrication processes, because it is believed that N_2 molecules give no unfavorable influence to Si properties. But recently Tokumaru et al.[1] and Abe et al. [2] observed deep levels in as-grown and post annealed N_2 doped FZ-Si , respectively. Hara et al.[3] reported diffused N_2 formed complexes with doped oxygen and they behaved as shallow donors in Si. We reported that N_2 related deep levels were induced by diffused N_2, when a silicon wafer was annealed in N_2 and then quenched to room temperature. The energy level of the deep level was located near the middle of band-gap, therefore it was possible to act as the effective recombination center for excess carriers and to decrease the minority carrier lifetime [4]. We also suggested that the deep level was introduced by the formation of N_2-vacancy complexes, because the deep level was very sensitive to the wafer cooling rate after N_2 annealing. In order to confirm this assumption, we attempted to control the deep level density by changing the vacancy concentration. Oxidation of the silicon surface are known to decrease the vacancy concentration, since they supply excess interstitials from the oxide and silicon inter surface. Experimental re-

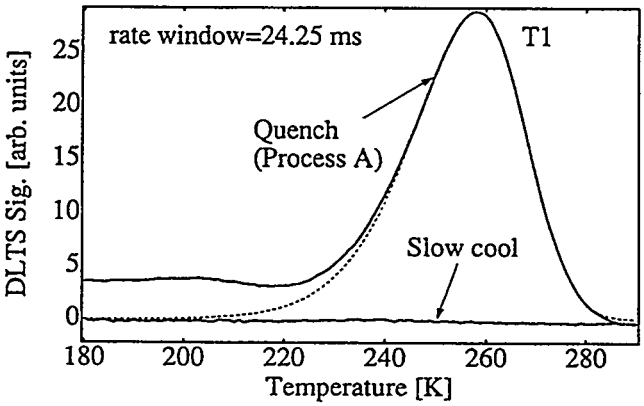


Fig.1 Examples of DLTS spectra of CZ specimen annealed at 750℃ for 1h in N_2

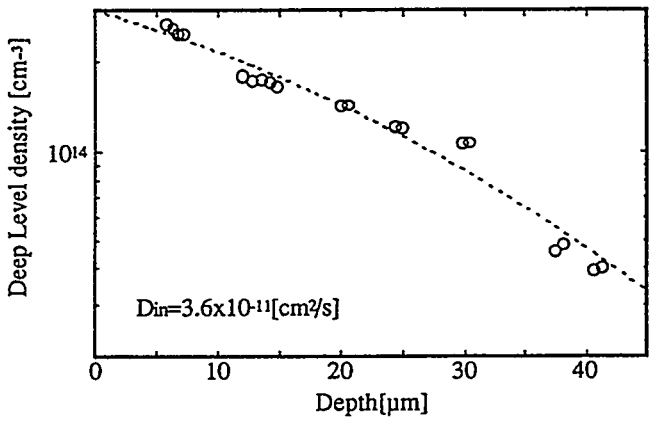


Fig.2 Depth profile of the deep level (E1) density in the specimen annealed at 750℃ for 1h in N_2

sults clearly show that the deep level density was very low in the specimen which was oxidized in N_2 and O_2 mixed gas[5].

In this report, at first the diffused N_2 related deep levels and the origin of them are explained in details. Second, influence of the deep level to the minority carrier lifetime is shown.

2. Generation of N_2 related deep level

Figure 1 shows typical DLTS spectra of n-type CZ-Si wafers annealed at 750 ℃ for 1h in N_2. Solid and broken lines are measurement and theoretical curves,

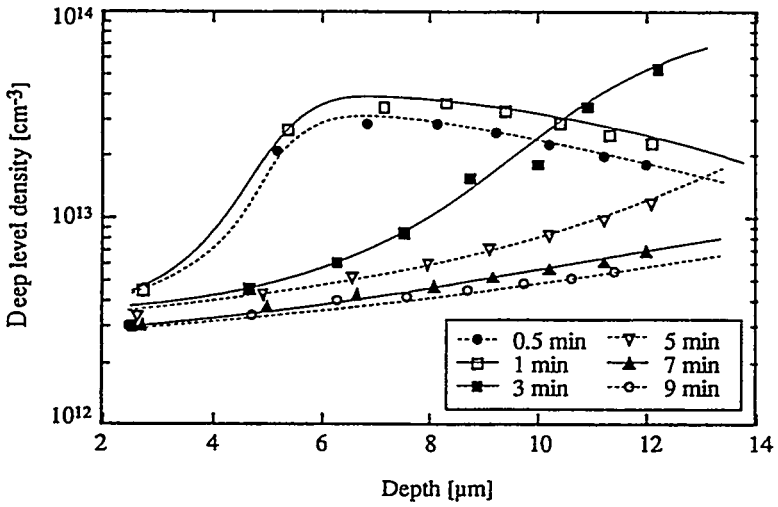


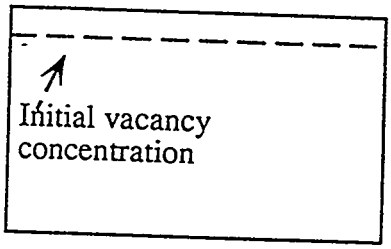
Fig.3 Depth profiles of the deep level E1 density in the specimen annealed at 1000℃ in N_2+O_2 mixed gas

respectively. Peak E1 was clearly observed in the quenched wafer, but was not observed in the slowly cooled wafer.

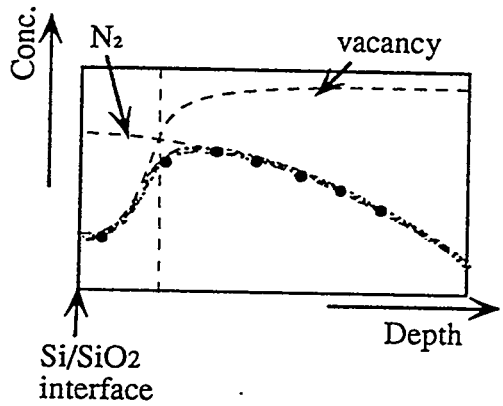
Figure 2 shows the depth profile of the deep level density. Of note is that the deep level E1 shows an in-diffusion distribution profile and that the profile agrees well with that of the complementary error function. The diffusion coefficient was estimated to be 3.6×10^{-11} cm²/s at 750 ℃. The value shows very good agreement with the diffusion coefficient of N_2 in Si [6]. From these results, the deep level E1 is assumed to be due to N_2 which diffused into silicon during N_2 annealing. This N_2 related deep level was observed in both CZ and FZ wafers, so the level has no relation to oxygen in Si.

As shown in Fig.1, the deep level density depends on the cooling rate of the specimen after N_2 annealing: the peak assigned to the deep level is not observed in the slowly cooled specimen, but is observed in the quenched specimen. From these experimental results, it is reasonable to think that the appearance of the deep level not only relates the diffused N_2, but also point defects especially vacancies. In order to confirm the above assumption, we performed the following experiments. Excess interstitials supplied from the growing SiO_2 interface recombine vacancies and decrease the vacancy density, therefore also the deep level density.

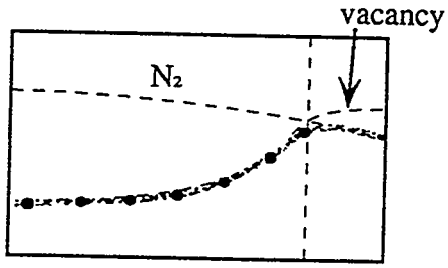
N-type, 8-12 Ω-cm, (100), FZ-Si wafers were annealed at 1000 ℃ in N_2 and O_2 mixed gas for 0.5-9 min and then quenched to room temperature. Figure 3



(a) Depth profile of vacancy just after heating specimens at 1000°C



(b) Depth profiles of vacancy, N_2 and the deep level after annealing for short time within 3min in $N_2 + O_2$



(c) Depth profiles of vacancy, N_2 and the deep level after annealing for longer time beyond 3min in $N_2 + O_2$

Fig.4 Schematic drawing of depth profiles of vacancy, nitrogen and the deep level density induced in the specimen annealed at 1000℃ in N_2+O_2 mixed gas

Table 1. Activation energy and capture cross section of deep levels in N_2 diffused Si

	n-type	p-type	
	E1	H1	H2
activation energy [eV]	Ec-0.5	Ev+0.6	Ev+0.25
capture cross section [cm^2]	$5.8\pm0.2 \times 10^{-16}$	$1.1\pm0.8 \times 10^{-15}$	1.2×10^{-15}

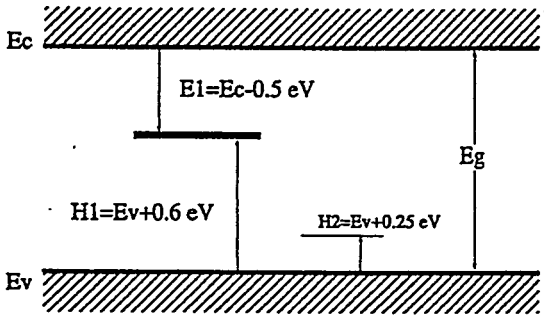


Fig.5 Deep levels in N_2 diffused n-type and p-type Si

shows depth profiles of the deep level density in the specimens. It is noted that the lower density region of the deep level expands gradually from the surface to the deeper region of the specimens as the annealing time increases. The experimental results are explained in the followings. During annealing in N_2 and 0_2 mixed gas, N_2 diffuses into the wafer and at the same time excess silicon interstitials are supplied from a growing SiO_2/Si interface and consequently vacancies are diminished near the interface. Changes of the depth profiles of the vacancy and the diffused N_2 are schematically shown in Fig.4.

The vacancy depth profile which is expected to be flat after the short time annealing(Fig.4a) will change gradually near the surface as shown in Fig.4b and 4c. On the other hand, the depth profile of the diffused N_2 changes under the complementary error function. The density profiles of the diffused N_2-vacancy complexes estimated from both of the vacancy and the N_2 profiles are also shown in Figs.4b and 4c. The results of the deep level profiles is understood by the above explanation.

The diffused N_2-vacancy complexes were found to make also deep levels in p-type Si. Activation energy and capture cross section of the deep levels in n-type and p-type Si are shown in Table 1. The energy levels of the deep levels are schematically shown in Fig.5. The deep level E1 and H1 are confirmed to be formed by the same level and behave as carrier recombination centers. Therefore, the deep level E1 and H1 make the minority carrier lifetime shorter.

3. Influence of N_2 related deep levels

In this section, experimental results that the lifetime is decreased in a oxidized wafer after boron diffusion are shown to be due to recombination centers made of N_2-vacancy complexes. Fig.6 shows the results of the DLTS and the lifetime measurements in an as-grown, n-type, 25 Ω-cm, FZ-wafer and B-diffused(1 h

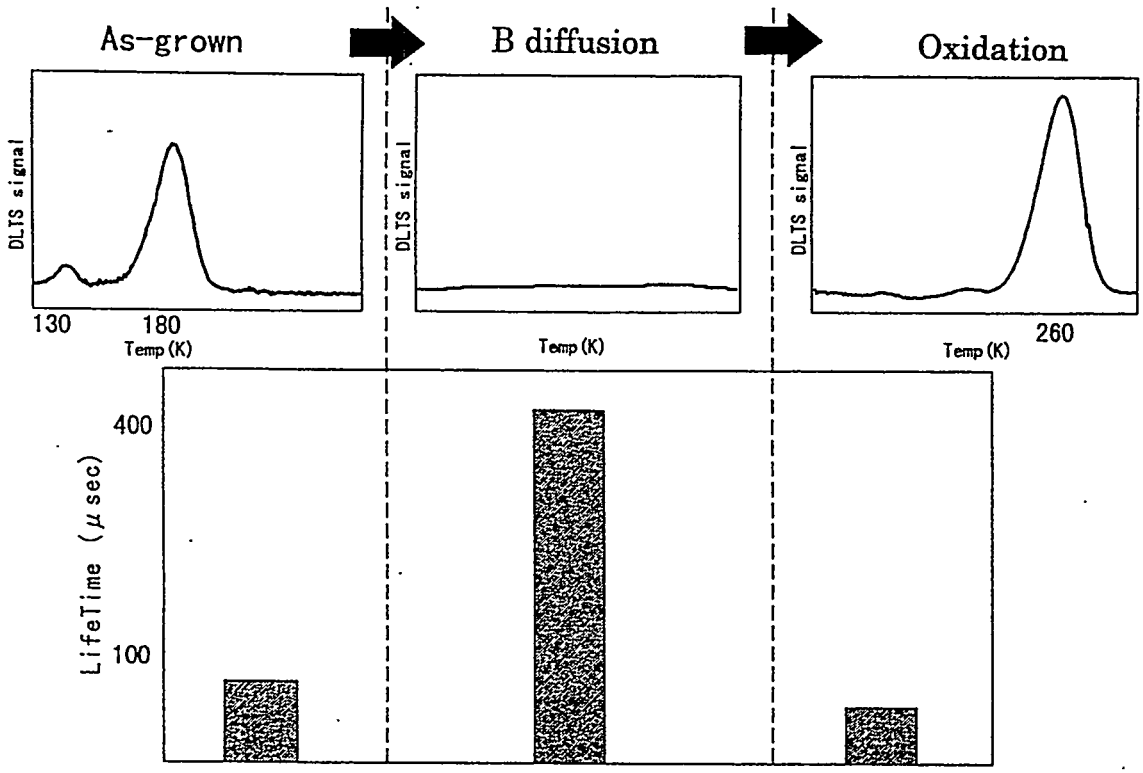


Fig.6 Measurements of DLTS and lifetime in as-grown, B-diffused (1h at 1000℃, BN source) and subsequently oxidized wafers(1h at 1000℃, dry O_2)

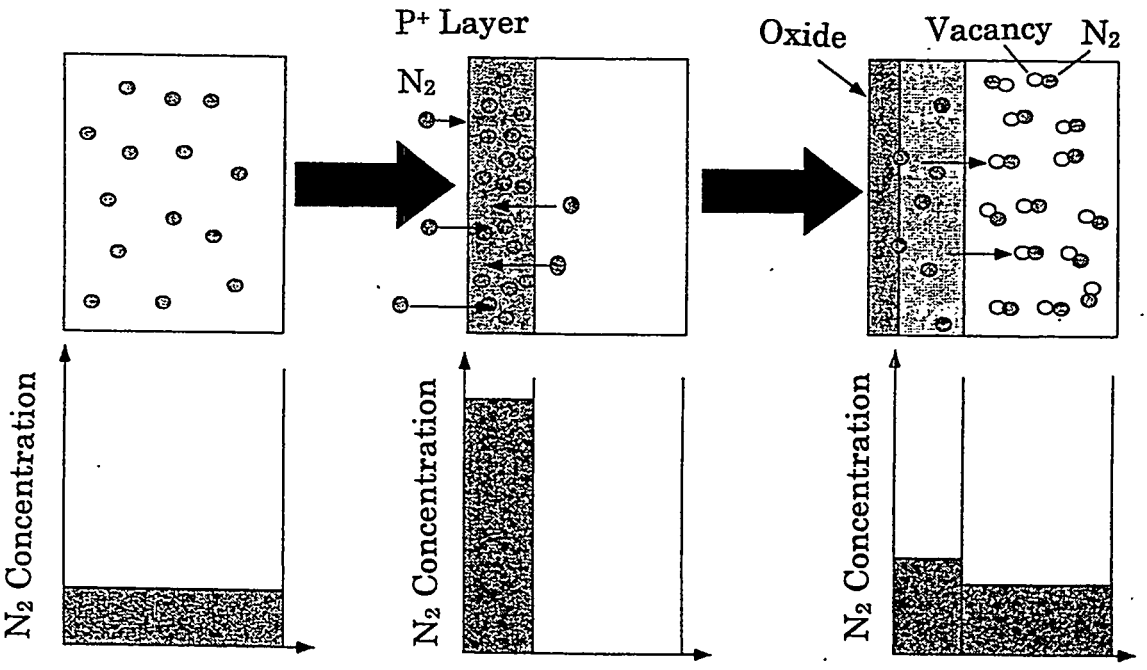


Fig.7 Movement of N_2 in B-diffusion and subsequent oxidation process

at 1000 ℃, BN source) and subsequently oxidized(1h at 1000℃, dry oxidation) wafers. In the as-grown wafer, two peaks are clearly observed near 130 K and 190K in the DLTS curve. The deep levels corresponding to peaks 130 K and 190K are shown to have energy levels of Ec-0.20 eV and Ec-0.31 eV, respectively. The peak temperatures and the energy levels agree with the reported values in N_2-doped FZ Si crystals[1].

After B diffusion, the DLTS peaks are completely disappeared, however, the another peak appears at 260 K after the subsequent oxidation as shown in Fig.6. The peak at 260 K corresponds to the deep level induced by N_2-vacancy complexes shown in the above. The lifetime measured in these specimens are shown in the below of Fig.6. The lifetime is drastically increased from 80 μs to 460 μs by the B diffusion. But the lifetime is sharply decreased again down to 60 μs by the subsequent oxidation. The deep levels measured by DLTS method are related with majority carrier traps, therefore the lifetime is not directly influenced by the trap. But, the deep level which makes the DLTS peak at 260 K may behave as the recombination centers[7]. Therefore, the decrease of the lifetime in the subsequent oxidized specimen seems to be due to the deep levels formed by N_2-vacancy complexes. In the as-grown specimen, it seems also that some N_2 related recombination centers decrease the lifetime. In order to confirm the above assumption, it is necessary to measure minority carrier traps in the as-grown specimen by using the method such as the optical DLTS. The phenomena of the N_2 related deep level shown in the above are explained in the next.

Figure 7 shows behavior of N_2 molecules in a Si during the B diffusion and the subsequent oxidation processes. It is known that N_2 is doped in Si to erase swirl defects in an as-grown FZ Si crystal[8]. N_2 molecules are diffused during B diffusion process, because N_2 is used as an ambient gas. Both of the doped N_2 and diffused N_2 molecules are gettered in the B diffused layer in the B diffusion process, therefore the lifetime is elongated as shown in Fig.6b. After the subsequent oxidation, the gettered N_2 molecules diffuse out again from the B diffused layer, because the B surface concentration is decreased by segregation of B into the oxide and driving-in diffusion into a Si substrate. In consequence of the B concentration decrease, the gettering power to N_2 molecules becomes weak and the lifetime decreases.

4. Conclusion

Electrical properties of N_2-diffused Si are studied and found as shown in the following. Deep levels are formed in n-type and p-type Si annealed in N_2 and then quenched to room temperature. The activation energy and capture cross section of the deep level are Ec-0.5 eV and 7.6×10^{-16} cm^2 in n-type Si and Ev+0.55 eV and 10^{-15} cm^2 in p-type Si, respectively. It is strongly suggested that the

deep levels are caused by N_2 –vacancy complexes, because the deep level is decreased by injecting interstitial silicon atoms from the interface between a growing SiO_2 film and a Si crystal. It is found that the deep levels make the lifetime shorter and disappear in B diffused Si wafers.

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Hydrogen in Crystalline Si: A Survey of Recent Results

Michael Stavola
Department of Physics, Lehigh University, 16 Memorial Drive East, Bethlehem, PA 18015

Even though hydrogen is the simplest atom, it is a complicated impurity in semiconductors that can have a dramatic effect on electrical properties. There have been many studies of the properties of hydrogen and hydrogen-containing defects in semiconductors over the past 15 years, and much progress has been made.[1-5] Nonetheless, there are many important open questions about isolated hydrogen and hydrogen-containing complexes. In this paper, a survey of selected results obtained for the fundamental properties of hydrogen in silicon will be presented.

I. The diffusion and solubility of hydrogen

The incorporation of hydrogen into silicon by diffusion is one of the properties of greatest interest, but it is also one of the most complicated. The diffusion constant for isolated H^+ appears to be well known, but the indiffusion of hydrogen into Si is made complicated by the existence of three charge states for hydrogen, interactions with other impurities, and the formation of slow diffusing hydrogen molecules. Here, results for the diffusion and solubility of isolated hydrogen are summarized first, followed by a qualitative discussion of the shapes of indiffusion profiles that result from hydrogen plasma treatment. Several critical reviews [5-8] on hydrogen diffusion and solubility have been written which should be consulted for information beyond the scope of the following survey.

A. Diffusion

The earliest determination of the diffusion of hydrogen in Si was performed by Van Wieringen and Warmoltz (VWW).[9] The permeation of hydrogen through thin-walled cylinders of Si was studied for the temperature range 1090°C to 1200°C to obtain the following relationship for the diffusion coefficient:

$$D_H = 9.4\text{x}10^{-3} \exp(-0.48 \text{ eV} / kT) \text{ cm}^2/\text{s}. \quad (1)$$

This relationship for the diffusivity is the most commonly used for isolated hydrogen and has been frequently extrapolated to room temperature. The diffusion coefficient given by Eq. (1) is plotted in Fig. (1) along with data points at 1090 and 1200°C. We will find in the following that recent data for the diffusivity of H^+ are consistent with Eq. (1) over a surprisingly large range of temperatures.

An alternative approach to measure the hydrogen diffusion coefficient gave a much smaller value for the diffusivity than Eq. (1) above. Ichimura and Furuichi [10] heated 150 Ω-cm p-type, floating-zone Si samples in a tritium ambient at 900 to 1200°C for 1 h to saturate the Si with tritium, followed by a quench to room temperature. The evolution of tritium was then measured for several temperatures between 400 and 500°C to determine the diffusivity and solubility of ^3H. These data are shown in Fig. 1. The diffusion constant determined by Ichimura and Furuichi [10] is approximately 740 time smaller at 500°C than the previous result by VWW [9] when extrapolated to this temperature. Possible explanations for the smaller

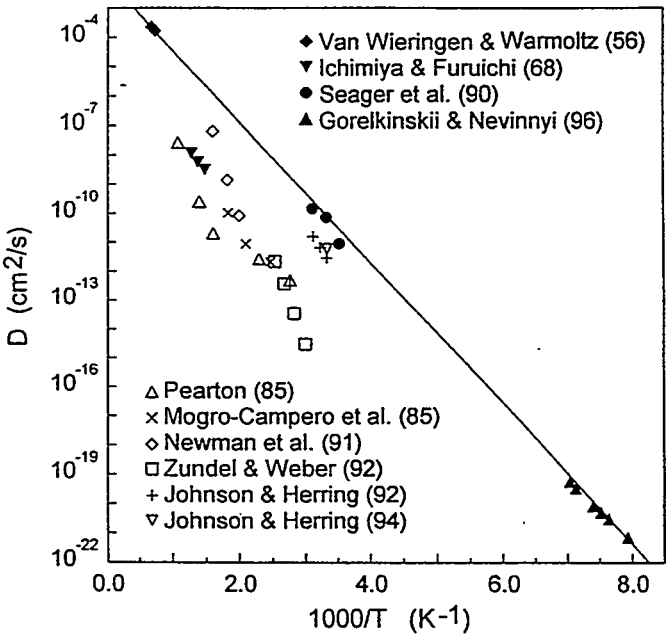

Fig. 1. Selected data for the diffusion coefficient of hydrogen (or deuterium) in Si. The data shown for each study are not complete, but have been selected to indicate the temperature range where the measurements were made and its extent.

values measured by Ichimura and Furuichi include (i) their suggestion that an oxide layer at the surface that may have impeded tritium out-diffusion [10] or (ii) the formation of slow diffusing tritium molecules in the Si.[11]

There have been numerous subsequent values reported for the hydrogen diffusivity that have been determined from measurements of the indiffusion depth during exposure to a source of atomic hydrogen.[12-14] A selection of values of the diffusivity determined by this method are shown in Fig. 1. These studies give diffusion coefficients about a factor of 1000 times smaller than the VWW result, Eq. (1).

A few early studies of hydrogen indiffusion made near room temperature suggested that under appropriate conditions, the migration of H was in agreement with an extrapolation of the VWW result for the diffusion coefficient, Eq. (1). For example, Tavendale *et al.* [15] introduced hydrogen into Si by wet chemical etching and showed that the drift of H^+ in these experiments was consistent with a room temperature diffusion coefficient of $3x10^{-10}$ cm^2/s, a result in approximate agreement with Eq. (1). Seager *et al.* [16,17] determined the diffusion coefficient of hydrogen in Si near room temperature in novel drift experiments in which they implanted protons with an ion gun into Schottky barrier diodes. They were able to determine the hydrogen diffusion coefficient by monitoring the evolution of the junction charge with real-time capacitance-voltage (CV) measurements made during the low energy H^+ implantation process In these experiments, the dopants in the diode were passivated as the hydrogen ions drifted across the junction. The data points shown in Fig. 1 are from the results of an H^+ transit time measurement made for p-type Si in which the drift of H^+ under the influence of the junction field was monitored.[17] The points lie near the line drawn for the VWW result, Eq. (1).

Several authors have concluded that the indiffusion of hydrogen is limited by trapping by other defects and H_2 molecule formation in many experimental situations. [See refs. 5-8 and the references contained therein.] Only when the concentrations of hydrogen and of trapping centers are small is the indiffusion depth consistent with the diffusion coefficient of isolated hydrogen. Thus at high temperatures, or in a few studies such as those of Seager *et al.* [16,17], the large value of the diffusivity characteristic of isolated H^+ is observed. In most

experiments where hydrogen profiles have been measured, an "effective diffusivity" has been obtained [5-8], in which the indiffusion of hydrogen is limited by molecule formation or trapping, explaining the results of the many studies that have found indiffusion depths decades smaller than the extrapolation of the VWW result [9] would imply. This point was nicely demonstrated by Zundel and Weber [18] who measured the redistribution of H^+ in boron-doped Schottky barrier diodes in which the boron had been passivated by hydrogen. They showed that the hydrogen motion was consistent with an effective diffusivity that was determined by the trapping and release of H^+ from the boron acceptors. The values of the effective diffusivity, D_{eff}, determined by Zundel and Weber are shown in Fig. 1 for an acceptor concentration of $N_A = 1.45 \times 10^{15}$ cm^{-3}. D_{eff} is in reasonable agreement with values determined from hydrogen indiffusion profiles.

Gorelkinskii and Nevinnyi [19] have studied the annealing of the electron paramagnetic resonance (EPR) spectrum AA9 that results when Si is implanted with protons at low temperature (80K). This spectrum has been assigned to isolated hydrogen and the charge state can be controlled by optical illumination. These authors find that H^+ is annealed away near 200K with an activation energy of 0.48 eV, consistent with a reaction limited by H^+ diffusion with an activation energy given by the VWW result, Eq. (1). The H^+ diffusion coefficient can also be determined from the recent results of Gorelkinskii and Nevinnyi, who have measured the reorientation kinetics of H^+ by EPR.[20] In these experiments, an applied uniaxial stress was used to produce a preferential alignment of the isolated H^+ impurities along particular <111> directions. Gorelkinskii and Nevinnyi measured the kinetics for the disappearance of the stress alignment for several temperatures near 135 K. The H^+ alignment disappears when H^+ jumps from one bond-centered site to another; this process is a single diffusion jump. The values of the diffusion constant calculated from the reorientation time constants measured by Gorelkinskii and Nevinnyi are plotted in Fig. 1. It is remarkable that these values, measured near 135 K, are consistent with Eq. (1), determined by measurements made in a limited range near 1200°C (1473K), extrapolated to values of the diffusivity of H^+ that are 18 decades smaller! Fitting the relationship for the diffusion coefficient to both the VWW data [9] and the values determined from the reorientation data measured near 135 K only changes the activation energy in Eq. (1) in the third decimal place, to -0.483 eV. The surprising agreement of these results may be misleading because quantum effects at low temperature, anharmonicity, and other effects might be expected to give deviations from Arrhenius behavior over such a wide range for an impurity as light as hydrogen.

The role of the charge state of hydrogen on the diffusion process has been treated casually above. In the VWW experiments [9] performed at high temperature, the charge state of hydrogen has been presumed to be H^+ or H^0. In the 1990 paper by Seager *et al.* [17], hydrogen was presumed to be in the positive charge state only a fraction of the time and neutral otherwise. More recent work by Seager and Anderson [21] concludes that H^+ may be the only species present during junction-field drift experiments made on p-type diodes. In the experiments by Gorelkinskii and Nevinnyi [19] it is argued that the reorientation data are for H^+.

Johnson and Herring [22,23] have reported experiments on D^- (i.e., $^2H^-$) in which minority carriers were injected into an n-type diode by pulsed optical illumination of the back surface to produce isolated hydrogen which could then be studied in its different charge states. For these experiments a diode was doped with phosphorus and passivated in a deuterium plasma. These authors report that P-D complexes are dissociated near room temperature by the injected minority carriers and that D is released.[22] Subsequent bias pulses allow the charge state of the released D to be controlled. The evolution of the mobile charged deuterium could be monitored by the time dependence of the junction capacitance. Johnson and Herring [23]

used electron flooding pulses to produce the D^- charge state following the production of mobile D in the reverse biased n-type diode. The diffusion coefficient of D^- was then determined near room temperature from the capacitance transients that resulted from deuterium migration and complex reformation. These results for the diffusion of D^- [23] are shown in Fig. 1 and are roughly a decade smaller than the extrapolation of the VWW results, Eq. (1). (A classical model for diffusion would predict that the diffusion coefficient for H would be a factor of $\sqrt{2}$ larger than for ^2H.) These experiments also provide a value for the diffusion coefficient for $^2H^+$ of $6x10^{-12}$ cm^2/s at 300K [24] which is shown in Fig. 1.

The ability to produce free hydrogen in junction diodes with minority carrier pulses has been challenged in work by Seager and Anderson [21,25] who have not been able to reproduce the capacitance transients reported by Johnson and Herring.[22-24] Instead, the behavior of the junction capacitance following bias pulses in experiments similar to those of Johnson and Herring was found to be complicated by a number of poorly understood charging effects.[21,25] Thus the conclusions of such measurements remain controversial and further work will be required to unravel the complicated behavior of hydrogen observed in such experiments.

There have been a number of theoretical calculations performed to explore the diffusion of hydrogen in Si. A recent review of theoretical studies of hydrogen in semiconductors has been written by Estreicher.[26] Total energy calculations were initially used to explore the configurations and migration paths of hydrogen in its positive, negative and neutral charge states.[27-30] Several possible migration paths were found for each charge state with activation energies of a few tenths of an eV. These studies have been followed by molecular dynamics simulations [31-33] of the diffusion of H^+ which give results in reasonable agreement with the early results of VWW [9]. Blochl *et al.* [34] have used a different approach to study the diffusion of H^+. Transition state theory was applied to a total energy *surface* that was calculated for H^+ with local density methods. The calculated diffusion coefficient is of the same order as the VWW result, Eq. (1) over the entire temperature range.

From the combination of the results by Van Wieringen and Warmoltz[9], Seager *et al.* [16,17], and Gorrelkinskii and Nevinnyi [19,20], the diffusion constant of H^+ has been measured from 1473K to 135K with all of these studies giving results that are in remarkably good agreement with Eq. (1) determined by Van Wieringen and Warmoltz in 1956. Several recent theoretical studies also yield diffusion constants for H^+ that are consistent with Eq. (1). The situation for H^0 and H^- is less clear. Some experiments suggest that hydrogen is a negative U defect, so that H^0 would be metastable and not ordinarily observed.[25] A diffusion coefficient has also been reported for H^-.[23] Both the negative U character of hydrogen and the ability to produce H^- with the methods that were reported have been contested.[21,25]

B. Solubility

The solubility of hydrogen in Si at elevated temperatures has been determined in a few different sets of experiments, all of which give results that are in reasonable agreement in the temperature range where they were measured. The earliest work is that of Van Wieringen and Warmoltz.[9] In these experiments, discussed also in the section above, the permeation of hydrogen through thin-walled Si cylinders was studied for the temperature range 1090°C to 1200°C. Data for the solubility, S_H, at one atmosphere pressure are shown in Fig. 2. (VWW originally reported results for H_2 molecules/cm^3, so their data have been multiplied by a factor of 2 to give atoms/cm^3.) A least squares fit to these data was performed recently by Herring

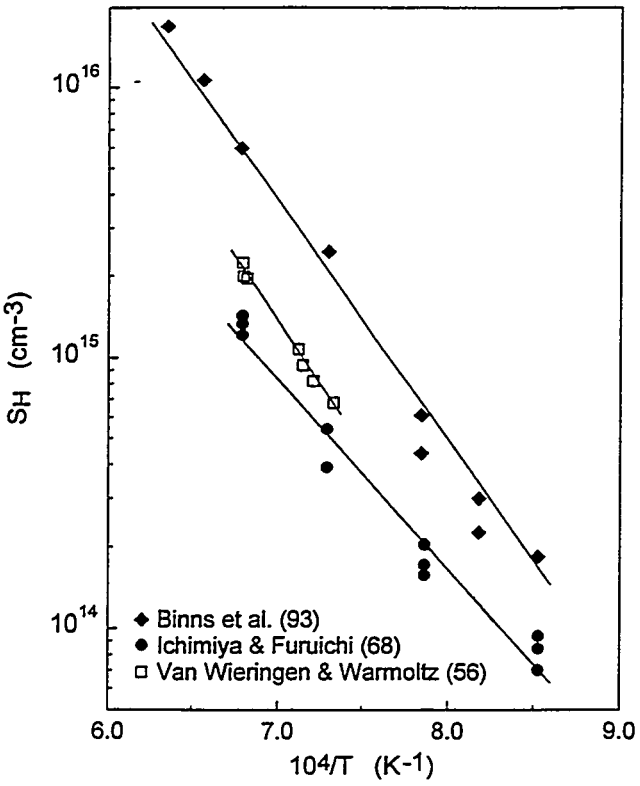

Fig. 2. Solubility of hydrogen in Si.

and Johnson [7] who give the following relationship for the solubility:

$$S_H = 4.96 \times 10^{21} \exp(-1.86 \text{ eV} / kT) \text{ atoms/cm}^3. \quad (2)$$

This fit to the data of ref. [9] is also shown in Fig. 2.

Ichimiya and Furuichi [10] performed experiments in which the radioactive beta decay of tritium (^{3}H) was used to determine its concentration in Si slabs following heat treatments in tritium gas in the range 900°C to 1200°C. Data for the solubility of ^{3}H determined in these experiments are shown in Fig. 2. The least squares fit to these data performed by Herring and Johnson [7] give the following relationship which is also shown in Fig. 2:

$$S_H = 6.61 \times 10^{19} \exp(-1.39 \text{ eV} / kT) \text{ atoms/cm}^3. \quad (3)$$

Recently, two groups [36, 37] have reported that acceptor-H complexes in Si can be formed by annealing bulk Si in H_2 gas at elevated temperature and then rapidly quenching to room temperature. Binns *et al.* [38, 39] have used this method to determine S_H. In these experiments, boron-doped silicon ($N_A = 10^{17}$ cm^{-3}) was annealed in H_2 gas and then quenched to room temperature. A calibration of the hydrogen-stretching infrared absorption band at 1903 cm^{-1} assigned to B-H was established so that the concentration of B-H complexes could be determined from the area of the vibrational absorption band. It was also found in these experiments that a large fraction of the hydrogen introduced by the high temperature treatment gave rise to a hydrogen defect that is not infrared active.[40] This hydrogen was found to react with boron during a subsequent anneal at 175°C, increasing the concentration of B-H complexes by as much as a factor of three. Binns *et al.* [38,39] have also shown with SIMS

measurements that the concentration of B-H complexes following the anneal at 175°C accurately reflects the total concentration of hydrogen that was introduced into the sample at high temperature. Data for [B-H] following a high temperature anneal in H_2 gas at various temperatures between 900°C and 1300°C, a quench to room temperature, and a subsequent 175°C anneal, are shown in Fig. 2. The relationship for the solubility determined from these data is given by the following and is also shown in Fig. 2:

$$S_H = 9.1 \times 10^{21} \exp(-1.8 \text{ eV} / kT) \text{ atoms/cm}^3. \quad (4)$$

This result is in good agreement with the early result of VWW [9], Eq. (5), over a wide range of temperatures.

Extrapolations of the results above to 500K give the results $S_H = 9 \times 10^2$ cm^{-3} from Eq. (2), $S_H = 6 \times 10^5$ cm^{-3} from Eq. (3), and $S_H = 7 \times 10^3$ cm^{-3} from Eq. (4). While the results of these extrapolations vary by roughly three decades, it is clear that they all predict that the solubility of isolated H is extremely small at the temperatures where hydrogen is introduced during typical hydrogen plasma exposures and most other introduction methods. Thus the high concentration of hydrogen that can be introduced into Si at, say, near 500K is explained by the formation of hydrogen molecules [11], other hydrogen-containing aggregates such as platelet defects [41], and hydrogen-impurity complexes.

C. Shape of hydrogen profiles

The complexity of the incorporation of hydrogen into Si is shown by a comparison of the solubility of isolated hydrogen and the atomic profiles of the hydrogen that is actually present in the material following exposure to a hydrogen-containing plasma (Fig 4, from ref. [42]). (Deuterium, or ^{2}H, is usually introduced into Si for the measurement of hydrogen depth profiles by SIMS because of its much lower background concentration.) For the typical hydrogen introduction temperatures used during a hydrogen-plasma exposure (T<300°C) the concentration of hydrogen is many orders of magnitude greater than given by the solubility of isolated H. Further, the effective diffusion coefficient, estimated from $D_{eff} = d^2/t$, where d is the indiffusion depth and t is the duration of the hydrogen-plasma exposure, is ~three orders of magnitude smaller that the diffusion coefficient determined by Van Wieringen and Warmoltz, Eq. (1).[9] For example, an indiffusion depth of ~2 μm for a plasma exposure of 30 min at 150°C corresponds to $D_{eff} = 2 \times 10^{-11}$ cm^2/s. This value can be compared to the VWW result for the diffusion coefficient, $D = 1.8 \times 10^{-8}$ cm^2/s, calculated with Eq. (1) at 150°C, which would correspond to an indiffusion depth of 57 μm in 30 min. Several groups have proposed models to explain the shapes of the indiffusion profiles.[43-47] The basic idea is that at low temperatures, and for the large hydrogen concentrations that are typical of most introduction methods, the diffusion of hydrogen is limited by trapping, either by the formation of less mobile hydrogen aggregates (molecules or platelet defects) or by trapping at impurity sites. Here the qualitative shapes of the profiles are discussed. More detailed treatments can be found in the work of Borenstein *et al.* [47] and in several reviews of hydrogen diffusion in Si.[5-8]

Near the surface (<0.2μm) of an n- or p-type Si sample that has been exposed to a hydrogen plasma, the large peak in the hydrogen concentration is explained by the formation of hydrogen-induced platelet defects.[41] A platelet defect is a microcrack that is stabilized by hydrogen and typically contains hundreds of H atoms.

For undoped or lightly doped Si (resistivities > 10Ω-cm), the indiffusion of hydrogen, for depths greater than 0.2 μm, is believed to be limited by the formation of immobile H_2 molecules. A model for the diffusion of hydrogen that is limited by the formation of H_2

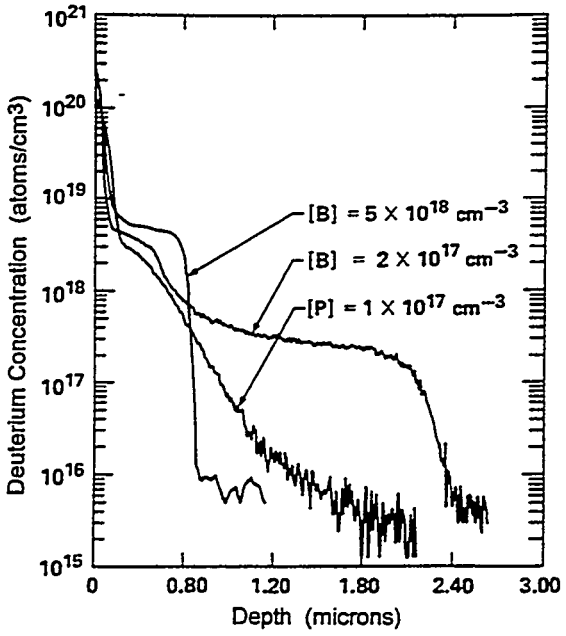

Fig. 3. Deuterium depth profiles measured by SIMS for crystalline Si that had been exposed to a deuterium plasma for 30 min at 150°C. (From ref. [42]).

molecules was first proposed by Hall [11] and further developed and applied by others.[5-8, 43,47] In this case, the effective diffusion coefficient for hydrogen depends strongly on the hydrogen concentration.

In n- or p-type Si with lower resistivity, the indiffusion of H is limited by trapping by the dopant impurities.[5-8, 18] Models for the diffusion of hydrogen into p-type Si have been developed further and will be discussed first. For the sample with [B] = $5x10^{18}$ cm^{-3} in Fig. 4, there is a plateau in the hydrogen concentration at the acceptor concentration. In this regime where the acceptor concentration is high and the temperature is low, the indiffusion of H is limited by trapping by the acceptors and the H concentration closely follows the acceptor concentration.[6,7,47] More lightly doped p-type material ([B] = $2x10^{17}$ cm^{-3}) also shows a plateau that extends ~2 μm into the sample with the hydrogen concentration mimicking the acceptor concentration. However, there is an additional plateau closer to the surface where the hydrogen concentration exceeds the dopant concentration by a factor of ~10. The height of this plateau also depends on the dopant concentration. Thus, it has been proposed by Borenstein *et al.* [47] that the p-type dopants can trap several hydrogen atoms and the near surface plateau has been fit by a multiple-trapping model in which each acceptor atom traps ~10 hydrogen atoms. Theoretical calculations also suggest that dopants can stably trap more than one H atom [48], although there is no spectroscopic evidence for hydrogenated acceptors with more than one bound H atom.

Model for the hydrogen profiles observed for n-type Si are not as well-developed. An excellent review of the complexity of the indiffusion of hydrogen into n-type Si has been given by Herring and Johnson.[7] For the profile shown in Fig. 4, for depths greater than the surface peak associated with platelets, the hydrogen concentration initially exceeds the n-type dopant concentration by more than a factor of 10 and then, deeper in the sample (>1.2 μm), drops to the ^2H detection limit. Plateaus are not typically observed in the hydrogen depth profiles for n-type samples. There has not been general agreement about even what the important hydrogen defects are in n-type Si. The role of H^- and its diffusion coefficient remain controversial.[21,22-25] A di-hydrogen complex called H_2^*, with one H atom at a bond-centered site and a second H atom at an antibonding site (see Sec III.B below) has been

found to be a more mobile species than molecular H_2 in theoretical calculations [49,50], and has been suggested to be a possible configuration for the hydrogen that is present in excess of the donor concentration in n-type Si.[7,49,50] The possibility that there may be multiple trapping of H by donor impurities has some theoretical [48] and experimental support.[51]

II. Transition-metal-hydrogen complexes.

Hydrogen-passivated shallow impurities in semiconductors have been studied extensively in recent years and much progress has been made toward understanding the structures and properties of these defect complexes.[1-5] The hydrogen passivation of deep-level impurities [53,54] has remained poorly understood because, in part, the application of structure-sensitive spectroscopic techniques has not been possible. For example, in pioneering studies of deep level passivation, the deep level transient spectroscopy (DLTS) features of deep level defects were shown to disappear following exposure to a hydrogen plasma.[53-56] Both the absence of electronic levels and the very small total number of defects that are in the very thin layers that are typical of plasma-passivated samples make most probes of defect properties difficult to apply. In the following sections, the application of structure-sensitive methods to transition-metal-hydrogen complexes and the observation that many hydrogenated transition metal impurities remain electrically active will be discussed.

A. Structure-Sensitive Spectroscopy

There have been a few cases where hydrogen has been introduced into *bulk* samples, either during crystal growth or by annealing in H_2 at elevated temperature. For example, it was noted in Sec. I.B above that shallow acceptors in Si can be passivated by annealing in H_2 at high temperature and quenching to room temperature.[36,37] Recently, the introduction of hydrogen into *bulk* Si has permitted samples to be fabricated with a sufficient number of hydrogenated transition metal impurities to be studied by EPR [57-59] and infrared (IR) absorption [57,59,60] spectroscopies.

A PtH_2 center has been identified by EPR [57,58] and the hydrogen vibrations of this defect have been assigned.[57,59] For the paramagnetic charge state of PtH_2, EPR [57,58] shows that the defect has orthorhombic (C_{2v}) symmetry. Hyperfine splittings of the EPR lines show that the defect contains a single Pt atom and two equivalent H atoms. These data are consistent with a structure proposed by Jones *et al.* [61] that is shown in Fig. 4(a). The PtH_2 center is only paramagnetic when the Fermi level is below $\sim E_c$ - 0.1 eV, showing that the defect has a level at this position.[57] Two hydrogen stretching modes have been observed near 1900 cm^{-1} for the paramagnetic charge state by IR absorption spectroscopy and have been assigned to the symmetric and antisymmetric stretching modes of the two H atoms.[59] Hydrogen stretching modes have also been observed for two nonparamagnetic charge states of PtH_2 [59] (that cannot be seen by EPR) and are consistent with there being two levels in the gap, one near $\sim E_c$ - 0.1 eV as was found by EPR and another near mid-gap.

In addition to the PtH_2 defect, the hydrogen stretching modes associated with two charge states of a Pt-H defect have also been observed in the same samples.[59,60] No EPR spectrum has been found for the Pt-H center, even though one of the charge states should be paramagnetic. Uniaxial stress studies of the vibrational lines are consistent with trigonal symmetry for the defect. The proposed structure of the Pt-H defect is shown in Fig. 4(b).

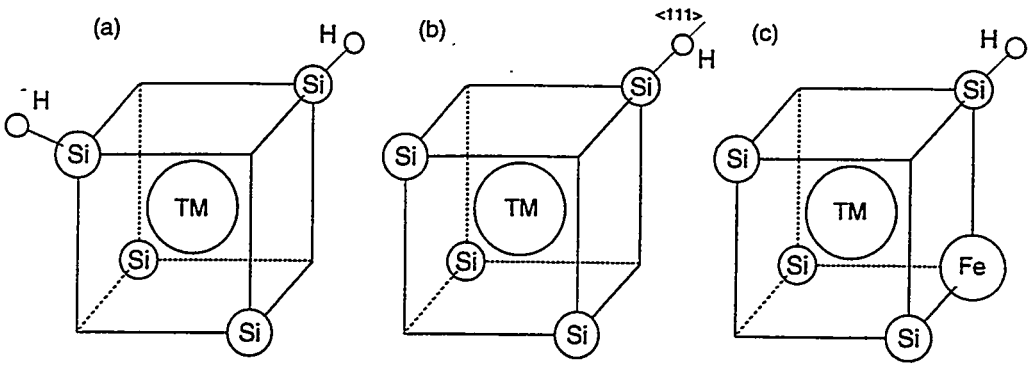

Fig. 4. Proposed configurations for hydrogenated transition-metal (TM) impurities in Si.

Similar experiments have been performed for Si that contains Au and H.[60] Three different Au and H containing centers have been identified in n-type Si by vibrational spectroscopy. Similar to the case of Pt-doped Si, vibrational modes have been identified near 1800 cm^{-1} for Au-H_2 and Au-H defects. The results of uniaxial stress studies [60,62] are consistent with orthorhombic [Fig. 4(a)] and trigonal [Fig. 4(b)] symmetries, respectively. An additional center with hydrogen vibrational modes similar to those of Au-H, but shifted slightly (~5 cm^{-1}) to higher frequency, is seen in some Si samples. Stress studies are consistent with a defect that has C_{1h} symmetry. This center has tentatively been assigned to a Au-Fe pair, complexed with a single H atom [Fig 4(c)].[62]

Little is known about the positions of the electrical levels associated with any of the above defects. Only the position of the level at ~E_c - 0.1 eV for the Pt-H_2 defect found by EPR [57] is known with any certainty.

B. Electrical Level Positions from DLTS studies

It is known that wet-chemical etching introduces hydrogen into Si.[1,2,63,64] This method has been used to hydrogenate transition-metal impurities in the first few micrometers of the surface of Si samples.[65-73] A Schottky contact was then deposited so that the hydrogenation of the metal impurities could be studied by C-V profiling and DLTS. The surprising result is that the introduction of hydrogen does not necessarily passivate the transition metals, but that electrically-active defects are created. It is important to note that if a Si sample is etched prior to the fabrication of a Schottky contact, hydrogen will be introduced.

Figs. 5 and 6 show typical results for transition-metal impurities that have been hydrogenated by etching from the work of Sachse *et al.*[72,73] The n-type Si samples used were doped with phosphorus, and Pt was introduced during crystal growth. Fig. 5(a) shows the P doping profiles measured by C-V profiling of Schottky barrier diodes fabricated on a cleaved sample (hydrogen free) and a sample that had been etched in an $HF:HNO_3:CH_3OOH$ (1:2:1) solution. The profiles show that etching passivates P near the surface. An additional anneal of 30 min at 400 K drives the hydrogen further into the sample and increases the depth of the P passivation. DLTS spectra for a cleaved sample and an etched sample are shown in Fig. 6. The cleaved sample shows only the isolated Pt-acceptor DLTS peak whereas the etched sample shows a reduced isolated Pt peak and two new DLTS peaks that have been assigned to complexes that contain Pt and H. Annealing at 650 K dissociated the Pt-H_n complexes and restored the Pt concentration. Profiles of the isolated Pt and Pt-H_n peaks [Fig. 5(b)] show that the new Pt-H_n peaks arise from a surface layer where the isolated Pt

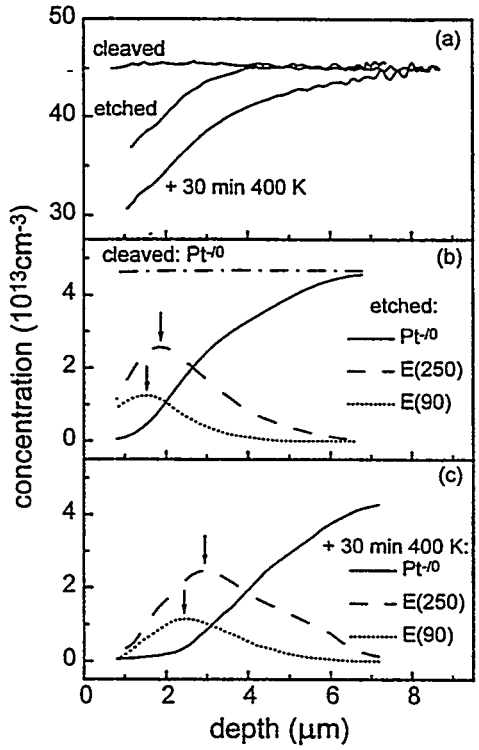

Fig. 5. Depth profiles determined from C-V data (a) and by DLTS (b) for n-type Si into which Pt had been introduced during growth. Hydrogen was introduced by wet-chemical etching prior to the deposition of a Schottky contact. The profiles in (c) were measured following an additional anneal (400K for 30 min.). From ref. [72].

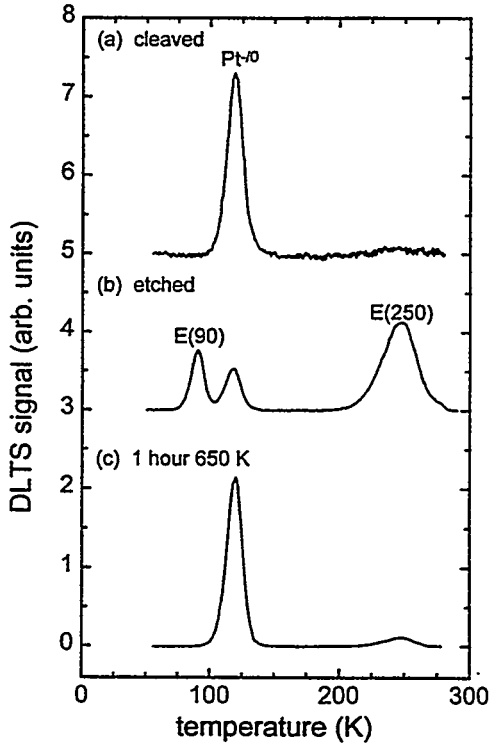

Fig. 6. DLTS spectra for n-type Si that contained Pt and H. From ref. [72].

concentration is reduced. The effect of an additional 400K anneal [Fig. 5(c)] is to reduce the isolated Pt concentration at greater depth and also to push the peaks in the concentration profiles of the Pt-H_n centers deeper into the sample. The ability to shift the profiles by low-temperature annealing strongly supports the assignment of the new DLTS peaks to Pt that is complexed with hydrogen that has been indiffused.

Similar studies have been performed for n- and p-type Si that contained various transition metal impurities.[65-73] A list of new levels that have been assigned to transition-metal-hydrogen complexes is given in Table I. While DLTS allows the electrical properties of the transition-metal-hydrogen complexes to be studied, little is known about the structures of these defects.

Table I. List of deep levels and their energies observed by DLTS in n- or p-type Si that contained the transition metal impurity that is indicated and hydrogen.

metal	type	label	energy level (meV)	ref.
Au	p	G2	E_v + 210	67
Au	p	G3	E_v + 350	67
Au	n	G1	E_c - 190	67
Au	n	G4	E_c - 560	67
Co	p	H(50)	E_v + 90	69
Co	p	H(90)	E_v + 170	69
Co	p	H(150)	E_v + 220	69
Co	n	E(60)	E_c - 60	70
Co	n	E(90)	E_c - 170	70
Co	n	E(120)	E_c - 220	70
Co	n	E(140)	E_c - 260	70
Co	n	E(175)	E_c - 390	70
Co	n	E(200)	E_c - 400	70
Ti	n	E(170)	E_c - 310	71
Ti	n	E(260)	E_c - 570	71
Pt	p	H(150)	E_v + 300	73
Pt	p	H(210)	E_v + 400	73
Pt	n	E(90)	E_c - 180	73
Pt	n	E(250)	E_c - 500	73

III. Di-hydrogen complexes, H_2 and H_2^*

Isolated hydrogen in semiconductors is mobile at low temperatures (for example, near 200 K in Si [19,74]) so at room temperature, H in semiconductors is bonded to other defects or present in the form of H_n aggregates. The smallest H_n aggregates involve just two hydrogen atoms. Two possible di-hydrogen defects have been considered theoretically and may play an important role during hydrogen indiffusion, as was discussed in Sec. I.C above. However, di-hydrogen defects were not observed spectroscopically so their structures might be confirmed until recently. The first is the hydrogen molecule, H_2, that has been predicted to lie at a tetrahedral interstitial site in Si [30,50,75]. Molecular hydrogen is believed to be a slow diffusing species in Si and has often been invoked as the product of reactions that release hydrogen from other defect complexes. The second is a species that has been named H_2^* [49,50,76]. The direct observation of H_2 and H_2^* has the potential to allow the role of these defects in indiffusion processes and defect reactions to be elucidated and will be discussed below.

A. H_2 in Si

The stretching vibration of an H_2 molecule does not give rise to an oscillating dipole moment and is therefore infrared inactive. However, Raman spectroscopy can be used to study the stretching vibration of an H_2 molecule. In a recent study, the Raman spectrum of H_2 in Si has been discovered.[77]

Exposure of a Si sample to a hydrogen plasma at a temperature below 250 °C gives rise to extended platelet defects.[41] For higher plasma exposure temperatures, platelet formation is suppressed and hydrogen is incorporated in a form that has been difficult to probe spectroscopically. In a recent Raman study, a broad vibrational band was observed at 4158 cm^{-1} at room temperature for Si samples treated in a hydrogen plasma at 400 °C.[77] When Si samples were exposed to a deuterium plasma, a band at 2990 cm^{-1} was observed. These vibrational frequencies are close to those observed previously for H_2 and D_2 in gas, liquid and solid phases, and led to the assignment of the 4158 and 2990 cm^{-1} bands to molecular H_2 and D_2 in Si. The direct observation of H_2 in Si that has been subjected to a hydrogen plasma exposure confirms the long standing hypothesis that molecular hydrogen is an important, and often present, species in semiconductors.[1-8,11]

B. H_2* in Si

An alternative configuration for a di-hydrogen defect named H_2* has been examined in several theoretical calculations.[49,50,75,78] The H_2* defect in Si has been predicted to consist of one hydrogen atom at a bond-centered site between two Si neighbors and a second hydrogen atom bonded to one of these Si neighbors at an antibonding site (Fig. 7).

It has been known since 1975 that implanting protons into Si gives rise to numerous hydrogen-related vibrational absorption bands.[79] Recently, several of these bands have been assigned to the H_2* defect.[80] From a comparison of the experimental frequencies to a theoretical calculation for H_2*, the vibrational bands at 2062 and 1838 cm^{-1} have been assigned to the stretching modes of hydrogen atoms at the bond-centered and antibonding sites, respectively. The line at 817 cm^{-1} has been assigned to the wagging mode of the hydrogen atom at the antibonding site and the 1599 cm^{-1} band has been assigned to be the overtone of the 817 cm^{-1} mode. H_2* has been proposed as a possible configuration for hydrogen in Si that might diffuse more quickly that H_2.[7,49,50] At present, the existence of H_2* in Si that has been subjected to hydrogen plasma exposure or evidence for its mobility have not been established.

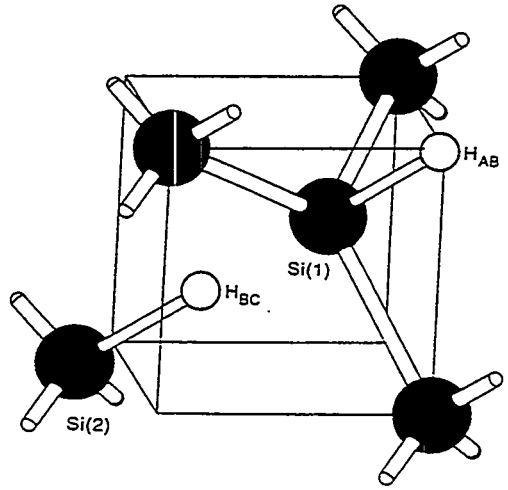

Fig. 7. Configuration of H_2 in Si. From ref. [80].*

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Solar Cell Passivation and Selective-Emitter Processes

Ronald A. Sinton
Sinton Consulting
San Jose, CA

Introduction

The benefit of surface passivation for improving silicon solar cell efficiencies has been clearly demonstrated. Passivated front emitters improve both the voltage and the blue response of the solar cell, giving a promising path towards high-efficiency production cells. These benefits have been characterized for a number of passivation techniques. Representative papers show these benefits for a number of passivation techniques including furnace oxidations (1), PECVD coatings (2), and rapid thermal oxidations (3).

In general, to obtain the greatest benefit from surface passivation, the doping levels in the emitter must be reduced, resulting in potentially-poor contact resistance for screen-printed lines and a necessity for dense gridlines to preserve a low emitter resistance. These drawbacks have hindered the adoption of surface-passivation technology into industrial process lines.

The enabling technology that will allow the use of surface passivation on production solar cells will be cost-effective selective emitters matched with dense, high-aspect-ratio metalizations. This need has driven a creative proliferation of potential and demonstrated techniques for forming selective emitters. A list includes buried-contacts, emitter etch-back techniques, laser-drawn heavy-dopant diffusions, shadow-masked RTA, and the use of patterned doping sources. Each results in the desired heavy doping under the metalization with lightly-doped emitters elsewhere.

Although the primary goal of these processes is to reap the benefits of surface passivation, each sequence also has implications central to the implementation of bulk gettering and hydrogen passivation. For example, the emitter etch-back schemes nicely incorporate P-gettering into the process due to the heavy initial phosphorus diffusion. In contrast, the patterned dopant source and buried-contact techniques may realize less gettering benefit. The costs and benefits of each sequence will therefore vary depending on substrate type and the integration into the full fabrication process.

Selective Emitters by Etch-Back

A number of techniques can be classified as etch-back emitters. The common element is that a deep phosphorus diffusion (typically 16 Ohm/sq) is done early in the process.

The metal gridlines will contact this diffusion, permitting excellent contact resistance. At some point in the process, the emitter between gridlines is etched back to a higher sheet resistance and is subsequently passivated.

In an IMEC process, after the P-diffusion, the wafer is textured using a printed polymeric mask to protect the regions that will have gridlines. This etch eliminates the dopant entirely between gridlines, so that a second lighter dopant diffusion is required. Subsequent processing aligns the screen-printed lines to the heavily-doped mesa regions(4).

Sandia National Laboratories etches the P-diffusion in a controlled manner, to leave a shallower diffusion of 80-100 Ohms/sq between the gridlines. By using a plasma etch, they are able to use the screen-printed metalization as a self-aligned etch mask. They propose that hydrogen passivation and PECVD-nitride AR coating deposition could be performed in the same plasma process tool(5).

A very persuasive demonstration of the potential for selective emitters was the R&S/ECN collaboration that produced a 15.7% module. The fabrication process used screen-print technology and a masked etch-back of the phosphorus-emitter in a nitric-acid solution(6).

The IMEC and the R&S/ECN processes are compared in Table 1. The Sandia process was presented as a module, dropped into the standard (unknown) process sequences of several solar cell manufacturers.

Table 1.	IMEC process	R&S/ECN process
	Saw-damage etch/Clean	Saw-damage/texture etch
	Deep P-diffusion	P-Diffusion
		Print backside Al
		Fire AL
		HCl etch
		Edge isolation
		Anneal
	Print mask	Print mask
	etch-back/texture	Controlled Nitric-solution etch back
	Clean/ Mask removal	Clean/ Mask removal
	Shallow P diffusion	
	Clean	
	Oxidation	
	ARC (TiO2)	PECVD nitride/hydrogenation
	Print metal	Print metal
	Firing	Firing

Buried-contact solar cells.

One selective-emitter process in wide-scale production is the Buried-Contact solar cell, originally developed at the University of New South Wales. This solar cell process integrates a selective emitter process with a high-aspect-ratio grid, and is a sophisticated design that has achieved 17-19% limited-production cells using float-zone material. Recent developments in this technology indicate that the selective-emitters designed for these high-efficiency float-zone cells may be unnecessary for use with multicrystalline or CZ material(7). In this case, a good compromise between a heavily-doped emitter for contact resistance and a lightly-doped emitter for good blue response and voltage can be found, because the contact-resistance of plated contacts is better than for printed metalization. A sheet resistance in the range of 80-140 Ohms/sq was found to limit voltages to 648 mV on good material, higher than the limit placed by a typical base material. These sheet resistances are known to give nearly perfect blue response as well for passivated emitters(8). The fabrication sequence for these cells is:

-Groove formation
-Clean/Etch/Texture
-P-diffusion
-Rear metal and fire
-AR coating (TiO_2 spraying)
-Electroless plating
-Edge isolation

So unlike the screen-printed technologies, it is quite possible that selective emitters are not necessary for the most cost-effective implementation of buried-contact cells. This is primarily possible due to better contact resistances of plated metalizations compared to screen-printed lines.

Several other techniques for fabricating selective emitters are at a earlier stage of development. These are described below.

Laser- or RTA-formed selective emitters

An interesting combination of RTA with laser scanning can be used to realize selective emitters. An optimized situation has been described.

-Spin-on phosphorus-doped glass
-RTA (850 °C)
-Laser scan lines, using
    -doubled YAG
    -5 kHz

-0-2 mm/second scan rate
- -1-4 J/cm^2 power density in pulse

Within this parameter space, the laser writes heavily-doped lines at 10-50 Ohms/sq(9).

With the use of a quartz shadow mask, selective emitters have also been accomplished using RTA without the laser writing. In this scheme, the area under the shadow mask gets less energy and a different spectrum of light. The result is that the region under the shadow mask has the same junction depth, but a lower surface concentration. For lower RTA temperatures, differences from 60-150 Ohm/sq were seen between the unshadowed and shadowed areas. At higher temperatures, the differences are less, ranging from 30 to 40 Ohm/sq(10).

Selective Emitters by Auto-doping

A new, very elegant process was proposed at the recent 1997 European Community Photovoltaic Solar Energy Conference. This scheme requires no additional steps beyond a traditional screen-print process. The difference is that the dopant source is screen-printed onto the cell only where the grids will be. Then, during the dopant diffusion step, the regions under the printed paste receive a high doping concentration. Between these lines, the wafer is auto-doped from vapor-phase phosphorus coming from the paste(11).

In an initial study, 10 by 10 cm CZ substrates were processed with the schedule shown in Table 2. Results included cells with J_{sc} of 34.0 mA/cm^2, V_{oc} of 612 mV, FF of 77% and efficiency of 16.1%. Better results are anticipated from additional optimizations of this process.

Table 2.

IMEC process II

Texture/Clean
Print Phosphorus lines
Diffusion
Clean
Dry oxidation
SiN or TiO_2
Aligned screen printing
Co-Firing

Conclusions.

It has been clear for some time that selective emitters with good passivation would improve the efficiencies of commercial solar cells. These techniques have not been widely adopted because the additional efficiency did not justify the additional cost of implementation. Recent work has become quite innovative, with a number of proposed solutions to this problem under active development. The success of one or more of these strategies will allow the application of the extensive R&D knowledge on surface passivations to influence commercial solar cell efficiencies. The proposed selective-emitter fabrication schemes differ in their compatibility with optimized gettering schedules, such that different solutions may be appropriate for each substrate type.

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A Summary of the NREL Silicon Materials Research Program

Bhushan Sopori

National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

The last NREL competitive program in Silicon Materials Research has just been completed, and a new 3-year program is about to begin. The last program was instituted nearly 5 years ago with the objective of performing research that would lead to technologies that can significantly improve the cell efficiencies and lead to a reduction in the solar cell cost. The status of silicon solar cells at that time was the following:

- Commercial solar cell efficiencies were about 12%, while laboratory small-area cells had yielded devices of about 16% efficiency.
- It was just recognized that phosphorus diffusions, used for junction formation, produced improvement in the minority carrier diffusion length in some PV materials. However, any reasonable knowledge of gettering resided primarily in the microelectronics community.
- Hydrogen passivation (done by ion implantation from the junction side) was known to improve the performance of some solar cells.
  - H was thought to diffuse through the grain boundaries (and perhaps through dislocations).
- It was observed that many process steps led to improvement in the minority carrier lifetime (diffusion length) – how and why was not known!
- Techniques for material or process control or interlaboratory correlation between the measurement techniques did not exist.
- Each process step was aimed at performing a single function.

It was recognized that improvements in the quality of the material produced by various vendors would be process-specific, and that any new technology for the crystal growth would require a significantly heavy financial investment – an option not available at that time. It was clear that, under a severely curtailed budget for a basic research program in Si, the research emphasis of the program should shift from analysis of the material growth to developing methods for post-growth quality enhancement. Thus, it was concluded that the research emphasis should be towards basic understanding of the effects of impurities and the role of defects in solar cell processing. The direction of the research was decided at the First Workshop on the Role of Point Defects in Silicon Device Processing.

The last program included seven subcontractors and sought interactions between subcontractors, industry, NREL, and Sandia. Table 1 lists the subcontractors, subcontract title, and the PI(s).

Contract #	Title	Subcontractor Name
XD-2-11004-1	Influence of Self-Interstitials by Phosphorus Diffusion on Defect Structures and Electronic Properties in Crystalline Silicon	Duke University
XD-2-11004-2	Fundamental Research on Post-Growth Quality Enhancement Techniques	Georgia Institute of Technology
XD-2-11004-3	Identification and Control of Lifetime-Reducing Defects in Polycrystalline Silicon Photovoltaic Materials	UC Berkeley
XD-2-11004-4	The Role of Point Defects and Impurities in the Processing Performance of Silicon Solar Cells	Massachusetts Inst. of Tech.
XD-2-11004-5	Optimization of Gettering Processes for Photovoltaic Silicon	Univ. South Florida
XD-2-11004-6	Detailed Non-Contact Electrical and Structural Characterization of Photovoltaic Silicon Substrates	North Carolina State Univ
RAX-5-15230	Theoretical Analysis of Hydrogen-Vacancy -Impurity Formation and Dissociation	Texas Tech Univ.

Table 1. List of the Subcontractors under the Silicon Materials Research Program

The objectives of the program were to:

- Perform basic research that would lead to technologies suitable for
  - significantly higher cell efficiencies
  - reduction in solar cell costs.
- Disseminate research results and assist in the transition of these technologies into production.
- Increase interaction with the silicon community.

The approach was to:

- Perform detailed characterization of various PV substrates and cells to develop a data base of impurities, defects, and uniformity
  - include development of suitable characterization and process monitoring techniques.
- Identify cell performance limiting defects and the associated electronic mechanisms.
- Perform modeling/analyses to determine how these limitations can be overcome by suitable processing.
- Develop a detailed knowledge-base for impurity gettering and defect passivation as post-growth quality enhancement processes
  - "import" knowledge from the microelectronics industry.
- Attempt to integrate quality enhancement steps into cell processing to ensure minimum cell

fabrication cost.

The subcontract program was supported by the internal research both at NREL and Sandia, and interacted strongly with the PV industry.

Highlights of the Program

Some critical developments in the approaches for post-growth quality enhancement have occurred through this program.

Defects/Impurities

Many commercially available materials were analyzed to identify impurities and the types of defects and their distributions. Development of PVSCAN5000 played a key role in this effort because it allowed acquisition of a substantial amount of information in a relatively short period of time. This effort was further complemented by the SPV facility at the USF and the development of Laser Microwave PCD technique at NCSU.

- The dominant defects are intragrain dislocations.
- Dislocations form extended loops and networks.
- The dominant impurities are C, O, Fe, and Cr.
- Under the CRADA with Crystal Systems, it was observed that a decrease in the average dislocation density was accompanied by formation of defect clusters. Similar aggregation of defects was observed in all multicrystalline PV silicon substrates.
- Zero-D grains have micro-defects. The exact nature of the micro-defects is not known, but it is believed to be related to oxygen or carbon precipitates, or frozen-in point defect clusters. These results emerged out of the work at UC Berkeley through diffusion and gettering of Fe into a variety of substrate materials. It was observed that precipitation of indiffused Fe occurred at the micro-defects.

Impurity Gettering

Impurity gettering received the major attention under the program. Cl, P, and Al gettering techniques all led to improvements in the average material quality of PV substrates. However, P indiffusion, Al alloying, and the combination of the two were studied in more detail because they are normally used in solar cell processing.

- Phosphorus diffusion, Al alloying, and TCA treatment all work well as gettering processes in IC grade or low defected material.
- High temperature gettering can degrade the material quality of PV substrates and cells (GIT, USF). It was proposed that this effect could arise from dissolution of impurities precipitated at the defect sites (NREL, Duke, USF). This mechanism suggested that dissolution of precipitates could be performed by a rapid high temperature process, such as an RTA, followed by gettering. Solar cell fabrication using RTA is being pursued at GIT.
- Optical Processing (NREL) and RTA (USF, MIT) was used to perform effective gettering of transition metals from Si at significantly lower temperatures (<700 °C).

- Gettering of transition metals during heat treatment leads to internal precipitation at defects, as well as the desired outdiffusion (MIT).
- Defect clusters cannot be gettered (or passivated). These results emerged out of work from NREL and USF. Detailed, high resolution mapping of the minority carrier diffusion length, internal LBIC responses, and defect mapping performed on gettered and ungettered ("sister") cells showed that improvements in the defect cluster regions was small or none. Network modeling (NREL) established that the localized regions of high dislocation density (defect clusters) can shunt the device. The defect clusters can act as current "sinks" that dissipate the power within the cell and thus can be very detrimental to the cell performance.
- A diffusion segregation model was developed at Duke University, the results of which are in excellent agreement with the experiments done at UCB. This theory helps in understanding the conditions needed for dissolving precipitates that appear to be the bottlenecks in im proving the overall cell performance by gettering.

Hydrogen Diffusion/Passivation

Investigations into hydrogen passivation included (i) theoretical studies (at Texas Tech Univ.) aimed at a number of fundamental questions at the microscopic level to address diffusion in various Si materials, nature of defects that benefit from passivation, passivation processes, interaction between hydrogen and oxygen, and interactions between H and selected transition metals, (ii) experimental studies (at NREL) to measure H diffusion characteristics in different Si materials, and to integrate observations from solar cell passivation into a coherent phenomenological model that can be useful to device process engineers, and (iii) incorporating these results into cell processing (GIT) and evaluating their validity.

- Calculations done at near the ab-initio, Hartree-Fock level in molecular clusters, and molecular dynamic (MD) calculations have yielded the following results: it is known that the "normal" diffusion of H^0 or H^+ occurs by hopping from bond center (BC) to BC sites with an activation energy of 0.5 eV. However, MD simulations show that a metastable state of H^0 results in much faster hopping among tetrahydral (T) sites without involving BC sites. Further, a (V-H) pair appears to be mobile.

The main results from the experimental work (NREL) are:

- Hydrogen diffusion at low temperatures occurs predominantly via a [V-H] complex.
- The diffusivity of H in Si can vary in materials grown by different vendors by several orders of magnitude.
- Hydrogen induced defects can act as very efficient gettering sites.
- Backside hydrogenation can be used in solar cells to prevent damage to the junction.

Solar Cell Fabrication

Solar cell fabrication, using the concepts developed under this program, was performed at GIT and Sandia laboratories. A great deal of support was provided by the PV industry, in terms of providing appropriate samples, cell fabrication, and in many cases handling samples that do not satisfy production specifications. The primary objective of the cell fabrication was to be able to quantify the effects of various processes. Some of the results are:

- Al gettering and Al-BSF formation reduces the back surface recombination velocity (BSRV) to 200-400 cm/s and improves the bulk lifetime, τ_b, of lower quality Si.
- The conditions for optimum gettering for different commercial PV materials were found to be different.
- PECVD nitridation, for depositing an AR coating, can produce passivation with a significant increase in τ_b. The optical constants of the optimum nitride were determined, and a neural network modeling was performed to correlate deposition parameters and properties of SiN. Higher temperature increases Q_{ox} and surface passivation while lower temperature produces richer H content; these features are used in the NREL's hydrogen diffusion model.
- Forming gas anneal produces passivation in some cells.
- In high quality materials like HEM, P gettering alone gives higher lifetime than Al gettering and Al-P co-gettering. It is important to point out that the results of the gettering model from Duke University suggest that cogettering with P and Al would enhance the gettering efficiency. Thus, there appears to be a disagreement. Further work is needed to address this discrepancy.

Solar cells, processed with implementation of these processes, yielded record 18.6% efficiency cells on HEM material, 16% on EFG, 17.2% on Dendritic Web, and 15% on String Ribbon.

Cleaning Chemistry (MIT)

Although solar cell processing is not done under a rigor comparable to microelectronic device processing, there is an increasing need to maintain cleanliness during processing. As the cell efficiencies increase, the need to minimize contamination is also growing. This is particularly important if the substrate already has a high concentration of metallic impurities. Because extrinsic gettering by P diffusion and Al alloying used in solar cell fabrication have to meet other functions of a junction and a contact respectively, the gettering region can get saturated if the bulk concentration of impurities is high. Thus, further indiffusion of impurities must be prevented. Such contamination can occur not only from high temperature processing but also from steps such as cleaning. This contamination issue was investigated at MIT through the use of PCD lifetime measurements and studying the kinetics of cleaning solutions.

- Developed contactless PCD technique for HF immersion and (I_2 + Methanol) immersion capabilities
  - measured both the bulk lifetime and the surface recombination velocity, injection level, surface band-bending, and the competition between surface and bulk recombination.
- Silicon pellets from Texas Instruments were measured during materials upgrade processing, and an optimum process sequence was determined.
- Cleaning kinetics were investigated and it was found that under certain pH the deposition of the metallic impurity is likely, whereas under different pH, a dissolution of the impurity in the solution is a preferred condition.

Conclusions

The program has been very successful in developing and applying post-growth quality enhancement techniques to improve solar cell efficiencies in the commercial silicon substrates. Many of these processes or process modifications have already been adopted by the PV manufacturers into their production lines. Detailed investigations and theoretical modeling has been very helpful in identifying the bottlenecks in the path of reaching 18% commercial solar cells. These issues, and development of thin Silicon solar cells are included in the new program.

Under this program, the subcontractors have worked with many PV companies in attempts to investigate applications of new results to their materials or devices, or both. In order to further enhance the dissemination of research results, the following workshops/meetings were held:

- An annual workshop on the Role of Impurities and Defects in Silicon Device Processing was established. Six workshops have been held.
- Two Working Group Meetings for the measurement of the minority carrier diffusion length/lifetime. These meetings addressed issues such as the limitations of the measurement methods, round robin measurements on the same set of samples, the significance of average values in a nonuniform material, and correlations with the cell performance.

Possibility of Lower Cost Multicrystalline Silicon Solar Cell Toward GW Production

K. Shirasawa

Kyocera Corporation
Kawai 10-1, Gamo-cho, Gamo-gun, Shiga, 529-15 JAPAN

ABSTRACT

We have investigated low cost and high efficiency solar cell technology using large area ($225cm^2$) multicrystalline silicon (mc-Si) materials. Surface texturing using RIE (Reactive Ion Etching) technique and high temperature hydrogen annealing after deposition of PECVD SiN film as a bulk passivation have been applied to obtain the high efficiency mc-Si solar cell[1]. The further cost reduction of solar cells is expected for large scale practical use of PV systems, and we have investigated the process sequences to produce high efficiency and low cost solar cells.

INTRODUCTION

Most of commercial photovoltaic solar cells for electric power application are single crystalline or multicrystalline silicon materials. Though mc-Si solar cells have very promising possibility for low cost, high efficiency and high reliability, further cost reduction is expected for large scale practical use of PV systems in near future. As there is a limit for cost reduction only by a scaling up of manufacturing, that is not only a scale merit but also high efficiency solar cell technology is very important and development of low cost materials is required. We have obtained the efficiency of 17.1% mc-Si solar cell with the area of 15cm X 15cm[1]. In this paper, we describe the tasks and the approaches to produce low cost 15% efficient PV modules using 17% efficient solar cells.

HIGH EFFICIENCY LARGE AREA mc-Si SOLAR CELLS

Reduction of surface reflectance is very important for mc-Si solar cells to improve cell performances. For mc-Si solar cells, texture etching which is conventionally used for single crystalline silicon solar cells is not able to give a surface morphology to reduce reflectance sufficiently because of the various crystalline orientation. We have developed a new surface texturing technique using Reactive Ion Etching (RIE) method, which is expected to form a low reflectance surface on various crystalline orientations of grains. This surface texture has a pyramid-like or a cone shape as shown in figure 1, and aspect ratio of which can be easily controlled by gas flow ratio[2]. We have optimized surface shape and emitter sheet resistance. And we have fabricated over 17% efficient large area ($225cm^2$) multicrystalline silicon solar cells as shown in figure 2 using this texturing technique and passivation schemes.

Emitter is formed on front surface by diffusion from $POCl_3$ liquid dopant source after texturing by RIE. The optimum emitter sheet resistance is investigated comparing with conventional surface structure because the surface morphology is quite different. The optimum sheet resistance is around 90 ohm/sq for RIE textured cell, however it is 50-60 ohm/sq for conventional structure cell. Efficiency is improved from 16.0% to 16.7% by optimization of emitter sheet resistance with using Sumitomo SiTix conventional cast Si materials. Back surface field is made by screenprinting and firing of aluminum paste. Silicon nitride film is deposited on both side of the cell by PECVD for bulk passivation and as an ARC. Plasma deposited silicon nitride film (P-SiN) used as an ARC is efficient for passivation of grain boundaries and intra-grain defects in mc-Si materials[3, 4, 5, 6]. The cells are annealed in hydrogen ambient for more effective bulk passivation at 600-700 deg.

Figure 1 Textured surface using RIE method

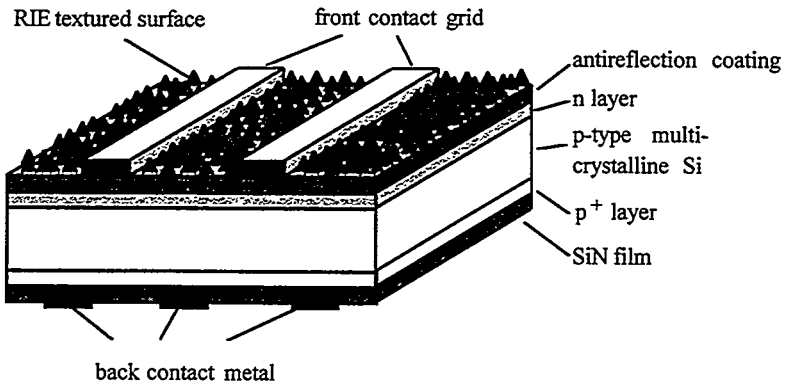


Figure 2 Cell structure with RIE textured surface

Voc is improved nearly 15mV by this passivation scheme. It is difficult to apply the oxide passivation to mc-Si solar cells, because oxide makes the effect of bulk passivation small for these type of cells. It seems that passivation oxide prevents the diffusion of hydrogen from P-SiN film to substrate. So we have investigated high temperature annealing in hydrogen after deposition of P-SiN film on both surfaces of oxide passivated mc-Si solar cells. Open circuit voltage for cells with (a) P-SiN film deposited only on top surface, (b) P-SiN film deposited on both surfaces and (c) oxide passivated and hydrogen annealed at 600℃ for 60 min. after P-SiN deposition on both surfaces of 10 cm X 10 cm conventional cast wafer made by Sumitomo SiTiX are 608 mV, 613 mV and 622 mV respectively. And unpaired electron spin density of oxide passivated mc-Si materials with these passivation schemes are measured by ESR method as shown in Figure 3. This shows that spin density is decreased and bulk quality is improved by hydrogen annealing. Front contact grid is evaporated and patterned by lift off method followed by copper plating. Back contact metal is deposited aluminum.

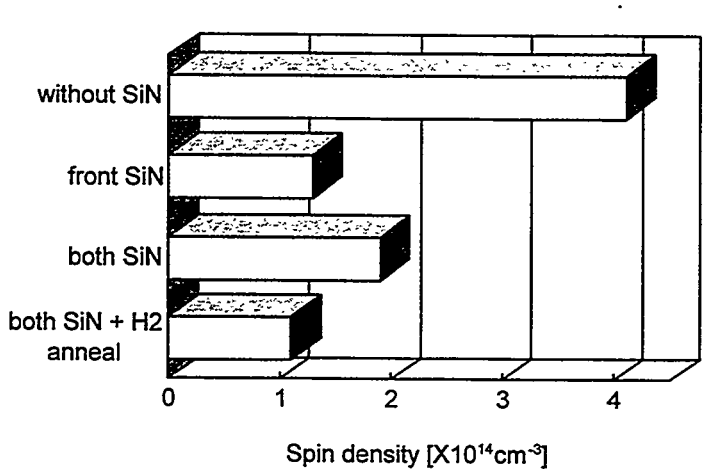


Figure 3 Improved unpaired electron spin density of oxide passivated mc-Si materials with various passivation

The maximum cell efficiency of 17.1% has been obtained using Sumitomo SiTiX conventional cast material of 15cm X 15cm. Performance of this cell measured at JQA (Japan Quality Assurance

Organization) is shown in table 1. And 18 solar cells have been fabricated using Daido-Hoxan cast Si materials (Drip control method [7]) of 15cm X 15cm. Figure 4 shows the distribution of these efficiency and figure 5 shows the I-V characteristics of PV module using these solar cells. The efficiency of this PV module is 14.3%.

Table 1 Performance of high efficiency cell measured at JQA
cell size=225cm^2, 25℃, 100mW/cm^2, AM1.5G

Isc(A)	Voc(mV)	F.F.	Effi.(%)
8.14	621	0.762	17.1

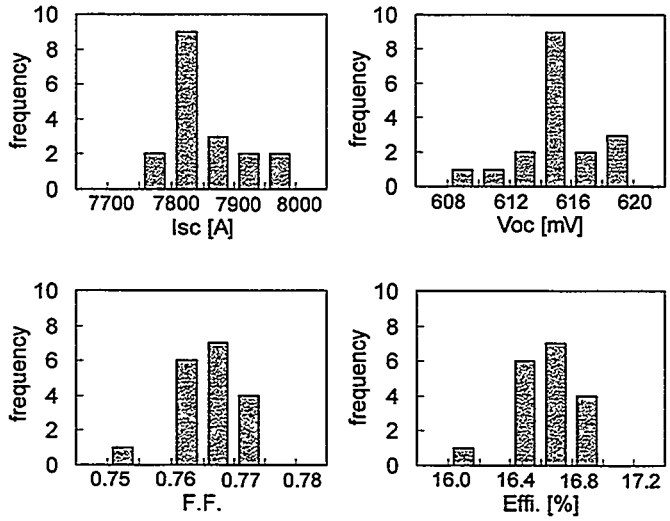


Figure 4 Performance of 18 solar cells of 225 cm^2 using Daido-Hoxan casting materials

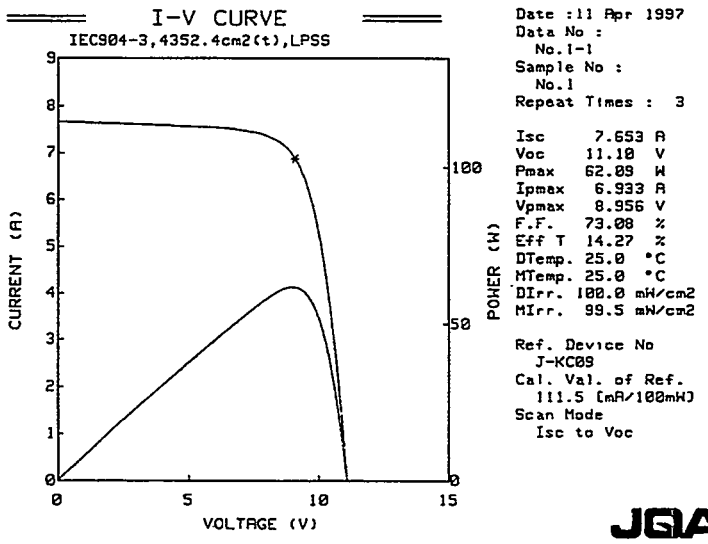
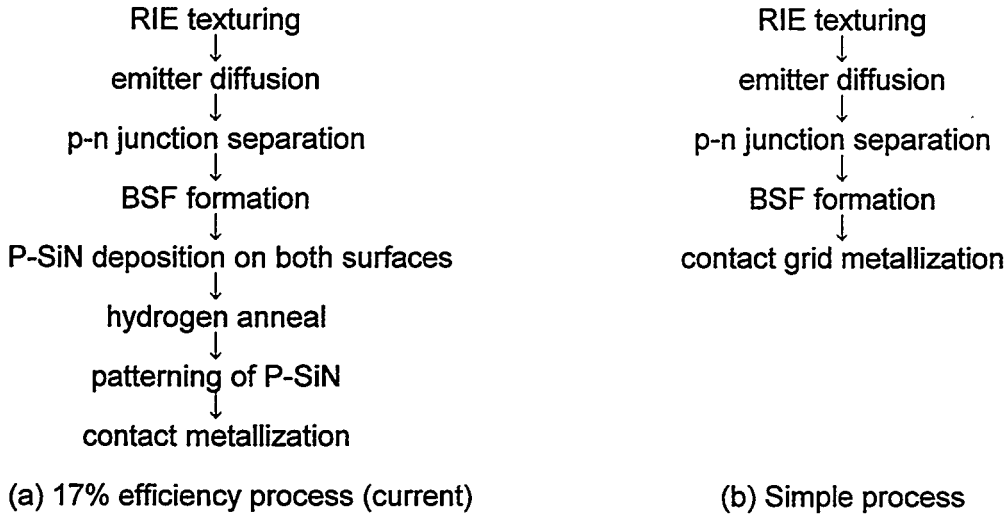


Figure 5 I-V characteristics of PV module (93.4 X 46.6=4352cm^2) using 225cm^2 cells

TASKS TO PRODUCE SOLAR CELLS OF GW / YEAR SCALE IN FY 2010

As there is a limit for cost reduction only by a scaling up of manufacturing, that is not only a scale merit but also high efficiency solar cell technology is very important and development of low cost materials is required. Our efforts are focused on developing the simple process sequence for

high efficiency solar cells and developing the production equipments and facilities with low cost and high productivity. We assume the simple process sequence at 1GW / year scale for cost reduction as shown in figure 6. At first, RIE is carried out for removing damages due to the wafer slicing. The emitter diffusion is carried out followed by p-n junction separation, BSF formation and contact grid metallization. We assume that ARC is not necessary due to the optimization of RIE texturing. About 40000 cells have to be produced in an hour at 1GW / year scale as shown in Table 3.



(a) 17% efficiency process (current) (b) Simple process

Figure 6 Simple process sequence

Table 3 Production ability which is necessary for 1GW / year

per month	per day (25days / month)	per hour (productivity : 92%) (3.825W / cell, yield : 98.6%)
83.3 MW	3.3 MW	151 kW (40000 cells)

The mc-Si solar cell manufacturing sequence can be divided into 5 major components: Si feedstock, casting, slicing, cell fabrication and module fabrication as shown in figure 7. Table 4 shows the major cost drivers in each process: wafer fabrication (Si feedstock, casting and slicing), cell fabrication and module fabrication. Our developing subjects which our efforts will be focused on are shown in table 5 from this investigation.

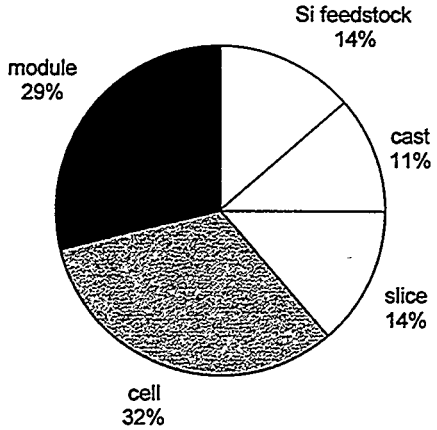


Figure 7 Cost share of solar cell process

Table 4 The major cost drivers in each process

process	cost drivers
wafer	materials ---------- Si feedstock, equipments for slicing (wire, slurry, chemicals, roller)
	equipments --------- casting, cutting, slicing
cell	equipments --------- RIE, diffusion, junction separation, contact metallization
	others ---------- efficiency, process number
module	materials ---------- junction box, module frames, glasses, EVA encapsulant, backsheets
	others .....efficiency, process

Table 5 Developing subjects in each process

process	developing subjects
wafer	casting ---------- high throughput, quality improvements (Tau>40micro sec) [7]
	slicing ---------- thinner wafer, reduction of kerf loss, high throughput
cell	texturing ---------- high throughput of RIE
	diffusion ---------- high throughput of in-line type furnace
	BSF ---------- firing furnace, boron diffusion
	ARC ---------- PECVD-SiN → RIE texturing
	p-n separation --------- plasma etching
	patterning of ARC---- printing of resist ink→unnecessary (RIE texturing without ARC)
	contacting ---------- printing, firing
module	materials ---------- long term durability with low cost
	equipments ---------- productivity
	ribbon to cell ---------- high throuput and low resistivity materials
	circuit lay-up ---------- high throughput without stress
	lamination ---------- high throughput
	curing ---------- high throughput
	others .....frameless modules and roof or wall integrated material PV modules

The mc-Si wafer fabrication process has to be improved by the quality improvement, thinning the wafer thickness and reducing the kerf loss. The results of PC-1D simulation[8] shows that it is necessary that bulk lifetime of mc-Si materials is larger than 40mivro sec. with high efficiency cell process sequences to obtain over 17 % efficient solar cells[9]. The costs in slicing are driven by wire saw consumable like wire, slurry, chemicals for wafer cleaning and rollers.

For cell fabrication, emphasis will be on improving and upgrading the process, equipments and facilities. High throughput texturing process using RIE is to be developed by designing the large in-line type RIE equipments and high speed process sequence. The emitter diffusion process is also to be high throughput using in-line type phosphorus diffusion furnace. The ports are used for load and unload of cells in this furnace as shown in figure 8. The phosphorus is diffused and driven into cells while running from entrance to exit of furnace. Table 6 shows the cell efficiency dependence on emitter diffusion throughput using conventional and this type of furnace. Throughput has been improved for 96 to 356 cells / hr with nearly same efficiency. Screenprinting of aluminum and firing is used as the dominant production technology for BSF formation. It is necessary that a new cost effective BSF formation technology because cells are warping while firing of aluminum and the production yield is decreased when using larger and thinner cells. We have investigated the

boron diffusion process as a new BSF formation technology using high throughput in-line type boron diffusion furnace. However the ARC is not necessary by optimization of the RIE texturing, the investigation will be focused on the passivation process combined use with like FGA at contact metallization. The high throughput separation of p-n junction is possible by plasma etching of stack cells. The high throughput one step process using RTP is the promising for the contact metallization[10].

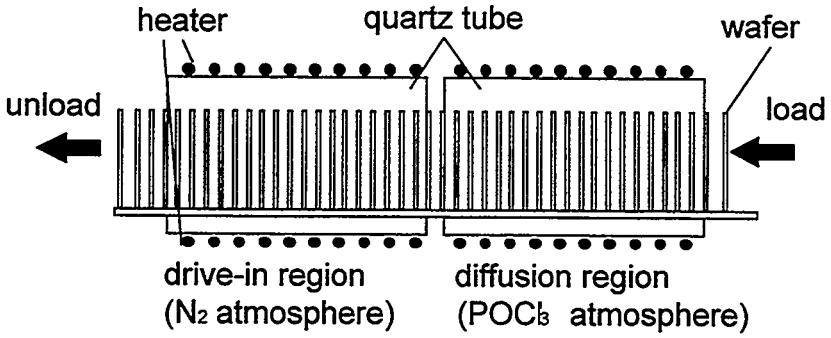


Figure 8 Schematic view of in-line type phosphorus diffusion furnace

Table 6 Cell efficiency dependence on emitter diffusion throughput using conventional and in-line type of furnace

furnace	throughput[sec / cell]	Jsc[mA/cm^2]	Isc[mA]	Voc[mV]	FF	Effi.[%]
conventional	30	31.67	7125	602	0.776	14.80
in-line type	11	31.82	7160	603	0.763	14.64

Module costs are driven by direct materials, the junction box, the module frames, glasses, EVA encapsulant and the backsheets. Both the developing the low cost materials and improving the module design are necessary for cost reduction. The new cover material which has long term durability with lower costs substitute for the glass, frameless modules and roof or wall integrated material PV modules are also promising for cost reduction.

CONCLUSIONS

In order to produce GW PV modules, it is absolute requirements to attain lower cost. GW PV market does not exist without low cost technology. In order to produce GW modules, cost reduction by scale merit is very important. In addition, high efficiency is also very important. We have obtained high efficiency of 17.1% using 15cm X 15cm mc-Si substrate. Basic technologies to obtain high efficiency are as follows.

1.high lifetime mc-Si substrates — lifetime: more than 40 micro sec.
2.low reflectance structure — reflectance loss: less than 6 %
3.high emitter sheet resistance — sheet resistance: around 90 ohm/sq
4.BSF

5.bulk passivation

6.fine emitter contact grid shadowing loss: less than 4.8 %

On the base of high efficiency technologies, we should develop lower cost technologies. In order to attain low cost and high efficiency mc-Si solar cells, following developments are necessary.

1.simpler high efficiency cell process using thinner wafers

2.development of high throughput process and equipment

3.lower cost materials of module

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Low Cost Production Technologies for Polycrystalline Silicon Solar Cells

T.Nunoi, T.Machida, A.Miyazawa, Y.Yokosawa,
H.Nakaya, S.Tanaka, T.Tomita, H.Kumada*, M.Murakami*

Energy Conversion Laboratories, SHARP CORPORATION
282-1 Hajikami, Shinjo-cho, Kitakaturagi-gun, Nara 639-21, Japan
E-mail: nunoi@shinjo.sharp.co.jp
*Precision Technology Development Center, SHARP CORPORATION
2613-1 Ichinomoto-cho, Tenri, Nara 632, Japan

Abstract

To develop a technology of forming grooves for low cost cell production, a multi-blade wheel grinding method was investigated. The process time of groove formation on the surface of 10X10cm^2 polycrystalline silicon substrate was reduced to 30seconds by newly developed high-speed groove formation machine. Junction and anti-reflection coating were simultaneously formed by atmospheric pressure chemical vapor deposition(APCVD) technique was also investigated. For electrodes formation process, single firing method for both side electrodes made possible to simplify the firing process and to speed up from a conventional speed of 400mm/min to 5000mm/min.

1. Introduction

Polycrystalline silicon solar cells are expected to realize much reduction of the cost in conjunction with the development of ingot making by the casting method[1]. A high conversion efficiency of 18.6%(1cm^2 area) have been achieved by a process which involves impurity gettering and effective back surface passivation[2]. We reported a mechanical groove method for reduction of surface reflectance of polycrystalline silicon solar cell[3] and then a conversion efficiency of 17.2% has been achieved for a 10X10cm^2 V-grooved polycrystalline silicon solar cell with the basic structure as shown in Figure 1[4]. And high throughput mechanical V-grooving technology is being reported for a practical application[5]. Doped spin-on diffusion which makes simultaneous formation of TiO_2 anti-reflection coating and N^+ diffused layer was established in 1980 as a low cost production technology[6]. Atmospheric pressure CVD method is suitable for continuous large area coating. There is a possibility of the new mass production technology.

For the reduction of solar cell cost, it is necessary to introduce the new technologies based on high efficiency cell structure for larger scale mass production.

This paper describes about the development of the basic technologies for high volume production such as speeding up of forming grooves, simultaneous formation of junction and anti-reflection coating, and speeding up of forming electrodes.

2. Speeding up of cell surface groove formation

Mechanical grooving technique is effective to uniform reduction of surface reflectance over all polycrystalline silicon solar cells. We have formed fine grooves on polycrystalline silicon substrates using a beveled single blade with a diameter of 50mm and a thickness of 100mm to fabricate high efficiency solar cells applying a dicing machine.

To develop a technology of forming grooves for high volume production, a multi-blade wheel grinding method shown in Figure 2 was investigated. V-shaped edges were sharpened

on the surface of a diamond wheel with a diameter of 200mm and a thickness of 70mm and V-shaped grooves are formed on substrates with the wheel. Fine groove structure shown in Figure 3, with a pitch of 70mm and a depth of 70mm formed by the multi-blade wheel effectively reduces the surface reflectance and gives light trapping effect. Figure 4 shows cell short circuit currents and open circuit voltages for the table speed at grooving the silicon surface. TX for conventional texture etching and G for V-groove by a dicing machine are reference samples. In the case of 6m/min table speed, almost same performances were obtained as the case using dicing machine. Multi-blade wheel grinding is suitable for high speed formation of grooves with precise shape. The process time of grooving on the surface of $10\times10cm^2$ polycrystalline silicon substrate was reduced to 30seconds by the wheel with a diameter of 200mm and a thickness of 28mm at 9000r.p.m and 6m/min of table speed. In view of more speeding up of grooving process, the optimum condition should be established synthetically.

Etching time reduction for removing the surface damaged layer after grooving was studied. As shown in Figure 5, the same level of conversion efficiency was achieved on the cell treated with an acid etching of 10seconds as compared to conventional one treated with an alkaline etching of 5minutes. As a result, the etching process time was substantially reduced.

3. Simultaneous formation of junction and anti-reflection coating(ARC)

A highest conversion efficiency polycrystalline silicon solar cell of 17.2%($10\times10cm^2$) was obtained using thermal diffusion of $POCl_3$ following TiO_2 anti-reflection coating by atmospheric pressure CVD. According to the cell process with doped spin-on diffusion source, etched silicon surface is coated with phospo-titanate glass(PTG) solution, followed by a diffusion process to form N^+ diffused layer and TiO_2 ARC simultaneously. But silicon substrates are processed one by one at spin coating of PTG solution.

In order to form PTG film on large area of many silicon substrates through the low cost process, we have examined the formation of PTG film by atmospheric pressure CVD. There is a possibility of uniform formation for micro-surface structure of the substrate, for example, texture etching or groove formation compared with the spin coating method.

Thermally decomposing titanium compounds and phosphorus compounds at atmospheric pressure, PTG film was deposited on silicon substrates with an in-line type apparatus at a temperature of 450℃. By annealing the substrates at a temperature of 920℃, N^+ diffused layer and TiO_2 ARC were simultaneously formed. Figure 6 shows cell performances fabricated by various N^+ diffused layer formation methods. 1 for $POCl_3$ diffusion followed by deposition of TiO_2 ARC and 2 for spin-on PTG solution are reference samples. 3 for PTG film deposited by APCVD is a newly developed sample. In case of 2 and 3, Jsc was lower mainly because of higher surface reflectance but Voc was higher because of high surface carrier concentration of N^+ diffused layer. Relatively high conversion efficiency was obtained for the first method even though Jsc was lower than that of a conventional cell mainly because of higher surface reflectance.

4. Speeding up of forming electrodes

The speeding up of electrode firing was investigated. Backside aluminum electrode and front side silver electrode were formed by screen printing and firing. The optimum firing temperature of aluminum paste was about 750℃. That of silver paste was about 600℃. Each paste has its own optimum firing temperature. So we used silver paste developed for a high firing temperature and investigated simultaneous firing of both front and back side printed electrodes.

In the investigation of electrode simultaneous forming process, when the speed of metal

mesh belt conveying the substrates in a firing furnace increased to 2000mm/min, the same conversion efficiency as the one under conventional separate firing condition(400mm/min) was obtained. Using conventional furnace with mesh belt conveyor system, there was a limit in ability of speeding up of electrode firing and the limit of belt speed was 2000mm/min. Because of a large amount heat capacity of mesh belt, the heat given from the lamps to silicon substrates was derived. It became possible to heat up the substrates effectively by newly developed furnace with wire conveyor system of which heat capacity is small. Figure 7 shows the comparison of the optimum firing temperature at various belt speed using the furnace and conventional one. The optimum firing temperature is more than 30℃ lower and the consumption of electricity can be reduced. It was clarified that reduction of heat capacity of the conveyor system is important for the speeding up of electrode firing. Further speeding up was performed by above furnace. Table 1 shows the optimized firing temperature for higher conveyor speed conditions more than 3000mm/min in a high speed firing furnace. Using these optimum firing conditions, solar cells were made. Figure 8 shows the cell performances for each conveyor speed. A reference processed cell characteristics(▼) at 500mm/min is also indicates after a ordinary furnace electrodes firing. As a result, the same level of conversion efficiency as the conventional one was achieved at a conveyor speed of 5000mm/min.

5. Conclusion

We have investigated basic technologies for high volume production. The basic technologies of surface mechanical grooving and simultaneous formation of junction and ARC and high speed electrode firing for high volume production have been established.

Acknowledgment

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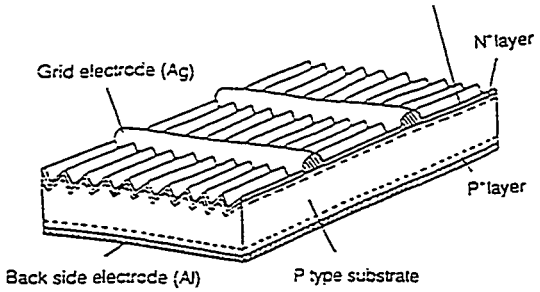

Fig.1 Basic structure of a high efficiency polycrystalline silicon solar cell.

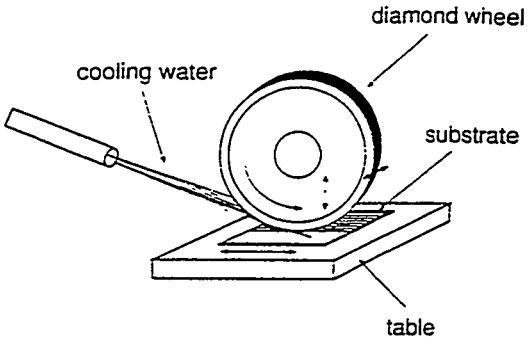

Fig.2 Outline of a multi-blade wheel grinding method.

Fig.3 Fine grooves formed by a multi-blade wheel.

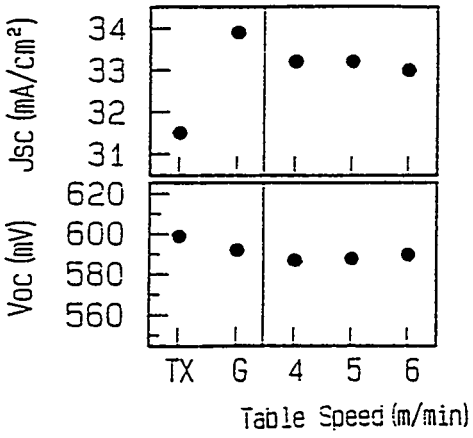

Fig.4 Cell performances for table at grooving on silicon substrate; TX:conventional texture etching, G:V-grooved using dicing machine.

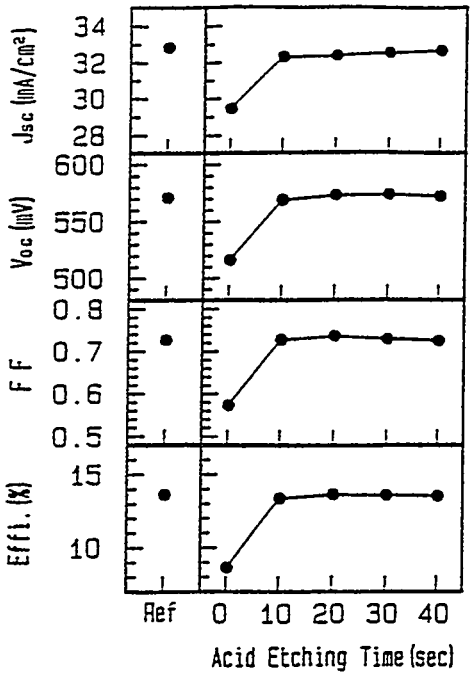

Fig.5 Cell performances for acid etching time; Ref:alkaline etching, 5min.

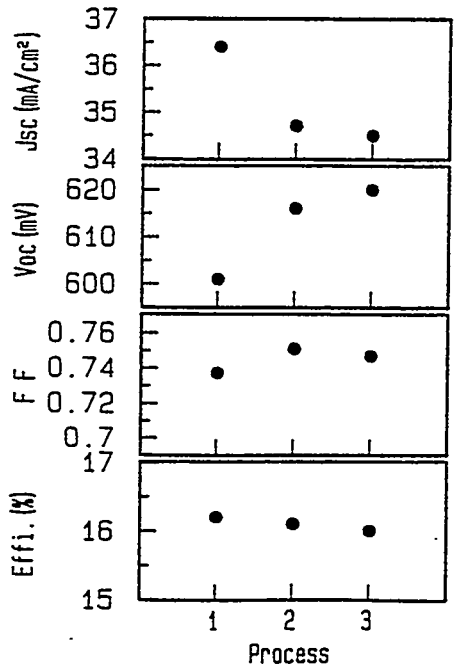

Fig.6 Cell performances fabricated by various N^+ diffused layer formation methods.
1:$POCl_3$diffusion+APCVD TiO_2
2:spin-on PTG
3:APCVD PTG

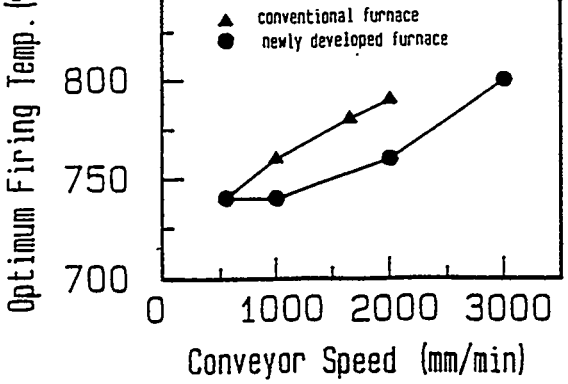

Fig.7 Comparison of optimum firing temperature at various conveyor speed.

Table 1 Optimum firing temperature at each conveyor speed(including Fig.7 result).

Conveyor speed (mm/min)	550	1000	2000	3000	4000	5000
Optimum firing temperature(°C)	740	740	760	800	840	880

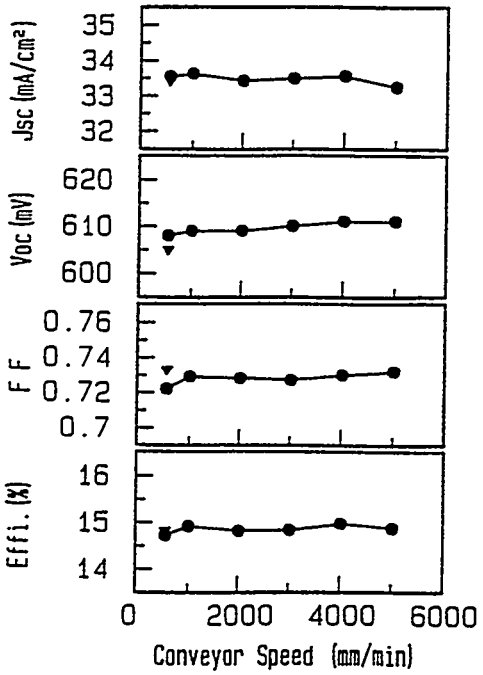

Fig.8 Cell performances as a function of conveyor speed.

Rapid Thermal Chemical Vapor Deposition : Example Processes and Their Applications

Mehmet C. Öztürk

North Carolina State University
Department of Electrical and Computer Engineering
Raleigh, NC 27695-7911

ABSTRACT

Single wafer processes are gradually replacing batch processes as the size of the silicon wafers continually increase. Of the potential single wafer processes, rapid thermal processing (RTP) is steadily emerging as a manufacturing technique. Traditional applications of RTP are implant activation, silicide formation and oxidation. Rapid Thermal Chemical Vapor Deposition (RTCVD) is a natural extension of RTP which carries such promises as uniform deposition on large area wafers and controlled growth of ultra-thin layers with abrupt interfaces. In this paper several novel processes are reviewed as examples to highlight key features of RTCVD.

INTRODUCTION

Continually increasing size of silicon wafers has introduced serious challenges for batch processing including across the wafer and batch uniformity, sharply increasing equipment costs and clean room real-estate. Single wafer manufacturing was proposed as a potential solution. This however required a paradigm shift and not surprisingly, the concept initially faced a strong resistance from industry. Nevertheless, it was not difficult to accept certain processes (e.g. physical vapor deposition and reactive ion etching) as single wafer processes since some of these processes were already practiced as small batch or single wafer processes. However, a microelectronics factory based entirely upon single wafer manufacturing meant doing everything the new way which had to include such traditional processes as annealing, oxidation and chemical vapor deposition. For such processes, rapid thermal processing (RTP) was proposed.

Rapid thermal processing, starting from its inception, has attracted considerable interest from universities and research laboratories. Publications from these institutions lead to a gradual but steady rise in our confidence level. This growing interest was also supported by several equipment manufacturers who constantly improved the RTP equipment.

In a typical RTCVD reactor, the wafer is heated optically through a quartz window, providing thermal switching to initiate and terminate chemical reactions on the wafer surface in a matter of seconds. Thus, thin films with abrupt interfaces can be grown at high growth rates which is an important concern in single wafer manufacturing. The technique aims at minimizing the

thermal budget instead of temperature. Satisfactory growth rates can be achieved at elevated temperatures while the process time can be controlled accurately down to a few seconds by means of temperature switching and computer control.

In this paper, several thin film deposition processes are reviewed as examples to highlight key features of RTCVD. These processes are selective silicon epitaxy, amorphous silicon deposition, rapid thermal etching and selective titanium disilicide deposition.

RTCVD PROCESSES

Low Temperature Selective Si Epitaxy

As devices scale for ultra large scale integration (ULSI), the demand for advanced techniques that provide selective processing, low temperature processing and low defect densities is rapidly growing. Among these, low temperature selective epitaxial growth (SEG) is currently being considered for various novel applications in Si integrated circuit processing. At NCSU, we have developed ultra high vacuum rapid thermal chemical vapor deposition (UHV-RTCVD) as a new approach for low temperature Si epitaxy in single wafer cluster tools. The technique combines a clean UHV environment with lamp heating in a cold wall growth chamber.

Surface preparation is achieved by an ex-situ clean and a low thermal budget in-situ prebake. The ex-situ clean consists of a standard RCA clean and a dip in a 5% dilute HF solution that provides a hydrogen passivated surface. The final step of the ex-situ clean is a short rinse in deionized water which results in a partial loss of the hydrogen coverage. The in-situ clean consists of a low thermal budget prebake (<800°C/10 s) in vacuum. With this prebake, any oxygen contamination due to lack of 100% hydrogen coverage is removed via desorption and the resulting interfacial oxygen level at the epitaxy/substrate interface is below the detection levels of secondary ion mass spectroscopy. As such, the process provides an efficient method for surface preparation with a thermal budget significantly lower than that used in conventional systems. The low thermal budget prebake relies on the capability to load the wafer at room temperature preserving the level of hydrogen coverage on the wafer surface. In contrast, in hot-wall reactors, the coverage is lost during wafer loading where the ambient is not sufficiently clean.

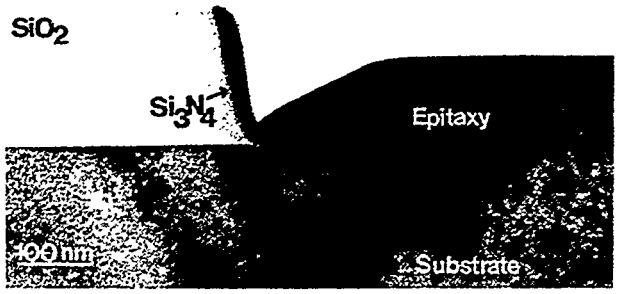

Figure 1. Epitaxial layer selectively grown by UHV-RTCVD using Si_2H_6/Cl_2 chemistry

In UHV-RTCVD, the Si source gas is disilane (Si_2H_6). In our experiments, we are using a mixture of 10% Si_2H_6 in H_2 or He. This choice is based upon the high efficiency of Si_2H_6 compared to other commonly used epitaxial Si source gases such as silane (SiH_4) and dichlorosilane (SiH_2Cl_2). By using Si_2H_6, growth rates compatible with single wafer manufacturing can be obtained at

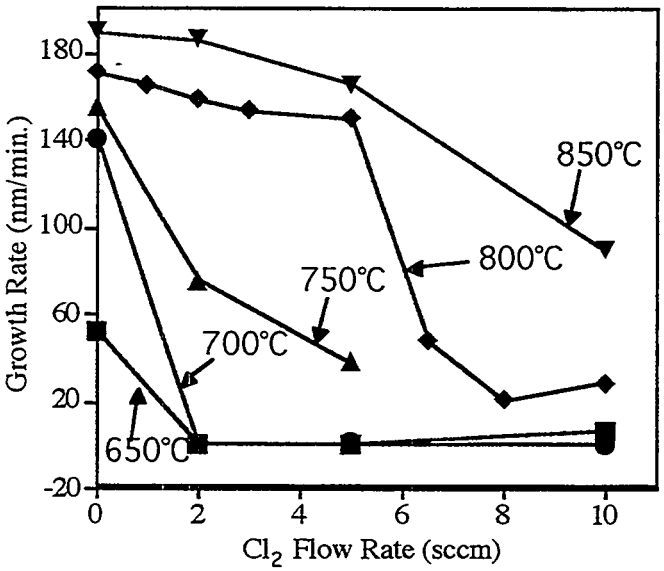

Figure 2. Selective Si epitaxy growth rate as a function of chlorine flow at different growth temperatures.

low temperatures (≈ 800°C) and at low pressures (total pressure ≤ 30 mTorr). Operation at low pressures is helpful in minimizing the amount of contaminants introduced into the reactor by the process gases. A typical epitaxial growth is performed at 800°C/30 mTorr with a growth rate on the order of 150 nm/min. Electrical characterization of these epitaxial layers indicate respectable generation lifetimes (≤ 100 μs).

Realizing the need for a robust selective deposition process, Cl_2 was added to the Si_2H_6 chemistry to provide a means to etch nuclei forming on SiO_2. By using Cl_2 instead of HCl, the effect of chlorine is decoupled from hydrogen. We have shown that epitaxial layers can be grown with an excellent selectivity with very low Cl:Si ratios in the gas phase (≤ 1:5). This is considerably lower than 2:1 ratio of SiH_2Cl_2 even without HCl addition. Furthermore, because Si_2H_6 can achieve growth rates comparable to SiH_2Cl_2 at much lower pressures, the total Cl in the system is also significantly reduced. Our results show that Cl_2 introduces an extremely efficient Si etching mechanism that proceeds via formation of $SiCl_2$. A typical cross-sectional transmission electron micrograph of an epitaxial selectively grown with respect to both SiO_2 and Si_3N_4 is shown in Figure 1.

For typical growth conditions, the effect of Cl_2 on Si growth rate is negligible. However, at temperatures below 750°C, a significant reduction in growth rate occurs due to Cl

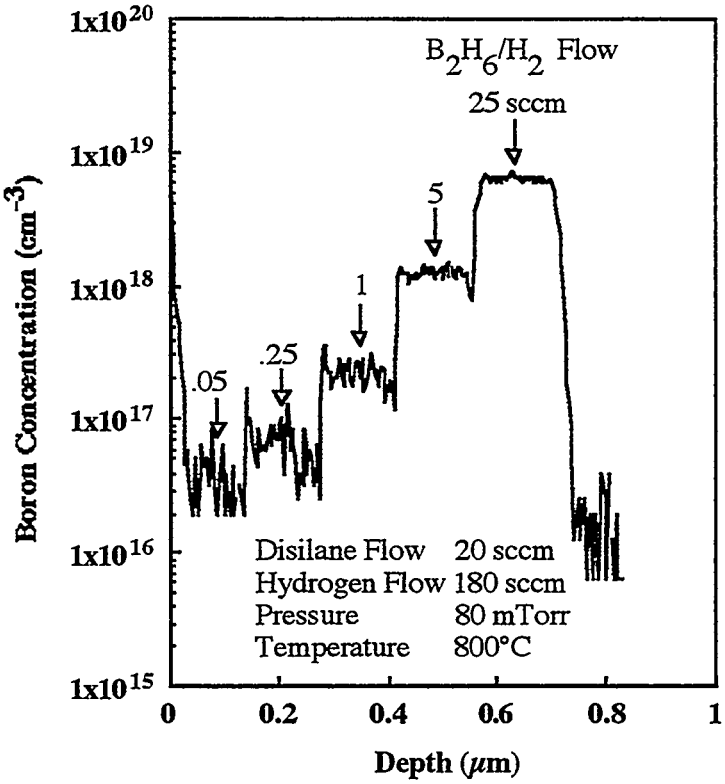

Figure 3. Epitaxial layers with abrupt boron profiles obtained by in-situ doping

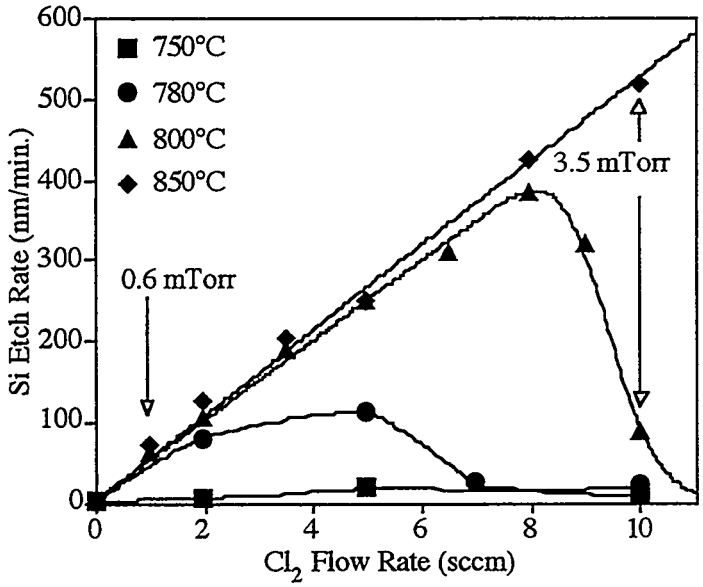

Figure 4. Rapid thermal etching rate of silicon in chlorine as a function of chlorine flow rate at different temperatures.

passivation of the Si surface. This is demonstrated in Figure 2. At and above 800°C, chlorine passivation is negligible unless a very high partial pressure of chlorine is used. Our optimum growth temperature is 800 °C with a Cl2 flow rate of 2 sccm which provides excellent process selectivity with negligible loss in growth rate.

We have also investigated growth of in-situ boron doped epitaxial layers using B_2H_6 as the source gas for boron. Our results indicate that a wide range of doping densities (10^{16} - 10^{19} cm^{-3}) can be obtained. Abrupt doping profiles (both high-to-low and low-to-high transitions) can be readily obtained with the help of cold wall processing and temperature switching (Figure 3) which is a unique advantage of RTCVD. Our results indicate that boron incorporation is achieved through an equilibrium process with very little dependence on temperature. Boron concentration is mainly determined by the B_2H_6 partial pressure in the reactor.

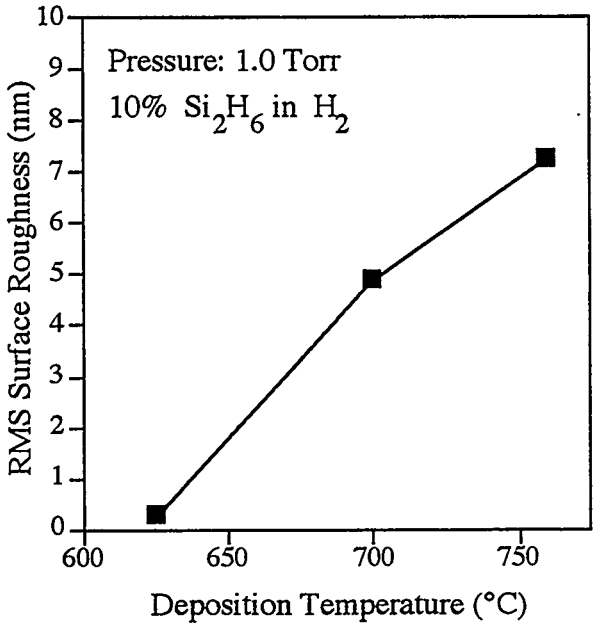

Figure 5. The effect of deposition temperature on RMS roughness of silicon deposited on SiO_2 using Si_2H_6.

Rapid Thermal Etching

Pure Cl_2 can be used to etch Si isotropically with excellent selectivity to SiO_2 and Si_3N_4. We refer to this technique as Rapid Thermal Etching (RTE) which may have applications in Si processing where anistropic etching is not a requirement. The process requires temperatures high enough for $SiCl_2$ desorption (≥ 750°C) at sufficiently low Cl_2 partial pressures to avoid surface passivation (Figure 4). Etch rates as high as 500 nm/min are possible at 800°C requiring the rapid temperature switching capability of RTP to start and stop the etching process.

Amorphous Silicon Deposition

Low pressure chemical vapor deposition

(LPCVD) of smooth polycrystalline Si films on SiO_2 is highly desirable in CMOS ultra large scale integration. In conventional, hot-wall, LPCVD furnaces, very smooth films are obtained via amorphous silicon (a-Si) deposition using SiH_4 requiring deposition temperatures below approximately 580°C, the transition temperature from amorphous to polycrystalline structure.

To meet the throughput requirements of single wafer manufacturing in RTCVD reactors, polysilicon is deposited at temperatures ≥ 700°C, well above the amorphous/polycrystalline transition temperature yielding rms roughness figures on the order of 10 nm for approximately 200 nm thick polysilicon films.The efficiency of Si_2H_6 is also helpful in depositing smooth amorphous silicon films on SiO_2 at low temperatures (≤ 600°C) at rates compatible with single wafer manufacturing. For these depositions, higher pressures (~ 1 Torr) are used to achieve acceptable deposition rates. Growth rates on the order of 50 nm/min can be obtained below 600°C. These films are amorphous in nature with surfaces approaching atomic roughness levels (Figure 5).

Selective $TiSi_2$ Deposition

Selective rapid thermal chemical vapor deposition (RTCVD) of TiSi2 is a promising alternative to the conventional self-aligned silicide (SALICIDE) process to form low-resistivity contacts to ultra-shallow source/drain junctions of deep submicron MOS transistors. The process makes use of TiCl4 and SiH4 as the Ti and Si source gases in a temperature range of 750 - 825 °C. The primary advantage of the process over the conventional SALICIDE process is that by providing sufficient levels of Si from the gas phase, junction consumption can be eliminated. Furthermore, the process eliminates a wet etch and reduces the number of process steps from four to one. The process exhibits excellent selectivity to deposited insulators. On boron doped silicon, process can be easily optimized to achieve consumption free deposition. Boron doped junctions with excellent electrical behavior can be obtained with silicide layers as thick as 100 nm. On arsenic implanted Si, we have observed resistance to nucleation as well as enhanced silicon consumption at arsenic levels above $1x10^{20}$ cm^{-3}. Methods to overcome this "arsenic effect" are currently under investigation.

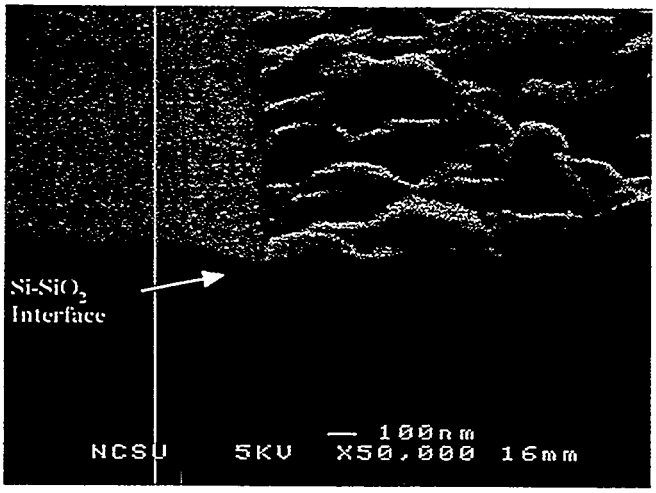

Figure 6. A typical scanning electron micrograph of a selectively deposited TiSi2 layer.

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A Survey of Material Options and Issues for Thin Film Silicon Solar Cells

Z. Shi
Pacific Solar Pty. Ltd, 82-86 Bay St. Botany, NSW 2019, Australia
M. A. Green
Photovoltaics Special Research Centre, University of New South Wales, Sydney NSW 2052, Australia

Abstract

The high production cost of thick high-efficiency crystalline silicon (c-Si) solar cells inhibits widespread application of photovoltaic devices whereas amorphous silicon (a-Si) suffers inherent instability and low efficiency. Thus, crystalline thin film Si solar cell can likely offer a long term solution for low cost but high efficiency modules for most applications. This paper reviews the progress in thin film Si solar cell development over the last two decades including thin film crystal growth, device fabrication, novel cell design, new material development, light trapping, and both bulk and surface passivation. Quite promising results have been obtained for both large grain (>100μm) pc-Si material and the recently developed μc-Si materials. A novel multijunction solar cell design provides a new approach to achieve high efficiency solar cells from very modest materials. Light trapping is essential for high performance thin film Si solar cells. This can be realized by incorporating an appropriate texture on the substrate surface. Both bulk and surface passivations are also important to ensure that the photogenerated carriers can be effectively collected within the thin film device.

Introduction

In the long term it is likely that thin film solar cells will displace bulk crystalline silicon (c-Si) devices for most applications[1]. The thin film technology that ultimately dominates will be dependent on not only cost but also efficiency. It is unlikely that any photovoltaic technology will compete with conventional sources in large-scale grid-connected applications unless the photovoltaic module costs can be reduced well below US$1/Wp while simultaneously achieving efficiencies at least as high as the present leading commercial wafer technologies in the vicinity of 15%[2].

Increased interest is now being shown worldwide in developing thin film c-Si solar cell technologies[3]. Many years ago, c-Si was discounted as being viable for thin film solar cells due to its relatively poor absorption. However, it is now well recognized that c-Si's poor absorption is no longer an issue provided light trapping is incorporated. More specifically, an optical pathlength in excess of 100 μm together with close to 100% internal quantum efficiencies for all photogenerated carriers is probably essential to achieve the long term efficiency goal of 15% photovoltaic modules. This rules out the option of using low cost substrates of the same or similar refractive index to silicon due to the apparent inability to prevent large amounts of light penetrating into the non-active substrate material. Similarly, it appears unlikely that schemes relying on progressive enhancement of material quality through continued growth, with the device then formed into the upmost high quality regions, will achieve the long term efficiency goals due to the same problem of light penetrating into non-active regions of the silicon.

The research and development of polycrystalline silicon (pc-Si) thin film solar cells on low cost substrate dates back to the early 1970s[4]. In the 1970s and early 1980s, the effort of research activities aimed at producing large grain size pc-Si thin film material on low cost substrates were based on the belief that the grain size in the thin film silicon needs to be at least two times greater than the film thickness to produce high performance solar cells. For cell thickness around 20 to 30 μm, the grain size has to be at least 50 μm to meet the requirement. Thus, technology development emphasized-large grain size thin film silicon materials. Correspondingly, the substrates being used in the early days generally were compatible with the high temperature silicon film growth processes. Such substrates included metallurgical grade (MG) silicon sheet[5,6], stainless steel[6,7], graphite[8], ceramics and quartz glass[9]. A number of growth techniques were used to deposit silicon films on these substrates, including zone melt recrystallisation (ZMR)[10,11], dipping into molten silicon[12], electrodeposition[13] and plasma spraying[14]. Most of the substrates and film deposition techniques were abandoned due to the lack of commercial viability. The techniques remaining under development to date include ZMR and plasma spraying and are reviewed here together with development in recent years.

Progress in Thin Film Silicon Solar Cell Technologies

1. High temperature thin film silicon crystal growth

The ZMR technique was developed since the 1960s in an effort to produce good-quality silicon thin films on insulators for integrated circuit applications[15]. ZMR involves the recrystallization of a film by heating and moving a narrow molten zone across it. A range of energy sources have been used for the ZMR of silicon (and other semiconductor) thin films, including laser beams, incoherent light sources, strip heaters, electron beams and radio-frequency (RF) heaters. In all these versions of ZMR, more-or less- crystallographically oriented Si films were prepared with corresponding grain sizes up to several millimetres wide and several centimetres long. An inconvenient but necessary complication for these approaches is the use of a dielectric capping layer, such as silicon dioxide or silicon nitride, to protect the molten silicon from balling up during ZMR if a substrate with poor wettability with silicon is used.

A group at Mitsubishi started the development of thin film cells from Si deposited onto oxidized Si wafers using this method in the early 1990s. The aim is to produce a good crystallinity silicon buffer layer on the oxide substrate by ZMR and subsequently to fabricate thin film solar cells by successive deposition of p- and n^+-type layers in conjunction with appropriate hydrogen passivation of the grain boundaries. Efficiencies up to 16% have been demonstrated by this approach over a cell area of 100 cm^2 and cell thickness of 77 μm[16]. The project aims at the development of a process that re-uses the oxidized Si wafer using the VEST technique (Vias Etching to Separate Thin Film from the Substrate)[17] and subsequently bond the film to a cover glass. A $5\times10cm^2$ test solar cell using this approach reached an efficiency of 11.8%[18]. Mitsubishi are aiming at a module cost of US$2/Wp by the year 2000 using the VEST process.

At the recent 14th European PV Conference, 11.0% efficiency was reported for a 30 μm thick thin film silicon solar cell deposited onto SiC coated graphite substrate using ZMR and CVD epitaxtial depositions by ASE and fabricated into a solar cell by the Fraunhofer Institute[19].

Astropower Corp., USA, is perhaps the only organization which has developed the ZMR based thin film silicon solar cell process on a ceramic substrate beyond the laboratory scale. The composition of the ceramic and details about the deposition process are not yet disclosed. The best independently

confirmed cell efficiency of a $1cm^2$ cell is now 15.6%[20]. In the most recent publication, Astropower reported 11.6% efficiency for a 675 cm^2 monolithically-interconnected module[21].

Tonen Corporation, Japan, has deposited pc-Si films using plasma spraying method which allows for extremely high deposition rates exceeding 10 μm/sec and produces grains of more than 20 μm in size[14]. Daido Hoxan Inc., Japan[22] is continuing this process and is able to achieve grain sizes of up to 5mm×10mm. The thickness of the layer is around 500μm. Most as-grown sheets showed a minority diffusion length of over 20μm. With post-growth gettering and hydrogen passivation, the minority diffusion length was improved up to 58.9μm. A $1.05cm^2$ test cell showed a conversion efficiency of 10.7%.

Low-temperature deposition techniques, well below the melting point of silicon, have attracted considerable attention since the 1980s for the formation of thin c-Si layers. Reduced impurity incorporation, compatibility with a wider range of substrate materials and reduced thermal expansion mismatch between the layers and the substrate are possible benefits of the low growth temperatures achievable with solution growth, a process similar to liquid-phase epitaxy. Barnett *et al.*[23] have demonstrated large-grained (>100 μm) continuous pc-Si thin films on steel, quartz and ceramic substrates from tin solutions at temperatures around 900°C.

The first activities to grow Si on glass by solution growth were started several years ago in the Photovoltaic Special Research Centre at University of New South Wales, Australia. The Sn based alloys with additions of Al and Mg were used to initiate nucleation by reducing SiO_2 on the glass surface. Nucleation was improved by depositing Si near the softening point of the glass by quasi-rheotaxie. Continuous pc-Si thin films on glass, with grain sizes up to 5 mm^2 and covering an area of 15 cm^2, were demonstrated by low temperature solution growth (below 800°C)[24, 25].

Max-Planck Institute für Festkörperforschung at Stuttgart deposited Si on quartz and glass substrates from Ga/Al alloys by using an Al-Si interlayer on top of the glass substrate and maximum grain size above 100 μm was obtained[26]. They recently also reported on the growth of pc-Si and pc-SiGe layers on glassy substrates from metallic solution in a centrifuge and tipping boat system. High speed spinning of the metallic solution in a centrifuge system overcomes surface tension and injects the metallic solution into the pores of a porous substrate. Si nucleation occurred in the pores upon cooling the solution and continuous pc-Si and Si-Ge layers were obtained by this method. The Si layers grown from In/Al solution exhibited much lower doping concentration (30~60Ω-cm) using this technique[27].

Similar to the solution growth technique, SUNY (State University of New York) at Buffalo reported on the growth of pc-Si layer on glass or Ti coated glass substrates using the vapor-liquid-solid process[28]. A thin prelayer of In or Sn was initially deposited on the substrate, followed by the DC sputtering of Si at substrate temperature around 700°C. During Si deposition, the metal is initially saturated with Si and subsequently becomes supersaturated with Si and thus Si solidification occurs. The Ti-In prelayer produced grain size above 25 μm and a lifetime of about 0.3 μs while a Sn prelayer only produced sub-micron grain size with a lifetime of 6 μs after hydrogenation, as measured by photoconductive decay.

2. *Low temperature crystallization techniques*

The recent effort directed at producing active-matrix liquid crystal displays based on pc-Si thin film on glass has resulted in significant progress in developing pc-Si thin films on glass at low

temperatures (<600°C)[29]. Laser crystallization of a-Si using excimer lasers has shown great potential to produce high quality pc-Si materials although the material is usually fairly thin (<5000Å) due to the small absorption depth at UV wavelength. The crystallization process and grain size is strongly determined by the hydrogen content in the a-Si film, pulse energy, number of pulses and substrate temperature. Multiple pulses are usually used in the process, with the first few pulses to dehydrogenate the a-Si sample[30] and the following pulses to crystallize the material. Large grained pc-Si is usually obtained by using such multiple pulses or keeping the substrate at high temperature during laser crystallization. The former approach continuously increases the grain size by multiple melting and resolidifying the Si film[31]. During this process, the small grains and defective crystals were melted and swallowed up by the surrounding big grains. The latter approach reduces the temperature gradient across the film thickness and thus the solidification rate is reduced, which results in a grain growth enhancement[31]. Although this technique may not be able to produce thick Si layer (>5000 Å) for thin film solar cell applications, it will certainly provide a good quality crystal seeding layer.

Solid phase crystallization (SPC) is another low temperature process being developed in the recent years for active-matrix liquid crystal displays. The first attempt at using this technique for thin film Si solar cell application is by Sanyo Corp., Japan. Sanyo uses SPC to produce pc-Si thin films on textured glass using a "partial doping" technique[32]. A thin layer (2000 Å) of heavily phosphorus doped (~$10^{20}/cm^3$) silicon was initially deposited on the glass substrate, followed by an intrinsic a-Si:H deposition with a thickness of 10 μm. The film was then annealed at 600°C in a N_2 ambient for 10 hours. A uniformly doped pc-Si film, with grain sizes up to 6 μm, was obtained on glass with an electron mobility of $623cm^2/Vsec$. An unconfirmed conversion efficiency of 8.5% was reported for a thin film silicon solar cell based on this approach. Subsequent refinements have increased this value to 9.2% (also unconfirmed)[33].

Max-Planck Institute at Stuttgart has investigated a similar approach to produce the pc-Si seeding layer on a unspecified home-made high-temperature glass substrate. The intrinsic or phosphorus doped a-Si precursor layer was deposited using a disilane based LPCVD process, which is known to produce large grain size pc-Si after SPC. The pc-Si layer after SPC exhibited grain sizes up to 7 μm. A photovoltaic active layer with thickness about 3 μm was then epitaxially deposited on the pc-Si seeding layer. The device exhibited a Voc of 370 mV after hydrogen passivation. The poor device performance was attributed to high recombination at grain boundaries[34].

Selective SPC is an approach which has the potential to achieve large grain size and controlled grain boundary locations in thin film Si material. Selective SPC has been reported to be achieved by selectively Si self-implantation[35], selective metal deposition to create metal induced nucleation spots[36] and selectively laser crystallisation to produce controlled nucleation spots[37]. Large grain size up to 25μm has been reported for thin film pc-Si by using metal induced selective SPC. However, the upbound of grain size is limited by the bulk nucleation in the Si film.

3. Recent development in thin film μc-Si Solar Cells

In the recent years, microcrystalline silicon has been successfully produced by PECVD (plasma enhanced chemical vapor deposition) and HWCVD (hot wire CVD) deposition using hydrogen diluted silicon precursor gases such as SiH_4, Si_2H_6 and SiF_4. Atomic hydrogen serves two functions during deposition, namely etching off defective silicon material[38] and enhancing surface mobility of the incoming silicon atoms from the plasma[39]. A ordered crystalline

structure is obtained. Microcrystalline silicon has been widely applied as the window layer for a-Si:H solar cells and for c-Si based heterojunction solar cells.

Since 1994, encouraging cell efficiencies have been reported for μc-Si thin film solar cells deposited on glass by Kaneka and the University of Neuchatel. Kaneka's approach[40] was to initially deposit a very heavily n^{++}-type thin layer (0.3 μm) of a-Si:H on glass (Corning 7059). This layer was subsequently crystallized using an excimer laser. The resistivity of the crystallized layer is around 5mΩ·cm which is low enough to be used as an electrode. Kaneka wanted to use this laser crystallized poly-Si layer for two purposes, namely as a back contact of a solar cell and as a nucleation layer for further Si deposition. More silicon, up to 4μm, was then deposited using PECVD. Although the n^{++} layer has no seeding effect on the following Si deposition, it does affect the crystalline quality and surface texture of the subsequent silicon layer deposition. The emitter of the cell is formed by a p-type μc-Si deposited on the poly-Si followed by ITO transparent contact deposition. The poly-Si layer was deposited using PECVD at substrate temperatures from 400~600°C with a deposition rate up to 25 Å/sec. The emitter was deposited at a temperature of 200°C. The total thickness of the solar cell device is about 3.6 μm. Recently Kaneka reported a cell efficiency of 9.4% for a 1 cm^2 cell using this approach with Voc of 480 mV, Jsc of 26.1 mA/cm^2 and FF of 75%. They attributed the high Jsc to the low doping level, ~$10^{16}/cm^3$, of the device as well as the textured surface of the device. The effective minority carrier's diffusion length (Leff) is far above 10 μm which is more than twice of the film thickness. The effective optical thickness of the device is about 70 μm.

The university of Neuchatel[41] has developed μc-Si thin film cells and "micromorph" a-Si:H/μc-Si:H tandem cells using a very high frequency glow-discharge (VHF-GD) technique. The VHF-GD process at 70 MHz and at higher plasma excitation frequencies favours the quality of μc-Si:H compared to the use of a standard RF glow discharge at 13.56 MHz. Figure 1 shows, in particular, the optical absorption of μc-Si:H deposited by VHF-GD at an excitation frequency of 70 MHz.

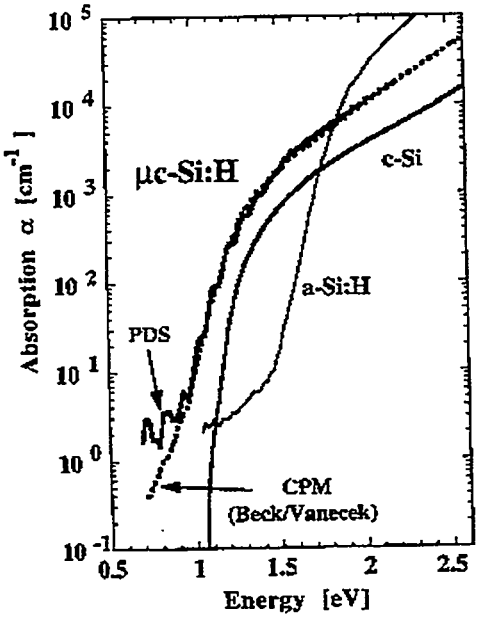

Fig. 1 Absorption spectra of a μc-Si:H film characterized by PDS and by CPM. The film is deposited on Corning glass. For comparison, the spectra of amorphous and crystalline silicon are added[41].

In contrast to all previous work performed on μc-Si:H, a more pronounced absorption edge is observed for μc-Si:H deposited by VHF-GD. The energy gap deduced is about 1 eV. Compared to a-Si:H and c-Si, the absorption edge of μc-Si:H is shifted to the infrared, into the vicinity of that of c-Si and the remaining subband-gap absorption turns out to be rather low. The overall absorption of μc-Si:H is increased over the whole spectrum used for photovoltaic energy conversion. The μc-Si:H p-i-n cells were deposited using strongly hydrogen diluted silane plasma at substrate temperatures about 220°C. As the undoped μc-Si:H exhibits a strong n-type character, adding small amount of diborane to the feed stock gas during deposition was necessary to obtain intrinsic μc-Si:H (microdoping). The microdoping process is eliminated by introducing a gas purifier and thus a truly intrinsic μc-Si:H is obtained. This leads to a remarkable increase of the spectral response at long wavelength. A total thickness of 3.6 μm p-i-n μc-Si:H cell exhibited an unconfirmed energy conversion efficiency of 7.7% over an area of 0.33 cm^2, with Voc of 448 mV, Jsc of 25.3 mA/cm^2 and FF of 68%. The high current density for such a thin cell is attributed to the higher absorption coefficient of μc-Si:H over the whole spectrum. The micromorph a-Si:H/μc-Si:H tandem cell exhibited an energy conversion efficiency of 13.1% over an area of 1 cm^2[41].

4. Multi-junction thin film Si solar cells

A novel parallel multijunction thin film Si solar cell was proposed at the Photvoltaic Special Research Centre, University of New South Wales, Australia[42]. The multijunction solar cell provides a new approach for achieving high efficiencies from poor quality material, with near unity collection probabilities for all generated carriers achieved through appropriate junction spacing. Heavy doping is used to minimize the dark saturation current contribution from the layers, therefore allowing respectable voltages and producing high lateral conductivity. The multijunction structure also has higher tolerance to grain boundaries than the single junction device. Figure 2 shows the schematic of the impact of both vertical and horizontal grain boundaries on both single junction and multijunction devices, in which all regions in closer proximity to a grain boundary than a junction, are considered inactive and therefore shaded. Quite clearly the multijunction structure has far greater tolerance to grain boundaries in terms of current collection than a conventional single junction device. Figure 3 shows an EBIC micrograph of a multijunction thin film Si solar cell. The inactive area along the vertical grain boundary is confined in the region in the immediate vicinity as outlined in Fig. 2c.

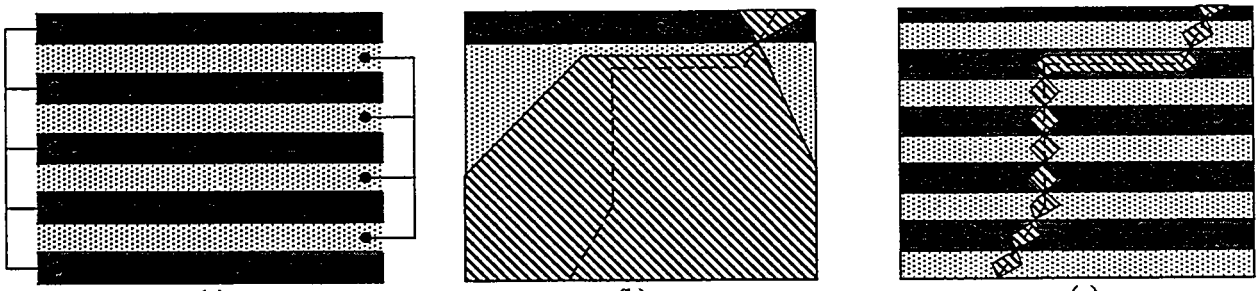

Fig. 2 A schematic of the impact of both vertical and horizontal grain boundaries on both single junction and multijunction devices, in which all regions in closer proximity to a grain boundary than a junction, are considered inactive and are shown shaded.

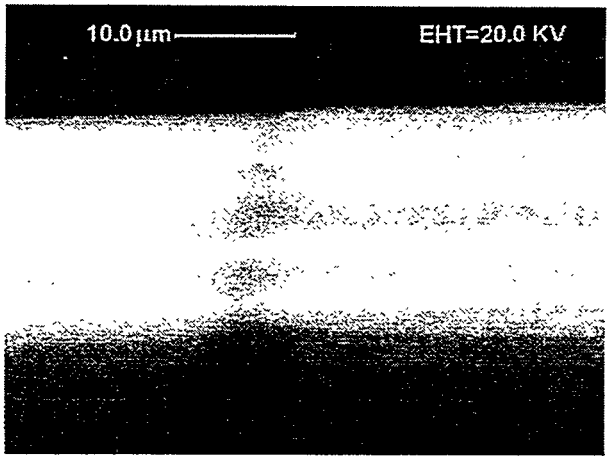

Fig 3. Higher magnification EBIC image (20kV) of a vertical grain boundary in an experimental multijunction device. The electron beam is incidentally at 90° to the cleaved surface.

Pacific Solar Pty. Ltd., Sydney, Australia, a joint venture between the Unisearch Ltd, the commercial arm of the University of NSW, and Pacific Power, a leading Australian electricity utility, is developing the multijunction thin film Si solar cell technology as a commercial product. Figure 4 shows a working prototype of the product being developed at Pacific Solar.

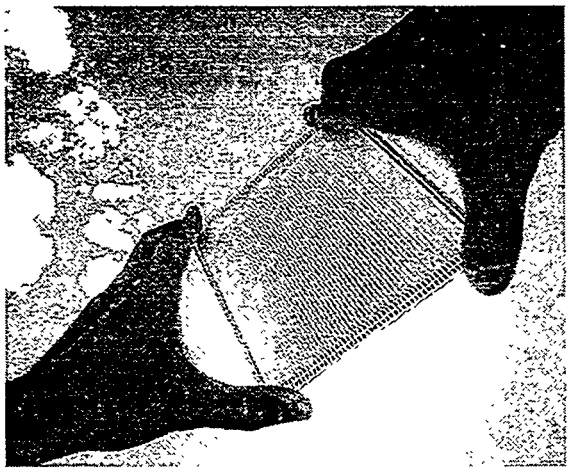

Fig. 4 Series interconnected thin-film silicon prototype sub-module (15cm×15cm) fabricated by Pacific Solar.

Other Issues for Thin Film Silicon Solar Cells

1. Light trapping

Thin film c-Si solar cells can achieve high efficiencies only if light trapping can be used to give a long optical path length, while simultaneously achieving near unity collection probabilities for all generated carriers. Light trapping offsets the relatively weak absorption of light in the near bandgap region of Si by maximizing the optical path length of light within the device. The methods of light trapping can be divided into three categories, namely, randomizing or

Lambertian scheme and geometrical schemes. Goetzberger[43] showed that the fraction of light reflected by total internal reflection at the illuminated surface is equal to $1-1/n^2$, where n is the refractive index of Si (~3.4). He pointed out that the front surface is highly reflective to Lambertian distributions of light, reflecting about 92% of incident light by total internal reflection. Yablonovitch showed that weakly absorbed light of Lambertian distribution travels an effective path length of $4n^2$ times the physical thickness of a non-absorbing layer. This path length enhancement is about 50 times for Si. Randomizing texturing can be achieved by a number of methods including sand blasting, "natural lithography"[44], porous etching[45], rapid thermal processing of an aluminum-Si interface[46], or by the use of random textured ancillary dielectric layers such as ZnO[46] or SnO_2[47].

Geometrical light trapping scheme is relatively easy to form on single c-Si surfaces by taking advantage of the orientation dependent etch rates generated by alkaline solutions. Common textures include 54 degree pyramids, inverted pyramids, slats and perpendicular slats. The Max-Planck Institute[48] reported a light trapping scheme of thin film pc-Si solar cells on glass using the so called "Encapsulated-V texture" with a back surface reflector. The experimental realization of the Encapsulated-V texture and ray tracing simulations showed that a maximum short circuit current density of 35 mA/cm^2 is feasible for a c-Si cell with a layer thickness of only 4 μm. This large current is primarily due to the shallow groove angle that reduces front surface reflectance and increases the active Si volume, and the detached back surface reflector. The University of New South Wales, Australia[49] developed a conformal light trapping scheme by conformally depositing Si on substrates textured with feature sizes greater than the film thickness. Ray tracing studies showed that 3D textures can provide a significant advantage over grooves, and with small enough features can out-perform Lambertian light trapping. Excellent antireflection properties and re-entry of escaping rays are responsible for the good performance. The reduced scatter with large textures can be compensated by adding a mildly scattering sub-facet microtexture. Reflectance measurements of a conformal a-Si:H film show good agreement with predictions.

2. Bulk and surface passivation

Hydrogen passivation or hydrogenation is widely used in research as well as in commercial fabrication of solar cells and thin film transistors (TFT). Hydrogen passivation has been shown to be an effective method for the reduction of the activity of the defects and grain boundaries. Hydrogen introduced into pc-Si is reported to diffuse in the positive charge state (H^+) and enhance the electrical conductivity[50]. The hydrogenation results in a decrease of the defect activity, thereby improving the electrical properties of the materials and devices[51-54]. The dangling-bond density is reported to decrease as a function of hydrogenation time to a residual saturation value that strongly depends on the passivation technique and passivation temperature. One of the most thoroughly investigated hydrogenation methods, so far, has been to immerse the pc-Si sample in the plasma produced by an RF glow discharge based on parallel plate reactor [55-57]. Another method is by immersing pc-Si sample in an electron cyclotron resonance (ECR) plasma [57, 58]. In both RF and ECR plasmas, the introduction of hydrogen into the device is accomplished through plasma-ion penetration and bulk diffusion. The rate of ion penetration is dependent on the plasma-ion density. An RF hydrogen plasma typically has an ion density of $n_i \approx 10^9/cm^3$, while for ECR hydrogen plasma, density can be as high as $n_i \approx 10^{11}/cm^3$. During hydrogenation, the pc-Si is usually kept near 300-450°C to enhance hydrogen diffusion. The relatively low ion densities characteristic of RF plasmas necessitate long processing times. While an ECR plasma has a higher ion density, the sheath potential limits the hydrogen ion current to the pc-Si devices, which also prolongs processing time. Plasma ion implantation (PII) is reported

to provide adequate hydrogenation of pc-Si within a short processing time [59, 60]. The PII process is performed by repetitively applying a large negative voltage pulse to a wafer placed in a hydrogen plasma. Hydrogen ions are accelerated by the target potential and implanted into the sample. Ion energies can range from 1-100 keV with average ion flux densities as high as $10^{16}/cm^{-2}$ sec^{-1}. The primary mechanism for the introduction of hydrogen into the device is ion implantation and additionally ion penetration takes place between the pulses. All these effects tend to enhance dose rates over methods which rely on surface penetration and bulk diffusion.

Surface passivation is frequently mentioned as being far more important than the bulk material quality in thinner devices. Low temperature surface passivation has been extensively studied by using PECVD deposited SiN[61, 62]. Significant progress in low temperature surface passivation of c-Si solar cells has taken place using SiN layer deposited in a remote PECVD system. Surface recombination velocities as low as 4 cm/s on polished 1.5 Ωcm FZ p-type Si wafers have been demonstrated by this approach[63]. In addition, growing interest has been shown in making use of phosphorus-doped surfaces on both the front and rear, owing to the resulting improvement in the effective surface passivation.

Conclusion

There has been increased research and development activities directing at developing thin film c-Si solar cells in recent years. The medium to high temperature processing technologies, including ZMR plasma spray and solution growth, are able to produce pc-Si materials with grain size greater than 100μm. Conversion efficiencies above 10% have been demonstrated by solar cells fabricated using these approaches. With advent of pc-Si liquid crystal display (LCD) technology, low temperature crystallization technologies such as laser crystallization and solid phase crystallization (SPC) were developed to produce pc-Si materials on glass substrates. The grain size obtained by these techniques is much smaller than those produced by higher temperature liquid phase approaches. However, quite respectable efficiencies up to 9.2% have been reported for the cell fabricated upon SPC materials.

There is significant difference in opinion as to the quality of pc-Si material which is required to achieve high performance thin film solar cells. Quite reasonable efficiencies, up to 9.4% have been reported for thin film μc-Si solar cells deposited on glass by PECVD from heavily hydrogen diluted silane gas. A recently developed multijunction solar cell structure provides a new approach to achieve high efficiencies from very quality material, with near unity collection probability achieved through the appropriate junction spacing.

Light trapping is essential for thin film Si solar cells. Both theoretical calculations and experimental measurements indicate that appreciable current (above $35mA/cm^2$) can be achieved for a thin c-Si film (4μm) deposited on an appropriately textured glass substrate.

Hydrogenation is an effective way to passivate grain boundaries and defects present in thin film Si materials. Both majority carrier mobility and minority carrier lifetime can be significantly improved by this process. Deposition of SiN on Si by PECVD is a promising low temperature surface passivation approach which is quite suitable for surface passivation of thin film Si solar cells deposited on low temperature substrates such as glass, although the surface passivation can be effectively achieved by using heavily doped n^+ or p^+ surface.

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Optical Confinement Effect for Below 5 μm Thin Film Poly-Si Solar Cell on Glass Substrate Fabricated at Low Temperature

Kenji YAMAMOTO, Takayuki SUZUKI, Masashi YOSHIMI,
Yoshifumi OKAMOTO, Yuko TAWADA and Akihiko NAKAJIMA
Central Research Laboratories, Kaneka Corporation, 2-80 Yoshida-cho,
Hyogo-ku, Kobe 652, Japan

ABSTRACT

The optical confinement effect of a thin film poly-Si solar cell on a glass substrate fabricated by plasma chemical vapor deposition (CVD) at low temperature has been investigated for a cell thickness of less than 5 μm. The structure of the cell is glass / back reflector / *n-i-p* poly-Si / ITO / Ag grid. The cell with a thickness of 3.5 μm demonstrated an intrinsic efficiency of 9.8%, as independently confirmed by Japan Quality Assurance. The cell is well characterized by the structure of naturally surface texture and enhanced absorption with a back reflector (STAR). The optical confinement effect of the cell with STAR structure explains both the excellent high short circuit current density of above 27 mA / cm^2 for the 4.7 μm thick cell and the markedly high quantum efficiency at long wavelength light as determined through PC1D analysis. At 1.5 μm-thick cell, the short circuit current density strongly depends on the surface feature of back reflector. Both quantum efficiency and reflectance at long-wavelength light of the cell are well correlated to the surface features of the cell. Our newly developed a-Si:H/poly-Si/poly-Si three-stacked solar cell exhibits the stabilized efficiency of 11.5 %.

1. INTRODUCTION

The use of thin-film polycrystalline silicon (poly-Si) for solar cells is one of the most promising approaches to realizing both high performance and low cost. Several thin film silicon growth techniques for solar cells have been reported[1-9]. Our aim is the fabricate a thin-film poly-Si solar cell on a glass substrate as is the case with an a-Si:H solar cell to realize a cost-effective and high-performance solar cell. Developing a low-temperature process for fabricating high-quality poly-Si thin films is essential for this purpose. We had been developed a novel low temperature process for fabricating thin-film poly-Si solar cell on glass substrates[1-4]. We demonstrated the excellent short circuit current density of thin film poly-Si solar cell (2-8 μm thick) on glass substrate despite of the low temperature fabrication[1-4]. It is a key issue for thin film poly-Si solar cell design achieving a high efficiency to enhance optical absorption since it enables the short circuit current density to be sufficiently high even in a few micron thick thin film poly-Si solar cell, which leads to cost reduction for the fabrication of poly-Si films. However there have been few reports on experimental studies of light trapping in a few micron thick thin film of poly-Si solar cell[10].

Here we report on the clear demonstration of enhancement of optical absorption of a thin film poly-Si solar cell. We would like to introduce our thin film poly-Si solar cell with "STAR Structure", which means that the cell structure and properties are well characterized by naturally surface texture and enhanced absorption with a back reflector. The optical confinement effect of a thin film poly-Si solar cell with STAR structure has been systematically investigated[11]. We have further studied the effect of surface feature by analyzing the quantum efficiency curve and reflectance. Moreover the performance of a new type of three stacked solar cell is demonstrated.

2. EXPERIMENTAL

A summary of the cell fabrication process follows. After the formation of the back reflector on a glass substrate, *n*-poly-Si films were deposited on it by plasma CVD or an improved

plasma CVD process[12]. Next, intrinsic(*i*) poly-Si film as an active layer was deposited on it by plasma CVD at a substrate temperature of less than 550°C. A *p-n* junction was formed by the deposition of *p*-type μc-Si:H. ITO was deposited on the solar cell as the transparent electrode. A Ag grid electrode was formed on top of the ITO. All fabrication processes were carried out with a maximum process temperature of less than 550°C. We believe that the *i*-layer has a slight *n*-type character since it is deposited on an *n*-type layer and the resulting impurity of *i*-poly-Si is thought to be oxygen[6]. Moreover the carrier concentration of *i*-layer would be around $1x10^{16}$ cm^{-3} as discussed below. Further investigation is needed. The diffusion length of our cell was determined by the intercept from the linear extrapolation of inverse surface photovoltage (SPV) vs light penetration depths for 670 nm and 980 nm under constant photon flux of $10^{15}/cm^2sec$.

3. RESULTS AND DISCUSSION

3.1 The performance of thin film poly-Si solar cell with STAR structure.

Figure 1 shows a schematic view of our thin film poly-Si solar cell with STAR structure. One of the characteristics of this cell is its natural surface texture. We have found that the surface features (texture) of poly-Si film can be changed *in situ* by control of the process conditions. An AFM image of the top surface of our poly-Si solar cell with STAR structure shows dendrite-like morphology with a surface roughness of the order of 0.2 μm for around 4μm thick cell. This surface texture would be expected to facilitate the optical confinement. In particular reflection control by texturing is one of the most important technologies for increasing the short circuit current density of thin film Si solar cells. Another characteristic of our thin film poly-Si is expressed by the columnar structure and strong (110) preferred orientation as determined by XRD measurement (see Fig. 2). In TEM analysis, no clear grain boundary was observed perpendicular to the growth direction[1]. It is expected that the structure of our poly-Si film is preferable for solar cells of which the carrier passes along a direction perpendicular to the substrate and that the grain boundary is well passivated by the hydrogen during the deposition of poly-Si by plasma CVD at low temperature. It was confirmed that the effective diffusion length which was estimated from the calculated inverse quantum efficiency[13] near the wavelength of 700 -

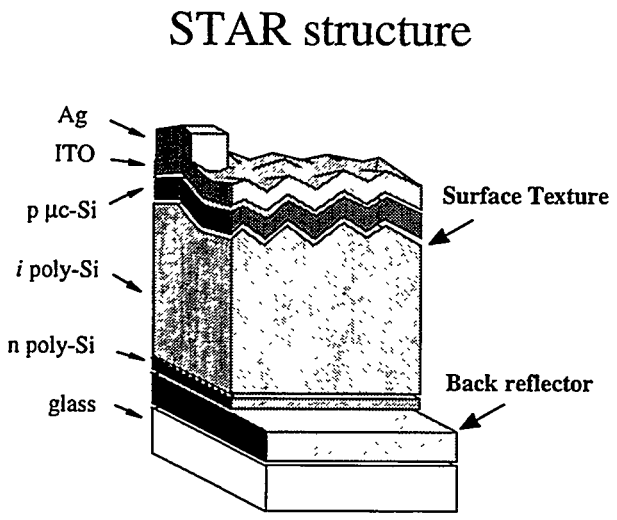

Fig. 1. Schematic view of our proposed thin film poly-Si solar cell with STAR (naturally Surface Texture and enhanced Absorption with back Reflector) structure.
Note that the cell structure are well characterized by the surface textured feature and back reflector.

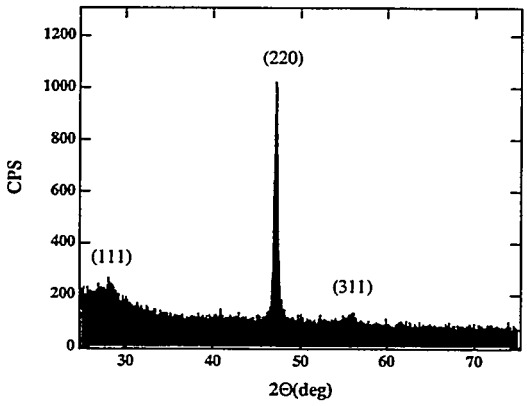

Fig. 2. XRD spectrum of thin film poly-Si on glass substrate fabricated by plasma CVD.

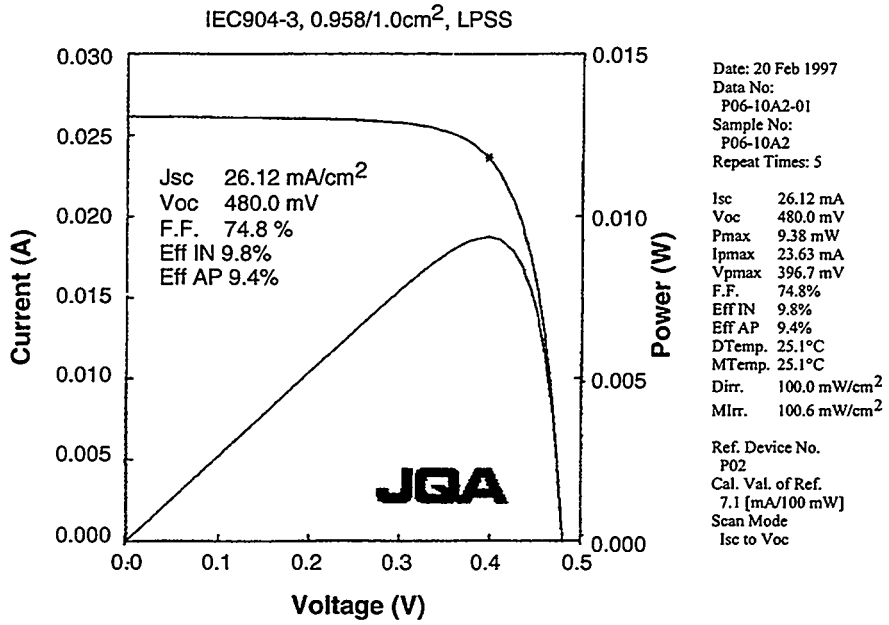

Fig. 3. The performance of the 3.5 μm-thick poly-Si solar cell with STAR structure confirmed by Japan Quality Assurance (JQA) and measurement conditions.
Eff IN and Eff AP represent the intrinsic and aperture solar cell efficiency, respectively. The discrepancy between the intrinsic and aperture efficiency comes from the Ag grid electrode on the ITO.

800 nm is longer than that of the cell thickness[1-4,11].

The performance of the 3.5 μm thick our poly-Si solar cell with STAR structure is shown in Fig. 3, and was independently confirmed by Japan Quality Assurance (JQA). We have obtained a short circuit current density (Jsc) of 26.12 mA/cm^2 and an open circuit voltage (Voc) of 0.480 volt. Prominently high Jsc of the 3.5 μm thick solar cell was obtained, while the Voc was fixed to the quite low value of 0.480 V. As mentioned in previous reports[1-4], the low Voc is plausibly explained by the leakage current of the *p-i-n* junction being much higher than that of a conventional *p-n* junction due to the higher electron and hole recombination density, which leads to lowering of the Voc. The calculated Voc as a function of carrier concentration[4] made it appear that Voc decreases with decreasing carrier concentration for the same diffusion length of each solar cell. As a future task, it will be important to adjust the carrier concentration to an appropriate value.

For the first step toward the large area production, we have prepared a thin film Si solar cell with the size of 5 inches by 5 inches. Figure 4 shows the contour-map of diffusion length determined by SPV method[14]. Although

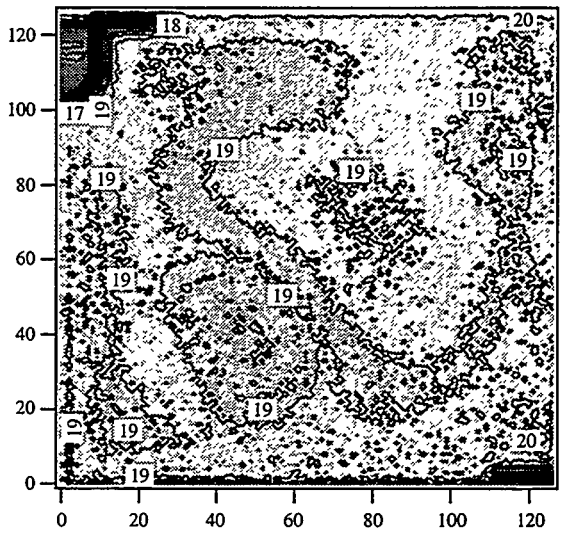

Fig. 4. The counter-map of diffusion length determined by SPV method. The diffusion length of cell was determined by the intercept from the linear extrapolation of inverse surface photovoltage (SPV) vs light penetration depths for 670 nm and 980 nm at constant photon flux of 10^{15}/ cm^{2}sec.

the absolute value of evaluated diffusion length (around 19 μm) may include the error due to the fact that the calculated diffusion length is longer than that of the thickness (beyond the SPV detection limit), it would be mentioned that the uniformity of diffusion length is quite excellent over 5 inches substrate.

3.2 Optical confinement effect of thin film poly-Si solar cell.

The quantum efficiency spectrum of a 4.7 μm thick solar cell with STAR structure was investigated, and is shown in Fig. 5 (a). Experimental results are plotted as the open circles in this figure. A markedly high quantum efficiency at long wavelength was observed even in the 4.7 μm thick silicon solar cell. Note that the Jsc for AM 1.5 obtained by integration of the quantum efficiency curve is over 27 mA/cm^2. Experimental results are modeled from PC1D[13,15] by assuming the light trapping parameter (ρ_{fi}), which is defined as the internal global reflectance at the front surface in PC1D. The three curves shown in Fig. 5 (a) are the calculated curves for ρ_{fi}= 0, 70, and 92 % with assumption of constant back reflectance (95 %) for each case, respectively. Other conditions for the calculation are listed in Table I. The shape of the experimental curve was well modeled from PC1D by assumption for ρ_{fi} =70% and an appropriate diffusion length L_{dif} = 7 μm. The values we extract ρ_{fi} indicates that our thin film poly-Si solar cell with STAR structure enables the few micron thick cell to yield efficient optical enhancement. Concomitant with optical enhancement of absorption, we find that the Jsc increase by optical enhancement is 3.7 mA/cm^2 from the calculated values in Fig. 5 (a). Further Jsc enhancement of 2.2 mA/cm^2 can be achieved by optical confinement up to ρ_{fi} = 92 % without increase of the thickness and improvement of the film quality. For evaluation of the effective optical length of this solar cell, the inverse of the internal quantum efficiency (I.Q.E.) based on Fig. 5 (a) was investigated as a function of the inverse of the absorption coefficient as shown in Fig. 5 (b). The data for the reflectance of our solar cell and the absorption coefficient of Si were estimated based on the measured reflectance and data for that of single crystal Si, respectively. An effective optical thickness (*Wopt*) of 280 μm and a corresponding effective

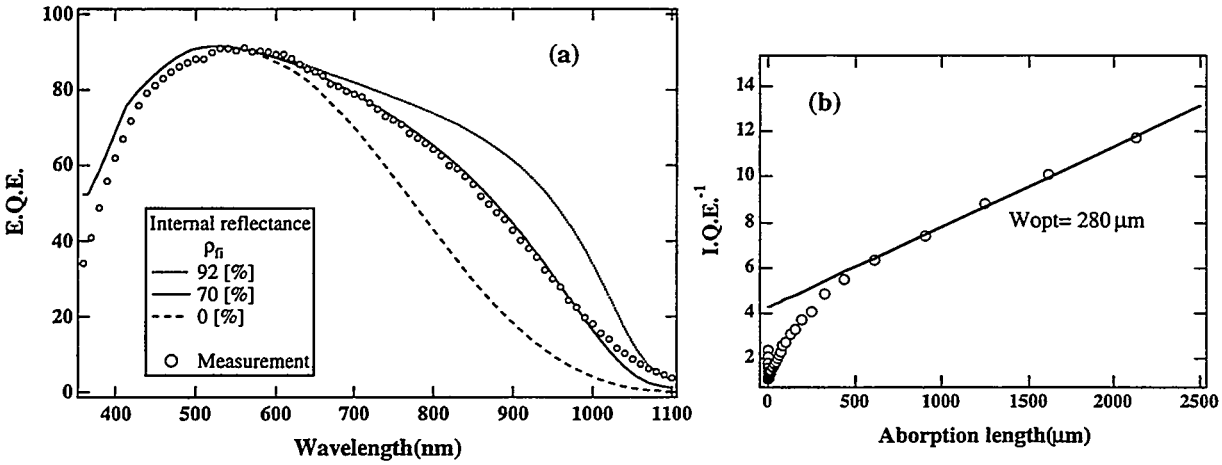

Fig. 5. (a) The external quantum efficiency (E.Q.E.) spectrum of 4.7 μm-thick solar cell with STAR structure. Experimental results are plotted as the open circles. The three curves (broken line, solid line, dotted line) are the calculated curves for ρ_{fi}= 0, 70, and 92 % based on PC1D under the conditions listed in Table I, respectively. ρ_{fi} is defined as the internal global reflectance at the front surface in PC1D.
(b) The inverse of the internal quantum efficiency (I.Q.E.) as a function of the inverse absorption coefficient. I.Q.E. was determined from the above quantum efficiency spectrum and by reflectance measurement of our solar cell. The absorption coefficient of Si was used as that of single crystal Si. *Wopt* in this figure means the effective optical thickness.

Table I. Conditions for the PC1D calculation of the three curves shown in Fig. 5 (a).

p-layer thickness	30 nm
i -layer thickness	4.7 μm
S_r	10^4 cm/s
S_b	10^7 cm/s
diffusion length	7 μm
p-layer doping density	10^{20} cm^{-3}
i -layer doping density	10^{16} cm^{-3}
n-layer doping density	10^{20} cm^{-3}
front internal reflectance	0,50,92 %

optical pass length of 60 times the layer thickness was obtained from the inverse of the slope of long-wavelength light (1050 - 1100 nm). This result also indicates the highly efficient optical confinement of our presented thin film poly-Si solar cell with STAR structure.

The thinner 1.5 μm-thick cell has investigated. This will help to overcome the problem of low deposition rate of poly-Si in preparing at low temperature. It is important to reduce the film thickness with maintaining the cell efficiency. Since our proposed feature size of naturally surface texture depends on the thickness of the cell, 1.5μm thick cell is not good enough to give the textured surface for light trapping. It is necessary to apply the another method for giving the textured feature such as by controlling that of back reflector. We have investigated the enhanced optical absorption of 1.5 μm thick cell by changing the feature structure of back reflector.

Figure 6 and 7 show the surface morphology and the reflectance of two kind ((a) cell on flat back reflector, (b) cell on rough back reflector) of 1.5μm thick solar cells with ITO (80 nm) at the top of it as seen by AFM and reflectance measurement, respectively. The surface feature is changed by that of back reflector, while the rest of conditions are kept constant. The AFM picture shows that one (Fig. 6 (a)) is not so much rough with a surface morphology of the order of 0.1μm and the other one (Fig. 6 (b)) is a surface roughness of the order of 0.2 - 0.3 μm. In Fig. 7 the minimum reflectance at wavelength of 550 nm is appeared at both samples, which is attributed to the effect of 80 nm-thick ITO. The excellent reduction of reflectance near long wavelength region was observed for the cell with the surface of Fig. 6 (b). The effect of surface structure depends on the size of texture relative to the wavelength of incident light. For feature size of 0.1 μm to a few microns, there can be strong interaction between light and features.

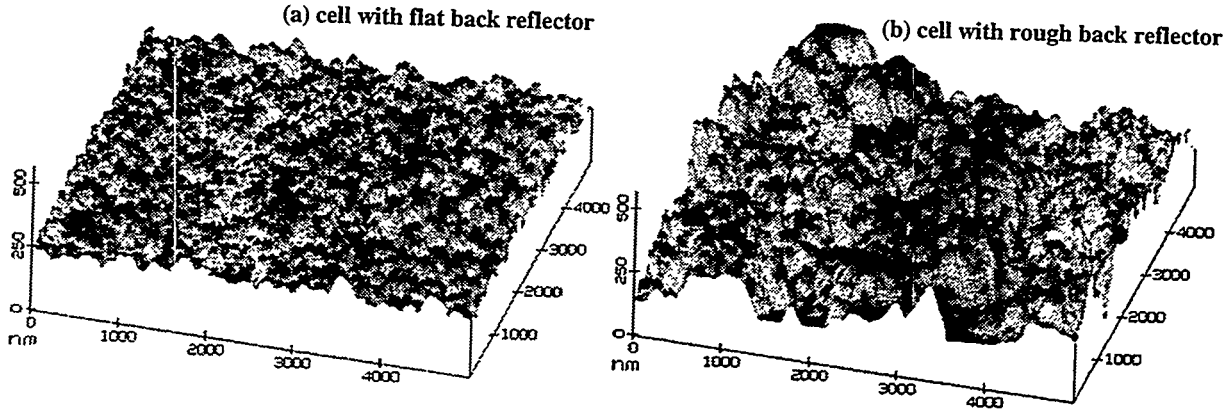

Fig. 6. The surface morphology of two kind ((a) cell on flat back reflector, (b) cell on rough back reflector) of 1.5 μm-thick solar cells with ITO (80 nm) at the top of it as seen by AFM.

Si solar cell with STAR structure was applied to the stacked cell with the combination of a-Si cell. Figure 10 shows the performance of a-Si:H (0.45 μm) / poly-Si (5 μm) two-stacked solar cell, which exhibited the efficiency of 12.9 % and the Jsc of 13.3 mA/cm^2.

In applying the a-Si cell to the stacked cell we must pay attention to the stabilized efficiency, since a-Si has a photo-degradation, while a poly-Si cell is stable[6]. We have prepared the new type of three stacked cell of a-Si:H / poly-Si / poly-Si (triple), which will be less degra-

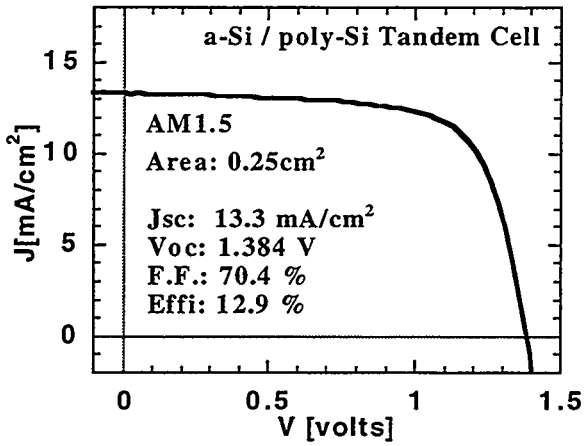

Fig. 10. The performance of the a-Si (0.45 μm)/poly-Si (5 μm) two-stacked tandem solar cell.

dation being used thinner a-Si. We have investigated the stability of both a-Si:H / poly-Si (double) and a-Si:H / poly-Si / poly-Si (triple) cell. The performance of these cells have not been well optimized yet. These devices were then subjected to indoor light soaking under 1 sun (AM 1.5), 50 °C, and open-circuit conditions. Figure 11 compares an example of the change in the device efficiency during light soaking at above conditions for two types of stacked cells. After the 200 h of exposure, the cell performance was substantially stabilized. The triple cell shows a stabilized efficiency of 11.5 %.

4. CONCLUSION

We have demonstrated the highest efficiencies of 9.8 % of ploy-Si solar cell with STAR

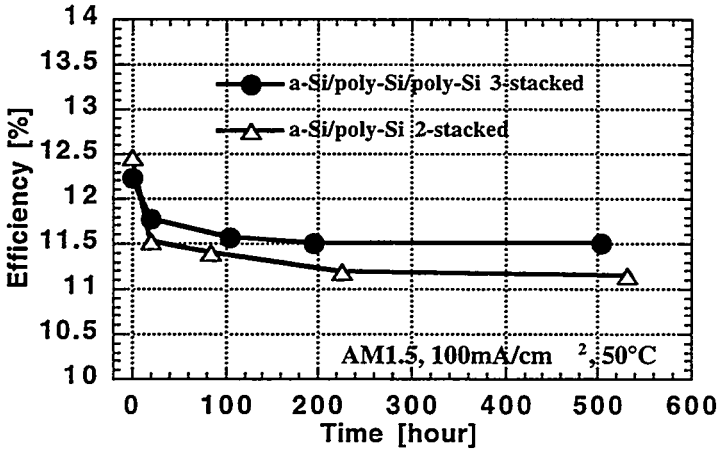

Fig. 11. The change in the device efficiency during indoor light soaking under 1 sun and 50°C. The circle and triangle show the three and two stacked cell, respectively.

structure. The optical confinement effect of the cell with STAR structure explains both the excellent high short circuit current density of above 27 mA / cm^2 for the 4.7 μm thick cell and the markedly high quantum efficiency at long wavelength as determined through PC1D analysis. By introducing the rough surface of back reflector, 9.0 % efficiency cell with a thickness of 1.5 μm has been achieved. For the first time we have shown the performance of three-stacked cell (a-Si/poly-Si/poly-Si). Preliminary trial shows the stabilized efficiency of 11.5%.

ACKNOWLEDGMENT

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Technologies for Thin Film Poly-Si Solar Cells

Stephen J. Fonash
Electronic Materials and Processing Research Laboratory, 189 MRI Building, Penn State University, University Park, Pa. 16802

Bhushan Sopori
National Renewable Energy Laboratory, 1617 Cole Boulevard, Golden, Co. 80228

I. Introduction

The technologies needed for manufacturable thin film poly-Si solar cells span substrate materials, doped layers, absorber layers, and light trapping. The substrate layer choice is a cost issue and it drives subsequent possibilities. Clear plastics limit processing temperatures to <200 °C, opaque plastics move this limit to <300 °C, inexpensive glasses must use T< 500 °C, and metal foil and graphite substrates can raise the processing temperature limit to ~900 °C. We examine here the poly-Si material possibilities given these temperature constraints and consider the critical light trapping possibilities. The poly-Si materials to be considered are (I) deposited poly-Si and (II) solid phase crystallized (SPC) and laser crystallized a-Si precursor films.

II. Deposited Poly-Si

In thin film deposited-poly-Si solar cells the silicon deposition avenues available are dictated by the substrate choice. The use of graphite or metal foils means well established, high temperature chemical vapor deposition (CVD) techniques such as low pressure CVD (LPCVD) or atmospheric pressure CVD (APCVD) can be used. In addition, plasma enhanced CVD and hot wire CVD could also be used. When one focuses on the use of inexpensive glasses for cost considerations, the processing temperatures now must be T <500 °C, the deposition approaches start to be limited and, generally, temperature is not enough to crack precursor gases and/or enable polycrystalline film growth. Overcoming these obstacles requires dependence on PECVD or hot wire approaches. Entering this temperature range means attaining the deposition rate needed for manufacturability can be an issue. This is especially critical for i-layer depositions. AMPS computer simulations at Penn State have shown these layers in p-i-n cells must be in the 8 μm to 20 μm range (depending on the light trapping and poly-Si quality) for cell efficiencies ~12-15%. When plastic substrates are considered (processing temperatures < 250 °C, depending on the plastic), then these issues of driving the reactions needed for useful material and attaining the needed deposition rate become quite severe. The table below summarizes some recent work on low temperature (<500 °C) poly-Si on foreign (non-silicon) substrates. As can be seen, hot wire approaches are able to attain good

deposition rates suitable for absorber i-layers at temperatures ~ 400 °C. As can also be seen, the most promising films so far for plastics are PECVD materials but their deposition rates are questionable for i-layer use.

Group	Deposition Temperature (°C)	Precursor Gases	Method	Deposition Rate	Quality
Lim et al., Appl. Phys. Lett. 66, 2888 (1995).	280	$SiF_4/SiH_4/He/H_2$	PECVD	?	m=12 cm^2/Vs
Wang et al., J. Appl. Phys. 77, 6542 (1995).	250	SiH_4/H_2 90%-99% dilution	ECR-PECVD	2.9 A/sec	?
Kim et al., J. Electrochem. Soc. **143**, 2640 (1996).	400	$Si_2H_6/H_2/SiF_4$	Remote PECVD	0.5-1.0 A/sec	?
Srinivasan et al., J. Appl. Phys. **81**, 2847 (1997).	250	$SiH_4/H_2/He$ 2:60:98	Pulsed-Gas PECVD	40 A/min	IR spectra showing dihydride stretching
Fischer et al., 25th IEEE PVSC, 1053 (1996).	200	SiH_4/H_2 1:40	110 MHz PECVD	1.2 A/sec	good
Lee et al., Jpn. J. Appl. Phys. **35**, L1243 (1996).	180	SiH_4/He 1:4	ECR-PECVD	1.9 A/sec	?
Middya et al., cm^2/Vs Materials Research Society Meeting, Spring '96 & '97. European Photovoltaics Meeting, July, 1997	400 250	SiH_4/H_2 5:95 2:98	Hot Wire	15 A/sec 4 A/sec	m= 20 ?
Kalkan et al., text Electrochem. Soc. Meeting, August, 1997	180-310	SiH_4/H_2 3:40	ECR+RF-PECVD	3A/sec	See

Figure 1 gives Raman data for the high density plasma deposited electron cyclotron resonance with/without RF substrate bias (ECR+RF) films of the above table. This data for the 220 °C film show the peak expected at 520 cm^{-1} and no broad feature at ~480 cm^{-1}, indicative of a significant presence of amorphous material. The fall-off in this low wavenumber range does, however, suggest microcrystalline material. However, unlike earlier reports of low temperature microcrystalline materials, these films show very high activation energy for conductivity (~0.66 eV) and low conductivities (~10-9 S/cm) as may be noted in Fig. 2. These facts are very important because they indicate little or no gap state activity in grains or grain boundaries.

Also presented in Fig. 1 are Raman data for films deposited at 120 °C (which also show crystallinity!) and also presented in Fig. 2 are conductivity data (Fig. 2) for films deposited at 310 °C. These show gap state activity. Figure 3 gives the photoluminescence results for the 220 °C and 310 °C films (ECR+ RF) films of Fig. 1. As may be noted, the strong band edge signals indicate that there is little competition from gap state recombination. These microcrystalline materials have band gaps> 1.05 eV. In fact the one with the excellent crystallinity seen in Fig. 1 and the excellent conductivity behavior seen

results of the activation energy analysis of Fig. 2. If one takes this band gap value and the conductivity data of Fig. 2, a carrier mobility > 100 cm^2/vs is deduced.

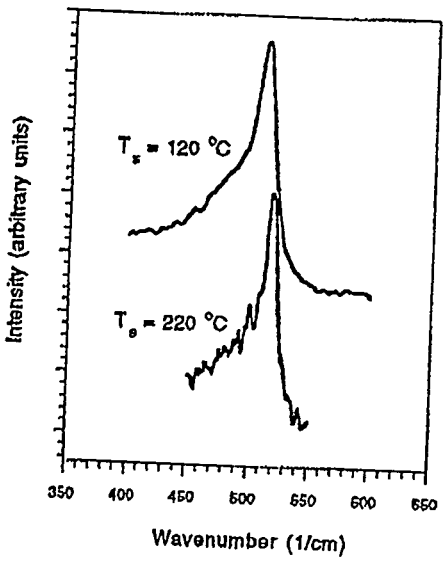


Figure 1. Raman data for films deposited using an ECR HDP source.

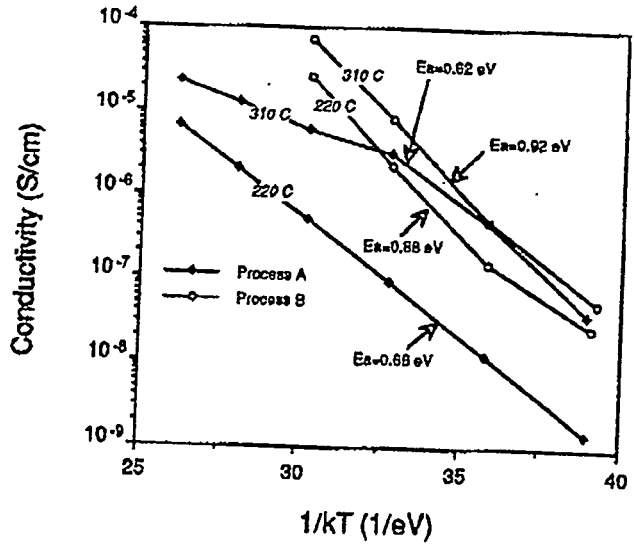


Figure 2. Conductivity and activation energy analysis for ECR+RF (Process) And ECR (Process B)

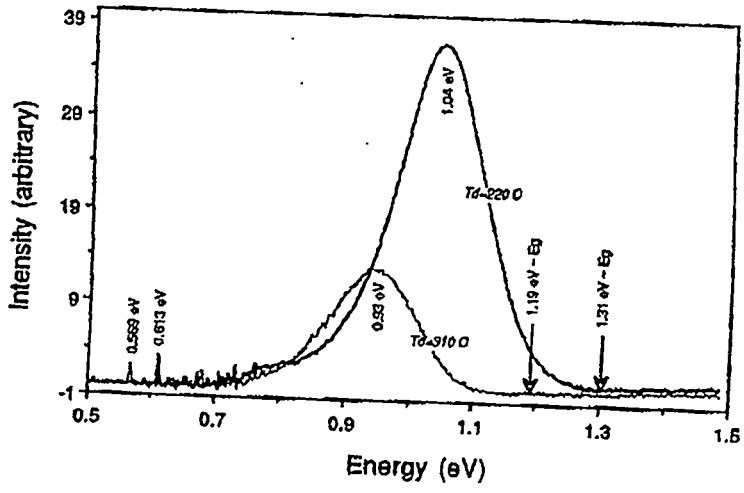


Figure 3. Photoluminescence data for ECR+ RF films deposited at 220 °C and 310 °C.

II. Solid Phase Crystallized and Laser Crystallized Poly-Si

The use of SPC necessitates having a precursor film that converts at a low temperature to poly-Si. Amorphous Si is the precursor of choice since it has no pre-existing nuclei and consequent large grain sizes are possible and because it does not have pre-existing grain boundaries which require high temperatures (~900) for their effective removal. Since SPC is a thermally activated process, crystallization times are of the order of 20 hours at 600 °C for high quality a-Si. This thermal budget can be reduced, however. The time can be significantly reduced (to 5 minutes allowing the use of RTA) or the processing temperature can be significantly reduced (to 500 °C) by using metal induced solid phase crystallization (MISPC). Recently we have achieved the application of the MISPC material using non-vacuum processing involving solutions of the metals. In MISPC only extremely thin applications are needed (~5-10A) to induce these dramatic thermal budget changes.

We have also recently found that different metals can influence the resulting grain size and even optical properties. We discuss below data for MISPC results where the metal was applied by thermal evaporation. Figure 4 shows the XRD data for SPC films crystallized from a-Si with no MISPC treatment (requiring 20 hrs.), with Ni MISPC treatment (requiring < 10 min. for crystallization), and with Pd MISPC treatment (requiring < 10 min. for crystallization). The average grain sizes, measured from TEM micrographs, are noted for each film. The corresponding absorption coefficients are seen in Figure 5. As may be noted, significant absorption enhancement is found in the small grain (microcrystalline) material.

The Raman data for these Pd and Ni MISPC samples are given in Fig. 6. As was the case for the deposited film data of Fig. 1, the Pd MISPC films do yield some signal at the wavenumbers where one expects a contribution from a-Si. If this material is "traditional" microcrystalline material with some a-Si present, the Raman and TEM data suggest that this a-Si content can not be that significant . In addition these films were re-evaluated after an additional 30 hour, 600 °C anneal. The enhanced optical absorption was still present after this anneal even though no amorphous phase could be present. These results all make it difficult to attribute the enhanced absorption coefficient in Fig. 5 to the presence of an a-Si phase.

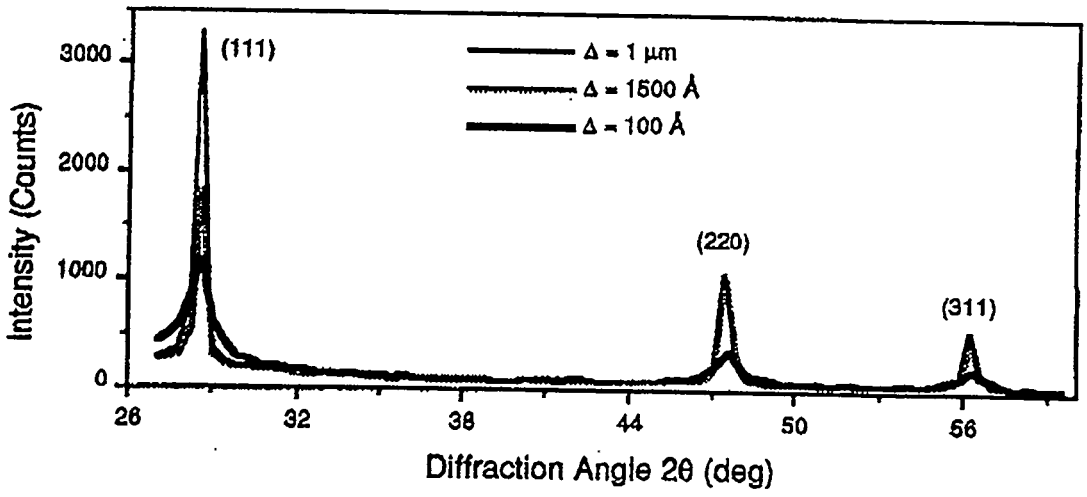


Figure 4. XRD pattern for the films of Fig. 5 and 6. Here ∇ denotes grain size.

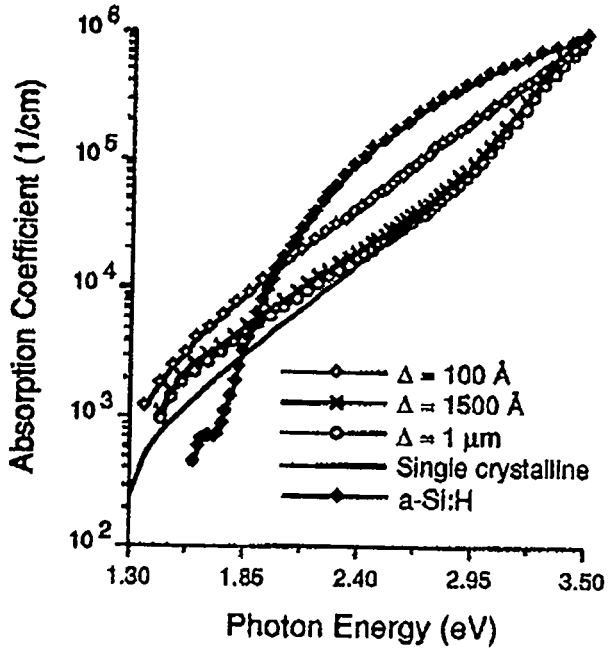


Figure 5. Absorption spectra for the films of Fig. 4 and 6. Data for single crystal and amorphous Si are given for comparison.

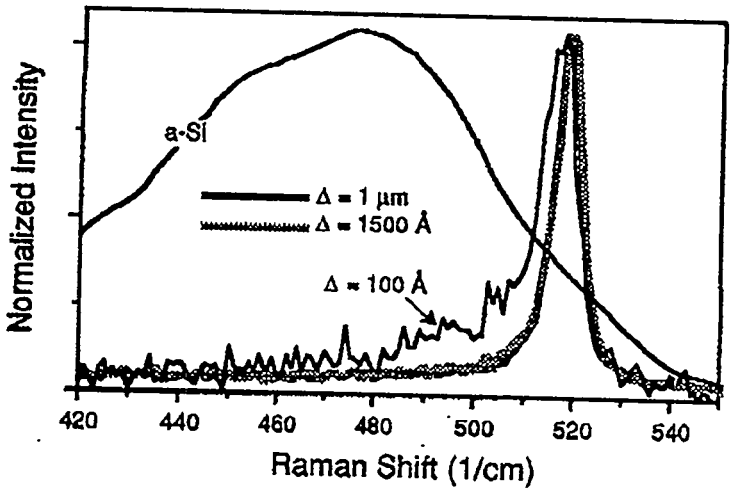


Figure 6. Normalized Raman spectra for the films of Fig. 4 and 5. The a-Si spectrum shown for reference was smoothed before plotting.

We have shown (Kakkad et al., Appl. Phys. Lett., 59, 3309,1992) that SPC of dopant-containing, thin (< 1000 A) a-Si precursor films can yield highly doped layers for contact and barrier forming applications. However, our research has shown that both doped and undoped layers with thicknesses > 0.5 microns tend to be highly defective after SPC. We believe this may be due to the volumetric changes that, by necessity, have to occur in the transition a-Si into poly-Si. This problem of these thicker SPC layers requiring defect passivation means hydrogenation would be needed for SPC-produced i-layer materials. This can be a problem in films with the thicknesses required for i-layers. The fact that SPC can only be pushed down at best to the 500 °C range means that in certainly is not applicable to plastic substrate use.

Laser crystallization has progressed to the point where it has now been applied to fabricating TFTs on plastic (P. Carey, Lawrence-Livermore National Labs.). Tight control of thermal profiles is obviously needed in this approach because, unlike SPC, laser crystallization actually melts the silicon precursor film. It has been found that non-hydrogenated amorphous silicon is an excellent precursor. The absence of hydrogen in the a-Si precursor apparently is beneficial due to the lack of hydrogen evolution during heating causing bubbles, delamination, etc. This approach has only been applied to the thin films needed for TFTs to-date. It has the still unsettled question of throughput.

III Light Trapping

Given the technological challenges arising from the need for 8-20 micron, high quality poly-Si material produced a manufacturable throughput rates, it is clear that light trapping to keep this i-layer thickness down is critical. Various light trapping strategies are seen in Figures 7-9 from studies done at NREL. Fig. 7 shows the maximum achievable current density resulting from an approach where just the back surface is textured. This modeling says the required silicon should be >12 microns. It also says that an Al back reflector is slightly disadvantageous due to the photon loss in the metal. The approach of having the front textured only is seen in Fig. 8 to be very effective. It allows the silicon absorber thickness to be somewhat reduced and removes any significant

negligible effect of putting Al on the back surface. Figure 9 shows that there is no advantage in texturing the front and back. It is seen that this forces the Si absorber to be thicker and introduces substantial loss from any back Al metalization.

IV Conclusions

Substrate choice is largely driven by economics and to some degree by weight, flexibility, etc. The substrate choice itself influences the thin film silicon formation (crystallization or direct deposition) techniques available. Light trapping and quality of the poly-Si together control how thick the absorber needs to be. Computer simulations, and now some cell results, say absorbers will have to be in the 8-20 micron range. Absorbers in this range from SPC , and probably laser crystallization in that thickness range, will require a hydrogenation, passivation step. With the film thicknesses required, this passivation will have to be fast and effective. Deposited films can be passivated as-deposited. However, at the temperatures where this occurs effectively, it remains to be seen if the deposition rates can be acceptable in manufacturing.

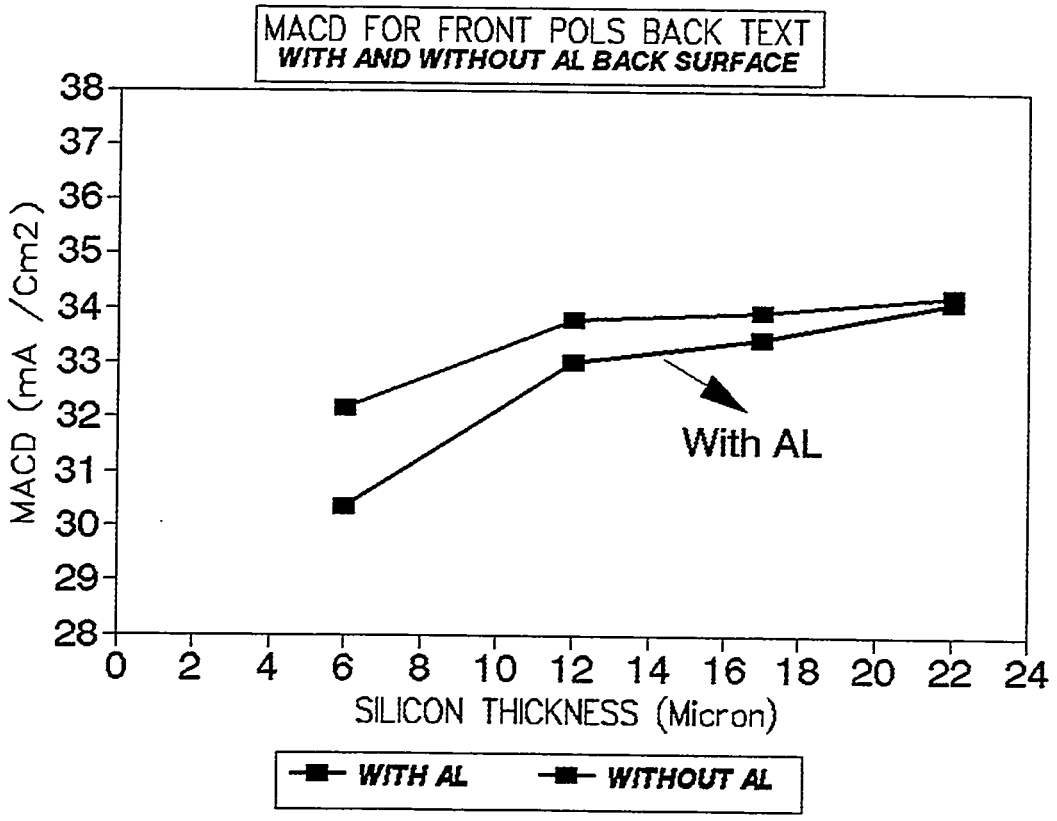


Figure 7. Trapping using polished front, textured back. MACD+ maximum achievable current density

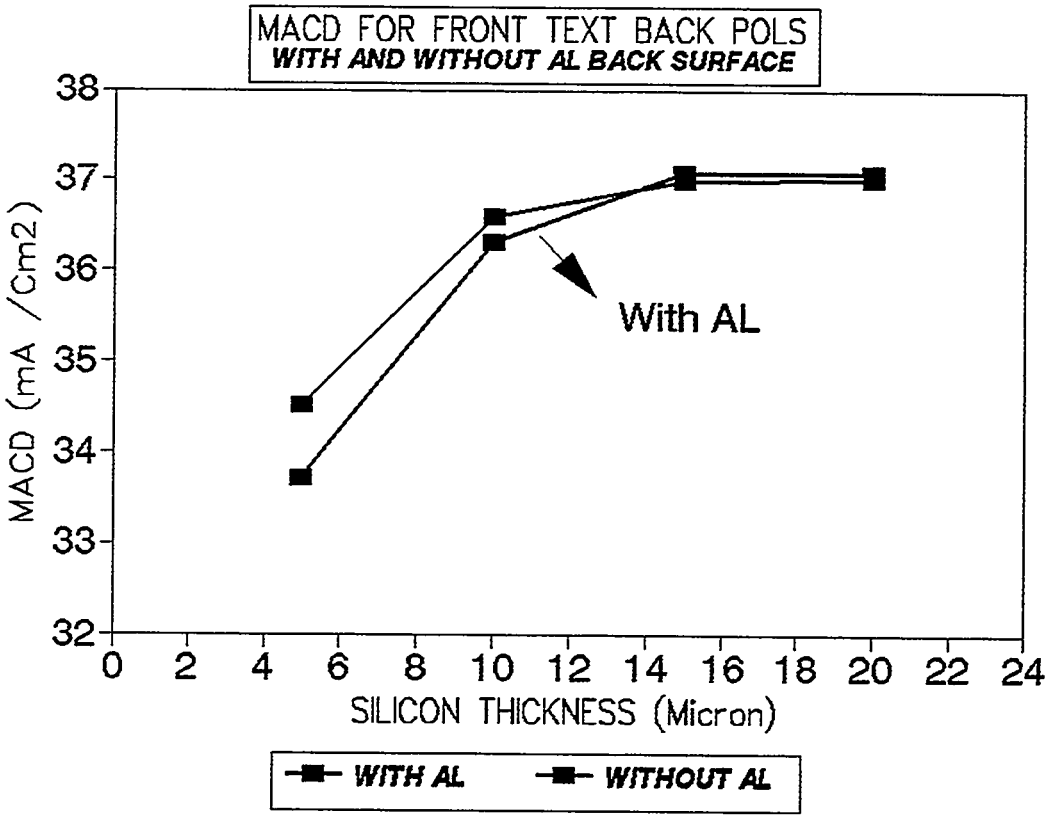


Figure 8. Trapping with textured front only.

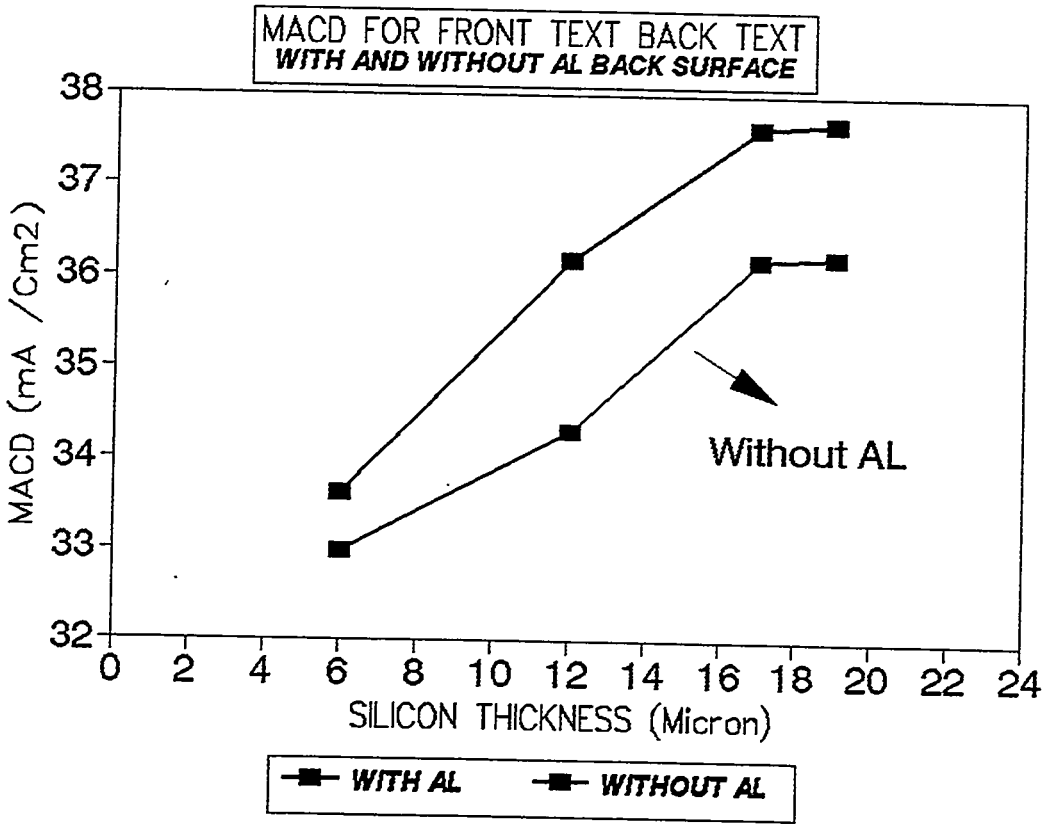


Figure 9. Trapping with textured front and back.

High-Efficiency Solar Cell Development at the Fraunhofer ISE

W. Wettling, J. Knobloch, S.W. Glunz
Fraunhofer Institute for Solar Energy Systems ISE, D 79100 Freiburg, Germany

An overview of the high-efficiency solar cell development at Fraunhofer ISE is given. Five types of cells are discussed: (1) the LBSF (= local back surface field) cell, (2) the RP-PERC (= passivated emitter and rear cell with random pyramids), (3) the MESC (= mesh-structured emitter solar cell), (4) the RCC (=rear contacted cell) and (5) the high-efficiency thin film cell based on SOI (= silicon on insulator). All these cells show very good efficiencies near and above 20 %.

Solar cell research at Fraunhofer ISE is carried out in a fairly comprehensive programme that covers monocrystalline, multicrystalline and crystalline thin film silicon cells as well as GaAs and other III-V compound solar cells. The goal of all activities is to develop technologies for efficiencies as high as possible but at the same time as simple as possible. Almost all developments are performed in close cooperation with German PV companies and/or with European research teams in the framework of projects of the European Commission. A list of the best efficiency values of the various solar cells developed in our laboratory which are *not* from monocrystalline silicon is given in Table 4.

1. LBSF solar cells

In the present paper we report on some recent progress in the field of monocrystalline silicon solar cells. Our „base" technology is the LBSF (=local back surface field) processing scheme [1] which is similar to the PERL cell of UNSW [2]. The main features of this technology are: front texture by inverted pyramids, two-step emitter, boron diffused local BSF under the rear point contacts and front and rear passivation by SiO_2.

This cell could be optimized to an efficiency of 23.3 % on a 230 µm thick floating zone (FZ) silicon wafer and a cell size of 4 cm^2. A very good value of J_{sc} = 42.0 mA/cm^2 was achieved by using a photoresist definition of the front contacts during electroplating and a double layer antireflection coating. With a single layer SiO_2-AR coating of 105 nm thickness a slightly higher value of V_{oc} = 700 mV was achieved, however with a somewhat smaller J_{sc} = 41.3 mA/cm^2, thus also leading to 23.3 %. When the LBSF processing sequence was applied to Czochralski grown (Cz) silicon the best efficiency so far was 22.0 % which is an international record value for this material (see Table 1).

Table 1. Confirmed results of silicon solar cells processed with the LBSF scheme.

Cell	Material	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF	η [%]
LBSF with SiO_2	FZ	700	41.3	80.6	23.3
LBSF with SiO_2	Cz	680.5	41.8	77.2	22.0
LBSF with $SiO_2/TiO_2/MgF$	FZ	685	42.0	81.0	23.3

2. RP-PERC solar cells

The LBSF/PERL scheme while yielding the highest efficiencies is too involved for a cost effective fabrication since it uses 6 to 7 photomasking steps. We have therefore adapted the PERC (= passivated emitter and rear) process [3] to our technology, however with a random pyramid texture (therefore using the acronym „RP-PERC" [4]). This cell has a simple emitter

and no LBSF (see figure 1). This process sequence uses three photomasking (pm) steps for front grid, rear contact points and cell area definition, respectively. We have also processed cells without this area definition thus simplifiing the process to 2 pm steps with only relaxed alignment definition. Best efficiencies up to 21.6 % were achieved (see Table 2) which makes this simplified scheme interesting for an industrial production.

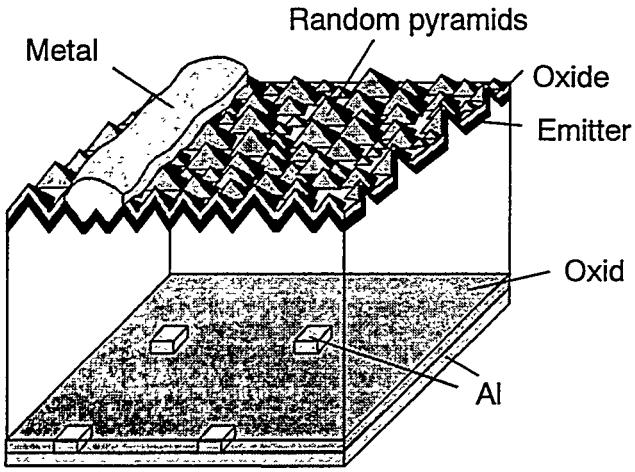


Fig. 1. Schematic design of the RP-PERC solar cell.

Table 2. Confirmed results of best efficiencies of RP-PERC cells.

Cell	Area [cm^2]	V_{oc} [mV]	J_{sc} [mA/cm^2]	FF	η [%]
RP-PERC (3 pm)	4	676	39.6	80.7	21.6
RP-PERC (3 pm)	21	675	38.7	79.9	20.9
RP-PERC (2 pm)	4	672	39.3	79.7	21.0

3. Mesh-stuctured emitter solar cells (MESC)

The LBSF processing scheme can also be simplified by reversing the order of texturing and deep emitter diffusion. As a result a deep emitter is processed that is formed as a mesh in the edges of the inverted pyramids (see figure 2). A shallow emitter may subsequently be diffused in the whole front area without pm. This MESC (=meshed emitter solar cell) scheme allows to engineer the sheet resistivity of the emitter by variing the geometrical form of the front texture [4]. This MESC scheme is presently explored with the aim to process a screen printed cell with higher efficiencies.

The MESC cell has shown remarkably good efficiencies if processed with the additional shallow emitter. 22.7 % were reached with LBSF contacts on the rear side, as seen in Table 3.

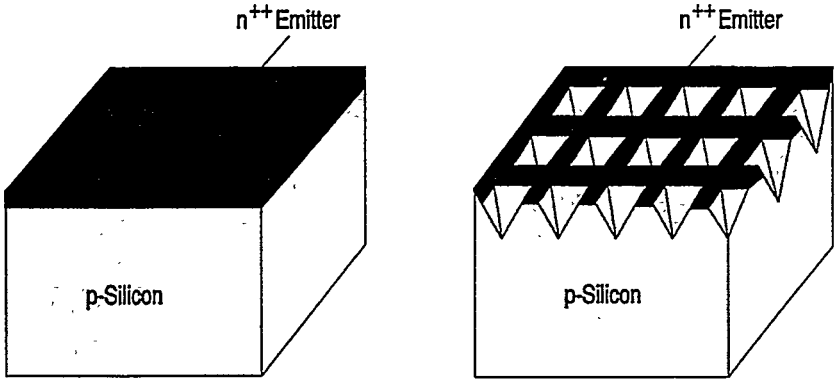
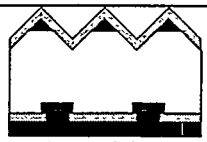
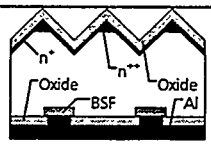


Fig. 2. Simplified process scheme of the mesh-structured emitter.

Table 3. Confirmed solar cell results of cells with mesh-structured emitter (MESC).

	 MESC without shallow emitter and local ohmic contacts	 MESC with shallow emitter and local ohmic contacts	 MESC without shallow emitter and local back surface fields	 MESC with shallow emitter and local back surface fields
V_{oc} [mV]	657.8	677.0	666.9	696.1
J_{sc} [mA/cm^2]	39.5	39.8	39.1	40.53
FF	0.739	0.783	0.777	0.803
η [%]	19.2	21.1	20.0	22.7

4. Rear contacted cells (RCC)

A high-efficiency interdigitated grid scheme was developed which was used for several purposes: (1) for a front-side contacted crystalline silicon film cell (see next section), (2) for a rear contacted cell (RCC) and (3) for a bifacial solar cell. Figure 3 shows a schematic cross section of the RCC with and without a floating emitter passivation on the front side (note that the light enters the cell from the bottom side of the figure). The emitter was selectively diffused as a local two step emitter. Under the n-fingers the emitter was highly doped (n^{++}) and deeper diffused than on both sides of the fingers (n^+). The shallow emitter was interrupted by the p^+ -diffused zone under the p-finger system. With this RCC structure on 230 µm thick FZ wafers of 1 Ω cm resistivity confirmed efficiencies of up to 21.4 % were recorded [4].

The RCC stucture has some similarity to the point contact solar cell [5]. But it differs in some details of the emitter structure. In particular the shadowing losses of the interdigitated grid fingers are small. Therefore, this cell can be operated as a bifacial cell with excellent characterisitcs from both sides. Best results of a RCC bifacial cell showed 20.2 % when illuminated from the grid side and 20.6 % when illuminated from the unmetallized side.

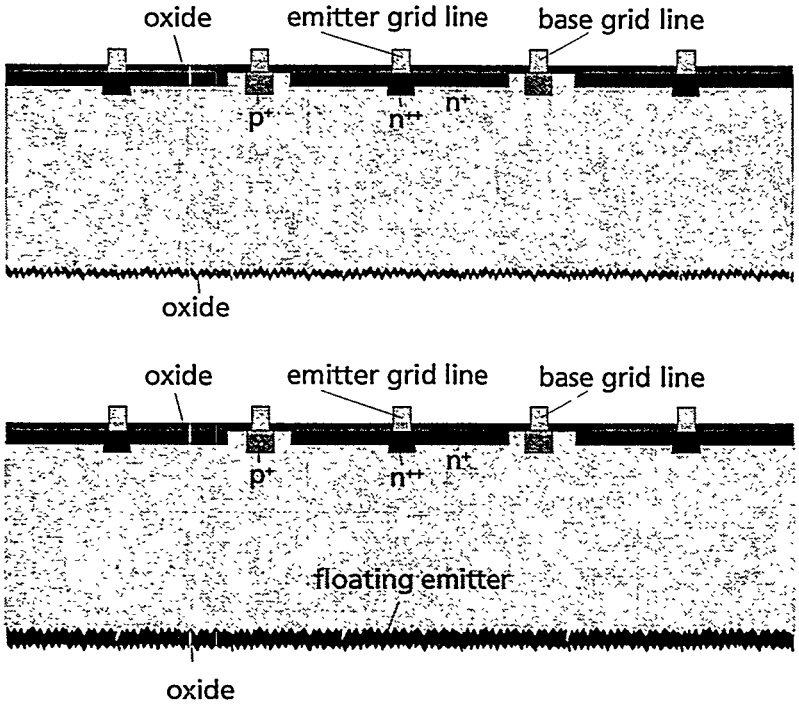


Fig. 3. Structure of the rear contacted cell (RCC) without (top) and with (bottom) floating emitter (note that the light is illuminated from the bottom side when operated as a RCC). The ratio of the base area to the emitter area on the metallized side is around 1:50.

5. High efficiency silicon film cell

The same interdigitated finger structure was also used to process a high-efficiency cell on a thin epitaxial layer. This layer was grown epitaxially by CVD on a SOI (=silicon on insulator) structure[6]. This resulted in a 46 µm thick monocrystalline layer on an ion implanted insulating SiO_2 layer. The thin film solar cell structure is shown in figure 4. Solar cell efficiencies up to 19.2 % were measured with this thin film cell. A careful analysis showed that the light confinement in this structure by the front texturization and the rear SiO_2 „mirror" plays a crucial role in achieving these high efficiencies.

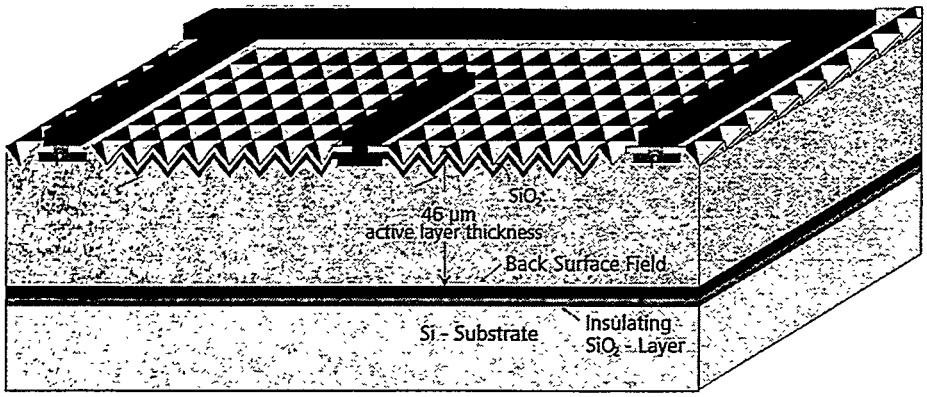


Fig. 4. High-efficiency thin film solar cell on SOI structure with interdigitated front grid.

Table 4. Highest efficiencies of multicrystalline, crystalline silicon thin-film and III-V compound solar cells processed at Fraunhofer ISE.

	mc-Si cast	Thin-film on ceramics	Thin-film on graphite	GaAs LPE	GaAs / GaSb 4 terminal
Area	21 cm²	1 cm²	1 cm²	4 cm²	0.13 cm²
Efficiency	17.4 %	9.3 %	11.0 %	23.3 %	31.1 %

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Review of The 4-Year R&D Project on Crystalline Silicon Solar Materials and Devices in the New Sunshine Program

T. Saitoh
Div. of Electronic and Information Eng.
Tokyo A&T University
Tokyo 184, Japan
Phone: 81-423-88-7108, Fax: 81-423-85-9055
E-mail: tadashi@cc.tuat.ac.jp

ABSRACT: Research and development for crystalline Si solar materials and devices in Japan have greatly advanced for the last 4 years. Efficiencies of large-area cells and modules using multicrystalline cast substrates attained to 17 and 14 % by improvement of the cast quality and development of high-efficiency cell processes. Research was carried out on recombination reduction of minority carriers at SiO2/doped Si interfaces and gettering in the bulk regions. Small-area cell efficiencies using single crystal Si substrates have reached 22 to 23 %. As a result of the steady progress for the last 20 years, government decided to terminate the technology development project for the bulk ingots and solar devices using them and to concentrate the R&D on Si feedstocks and thin Si film cells.

1. INTRODUCTION

Flat-plate crystalline silicon solar modules have still prevailed in recent photovoltaic(PV)market for both remote and grid-connected power applications[1]. However, the market growth in the coming next century might be suppressed if production technologies on low-cost silicon feedstocks and high-efficiency, low-cost solar cells and modules are not developed. In 1993, Japanese government had decided to restructure the past Sunshine Program by taking account of an environmental issue and to restart the New Sunshine Program. One of the aims in the program is to contribute the reduction of carbon dioxide emission in the earth environment. The other, of course, is to supply electrical energy in the power market by cost-effective PV energy. In 1994, an aggressive subsidy program for private houses and public buildings was implemented by Ministry of International Trade and Industry to promote PV market exploitation[2]. In this year, more than 9,000 PV systems are expected to be installed on the roofs of private and public houses using the subsidy program[3].

Since then, Japanese PV industry has invested to expand their production capacity to meet the PV market corresponding to 30 MWp. As for R&D in the past project, steady progress had been made especially in the fundamental research on surface passivation and minority-carrier recombination and the development of new process technologies for Si feedstocks and solar devices[4-6]. For the recent Si feedstock issue, a new association has established in 1996 to promote the R&D on Si feedstocks concerning with removal of impurities by evacuation and solidification processes.

This paper describes the technological results achieved in the last 4-year government R&D project for crystalline Si materials and devices. Primary results include the developments of equipments and technologies to produce gigantic cast ingots and also fast cell fabrication processing technologies for multicrystalline Si solar cells. The results of high-efficiency, large-area multicrystalline Si solar cells are described with those of module fabrication using the multicrystalline Si solar cells. In addition, fundamentals and fabrication of very-high efficiency, single-crystal solar cells are also described.

2. EFFICIENCY IMPROVEMENT

Since 1986, primary efforts have been directed towards improving conversion efficiency for large-area multicrystalline silicon solar cells. The Japanese government has promoted technology developments by planning a 3-year project from 1986 to 1988, a subsequent 4-year project from 1989

to 1992 and a recent 4-year project from 1993 to 1996 with target efficiencies of 15% and 24% for a multicrystalline solar module and single crystal solar cell, respectively. The past promotion successfully improved cell efficiencies as indicated in Fig.1. In 1985, cell efficiency was 12.5% for a multicrystalline cell with a large cell area of 100 cm^2 prepared using a low-cost technique. Cell efficiency later improved steadily to 15-16% in 1988[7,8] but remained saturated for the next 3 years up to 1990. However, as indicated in Table 1, cell efficiencies for 100 and 225 cm^2-area cells in 1997 have been improved to very high values of 17.2 [9] and 17.1%[10], respectively, which are close to the 18.6%-efficiency for a 1 cm^2-area cell prepared using expensive evaporation and photolithography techniques [11].

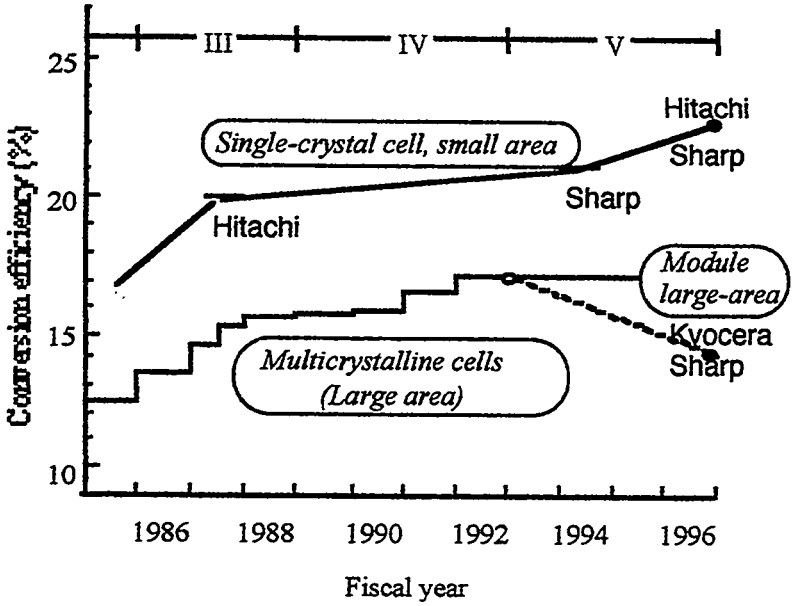

Figure 1: Yearly improvement of conversion efficiencies of single-crystal and multicrystalline Si solar cells and modules.

Using the developed high-efficiency multicrystalline cells, preliminary solar modules were fabricated. Efficiencies of modules with an area of 4,000 cm^2 were obtained to be around 14% a little smaller than the government target of 15%[12]. This was due to the limited number of cell fabrication and the shortage of the production time. With the progress of multicrystalline silicon cells, conversion efficiency of single-crystal silicon cells has also been improved as indicated by an upper curve in Fig.1. As for the single-crystal cells, two kinds of approaches have been carried out through high and low temperature processes. The high-temperature process[13] in addition to a new boron gettering process[14] was effective to obtain a high open-circuit voltage close to 0.7 V resulting in 2 cm^2-area cell efficiency of 22.6 %[15]. The low temperature process less than 850 C for thermal oxidation was also useful to realize an active area efficiency of 23.5 %[16].

Table 1: Conversion efficiencies of solar cells and modules achieved under the last 4-year R&D program in Japan.

Devices	Class	Eff.(%)	Area(cm^2)	Company	Eff. in 1992 (%)
Cells	Single	22.6	2	Hitachi	20.5
		23.5*	25	Sharp	---
	Cast poly	17.2	100	Sharp	17.1
		17.1	225	Kyocera	16.4
Modules	Cast -poly	14.3	4,352	Kyocera	~12
		13.7	4,032	Sharp	---

* Active-area eff.

3. SOLAR-GRADE MATERIALS

3.1 Silicon Feedstocks

In the past until 1992, a low-cost process for silicon feedstock by carbothermic reduction of high-purity silica had been investigated[17]. The process consisted of the chemical reduction of high-purity silica produced by acid treatment with water glass with high-purity carbon prepared by thermal cracking of propane gas. After reduction of the high-purity silica in an AC-arc furnace, the silicon obtained was solidified unidirectionally. Solar cells using the silicon were fabricated to have a maximum efficiency of 14.2%[18].

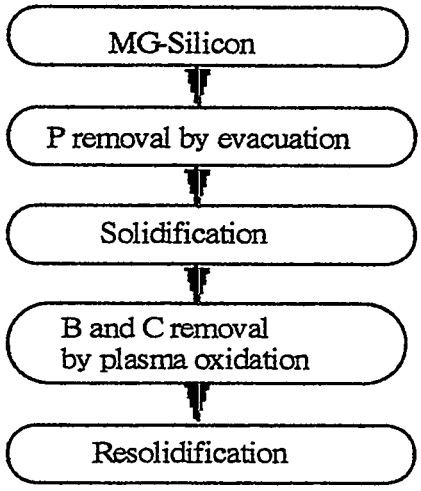

Figure 2: Production flow of Si feedstocks refined from metallurgical-grade silicon source[20].

However, the process was not selected for a recent urgent need to produce cast ingots. Instead, refining of metallurgical-grade materials has been conducted. Phosphorus impurity was firstly removed by evacuation and then boron impurities using a plasma oxidation shown in Fig. 2. By mixing water vapor in an argon plasma, the boron content could be reduced to a 0.1 ppm level[19]. Metallic impurities were reduced to a ppb level by resolidification of the refined MG-Si. Using cast substrates from the solar-grade (SOG) feedstocks, maximum cell efficiencies of 14 and 16 % were obtained by conventional and high-efficient cell fabrication processes[20].The cell efficiencies did not vary with the length of the cast ingot. Last year, the government has driven the SOG-Si process to a pilot production level with a capacity of 60 t/y.

3.2 Cast Substrates

In the past from 1985, quality improvement of conventional cast ingots had been conducted persistently by investigating the effects of solidification conditions on the crystal quality and also on the cell characteristics. Using the high-quality cast ingots, high-efficiency, large-area and small-area solar cells were fabricated in Japan[6] and also in Europe[21].

Since 1985, a cold-crucible casting process with a magnetic field[22] was selected owing to its inherently inexpensive nature[23]. As shown in Fig. 3, the growth process does not require an expensive quartz crucible. The temperature gradient during ingot solidification was found to affect the ingot quality substantially. Cell efficiency using the electromagnetic casting (EMC) ingot was a little smaller than that using conventionally cast substrates. The defects were generated in the bulk regions by a steep thermal gradient around crystallization region. However, cell efficiency of about 16% was reported to obtain by annihilation of active defects through hydrogen passivation. In 1992, 25 cm square ingot was firstly fabricated by the EMC technology and an ingot with 1.6 m in length was grown. In 1996, as indicated in Table 2, a production-level EMC

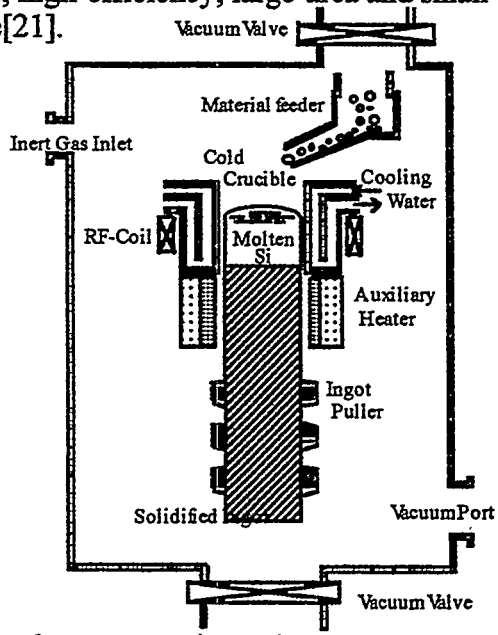

Figure 3: A magnetic casting setup to grow a 35 cm square, 500 kg ingot.

furnace was constructed to grow a record 500 kg ingot with 35 cm square and 2.2 m in length at a solidification rate of about 1 mm/min[24]. A key parameter to improve the crystal quality was elucidated to be thermal stress during solidification and cooling down of the EMC ingots by computer simulation[25].

A new casting process indicated in Fig.4 had been proposed by dripping molten Si on crystallized ingot, so-called drip-controlled method (DCM)[26]. By using a high-purity graphite mold and optimizing the crystallization condition, very-high quality ingots were fabricated. Cell efficiencies of 16 to 17% were reported using a higher-quality region of the DCM cast ingot. The DCM process was applied to develop a continuous production technology of a 170 kg ingot with a size of 43 cm square and 40 cm in height[27]. Using 26 DCM cast substrates, an average cell efficiency of 16.6% and a maximum efficiency of 17.1% were realized for 225 cm^2 area substrates[12].

Table 2: Status of large cast-ingot fabrication technology.

Company	Ingot size* (cm)	Ingot weight (kg)	Growth rate (mm/min)	Quality
Sumitomo STX (EMC)	35×35 ×200	500	~1	Medium (τ=14μs)
Daido-Hoxan (CCM)	44×44 ×40	170	~0.5	High (τ=20~40μs)
Bayer	33×33 ×20 (?)	?	0.5	High
Eurosolare	55×55 ×21	150	0.1~0.2	High

* Width×depth×Height

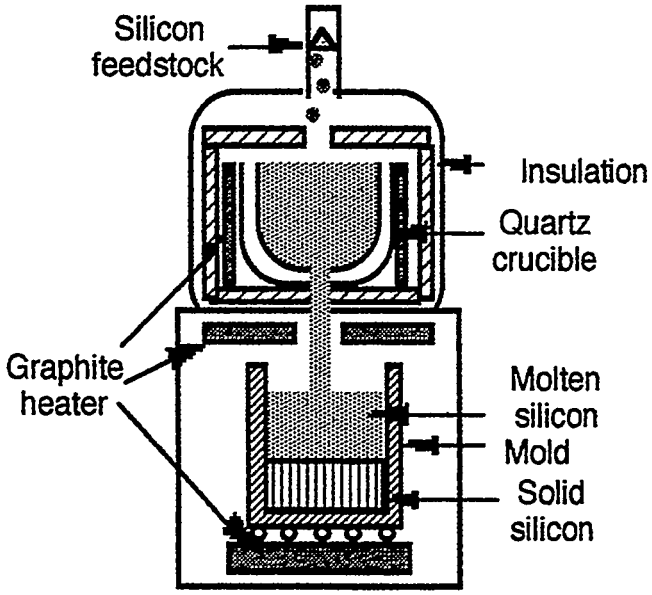

Figure 4: A schematic diagram of Drip-Controlled Method (DCM) for growing cast ingots continuously[26, 27].

4. CELLS AND MODULES

4.1 High-Efficiency, Single-Crystal Solar Cells

Firstly, trichloroethane (TCA) process had been investigated to clean the inside of an oxidation furnace as a function of TCA flow rate and oxidation time[28]. A low surface recombination velocity of 17 cm/s was obtained for a substrate with a bulk lifetime of 300 μs. The effects of oxide passivation on effective lifetime, density of interface states and cell performance had also been examined. Both the effective lifetime and the density of interface states were improved by hydrogen annealing of SiO_2 layers.

To fabricate high-quality back-surface-field structures, high-temperature boron-diffusion and low-temperature p^+-type microcrystalline(μc) Si deposition have been employed. As for the boron diffusion, a pyrolytic boron nitride diffusion source was the best owing to the lowest content of lifetime killer impurities. Gettering process of the lifetime killer impurities was found to exist during the boron diffusion at 1000 C as shown in Fig.5[14]. On the other hand, lifetime degradation occurred after oxidation of the boron diffused samples. This was considered due to the trapping or out-diffusion of lifetime-killer species in the heavily-doped boron-diffused region. By increasing the p^+-region area at the rear, short-circuit current density and conversion efficiency were found to increase as shown in Fig.6. A high-efficiency solar cell with 22.6% efficiency was fabricated using high quality 2 ohmcm, FZ crystals[15].

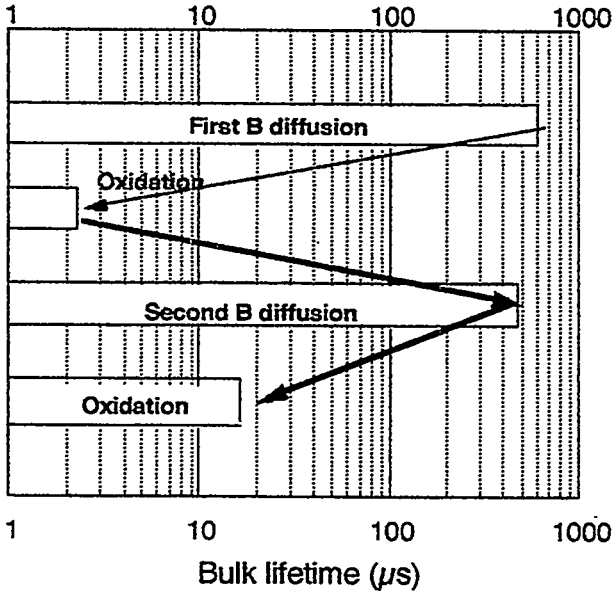

Figure 5: Variation of minority-carrier ifetime with boron diffusion and oxidation processes for high-efficiency single crystal solar cells[14].

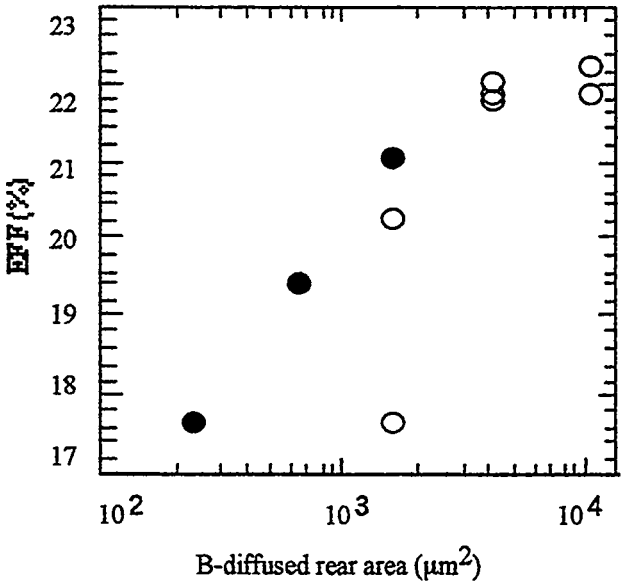

Figure 6: Effect of boron-diffused area on cell effiiciency for single-crystal solar cells[15].

Another highly efficient single-crystal cells were also fabricated using low-temperature oxidation for an n^+-type emitter and low-temperature plasma-deposition of the μc-Si:H layer for a p^+-type rear. A relatively heavily P-doped region in the emitter was removed by chemical etching and then oxidized at a low temperature less than 850 C. Annealing effects on the resistivity of boron-doped, p^+-type μc-Si:H layers and cell efficiency were examined. The resistivity tended to decrease to $10^{-1}\Omega$cm with annealing. Cell efficiency reached a maximum at an annealing temperature of 200 to 250 C due to the fact that effusion of hydrogen atoms occurred at temperatures higher than 250 C. Fabricated cells consisted of a randomly textured front surface with a MgF_2/TiO_2 antireflection film-coated and SiO_2-

passivated emitter and the p^+-type μc-Si:H back-surface-field with a SiN:H plasma film. A maximum active-area cell efficiency of 23.5% was achieved for a cell area of 25 cm^2 by attaching specially designed finger and busbar electrodes[16].

4.2 Large-area multicrystalline Si solar cells

In order to improve cell efficiency of large-area multicrystalline solar cells, competitive R&D has continued since 1986. Using higher-quality cast substrates, the conversion efficiency of large-area, multicrystalline silicon solar cells has steadily improved. One of the approaches was to use mechanically grooved emitter surfaces to reduce light reflection at the front as shown in Fig.7.

Using the surface, conversion efficiency of 17.1% had been realized in 1993 for a large cell area of 100 cm^2 using MgF2/TiO2 double antireflection films, oxide surface passivation and narrow printed electrodes[9]. Recently, a multi-blade wheel grinding technique was developed for low-cost cell production. The grooving process time for a 100 cm^2-area substrate reduced to 30 s. A simultaneous formation of a pn junction and antireflection film was carried out using atmospheric CVD of phospho-silicate glass and firing at 920 C. A fast firing method to make silver printed electrodes for both sides was developed by investigating the effects of conveyer speed on cell performance. A maximum conveyer speed of 5 m/min was realized at a relatively high temperature of 880 C, which is ten times higher than an ordinary speed.

The other approach for reducing the fabrication cost of solar modules is to use a larger-area multicrystalline cell. A large multicrystalline cell with an area of 225 cm^2 was fabricated with cell efficiency of 16.4% by fabricating a low surface reflection using photolithography. Reactive ion etching(RIE) method was applied to make a textured surface at multicrystalline Si substrates. The surface geometry was controlled by Cl2 flow rate, reaction pressure and RF power. By optimizing the RIE condition, a very low surface reflection was obtained at a wider spectrum range, which contributed to realize a very high efficiency of 17.1% for a 225 cm^2-area, multicrystalline cell shown in Fig.8[10].

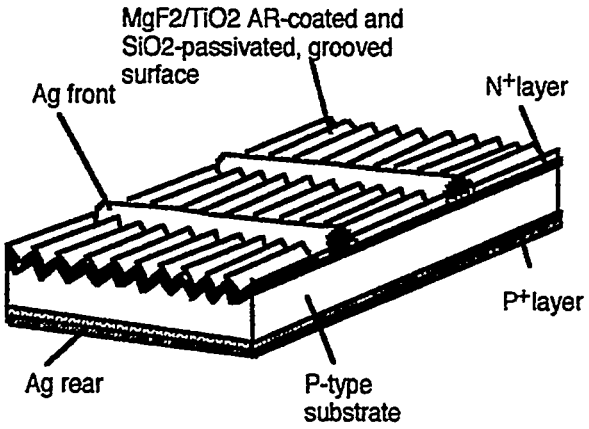

Figure 7: A schematic multicrystalline Si cell structure with a mechanically grooved emitter surface[9].

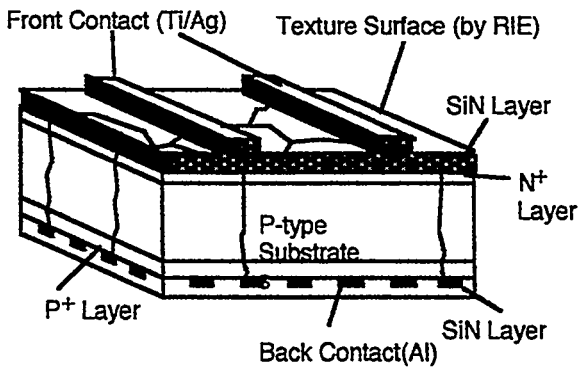

Figure 8: A structure of 225-cm^2-area, high-efficiency, multicrystalline Si solar cell with SiN:H plasma film at the front and rear surfaces[10].

4.3 Solar Modules

Using the DCM multicrystalline Si substrates, solar modules were fabricated to achieve the government target efficiency of 15%. One of the approaches was the use of 225cm^2-area cells to fabricate a 18-cell, series-connected structure. An average cell efficiency was 16.6 % with a short-circuit current of 7.92 A, open-circuit voltage of 614 mV and fill factor of 0.767. However, as already indicated in Table 2, a realized module efficiency was 14.3 % for a module size of 93.4 cm in width and 46.6 cm in depth. Another solar module was also fabricated using 100 cm^2-area cells. A module efficiency was obtained to 13.7 % for a 4,032 cm^2-area module. Technologies relating to module fabrication were also developed including fast cell interconnection, low surface reflection of superstrate glass surfaces and so forth.

5. FUTURE DIRECTIONS

As already mentioned above, the government subsidy program is expected to create a new 30 MWp market for PV-equipped houses. Next issues are a restriction of PV market expansion by Si feedstock shortage for solar cells and saturation of cost reduction.

As for the silicon feedstock supply, the new association will promote the technology development of the SOG-Si production in pilot production scale. In May 1997, Kawasaki Steel announced that they will construct a bigger production plant of 600 tons/y in 1999 if the current technology development proceeds as expected.

In the future, we should consider a creation of an independent PV industry without the government subsidy program. Toward the future PV industry, high-efficiency R&D programs should continue firstly to implement a smaller array on the restricted roof area in Japan. Further cost reduction will be realized by the following means including cost reduction by building integration and static concentrators and the technology development of automated production in GWp level ranging from Si materials and devices.

6. CONCLUSIONS

Technological results achieved in the recent 4-year government program for crystalline Si materials and devices have been remarkable. Primary results include the developments of equipments and technologies to produce gigantic cast ingots and also fast cell fabrication processing technologies for multicrystalline Si solar cells. Efficiencies of multicrystalline Si, large-area cells and modules using them have achieved to 17 and 14 %-levels, respectively. With fundamental research, very-high efficiency, single-crystal solar cells were also fabricated. Based upon the realized results, cost estimation has been carried out, which indicated that the cost is competitive with thin-film amorphous Si and CdTe solar modules.

As a steady progress in the last 20-year R&D program and also the recent market growth using c-Si modules, government has decided to terminate the technology development project for the multicrystalline Si ingots and devices, which expects to contribute the accelerated transfer of the developed technologies to a real production stage in PV industry.

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Getting to a Gigawatt

J. I. Hanoka
Evergreen Solar, Inc., 211 Second Avenue, Waltham, MA 02154

This talk was originally meant to address the question, "How do we get to a Gigawatt/year by 2010?" In the light of President Clinton's recently announced million roofs program, we need to modify this question. If we assume that there will be 2-4 kW/roof, then we are looking at 2-4 GW—and by the year 2007! Furthermore, we should recall that the Japanese are projecting 4.6 GW installed by the year 2010. With the world's total PV production at something like 90MW this year, we are talking about anywhere from 50 to about 100 times the present production capacity in ten to thirteen years. Where will all these Gigawatts come from and how will we get there? These are large and difficult questions, but we attempt here to give some possible answers.

First, we should preface our remarks with the belief that it is naïve to think that there will be only one technology winner to reach this goal. Markets of this size will accommodate a variety of technologies. Having said this, we must, at the outset, acknowledge our bias that crystalline silicon ribbon will be one of the technology winners, and we will try to show how this technology in particular can reach such a goal.

A recent multi-year, multi-country study performed in Europe and announced at the Barcelona meeting [1] concluded that cast polycrystalline silicon, along with screen printing, 15% cells, and assumptions on the economies of scale could allow us to reach a level of 500 MW/yr at a module cost of about $1.25/Watt. Ribbon silicon came in at an even lower cost of less than $1.00/Watt, thus supporting the bias we mentioned above [2]. What was especially interesting about this study was that it assumed that basically present technology would be used and that, again relying on economies of scale, the costs could reach this level. This general endorsement of crystalline silicon as the vehicle to reach the approximate $1/Watt goal has been mentioned elsewhere as well [3].

As much as we at Evergreen, being a silicon ribbon company, agree with the conclusions of this study, we would take issue with the assumption that extrapolating from current technology will be sufficient to reach the long sought $1/Watt goal. Before detailing what is meant here, let us set out some basic assumptions. First, we assume that the maximum factory size will be 100 MW. So we will deal in factory "quanta" of this size, 100 MW. Second, for simplicity we divide up the problem into four different areas: silicon supply; silicon wafer production; cell making; and module making. This division is somewhat arbitrary, and, as will be shown, with the appropriate technical advances, some of these areas will merge into each other and not be necessarily discrete.

Silicon Supply

It is assumed in the polycrystalline cast and sliced scenario discussed in Barcelona that 400-μm thickness is initially needed. This translates to about 8000 metric tons of Si/year for a Gigawatt. According to Jim McCormick's (Hemlock Semiconductor) numbers from last summer, the semiconductor industry will be at about 25,000 tons/year by Year 2000, and this might be doubled to 50,000 tons/year by, say, 2005. Relying on the fallout and reject material may not generate enough silicon for PV needs. The European study cited before concluded that, again with suitable scale-up factors and some simplification of the process, even the Siemens process could result in satisfactory quantities of silicon. Here are two other scenarios. First, if we could grow thin silicon ribbon directly from the melt of, say, 100-μm thickness, then the silicon

requirement could be reduced by almost a factor of four to about 2000 tons/year. A second scenario is much more "researchy." Years ago, JPL sponsored a project in which Union Carbide developed a low cost method to produce silane, SiH_4. Silane thermally decomposes at somewhere around 400 – 500°C. If a way could be found to pump gaseous silane directly into a silicon melt, then the intermediate step and costs of making solid silicon can be bypassed. For our ribbon growth method which is open to the atmosphere where the ribbon emerges from the chamber, safety issues would be considerable—given all the hydrogen which would be produced and the fact that silane is pyrophoric. In such a scenario, silicon production and wafer production are somewhat merged. One can envision such a scenario for cast poly-silicon also, once some melt has been formed so that the SiH_4 could somehow be introduced into the molten silicon.

Wafer Production

The String Ribbon growth method practiced by Evergreen now produces a single ribbon per machine. The usual question here concerns the throughput per machine. Can a cost of $1/Watt goal be met with the usual growth rates of 15-20 mm/minute for a single machine? Evergreen's response here is that yes, definitely, if the following tasks are accomplished: growth of 100-μm thick, 10-cm wide ribbon, and growth rates of 30-40 mm/minute. With this, a 100 MW factory would have on the order of 500 crystal growth machines. This seems like a large number, but not when considering the size and scope of a typical large industrial operation. Assuming each crystal growth machine would require a total foot print of about 20 sq. ft. (this includes operator space and accessory needs—machine footprint could be as low as 6 sq. ft.), the factory only needs then about 10,000 sq. ft. The capital costs of such a crystal growth machine could readily be projected to be low enough to warrant a large number of such crystal growth machines.

Evergreen's present operating experience with running ten crystal growth machines in production, full time, indicates that such low cost machine projections are reasonable. Furthermore, given the robustness and simplicity of the process, the other goals above also seem attainable. More details will be provided in the talk.

Solar Cell Making

The approach suggested here also will seem radical to some. First, some numbers and general considerations. If we assume 1.5 watts per cell, then a 100 MW/year factory will call for approximately 8000 cells/hour. For comparison purposes, we estimate that present screen printers used for contact printing on solar cells do, at best, 500 cells/hour. Theoretically, a screen printer could do 1000 cells/hour but the issues are handling, breakage, and time to get in and out of the "nest"—the place where the cell is held before being printed. The biggest issue will be handling, in general in the cell process area. For example, if wet chemistry is necessary, then cell blanks need to be loaded and unloaded into plastic carriers. With 200 or 250-μm thick silicon blanks, robotic insertion and removal will not be straightforward. Ideally, either wet chemistry steps are eliminated or belt methods are developed to accomplish etching [4]. Handling is also a major issue for any process which calls for plasma or vacuum processing, and certainly for one in which cell blanks need to be inserted into and be removed from carriers for tube furnace diffusion.

So with all this, we would assert that the ultimate ideal solar cell process is one in which there are only belt processes and belt-to-belt transfers. This means no vacuum processes. Examples will be shown to indicate that this ideal is attainable, based especially on the author's personal experience. In fact, at Evergreen we are working on a cell making process which satisfies a number of these criteria, and, we believe, with suitable R&D advances over the next three years, we will satisfy all of them. Methods for belt furnace surface and bulk passivation will need development—but we believe that this can be done.

Module Making

Lower costs which will lead to the Gigawatt level goals will be achieved in conjunction with a number of developments in polymeric materials for modules which we have worked on under a PVMaT program over the last two years. These developments include a new backskin material which allows for a frameless module, a new encapsulant to replace EVA, a method for continuous lamination in air, and novel, low cost module mounting methods made possible by this new backskin material.

Summary

We have listed the developments we view as necessary to reach Gigawatt levels of PV production at costs of about $1/Watt. Specific examples from the author's experience at Mobil Solar and more recently the approach taken at Evergreen Solar are discussed. Two areas where NREL and Sandia could help are in the silicon supply question and the development of methods for continuous non-vacuum bulk and surface passivation.

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Status of EBARA Solar, Inc.

D. L. Meier

EBARA Solar, Inc.
811 Route 51 South
Large, PA 15025

EBARA Solar was founded in December, 1993 to commercialize the dendritic web silicon photovoltaic technology invented by Westinghouse. EBARA Solar, located in south suburban Pittsburgh, PA, currently employs over 70 people. Attractive features of dendritic web material include the high silicon utilization rate (4 m^2/kg), some flexibility derived from the small thickness (100 μm), and high electrical quality associated the single crystal nature of the substrate. EBARA Solar has recently participated in several demonstration projects. In November, 1996, EBARA Solar provided modules for a 2 kW installation at the NTT training center in Suzuka, Japan. In March, 1997, a 12 kW installation was completed at the same site. Modules had a tefzel front cover, a backing plate of fiber-reinforced plastic or aluminum, and soldered interconnects. The cells for these modules were fabricated using an RTP diffusion, APCVD AR coating, and screen-printed metallization. Distinguishing features of these cells include an n-type base and alloyed aluminum self-doping emitter contacts. Encapsulated cell efficiencies were typically 11%, limited primarily by high series resistance and excessive grid shadowing. More advanced cell processing, done in collaboration with Georgia Tech UCEP, and including emitter etch-back, oxide passivation, evaporated contacts, double layer AR coating, and forming gas anneal, has been used to produce web cells with efficiencies as high as 17.3% and lifetimes greater than 150 μs. Some of these features will be incorporated in future web cells. Having demonstrated a viable cell structure and module assembly technology, attention has shifted to perfecting the web growth process. Twenty web furnaces are being utilized to systematically study the factors which limit the ability to start and sustain web crystals. It must be recognized that the operating window in melt temperature for web growth is only about 1°C. Emphasis is currently placed on precise measurements to map the temperature field within the silicon melt and the growth hardware, along with detailed finite element modeling of temperature and fluid flow within the system. The hardware configuration, processing conditions, and control requirements for producing web crystals of the desired length, width, and thickness are thereby being defined. Additional study and improvement of the web growth process is underway at EBARA Research in Fujisawa, Japan, and at NREL. The goal of these combined efforts is to reduce dendritic web production costs in order to bring to the marketplace an advanced silicon photovoltaic technology in 1998.

Abstract

Recent Results on Growth and Handling of 125 μm String Ribbon Silicon

R.L. Wallace, A.M. Gabor, X.F. Ma, and J. I. Hanoka
Evergreen Solar, Inc., 211 Second Avenue, Waltham, MA 02154

A novel method to address the thin film silicon question is to eliminate the substrate altogether and simply grow self supporting silicon ribbon. Toward this end, Evergreen has been involved in an R&D effort to explore this possibility using the String Ribbon crystal growth method. The goal here would be that of producing 40-μm ribbon. In earlier work [1,2] we reported on the use of an active or tunable afterheater to grow 100-μm ribbon of 5.6-cm width. Research sized cells (1 cm^2) made on this material (in Dr. Rohatgi's lab at Georgia Tech) have yielded cells with efficiencies as high as 15.2%, and, in one case, a cell with a Voc of 638 mV. These results indicate that the initial electronic quality of the material can be quite high, and that with processing optimization, 16% cells should be achievable on 100-μm String Ribbon.

The String Ribbon crystal growth process, now in commercialization at Evergreen, is simpler and more robust than other silicon sheet growth methods. As a consequence, we believe that extending the work to grow 40-μm material is very feasible. Further evidence to support this has been obtained recently in work done using a simplified passive afterheater. It was found that with small modifications in growth speed and melt temperature, flat, low stress ribbon of 125-μm could easily and reproducibly be grown. This material could be diamond scribed into 15 cm x 5.6 cm solar cell blanks, suitable to be run through Evergreen's solar cell production line. A number of such pieces are being processed this way and the results will be reported. The handling issues are not trivial but appear tractable.

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TERMINATION OF WEB SILICON GROWTH DUE TO POLY FORMATION

B. Ingram*, B. Bathey*, D. Meier** and S. Mahajan*

*Department of Materials Science and Engineering

Carnegie Mellon University

Pittsburgh, PA 15213

** Ebara Solar, Inc.

Large, PA 15025

ABSTRACT

Origins of the termination of web silicon growth have been investigated by etch pitting and x-ray topography. Results indicate that the formation of the polycrystalline grain structure constitutes the major source for the cessation of growth. The evolution of the structure is attributed to the interaction between dislocations that are introduced by thermal gradient-induced stresses.

1. INTRODUCTION

Silicon is an attractive material for solar cells that require large areas. Three approaches have been used to produce these large areas. In one of the schemes, cylinders of single crystal silicon are sliced into wafers, polished and then processed into solar cell panels. Solar cells have also been fabricated from polycrystalline ingots. In the second approach, large areas of amorphous silicon containing hydrogen are produced by chemical vapor deposition. This technique is attractive, but the efficiency of the cells is low. In the third scheme, thin silicon ribbons are grown directly from the melt and are then processed into solar cells, thus avoiding cutting and polishing.

Two techniques are used for the growth of silicon ribbons: (I) edge-defined film fed growth, and (ii) dendritic web growth. For these processes to be economical, it is desirable to continuously grow large lengths of ribbons. In the present study, the termination of web silicon growth due to the formation of polycrystalline grains has been investigated using etching and x-ray topography.

2. WEB GROWTH OF WEB SILICON RIBBONS

In the dendritic-web growth, crystals are grown using a dendrite seed about 0.5 to 1.0 mm square which is etched to ~ 0.1 mm square. When the melt is slightly supercooled (~2-3°C), a "button" spreads laterally across the melt surface and dendrites form at the ends of the button. These features are

illustrated in Fig. 1. A ribbon can be grown by pulling the seed upwards. In principle, long lengths of ribbons can be produced by replenishing the melt.

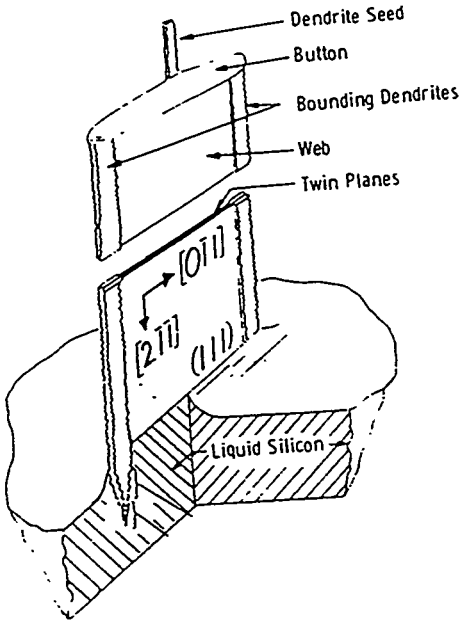

Figure 1: Schematic of dendritic web silicon growth process

Seeding is a crucial step in the web growth. Prior to growth, a thin dendrite is etched to remove any oxide and to generate a needle-like tip. The melt temperature is adjusted so that the seed does not melt. This is referred to as the "hold" temperature. With the seed in contact with the melt, the temperature is lowered by a few degrees. As the temperature drops, a "button" spreads laterally from the seed along the <110> directions across the melt surface. The shape of the button is controlled partially by the temperature distribution in the melt, partially by atomic attachment kinetics at the solid-liquid interface and partially by heat flow along the seed. When the button is of the right size, it is withdrawn from the melt. This results in the propagation of two bounding dendrites into the melt as shown in Fig. 1.

The molten Si forms a film between the dendrites. With the continued withdrawal of the button, a silicon web can be grown.

3. RESULTS AND DISCUSSION OF WEB GROWTH TERMINATION

One of the major obstacles to growing larger crystals by this method is the ease with which the growth terminates. Due to the thin solid/liquid boundary, fluctuation in temperature, mechanical movements, and the high surface tension of liquid Si, the solid easily pulls away from the melt. For the method to be economically viable, crystals of 4 meters need to be consistently produced on average. However, terminations cause the average length of crystals to be much smaller. One of the dominant factors causing the cessation of growth is the formation of polycrystalline silicon.

ETCHING

To etch the (111) surface of web silicon, Sirtl etch was used which is a mixture of 1 HF : 1 CrO_3. The etching time was three minutes which leaves behind pyramidal shaped etch pits. Results indicate that there is a band of high dislocation density (10^6 cm^{-2}) approaching the wish-bone shaped polycrystalline regions. It appears that the dislocations group together to form sub-boundaries. This assessment was also supported by the etching studies on cross-sectional samples. Using Laue back reflection technique, the average angle of the boundaries was determined to be 3°. The accumulation of the dislocation appears to form a low angle tilt boundary, which once formed can

lead to further deterioration of the web, such as severe polycrystalline formation which leads to nonplanar growth.

TOPOGRAPHY

The topographic images indicate the same results as the etch pit analysis. They do show, however, the dislocation in the center of the web run generally along the [2 -1 -1] direction. These dislocations are termed "stringers" and are a result of the interaction between two dislocations on the slip system of $\pm a/2$ [1 0 -1] (-1 1 -1) and $\pm a/2$ [1 -1 0] (1 -1 -1) as they are blocked by twin planes in the crystal. Stringers become quite extensive through the center of the web.

4. CONCLUSIONS

In conclusion, the formation of polycrystalline growth is caused by the deterioration of the crystal quality. Introduction of a low angle tilt boundary is the first step towards termination of growth by this mode. High thermal gradient-induced stresses appear to play a major role on the formation of polycrystalline regions.

Potential influence of the recombination of minority carriers on interstitial and precipitated copper in silicon on solar cell efficiency

A.A.Istratov, H.Hieslmair, T.Heiser, C.Flink, E.R.Weber

Department of Material Science and Mineral Engineering, University of California at Berkeley, 577 Evans Hall, Berkeley CA 94720-1760, USA

W.Seifert, M.Kittler

Institute for Semiconductor Physics, Walter-Korsing-Str.2, D-12530 Fankfurt(Oder), Germany

Lifetime and diffusion length of minority carriers in silicon are important parameters, characterizing the quality of silicon. The most common impurities in silicon device fabrication are the transition metals (primarily Cu, Fe, Ni, Co), which decrease the lifetime by forming electrically active levels, i.e. recombination sites, in the bandgap. Precipitates of copper can degrade the dielectric properties of gate oxides[1] and p-n junctions[2] causing premature breakdown and junction leakage. However, until now, the recombination activity of copper, particularly interstitial copper, was still uncertain. Experiments on copper contaminated silicon, via chemomechanical polishing[3] or high temperature copper-diffusion followed by quench[4] as well as Transient Ion Drift studies[5], indicated that significant concentration (comparable to the doping level) of copper can be kept in the interstitial state for several hours after the quench. This is due to the formation of copper-acceptor pairs which are unstable at room temperature. It is thus possible to study the electrical properties of interstitial copper.

Samples of float zone boron-doped silicon, with a concentration of shallow acceptors of about $2\cdot10^{15}$ cm^{-3}, were copper diffused in a vertical furnace at 600°C, quenched in ethylene glycol, cleaned and etched, and finally stored in liquid nitrogen to prevent further copper precipitation until the beginning of the measurements.

The decay of the concentration of interstitial copper was monitored by the methods of capacitance-voltage characteristics (used to determine the concentration of non-compensated shallow acceptors) and by Transient Ion Drift (TID)[5] (used to measure low concentrations of interstitial copper). The decay of the concentration of interstitial copper was approximated by an exponent. The time constant at room temperature was about four hours both as obtained from CV data and TID. The concentration of interstitial copper at the beginning of the measurement was about 65% of the expected copper concentration of $1.4\cdot10^{15}$ cm^{-3}, determined by the diffusion temperature. The rest of the copper has already precipitated during quench and during the time required for the preparation of the Schottky diodes.

Starting minority carrier diffusion length was about 51.5 μm after the quench and saturated at 58.5 μm during the next 12-15 hours. Diffusion length in the beginning of measurements was limited by recombination on two types of defects: copper in the form of interstitial atoms, partly paired with boron and by already existing copper precipitates. Substituting τ's in the standard formula for the lifetime of minority carriers in the case of several recombination channels $1/\tau_\Sigma=1/\tau_1+1/\tau_2$ by diffusion length $L_D=(\tau D)^{1/2}$, one obtains the relation:

$$L_1^{-2} = L_{precip}^{-2} + L_{Cu+CuB}^{-2} \qquad (1)$$

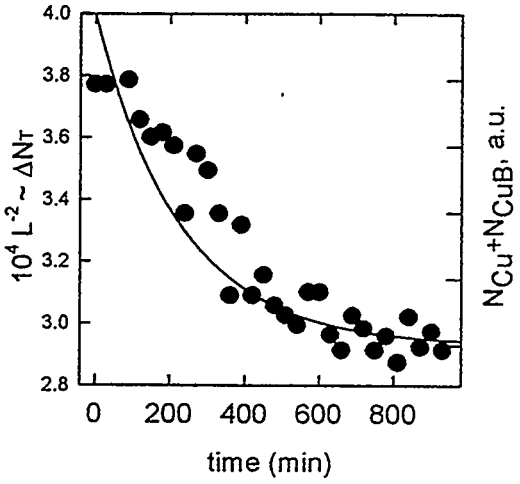

Fig.1. Time dependence of estimated concentration of traps for minority carriers, calculated from the SPV data (circles) and obtained from CV and TID decrease of concentration of interstitial copper (solid line).

Since the final value of L_2=58.5 μm was due to precipitates only, Eq.(1) reduces to the form: $L_2^{-2}=L^{-2}_{precip}$. It is natural to assume, that the most favorable precipitation sites for interstitial copper are already existing precipitates. Since almost half of the initial concentration of copper has already precipitated prior the beginning of measurements, the volume of precipitates should double after the precipitation of the remaining interstitial copper. The linear size of the precipitates, however, should change rather insignificantly - by a factor of 1.3-1.4. Assuming that the recombination activity of growing precipitates did not change much during our measurements, the diffusion length, L_{Cu+CuB}, limited solely by interstitial copper in concentration of about 10^{15} cm^3 would be about 110 μm, and the precipitate-limited component would be about 60 μm. This estimation is consistent with the data of Prigge et al[3]. After compensating up to 60-90% of the acceptors in silicon by chemomechanical polishing, they observed a diffusion length of about 150 μm. Polishing for longer times, which could provide compensation up to nearly 100%, decreased the diffusion length to approximately 50 μm (Ref.3). This can easily be explained by the formation of copper precipitates and is also consistent with our data. It should be noted that even if the diffusion length limited by copper precipitates, L_{precip}, changed with the growth of precipitates, the diffusion length limited by interstitial copper alone can not be lower than 66-70 μm. Again, this does not differ significantly from the estimate above.

The change of concentration of the recombination centers N_T can be estimated using the well-known formula, based on Shockley-Read-Hall statistics. The formula relates the minority carrier diffusion length L_D with the density of recombination centers N_T

$$N_T = (D / \upsilon_{th}\sigma_n)\cdot L_D^{-2} \qquad (2)$$

where D is the diffusion coefficient of electrons, σ_n is the capture cross-section of minority carriers (electrons) by recombination traps.

Substituting diffusion length L_D^{-2} in Eq.(1) by N_T from Eq.(2), and assuming that the density of copper precipitates does not change, one can show that $\Delta N_T \sim \Delta L_D^{-2}$. The dependence of L^{-2} on time is plotted as a function of time in Fig.1. On the same graph, the exponential dependence of decrease of concentration of interstitial copper for the same temperature is plotted. The minority carrier diffusion length data fit the decay of interstitial copper very well. This suggests that the increase of minority carrier diffusion length is entirely due to the precipitation of 10^{15} atoms of interstitial copper.

From these data, the capture cross-section of interstitial copper can be readily estimated. Assuming that the diffusion length, limited by interstitial copper, is 110 μm, the correspondent lifetime of electrons, limited by Cu_i, would be 12.1 μs and, as follows from Eq.(2), the capture

cross-section of interstitial copper ($N_{Cu}=10^{15}$ cm^2) should be about 10^{-17} cm^2. One should however take into account that a significant part of interstitial copper could be paired with boron, forming neutral CuB pairs. These pairs should not substantially contribute to the decrease of the lifetime. Thus, if the fraction of unpaired interstitial copper is 10%, then the estimated capture cross-section of interstitial copper would be 10^{-16} cm^2 , and if the fraction is 1% then the capture cross-section is about 10^{-15} cm^2. TID measurements of the diffusion coefficient of copper[5] showed, that the pairing with boron makes only a small correction to the diffusion coefficient of copper, so that the fraction of paired copper can not be very large. Special experiments, however, are required to determine exactly the ratio of interstitial copper to copper-boron pairs.

These results demonstrate that interstitial copper in p-type silicon is much less dangerous as a life-time killer than interstitial iron or iron-boron pairs. For comparison, only about $4\cdot10^{12}$ cm^{-3} FeB pairs would result in the same 110 μm diffusion length[6] caused by 10^{15} cm^{-3} of Cu contamination in interstitial site.

However, even low concentrations of copper precipitates can drastically reduce the efficiency of solar cells because of the much higher recombination activity of the precipitate. As copper silicide has a unit cell volume of approximately 150% of that of silicon, copper precipitates should have large lattice mismatch. This results in strong stress fields, stacking faults, and punched out dislocations. Though the origin of electrical activity of copper precipitates is still unclear, there are studies which show that copper precipitates, formed through similar treatments as in this study, form a wide defect band in the upper half of the bandgap of silicon[7]. This would provide excellent recombination sites for electrons and can not be represented simply adding recombination properties of single atoms of interstitial copper.

The recombination activity of precipitated copper was studied by Electron Beam Induced Current (EBIC) in n- and p-type silicon. The measurements were made on the same samples prepared for the DLTS and TEM studies[7]. As both methods required high density of precipitates, copper was diffused at 850°C, which corresponded to the equilibrium copper concentration of 10^{17} cm^3. To obtain samples with precipitates of different size, cooling rates were varied by using different quenching solutions, i.e. silicon oil (estimated quench rate 100-250 K/s), ethylene glycol (1000 K/s) and 10% solution of NaOH (2000 K/s). The copper precipitates had the form of thin platelets, lying primarily in {111} planes. Their diameter was determined by the quenching rate and ranged from 250-300 nm after quench in silicon oil to 50-60 nm in ethylene glycol and 30 nm in NaOH. The diffusion length of minority carriers was determined from the dependence of EBIC collection efficiency versus accelerating voltage. The contrast of separate precipitates could be distinguished only on the sample, quenched in silicon oil, which had the lowest density of precipitates due to their larger size. The EBIC image, obtained

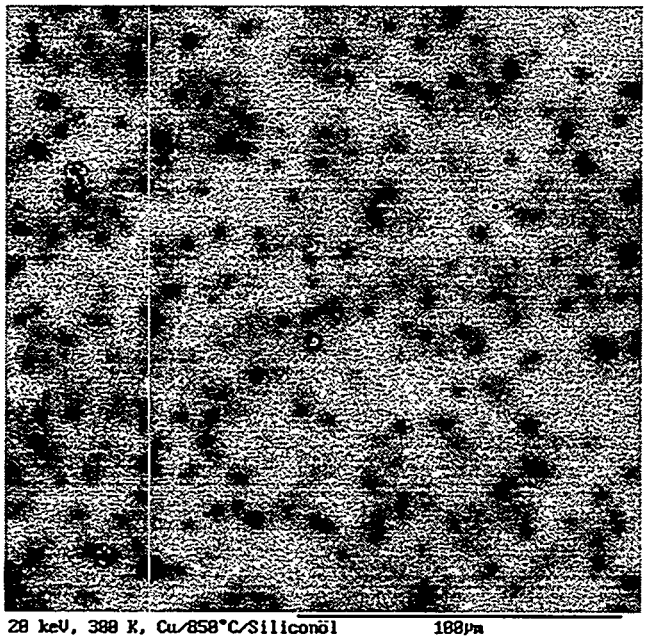

Fig.2. EBIC image of n-type silicon sample, contaminated with copper at 850 C. The image was taken at 300 K.

at the temperature 80 K, is presented on Fig.2. The distance between separate precipitates was about 5-10 μm. The contrast of the EBIC image was rather low and increased from 6% at 80 K to 7% at 300 K. The diffusion length slightly decreased with increasing temperature and was equal 14 μm at 80K and 13 μm at 300 K. Samples, quenched in ethylene glycol, had smaller size and larger concentration of precipitates and had diffusion length 2.6 μm at 80 K and 2.2 μm at 300 K. Finally, n and p-type samples quenched in NaOH solution had a diffusion length less than 2 μm.

The recombination activity of copper atoms in interstitial sites and in precipitates can be compared using this experimental data. The precipitates of copper were about 30 nm in diameter and 1-2 monolayers thick after quench in NaOH solution. Assuming that the precipitates were $CuSi_3$, one can estimate that each precipitate contained about $5 \cdot 10^4$ atoms of copper. Thus, for an initial concentration of copper of about 10^{17} cm^3, the density of precipitate sites is about $2 \cdot 10^{12}$ cm^{-3}. Based upon this data, to obtain a diffusion length of 200 μm, the density of similar sized copper precipitates must be less than $2 \cdot 10^8$ cm^{-3}, which corresponds to an initial copper concentration in the range of 10^{12} cm^{-3}.

The deleterious role of microdefects on the lifetime of minority carrier in solar cells has been discussed for a long time (see for example Ref.8). Recently, M.Werner[9] detected by TEM several types of microdefects. One of these types were planar defects lying in {111} planes. Though there is no direct experimental data on the structure of defects, the similarity of planar {111} defects reported in Ref.9 to the structure of Cu-precipitates suggest them as a possible candidate to the main lifetime reducing defects in silicon. This assumption is in line with the data, recently reported by A.Correia et al.[10] who found that in samples, contaminated with copper, the diffusion length of the minority carriers dropped to more than an order of magnitude due to the defects, which had the form of platelets in (111) planes with the diameter of about 12 nm. These defects were surrounded by strong deformation fields, which is typical for Cu-precipitates.

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Selective Nucleation and Solid Phase Epitaxy Process For Si Thin Film Photovoltaics

Claudine M. Chen and Harry A. Atwater
Thomas J. Watson Laboratories of Applied Physics
California Institute of Technology, Pasadena, CA 91125

INTRODUCTION

Future thin film poly-Si solar cells on low-cost substrates, will require methods for fabrication of approximately 10-30 μm thick Si films with large (30-100 μm) grain sizes at low temperatures. In order to take advantage of present low-cost glass substrates, processing temperatures are limited to 600 °C or lower. With a selective nucleation and solid phase epitaxy (SNSPE) process, grain sizes of 10 μm have been achieved to date at 600°C in 100 nm Si thick films on amorphous SiO_2, with potential for greater grain sizes. Selective nucleation occurs via a thin film reaction between a patterned array of 20 nm thick In islands which act as heterogeneous nucleation sites on the amorphous Si starting material. Crystal growth proceeds by lateral solid phase epitaxy from the nucleation sites, during the incubation time for random nucleation. The largest achievable grain size by SNSPE is thus approximately the product of the incubation time and the solid phase epitaxy rate. Electronic dopants such as B, P, and Al, were found to enhance the solid phase epitaxy rate at high concentrations. The optimum doping concentration to produce large grain size by SNSPE is constrained by several competing factors, including the electronic enhancement effect, doping segregation at the amorphous-crystal interface, and unwanted heterogeneous nucleation resulting from dopant precipitation at concentrations above the solid solubility limit.

SELECTIVE NUCLEATION AND SOLID PHASE EPITAXY PROCESS

The overall process for selective nucleation and solid phase epitaxy (SNSPE) of Si is shown in Fig. 1. A thin film of a-Si is first crystallized by SNSPE. To maximize the extent of grain growth during the incubation time for nucleation, crystals are nucleated at specified locations in a periodic array at the beginning of the anneal. Metal induced crystallization enables crystal nucleation at these specified sites with virtually no incubation period [1]. The crystallized film then forms a template upon which a thicker Si layer can be grown by vertical solid phase epitaxy of deposited a-Si layer grown on the template.

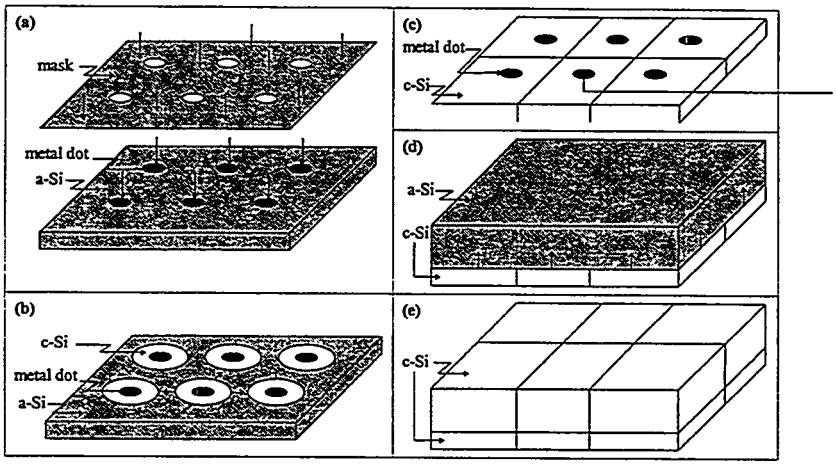

Figure 1: Procedure for fabricating large grain poly-Si: (a) metal is deposited through a mask to form patterned film on a-Si layer, (b) sample is annealed to nucleate and grow c-Si, (c) seeded grains impinge on each other, film is completely crystallized, (d) additional layer of a-Si is grown on the thin film seeded layer by vertical SPE of an a-Si layer deposited on the template, and (e) sample is annealed to crystallize device layer.

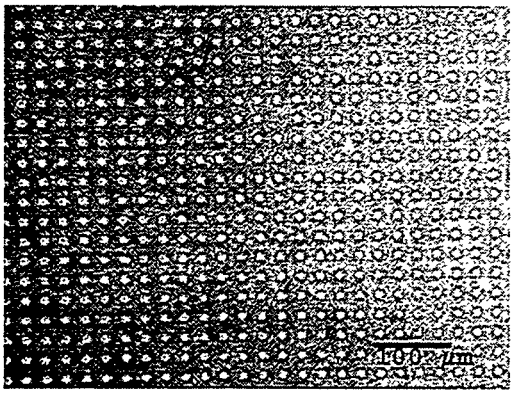

Figure 2: Optical image of Al-doped a-Si (peak conc. 5.5E19/cm^3) samples after 450 °C/20 minutes, 600°C/3.5 hours anneals. The brighter areas, corresponding to c-Si, are separated by 20 μm and were nucleated by In.

The expected grain size can be very roughly estimated as the product of the transient incubation time, t_{inc}, and the solid phase epitaxial growth rate, v_{SPE}. Once random nucleation starts, further growth of the seeded crystals will be inhibited by impingement of randomly nucleated grains, thus limiting the grain size to that which is achievable before random nucleation occurs. The SPE rate of Si as an Arrhenius function of temperature (T) [2] is given by,

$$v_{SPE} = v_0 e^{-E_A/kT}, \text{ where } v_0 = 2.3 \times 10^8 \text{ cm/s and } E_A = 2.7 \text{ eV},$$

and the transient incubation time as an exponential function of T is given by [3],

$$t_{inc} = t_0 e^{E_A/kT}, \text{ where } t_0 = 1.12 \times 10^{-11} \text{ s and } E_A = 2.7 \text{ eV}.$$

EXPERIMENTAL RESULTS

Selective nucleation and solid phase epitaxy was investigated in 100 nm a-Si films, deposited by ultrahigh vacuum electron beam evaporation at low temperatures onto SiO_2 films on Si substrates. Films were implanted with 13 keV $^{10}B^+$, 37 keV $^{31}P^+$, or 30 keV $^{27}Al^+$; at these energies, the dopant distributions span the a-Si thickness. Peak concentrations were: for B, 2.0x10^{20}/cm^3 and 9.8x10^{20}/cm^3; for P 2.1x10^{20}/cm^3, 1.1x10^{21}/cm^3, and 2.1x10^{21}/cm^3; and for Al, 1.0x10^{19}/cm^3, 1.9x10^{19}/cm^3, and 1.0x10^{20}/cm^3.

Indium dots, deposited by thermal evaporation in a high vacuum evaporation chamber, created seed regions that enabled selective heterogeneous nucleation. The 20 nm thick In layer was evaporated through a mechanical mask in a grid pattern of 5 μm diameter circles with a periodic spacing of either 20

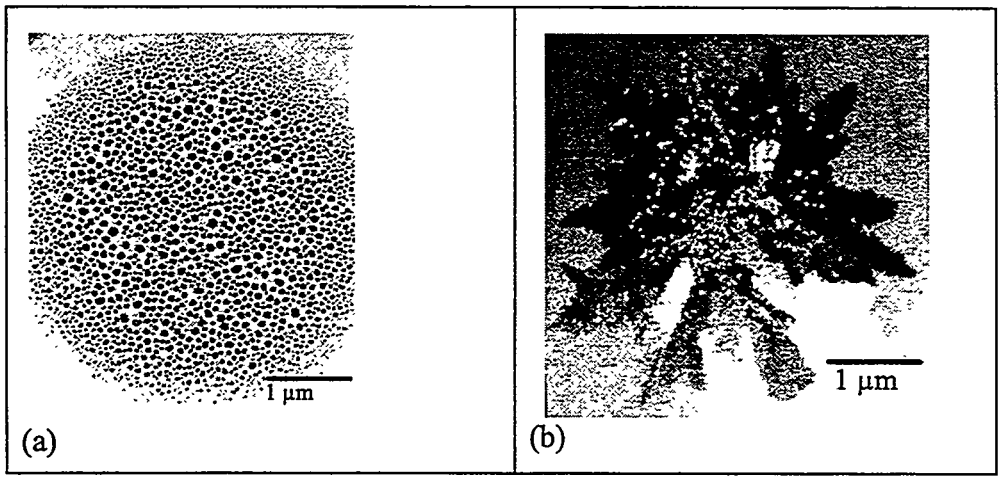

Figure 3. (a) TEM bright field image of an In dot after initial 20 minute anneal. (b) TEM plane-view DF image of an In seeded grain.

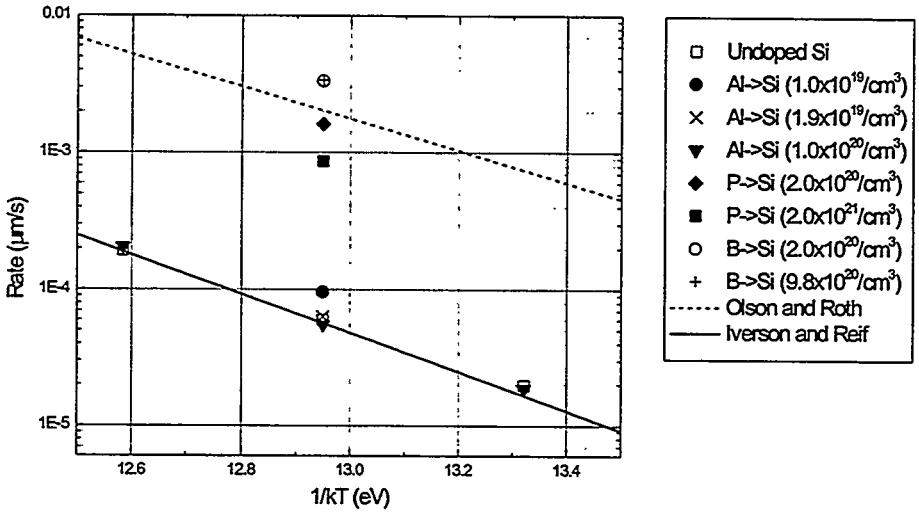

Figure 4. Current work and other experimental data for solid phase epitaxy rate for intrinsic and doped Si as function of temperature.

μm or 25 μm. The samples were annealed at 450°C for 20 minutes to induce selective nucleation of a-Si, and then an additional 600°C for various times, depending on the growth rate. Anneals at 575°C and 625°C for intrinsic Si and Al with a peak concentration of $1.0x10^{20}/cm^3$ were also done. After the 450°C anneal, the In dot separated into many In islands as seen in Fig. 3. The discontinuous film seeded several Si crystals per In dot. This results in multiple crystals with different orientation at each nucleation site, which reduces the maximum possible grain size. Development of a method for nucleating one crystal for each nucleation site, which is more desirable, is underway.

In Fig. 4, the growth rates versus temperature of the various samples are compared to the results of Ref. [2] (for vertical SPE for <100> orientation), and Ref. [3] (for polycrystalline silicon nucleated by random nucleation). The SPE rate was determined by measuring the change in the position of growth fronts at successive anneal times. The growth rate as a function of temperature of the intrinsic Si coincided with the results of Ref. [3]. This suggests that the indium, which nucleates the crystals, has little influence on the growth kinetics.

Electronic dopants such as B, P, and Al enhanced the solid phase epitaxy rate in some samples. The growth rate of the Al-doped Si coincided with intrinsic Si for the two higher doses(peak conc. $1.9x10^{19}/cm^3$, and $1.0x10^{20}/cm^3$), and was enhanced by a factor of 2 relative to intrinsic Si for the lowest dose ($1.0x10^{19}/cm^3$). The growth rate of P-doped Si was enhanced by a factor of 15 relative to intrinsic Si (peak conc. $2.0x10^{21}/cm^3$) and 27 relative to intrinsic Si (peak conc. $2.0x10^{20}/cm^3$). The growth rate of B-doped Si (peak conc. $2.0x10^{20}/cm^3$ and $9.8x10^{20}/cm^3$) was enhanced by a factor of over 50 relative to intrinsic Si. An unexpected result is that the growth rate for higher concentrations is less than lower concentrations, which may be related interfacial dopant segregation for dopant peak concentrations near or above their solid solubility limits in crystalline Si at the anneal temperature. At 600°C, Al has a solid solubility of $7x10^{18}$ atoms/cm^3, whereas the solubility limits for B and P can be linearly extrapolated to be roughly $6x10^{18}$ atoms/cm^3, and $6x10^{19}$ atoms/cm^3, respectively[4]. We speculate that doping concentrations in excess of the solubility limit can drive impurity precipitation, and that precipitates could then impede interface motion, resulting in a lower growth rate. However, the coincidence of the solid phase epitaxy rates for Al-doped films at the two higher doses with the intrinsic solid phase epitaxy rate is not understood, and may indeed be purely coincidental.

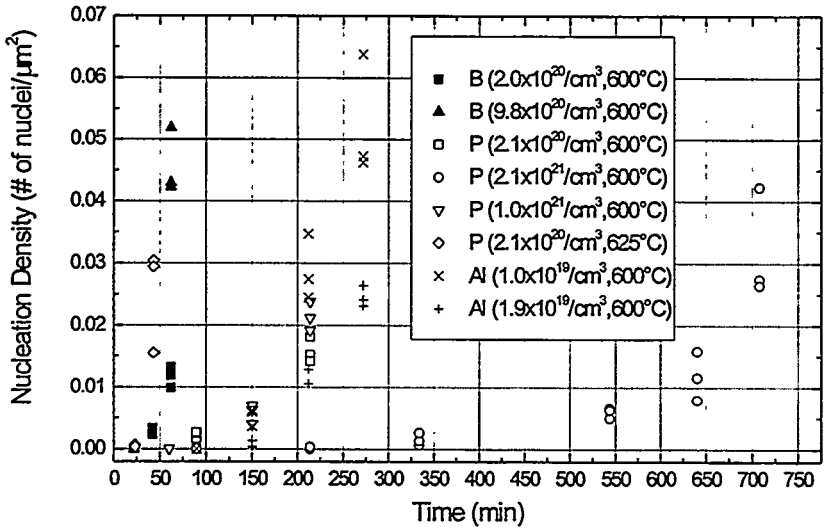

Figure 5. Observable random nucleation density for doped Si as a function of anneal time.

As important as the growth rate in SNSPE is the random nucleation rate in the "bulk" of the a-Si film, and at its surfaces, since the random nucleation rate essentially determines the achievable grain size. The larger the random nucleation rate, the sooner the seeded crystal will be impinged by randomly nucleated crystals. For example, among all the dopant types and concentrations investigated, the solid phase epitaxy rate for boron was highest, but B doping also yielded a high random nucleation rate relative to other dopant species, so there was no increase in the maximum crystal grain size nucleated by the seed. Figure 5 shows the observable random nucleation density for the doped Si layers as a function of anneal time. This figure does not distinguish between homogeneous or heterogeneous nucleation events, and only reflects nucleation observable by optical microscopy, with minimum size of 0.1 μm.

Grain size determination was complicated by the irregularly-shaped growth fronts and twin boundaries observable during grain growth, and also by deformation of the layer after specimen thinning for TEM imaging. The largest observed grain sizes were approximately 10 μm for P-doped Si with a peak P concentration of $1.0x10^{20}/cm^3$.

CONCLUSIONS

Selective nucleation and solid phase epitaxy (SNSPE) was demonstrated for intrinsic and B, P, and Al doped Si layers. Selective nucleation by metal-induced nucleation, has not led to date to a single crystal per nucleation site, which reduces the area into which the crystal can grow and therefore limits the maximum crystal size. Alternate methods of nucleating one crystal per site will be studied in future work. Dopant enhancement of the solid phase epitaxy rate was demonstrated, but the dopant concentrations appeared to be higher than optimum. Further experiments with dopant concentrations below the solubility limit are underway.

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RELATIONSHIPS BETWEEN ROOM TEMPERATURE PHOTOLUMINESCENCE AND ELECTRONIC QUALITY IN MICROCRYSTALLINE SILICON

J. Koshka, S. Ostapenko, J. Cao* and J. P. Kalejs*
Center for Microelectronics Research, University of South Florida,
E. Fowler Avenue, Tampa, FL 33620-5350
* ASE Americas Inc., 4 Suburban Park Drive, Billerica, MA 01821

Introduction

The study of recombination mechanisms in solar materials is an important activity directed toward understanding of processes which will improve bulk quality during cell processing and increase solar cell efficiency. We extend this study here for the first time to non-radiative recombination centers in crystalline silicon by relating room temperature photoluminescence (RTPL) intensity to bulk material electronic quality. Our studies are carried out in multicrystalline silicon grown by the Edge-defined Film-fed Growth (EFG) technique. EFG silicon wafers, as many other crystalline silicon photovoltaic materials, require special device processing steps to improve performance of solar cells and achieve optimal efficiencies. Each process step has a synergetic effect on bulk diffusion length, and contributes integrally to determining wafer quality in the solar cell. We have previously described bulk minority carrier diffusion length improvements monitored by surface photovoltage (SPV) measurement, or lifetime "upgrading", for individual steps used in the EFG cell manufacturing line: phosphorus diffusion, hydrogen passivation and aluminum alloying (1). Each of these processes acts to reduce recombination activity at minority carrier traps during the upgrading.

Non-radiative recombination, on the other hand, can be monitored using the PL technique, specifically, by spatially resolved PL mapping. We present here results which show a large band-to-band PL intensity increase for the same processing steps which produce material quality upgrading and the SPV diffusion length changes usually associated with increases in cell efficiency. PL mapping is repeated on a given area of a wafer undergoing a sequence of processing steps, and this repeated mapping over the full 10 cm x 10 cm area of an EFG wafer provides a weighted average measure of the PL intensity changes for a given processing step. We discuss the relation of the RTPL intensity changes to SPV results, and show that RTPL provides a means of monitoring processing steps which contribute toward optimizing solar cell efficiency and are as convenient a method for mapping of the wafer as is SPV.

Experimental Details

We have developed and applied a spatially resolved PL non-contact technique to mapping EFG polycrystalline silicon wafers and solar cells (2). The PL spectrum was analyzed using a SPEX-500M grating spectrometer coupled to a liquid nitrogen cooled Ge detector, or alternatively with a PbS detector cooled with dry ice. The PL intensity was modulated with a mechanical chopper and converted by a photodetector to a signal which could be monitored by a lock-in amplifier. The 514 nm Ar laser line with power ranging from 30 to 100 mW was used as the PL excitation source. Room temperature PL mapping of the silicon wafer was carried out with a spatial resolution controlled by the Ar laser spot size, which ranged from 100 μm up to 3 mm. The smallest step of the x-y table driver was 1 μm. The PL spectra were corrected to the

sample mounted to the cold finger of a cryostat capable of ranging between 4.2 and 300 K. The SPV diffusion length (L) measurements were carried out using a system described previously (3).

PL spectra data were obtained on EFG wafers by mapping PL responses at the same locations over the surface of a 10 cm x 10 cm wafer before and after an individual solar cell processing step. PL spectra and L value measurements were made on the same samples to provide data for correlation.

Results

Typical PL spectra of an EFG wafer at 4.2 K and at room temperature are shown in Fig. 1. The dominant PL line at 4.2 K is the boron-bound exciton (B^{TO}) at 1.093 eV. This arises from the boron dopant present at levels of 3-5x10^{15}/cm^3. At 300 K, the exciton lines are quenched and two broad PL bands persist and can be resolved. The maximum at 1.1 eV corresponds to band-to-band recombination in silicon and its intensity is related to the concentration of non-radiative recombination centers in the material. The band peaked at 0.8 eV is attributed to a "defect" arising from oxygen precipitates. We use the band-to-band peak to correlate to the local SPV diffusion length at each point in the wafer after different stages of processing.

RTPL maps were obtained initially on as-grown wafers. These maps formed the basis of the reference PL intensity distribution obtained over the full area of an individual wafer, as shown in the bottom trace of Fig. 2. The reference bar designated as "initial", on the far left for each wafer designation in Fig. 3, gives the averaged PL intensity over the 10 cmx10 cm area of each of the 5 wafers that were mapped in this study. After the initial PL mapping, each wafer next was subjected to phosphorus diffusion (N1-second trace from bottom in Fig. 2 and second bar from left in Fig. 3) and the mapping repeated again; the N2 and N3 distributions in Fig. 2 and the rightmost two bars for each wafer in Fig. 3 represent the PL measurements repeated on the same wafers at the same locations after hydrogen passivation and then after combined hydrogen passivation and aluminum alloying, respectively. These processing steps are identical to those used in producing SPV diffusion length changes and material upgrading that we reported previously for the EFG manufacturing line (1). Note that the spectral amplitudes reported in Figs. 2 and 3 are plotted with logarithmic scales, and that the changes in the PL intensity represent large variations spanning several orders of magnitude.

SPV measurements to correlate to the PL intensity have also been performed, by taking PL and L line scans across the same location on the same sample. These are shown in Fig. 4. A map of PL intensity and L is given in Fig. 5. The best fit line correlation indicates that PL intensity $\sim L^2$. Since $L^2 \sim \tau$, the data in Fig. 5 are a strong indication that RTPL intensity is indeed a measure of recombination lifetime and can be used, like L, to track material electronic quality changes in polycrystalline silicon wafers.

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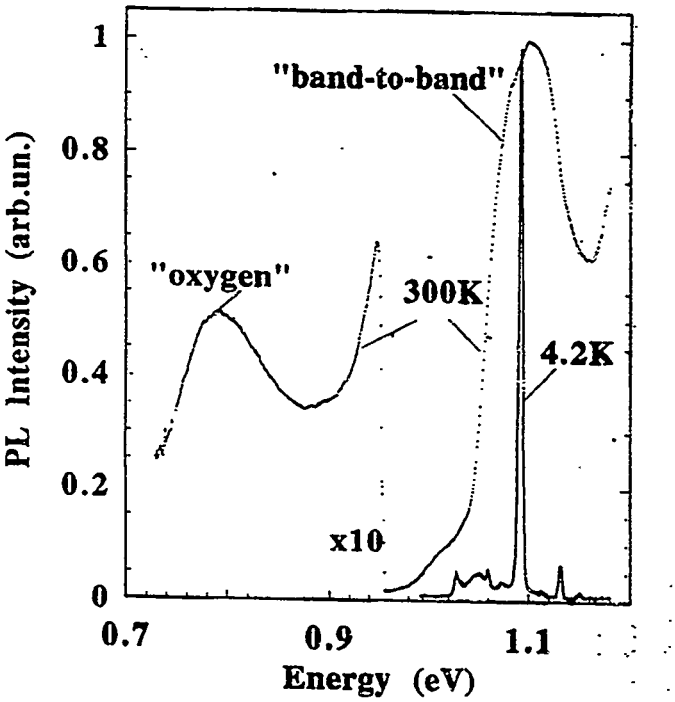

Fig. 1. Photoluminescence in EFG Si at 4.2 K and at room temperature; excitation 514 nm, 40 mW.

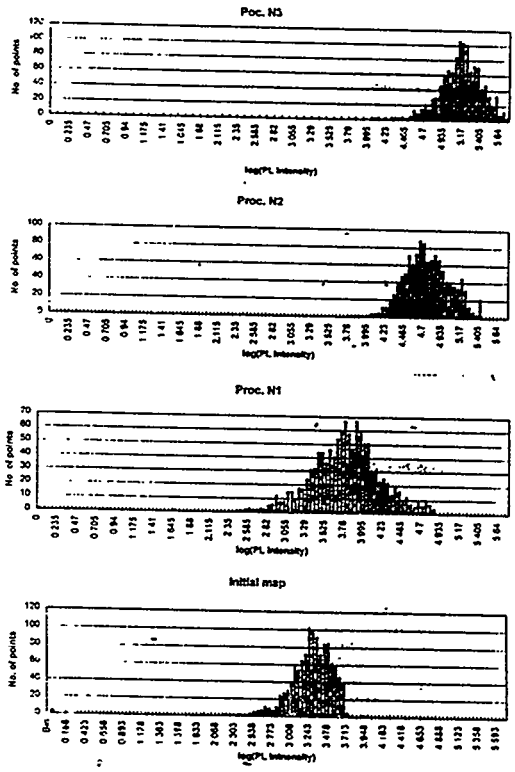

Figure 2. Changes in B^{TO} PL intensity distribution over a 100 cm^2 sample for each cell processing step.

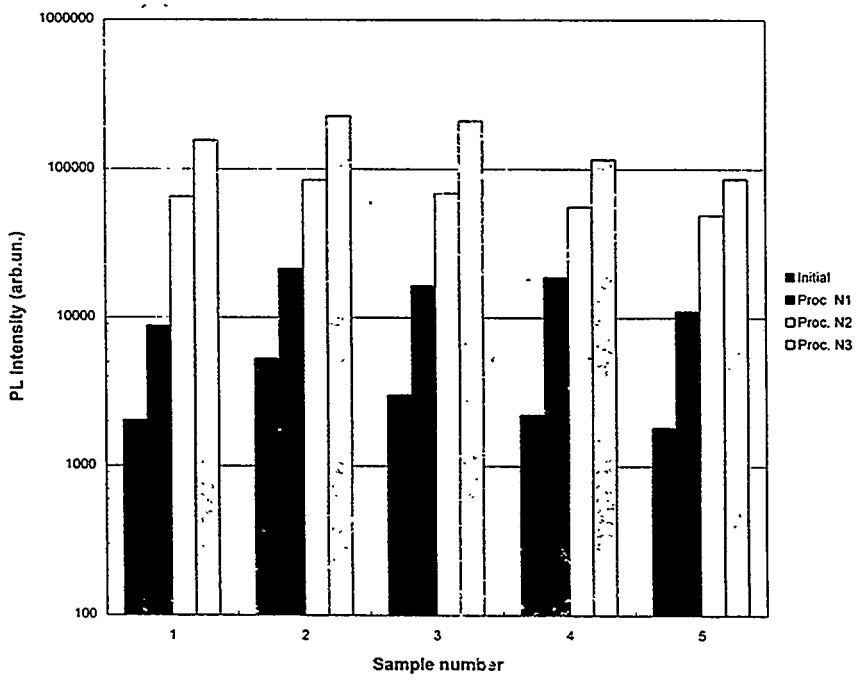

Fig 3. Increase in PL B^{TO} peak intensity averaged over a 100 cm^2 sample (Nos. 1-5) at each processing step.

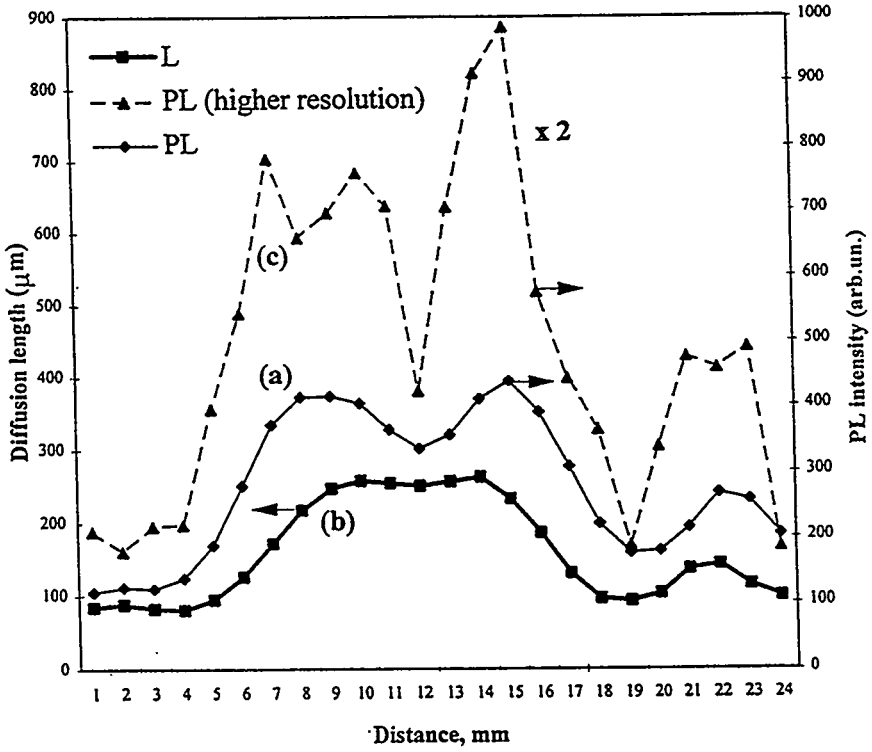

Fig.4. Room temperature band-to-band PL intensity (a) correlates with distribution of the bulk minority carrier diffusion length (b). At higher resolution about 1mm, additional features of the bulk recombination are revealed in the PL

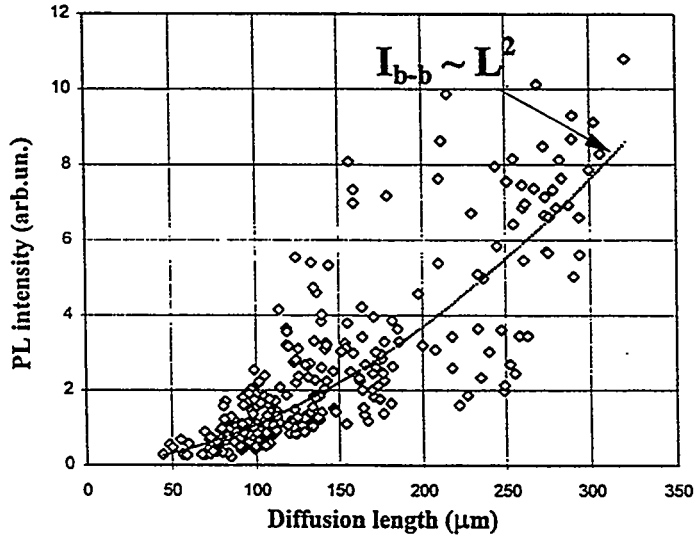

Fig. 5. Band-to-band PL intensity measured across the entire 10cm x 10cm EFG wafer reveals the power-law dependence versus minority carrier diffusion length.

MODELING OF VOID NUCLEATION AND GROWTH IN SILICON

P.S. Plekhanov, U. M. Gösele, and T. Y. Tan
Department of Mechanical Engineering and Materials Science, Duke University, Durham, NC 27708-0300

The trend of using Czochralski grown (CZ) Si crystal wafers of very large diameters, up to 30 cm or beyond, raised new problems of gate oxide integrity. Recent studies have shown that it was degraded by the so called D-type swirl defects[1] that were identified to be voids in Si reaching 100 nm in size. When unaltered by processing the voids are polyhedral-shaped, with their faceted surfaces consisting of Si {111} planes covered by thin SiO_2 layers.[2-4] These defects form under vacancy (V) supersaturation conditions due to the precipitation of V. In this process, there are two forms of competition: between nucleation of voids and V-type dislocation loops (DL) and between growth of existing defects and nucleation of new ones. In this work, the nucleation and growth of the V-type extended defects is examined assuming that the process is homogeneous and is due to precipitation of V only, i.e., with the contribution of self-interstitials ignored.

At the V concentration C_V, the Si crystal Gibbs free energy change due to the formation of a V-type edge DL, which may or may not contain also an intrinsic stacking fault (SF), is

$$\Delta G_d=\pi r_d^2\gamma+ r_d\frac{\mu b^2}{2(1-\nu)}\left(\ln\frac{8\alpha r_d}{b}-1\right)-\frac{\pi r_d^2 b}{\Omega}k_B T\ln\frac{C_V}{C_V^{eq}}, \qquad (1)$$

where r_d is the radius of the DL, γ=60 ergs cm^{-2} is the intrinsic SF energy density (γ=0 for the perfect DL), μ=6.45x10^{11} dynes cm^{-2} is the shear modulus of Si, b is the magnitude of the dislocation Burgers vector (b=3.135x10^{-8} cm for the <111>/3 Frank partial DL and 3.84x10^{-8} cm for the <110>/2 perfect DL), ν=0.228 is Poison's ratio of Si, α=4 is a parameter accounting for the dislocation core energy, Ω=2x10^{-23} cm^3 is the volume of one V, k_B is Boltzmann's constant, T is the absolute temperature, and C_V^{eq} is the V thermal equilibrium concentration. On the right-hand side of Eq. (1), the first term is due to the intrinsic SF energy, the second is due to the edge dislocation elastic and core energy, and the third is due to the consumption of V. Similarly, for a spherical void of radius r_v,

$$\Delta G_V = 4\pi r_V^2\sigma-\frac{4\pi r_V^3}{3\Omega}k_B T\ln\left(\frac{C_V}{C_V^{eq}}\right), \qquad (2)$$

where σ=1230 ergs cm^{-2} is the Si surface energy density. Both ΔG_d and ΔG_v are zero for r=0, increase to a maximum (critical) value ΔG^* at the critical size r=r^*, and then decrease. The quantity ΔG^* is the needed activation energy for defect nucleation to occur. In Fig. 1, the T=900°C ΔG_d^* and ΔG_v^* values are plotted as functions of the V-supersaturation value C_V/C_V^{eq}. These curves are fairly insensitive to temperature changes within the range of 700 to 1200°C. Assuming that the V concentration in as-grown Si crystal just after crystallization is equal to the thermal equilibrium concentration at the melting temperature, $C_V(T) = C_V^{eq}(T_m)$, and V are frozen into a crystal section when it is cooled down, we have calculated the values of C_V/C_V^{eq}. They are plotted in Fig. 2 as functions of T and using enthalpy of V formation h_V^f as a parameter in the range 1 to 4 eV, for it is not known precisely. From Figs. 1 and 2, it can be seen that in the considered temperature range the DL nucleation barrier cannot be lower than ~15 eV. Thus, the possibility of nucleating a V-type DL can be ruled out, because the ΔG_d^* values are excessively large. But the nucleation barrier of voids is significantly smaller than that of both faulted and perfect DL at any V supersaturation value. Besides, the free energy of a void is significantly smaller than that of a DL containing the same amount of V, as can be seen in Fig. 3. The situation changes only for voids larger than ~50 nm and DL larger than ~0.8 μm in radius. Hence, even if a V-type DL has nucleated, it is likely to transform into a void.

The void nucleation rate can be written as $J = C_{nucl}^{eq} Zw/\Omega$, where C_{nucl}^{eq} is the thermal equilibrium concentration of the critical nuclei, Z is Zeldovich factor for nonequilibrium distribution taken to be equal to 0.001, and w is the frequency of V impingement onto a void. In more details,

$$J = \frac{C_V}{\Omega} \exp\left(-\frac{\Delta G_V^*}{k_B T}\right) Z\, 4\pi (r_v^*)^2 \frac{C_V D_V(T)}{\Omega d}, \qquad (3)$$

where d is the interatomic distance (2.35 Å). The V contribution to Si self-diffusivity is[5]

$$C_V^{eq} D_V = C_V^0 \exp\left(-\frac{h_V^f}{k_B T}\right) D_V^0 \exp\left(-\frac{h_V^m}{k_B T}\right) = 0.6 \exp\left(-\frac{4.0\ \text{eV}}{k_B T}\right) \text{cm}^2/\text{s}, \qquad (4)$$

but the individual D_V and C_V^{eq} values are not established. Using h_V^f as a parameter in the range 2-4 eV and assuming that all V frozen in the crystal eventually precipitate to form voids of final radius r_f=50 nm distributed within the crystal at volumic concentration ρ=5x10^5 cm^{-3} (these values were taken from the paper by Ueki *et.al.*[4]), we calculated the void nucleation rate as functions of T and h_V^f. Integrating it with respect to time and taking into account the time dependence of temperature one can obtain concentration of void nuclei as a function of time or temperature. For our calculations, we used cooling rate 0.02 K/s for T>300 °C and 0 for T < 300 °C. The void nuclei concentration, calculated by assuming that C_V does not change, is plotted in Fig. 4. The intersection of each curve with the line of observed void concentration ρ corresponds to the temperature of nucleation, T_N. Nucleation of most voids occurs close to T_N. At higher temperature (earlier stage), the nucleation rate is significantly smaller, but at lower temperatures (later stage) V concentration is decreased due to the growth of voids. The plot of T_N versus the enthalpy of V formation is shown in Fig. 5. It is noted that in the actual process, the void concentration asymptotically approaches ρ.

We have modeled also void growth under the assumption that they are spherical in shape and the process is limited by V diffusion. Voids were assumed to be distributed homogeneously within a section of the crystal, so that each void grows by the precipitation of V from a spherical diffusion domain of radius $R_{max} = (3\rho/4\pi)^{1/3}$ surrounding it. Since r is changing, the probelm involves a moving boundary. At the void surface the V concentration is the dynamic equilibrium value $C_V(r_v,t)$= $C_V^{eq}\exp(2\sigma\Omega/(r_v k_B T))$ while at the outer border of the diffusion domain the V flux is zero. A set of differential equations has been written subject to these conditions and solved numerically using the same set of constants as for the nucleation rate calculations. The growth process was found to have two distinct phases: reaction limited with linear dependence of r_v on time and diffusion limited with parabolic time dependence. The growth is faster at higher h_V^f values. Temperature dependence of growth rate has a maximum. With h_V^f=3 eV, it occurs at about 1100 °C at the early, linear stage of growth and higher than 1300 °C at the final, parabolic, stage. This is consistent with the observation that the temperature of the fastest nucleation is lower than the temperature of the fastest growth. Due to lower V supersaturation, the growth rate is lower at a higher temperature. Since nucleation of most voids occurs close to T_N, the characteristic growth time can be defined as the time necessary for a void nucleated at T_N to grow to radius r=0.9r_f. The characteristic growth time as a function of the h_V^f value is shown in Fig. 6. The cooling rate used is the same as in the nucleation case.

Figure 4 shows that the observed concentration of voids of 10^6 will not be obtained for h_V^f lower than ~2.8 eV, even if the concentration of V is assumed to remain constant. Also, Fig. 6 shows that for h_V^f lower than 3.1 eV, the radius value close to r_f cannot be obtained within a reasonable time. The corresponding minimum nucleation temperature is about 720 °C. It should also be taken into account that concentration of V does not remain constant during the nucleation process, since V are consumed by nucleation and growth of voids, which makes the lower limit of h_V^f even more stringent. On the other hand, if too high a value of h_V^f is assumed, some voids nucleated at early stages of cooling will have enough time to grow and absorb most of V, leading to a significantly smaller number of nucleated voids which will grow to much bigger sizes. Their concentration may be reduced by a factor of 1000 or more while radius increased by a factor of 10 or more. This consideration allows us to determine the high limit of h_V^f.

The outcome of the competition between the growth of existing voids and the nucleation of new ones depends on the enthalpy of V formation. High h_V^f value results in high nucleation temperature, low void concentration and large void sizes. Low h_V^f value results in low nucleation temperature, high void concentration and small void sizes. To obtain results compatible with observed void concentra-

tion ρ and sizes r_f, *characteristic* times associated with void nucleation and growth processes need to be close to each other. The characteristic time of nucleation can be defined as the time necessary to nucleate voids to concentration 0.5ρ at the rate corresponding to T_N. A characteristic time of V depletion due to void growth can be defined as the time needed to reduce the V concentration at the diffusion domain outer boundary by a factor of 2 from its original value, provided that the temperature reaches T_N at this moment. This time was obtained from the growth simulations. Plots of nucleation and V depletion characteristic times as functions of h_V^f are shown in Fig. 6. These times are equal at h_V^f=3.2 eV and differ by no more than a factor of 5 at h_V^f<3.6 eV which seems to be a safe estimation of the upper limit of h_V^f value while the lower limit obtained from the growth kinetics considerations is 3.1 eV. The corresponding values of T_N are 890 and 720 °C. Our present findings appear to be reasonable in view of the facts that: (i) in one observation the D-defect formation temperature is given to be ~900°C;[6] (ii) low temperature (4 K) electron irradiation produced V migrates with h_V^m<0.5 eV between 80-100 K;[7] and (iii) a recent theoretically calculated V formation enthalpy is 3.65 eV.[8]

The enthalpy of formation values were obtained assuming that all V in excess of thermal equilibrium concentration are consumed by the end of the crystal growth. In the actual process, this may not be the case, and a significant fraction of V may stay frozen into the crystal. This can happen if h_V^f value is lower than 3.1 eV and the initial amount of V exceeds that needed to form voids at concentration ρ and radius r_f. In this case, the observed concentration of V and their sizes will depend on the cooling rate strongly. The above assumption can be verified by analysis of the growth rate and its correlation with concentration and sizes of voids, or a specific growth experiment can be carried out. In the experiment, the growing crystal should be cooled down to about 500 °C at a regular rate and then kept at that temperature for about 3 hours. This will ensure almost complete precipitation of V into voids without the voids start to shrink due to V outdiffusion. After that, the concentration and sizes of voids should be analyzed.

In conclusion, from the calculations of nucleation barrier of vacancy-type extended defects in Si, we have shown that the nucleation of voids is more favorable than that of dislocation loops. Under the assumptions V are at thermal equilibrium concentration at the crystal growth front, and their excess is almost totally precipitates into the growing voids by the end of the cooling, the homogeneous nucleation of voids was shown to be thermodynamically and kinetically possible. The calculated results can be matched to observed void concentrations and sizes if the enthalpy of vacancy formation is within the range 3.1 to 3.6 eV and the nucleation temperature is 720 to 890 °C.

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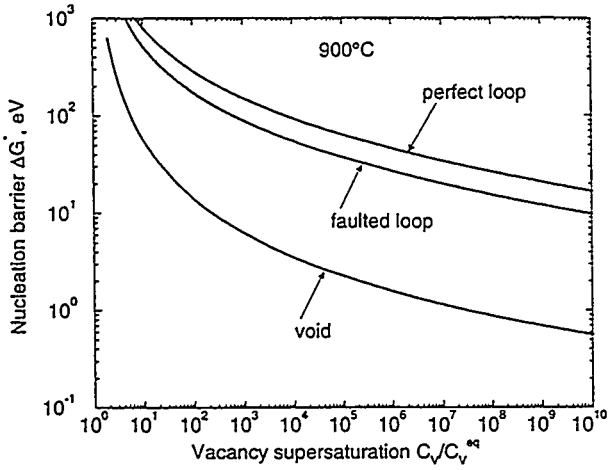

Fig. 1 The extended V-type defect critical nuclei activation free energies ΔG^* as functions of the V-supersaturation value C_V/C_V^{eq}.

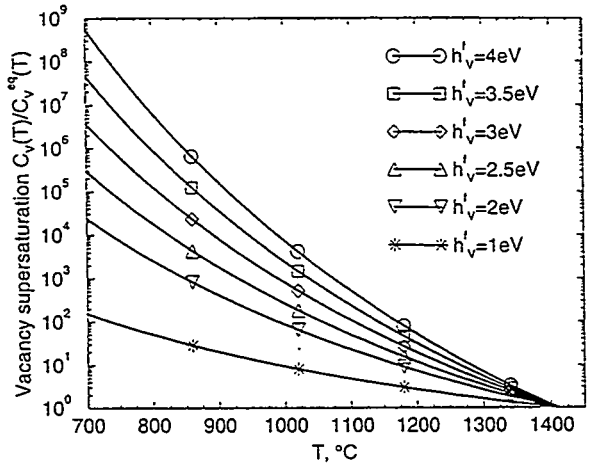

Fig. 2 The attainable V-supersaturation value as a function of temperature with the V formation enthalpy h_V^f as a parameter.

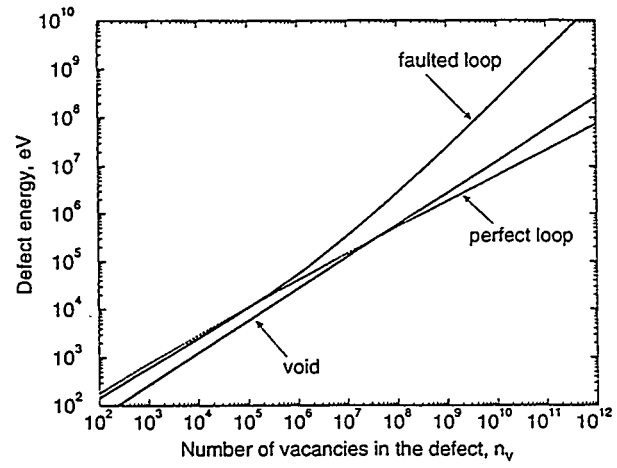

Fig. 3 The calculated free energies of extended V-type defects as functions of number of V contained in them.

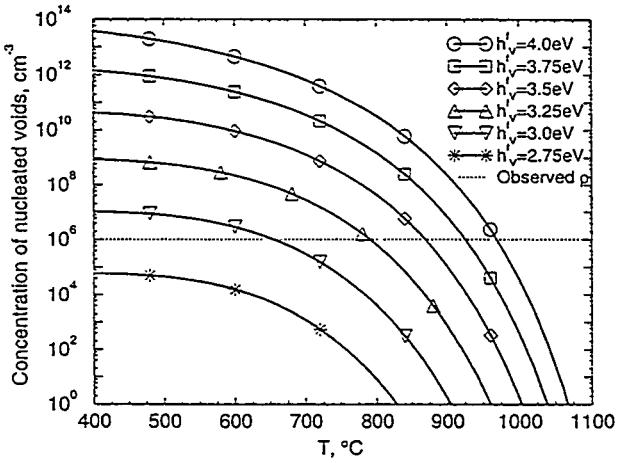

Fig. 4. Concentration of nucleated voids as a function of temperature, plotted using h_V^f as a parameter. The experimentally observed value ρ is shown for reference.

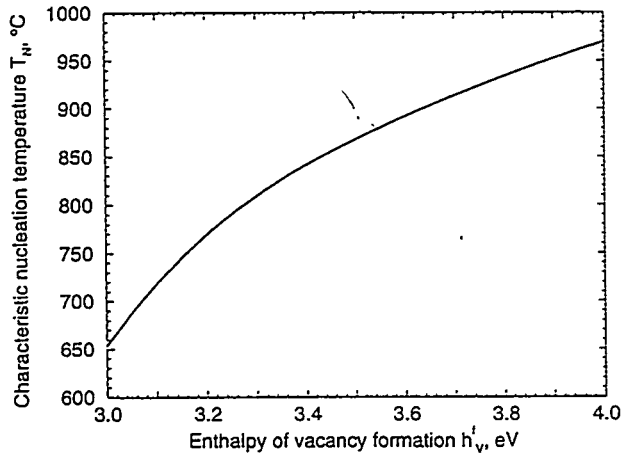

Fig. 5. Characteristic temperature of void nucleation T_N as a function of V formation enthalpy h_V^f.

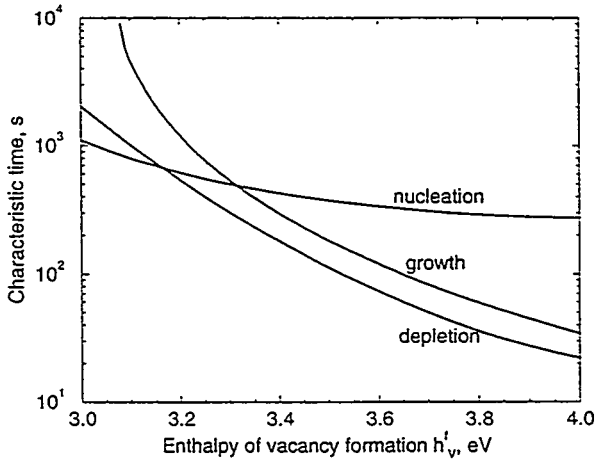

Fig. 6. Characteristic times of diffusion domain depletion, void nucleation and growth as functions of V formation enthalpy h_V^f.

Recent Improvements on the PVSCAN5000

Bhushan Sopori, Chris Gaylord, Karen Nemire, M. I. Symko and Jamal Madjdpour
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

PVSCAN5000 is a commercial instrument that was developed to rapidly map several key parameters of semiconductor materials and photovoltaic devices. The material parameters that PVSCAN5000 measures are the dislocation density and grain boundary distribution. These parameters provide feedback to the material manufacturer on the quality of the material and an insight for improving the manufacturing process. The cell parameters include reflectance and light beam induced current (LBIC) at two different wavelengths of light excitation. These data are used to produce the internal response of the cell. Because the internal responses for the long- and the short-wavelength excitation can be related to the bulk and the junction recombination, the generated data are used to produce maps of the minority carrier diffusion length and the near-surface recombination. These parameter maps allow PVSCAN5000 to be used for device analysis, process optimization, and process monitoring. PVSCAN5000 also provides information on the uniformity of the substrate material or a solar cell.

Figures 1 and 2 are schematics illustrating the operation and optics of PVSCAN5000. The operation is described in detail in previous publications. However, PVSCAN is continually being improved to enhance its applications and to incorporate user requests. The following items describe recent upgrades to the instrument.

- Average value of the measured parameter over the scanned area: this software addition produces a spatial-average value of the parameter over the entire scanned area. Figure 3 is a dislocation density map of a commercial 4 in x 4 in polycrystalline wafer. Local dislocation densities are depicted by the color legend, while the average value is 8.3 x 10^4 defects/cm^2. Similar averaging can be performed on any other parameter map, such as LBIC, minority carrier diffusion length, and reflectance.

- Zoom-in feature: selection of a limited area of interest and averaging its parameter value. Figure 4 illustrates this feature. It shows a zoomed image of the upper left corner of the wafer shown in Figure 3. The average dislocation density in this defect cluster is 3.0 x 10^5 defects/cm^2.

- Saving split images: PVCSAN5000 can simultaneously map and display grain boundaries and dislocations or specular and diffused reflectance. In the past, saving these

data as individual scans was not possible. We now have added a feature that allows each scan to be saved as a separate file.

- Parameter distribution (number versus range of the parameter values): this statistical capability has been added to allow the user to compare variations in the parameter values for different samples.

The following items describe future upgrades to PVSCAN5000.

- Etch pit size correction: this capability will automatically correct for any variations in the etching process that may arise from changes in the etch composition, etch time, and process differences (operator to operator).

- Standard samples: reference samples will be provided for calibrating dislocation density, reflectance, and the minority carrier diffusion length.

- Optional light source: interest in other materials has led to requests to change the wavelength of light suitable for these specific semiconductors. This feature will extend the range of wavelengths to those suitable for GaAs, CdTe, CIS, and a-Si.

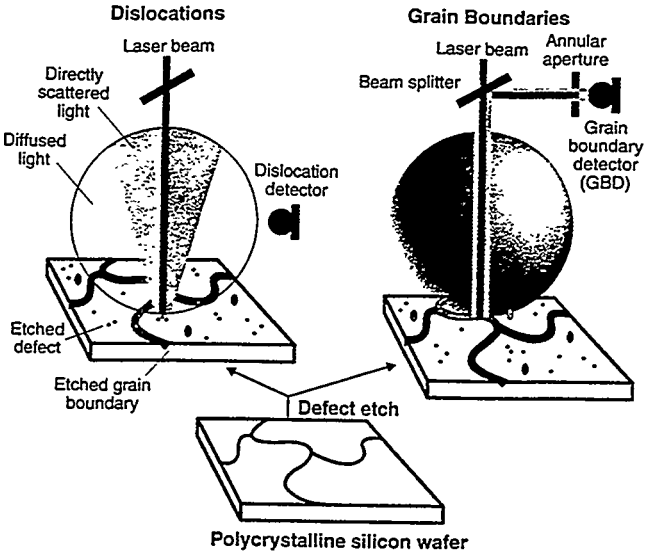

Figure 1. PVSCAN5000 uses differentially reflected light to distinguish between defect types.

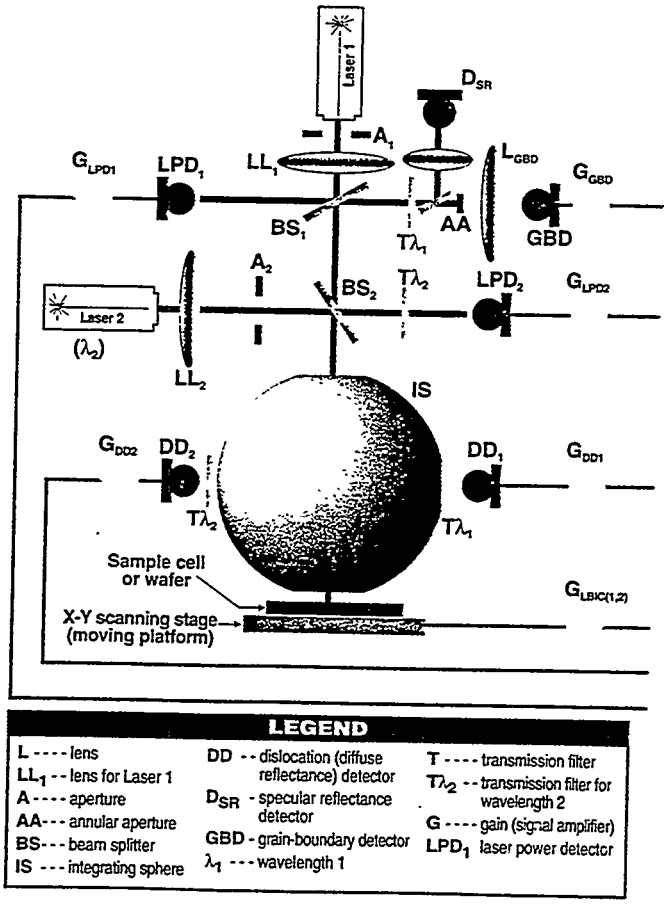

Figure 2. Schematic showing the optical components of PVSCAN5000.

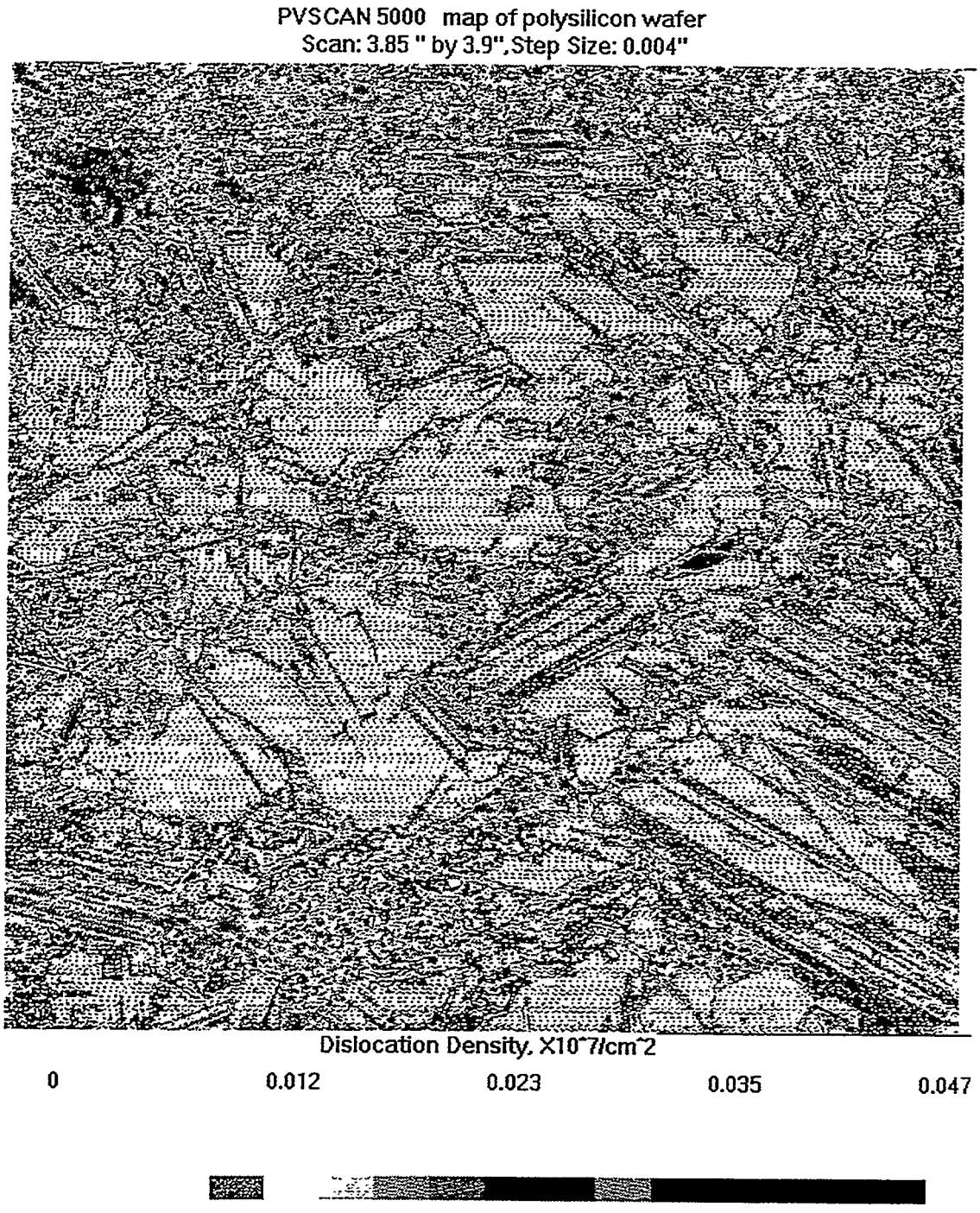

Figure 3. Dislocation density map of a commercial polycrystalline silicon wafer.

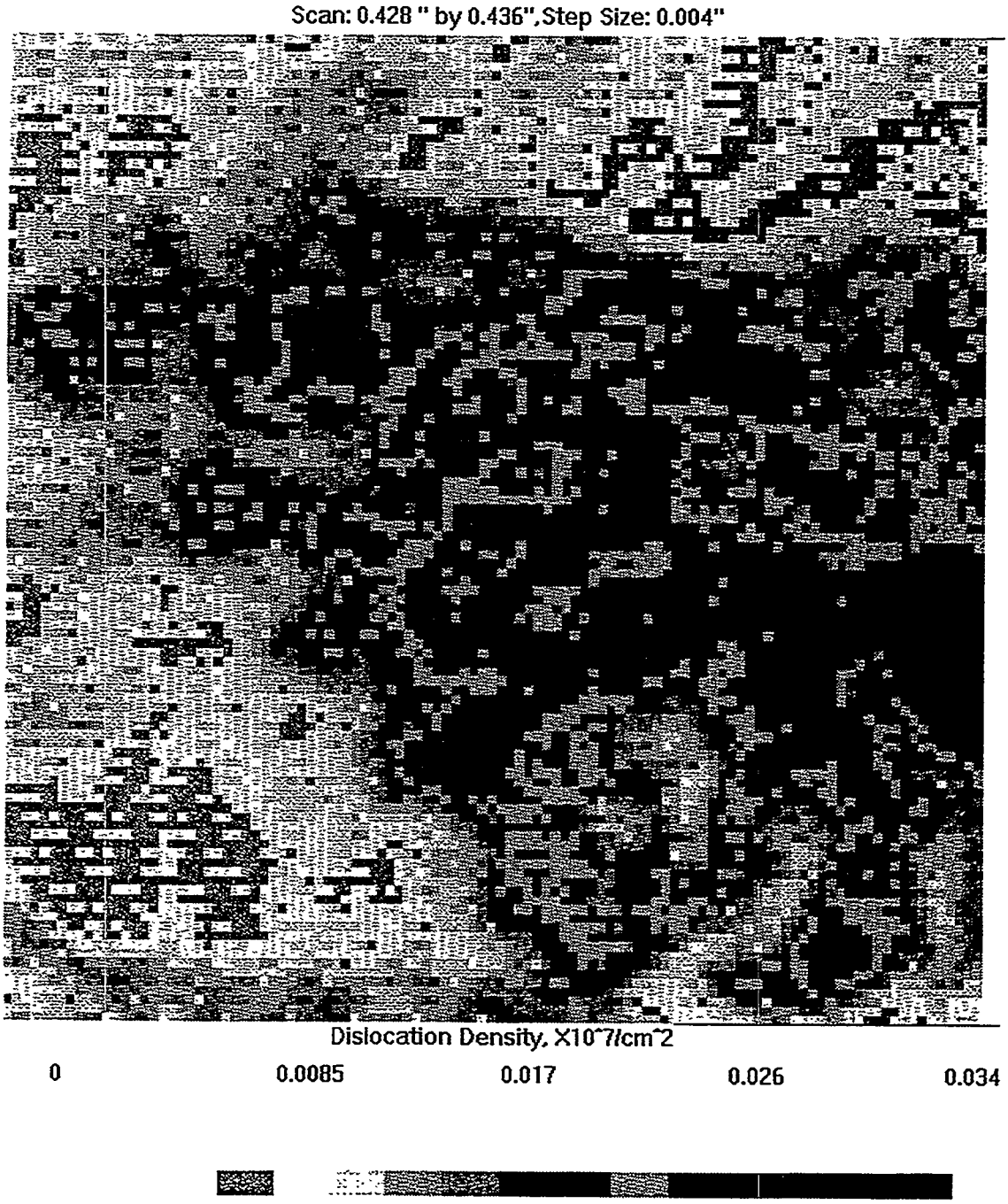

Figure 4. Map of the high dislocation density region in the upper left corner of the wafer shown in Figure 3.

RADIATIVE PROPERTIES OF SILICON

N.M. Ravindra, S. Abedrabbo, W. Chen, F.M. Tong, O.H. Gokce
New Jersey Institute of Technology, University Heights, Newark, New Jersey 07102

Ray Eby
Focal Point Instruments, Glen Gardner, New Jersey 08826

B.L. Sopori
National Renewable Energy Laboratory, Golden, Colorado 80401

Abstract

A joint effort between NJIT and NREL aimed at an understanding of the effects of surface roughness on emissivity of semiconductors is in progress. While the surface roughness measurements are in their initial stages, the emissivity measurements have been investigated in detail. Atomic Force Microscopy (AFM) has been employed to quantify surface roughness on semiconductors such as silicon, SiO_2/Si and W/SiO_2/Si under various conditions of annealing. Temperature and wavelength dependent emissivity measurements have been performed using a spectral emissometer operating in the wavelength range of 0.8 to 20 microns and temperature range of 300 to 1400 K.

Introduction

Optical properties of semiconductors are of fundamental importance. The applications of semiconductors in optoelectronic devices such as detectors, solar cells etc. are determined by their optical properties. For semiconductor device processing, pre-knowledge of the optical properties is essential for process monitoring and control. Semiconductor processing techniques such as Rapid Thermal Processing (RTP) and Molecular Beam Epitaxy (MBE) require stringent temperature uniformity and control for each process run and from run to run, i.e. across the wafer and from wafer to wafer. Pyrometers are the standard sensors for semiconductor process monitoring and control. Wafer radiance, as function of wavelength and temperature, determines the choice of the operating wavelength of the pyrometer. Emissivity is a ratio of the wafer radiance to that of the blackbody operating at the same temperature. It is a function of wavelength, temperature, wafer resistivity/doping concentration, surface conditions such as presence of over-layers, surface roughness, etc. Studies of the optical properties in the literature have focussed, primarily, in the visible range of wavelengths. The dependence of optical properties on surface roughness in the infrared range of wavelengths has not been studied in detail [1,2].

Experimental Details

A Burleigh METRIS 2000-NC Atomic Force Microscope (AFM) and a Burleigh Horizon 200 profilometer have been deployed for measurements of surface roughness of four kinds of samples. The AFM was operated in two scan modes. For the very flat samples (average roughness < 1nm), the AFM was run in high-amplitude resonance AC mode, i.e., intermittent contact, using a fresh silicon tip with resonant frequency of approximately 225 kHz, operating at 60% amplitude damping. The Si-tip was characterized for quality with an appropriate standard sample. The rougher samples, such as tungsten films, were run in standard contact AFM mode. For non-contact optical profiling, the profilometer was operated in a phase-shift mode, with a z-piezo having 1.8 micron maximum z-range. Imaging was performed using multiple image averaging of five images in order to minimize standard deviations and maximize reproducibility. A spectral emissometer [3] operating in the wavelength range of 0.8 to 20 microns and temperature range of 300 to 2000 K has been utilized to obtain the emissivity of the samples. The emissometer consists of a hemi-ellipsoidal mirror with a blackbody source at one focus and the sample under study at the other focus. A chopper combined with a set of mirrors permits a simultaneous measurement of the sample transmissivity, reflectivity and emissivity. Ge and HgCdTe detectors coupled

with an on-line Bomem high-resolution Fourier Transform Infrared (FTIR) spectrometer permit data acquisition of the measured properties.

Results and Discussion

Four types of samples have been considered in this study. They consist of (1) amorphous-Si/SiO_2, (2) double-side polished Si, (3) poly-Si/SiO_2/Si and (4) W/SiO_2/Si. The roughness of these samples is summarized in Table I. AFM images and analyses were done on scan areas between 2-2.5 μm2 for the flat wafers, and on 5 μm2 for the W films. The profiler scans were much larger, of area 211 μm2. The AFM results for the W films are probably more accurate than with the profilometer data because the surface features on these samples are very small. That is to say, the AFM tip can get down in between the grain boundaries, whereas, the profiling device does not even recognize individual grains (0.5 μm resolution). Non-contact AFM scan mode was used for the flat wafers (# 1-3) and contact mode for the rougher W films. The results of the surface roughness measurements are presented in Fig. 1.

Some tip artifacts are seen in the contact mode AFM data of the W films, specifically for the larger grains; however, the roughness data are not compromised, as the grain interstices are still well resolved in these films. In comparison, roughness numbers for the same W films using the profiler show smaller numbers. Clearly, the grain structure is not sampled effectively with this large-area profiling technique, which has only 0.5μm lateral resolution. In general, the features sampled with the horizon profiler are of different spatial frequency, relative to AFM, and thus the data from these two techniques are complimentary. The profiler data of the flatter samples is also different in nature from the AFM data, showing large-scale undulations, rather than the discrete surface features resolved with the AFM on a scale one order of magnitude smaller.

Bulk optical properties of silicon as function of temperature and wavelength and the influence of the growth of thin epitaxial films on emissivity are of fundamental importance for RTP. An experimental study has been performed on thin double-side polished silicon slab of thickness t = 10 μm, resistivity = 5.0 - 12.0 ohm-cm. The details of the samples were supplied by the manufacturer, Virginia Semiconductors, with ± 20% deviation in the wafer thickness. The first sample was compared with yet another specular silicon sample of thickness t = 250 μm, ρ = 10 - 100 ohm-cm. This experiment has been inspired by the pioneering work of Minkov and Swanepoel [4]. In their study, Minkov and Swanopoel use the interference fringes to determine the optical refractive index of thin dielectric films deposited on quartz substrates. In this study, a similar approach is utilized to investigate the optical properties of silicon.

A number of studies aimed at determining the refractive index (n) and extinction coefficient (k) of silicon at different ranges of wavelengths and temperatures have been reported in the literature. One such study has been performed by Li [5]. His studies cover a wavelength range of 1.2-14 microns and temperature from 100 to 750K. No results however, were reported at temperatures above 600°C where a thick silicon slab would be opaque. In Figs. 2(a) and 2(b), the optical properties of the 10 micron thick silicon are shown as function of wavenumber and wavelength, respectively. Fig. 2(a) is utilized for the deconvolution of the measured optical properties to yield refractive indices of silicon at room temperature and Fig. 2(b) is used for showing the smoothness of the interference fringes versus wavelength. This is usually accomplished when the numbers of data points, i.e. resolution, of the FTIR is enough in the measured range of wavelengths. This feature means that the refractive index data obtained by this method is reliable. In Fig. 2(a), it is noticed that the number of fringes in each 1000cm^{-1} is consistent which means that the refractive index in this long range of wavenumber is not changing much. This agrees with the literature [6]. Another important observation in Fig. 2(a) is that the fringe amplitude is in accordance with fundamentals of optics, in which the amplitude is increasing with decreasing wavenumbers, i.e. increasing wavelength. In optics, this is known as the visibility of the fringes. Here the intensity, I, of each monochromatic fringe is as follows:

$$I(\delta) = \{ \sin(\delta/2)/(\delta/2)\}^2 I_{max}$$

where

$$\delta = (2\pi/\lambda)(2ndcos(\theta))$$

δ is the phase difference between the two or more interfering waves, θ is the internal incident angle and d is the film thickness. In Fig. 3, a qualitative comparison is made between the fringe dependent refractive indices and the refractive indices deconvoluted from reflectivity and transmissivity of the 10 μm thick silicon wafer. At the short wavelength, the fringe dependent n is not stable. This is understandable since at such wavelengths, the visibility of the fringes is small and the compatibility of the wavelengths to the optical path difference and hence phase difference is not good. This could also be attributed to the slab thickness and the way of polishing or thinning wafers. Fig. 4, shows the optical properties of a double-side polished silicon sample with thickness t = 250 μm at room and high temperature. At this thickness, interference fringes will not show up. This is because the rays reflected internally are attenuated and the coherency of these waves and the one reflected at the top surface of the sample is not available.

As can be seen in Figs. 2 and 4, at short wavelengths, the emissivity of the thicker silicon wafer is higher than that of the thin wafer. The transmittanace in Fig. 4(a) is high and is independent of wavelength from 1.2 to 20 μm. It becomes small at high temperatures due to the high absorption in silicon. Single-side polished silicon is not as good an IR window as a double side polished silicon. Further, single-side polished silicon is characterized by comparatively higher emissivity. It appears that, qualitatively, roughness should have a direct correlation with emissivity. Surface roughness leads to decreased reflectance and enhanced light trapping thus leading to increase in emisssivity. Detailed investigation aimed at establishing a correlation of the AFM data with emissivity of various semiconductor materials and structures is in progress. A software package that includes the effects of roughness on optical properties in the visible and near-IR range of wavelengths has already been put together by NREL.

Conclusions

Atomic force microscopy and surface profilometry techniques have been utilized to quantify surface roughness of silicon related materials and structures. Emissivity measurements have been performed on double-side polished silicon wafers as function of wafer thickness. Interference fringes have been observed for very thin silicon wafers. These fringes have been utilized to determine the refractive index of bulk silicon. Further studies are in progress to understand the effects of surface roughness on emissivity in electronic materials.

Acknowledgements

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TABLE 1 - Roughness Data

Sample	Surface / Substrate	AFM roughness, Ra (nm)	Profiler roughness (nm)
1	amorphous Si / SiO_2	0.056	1.13
2-A/B	double-sided polished Si	0.026 / 0.028	0.62 / 0.79
3	polysilicon / SiO_2 / Si	0.084	0.73
4	W / SiO_2 / Si , 500°C	17.7	3.67
5	W / SiO_2 / Si , 700°C	16.9	3.82
6	W / SiO_2 / Si , unannealed	15.3	3.68

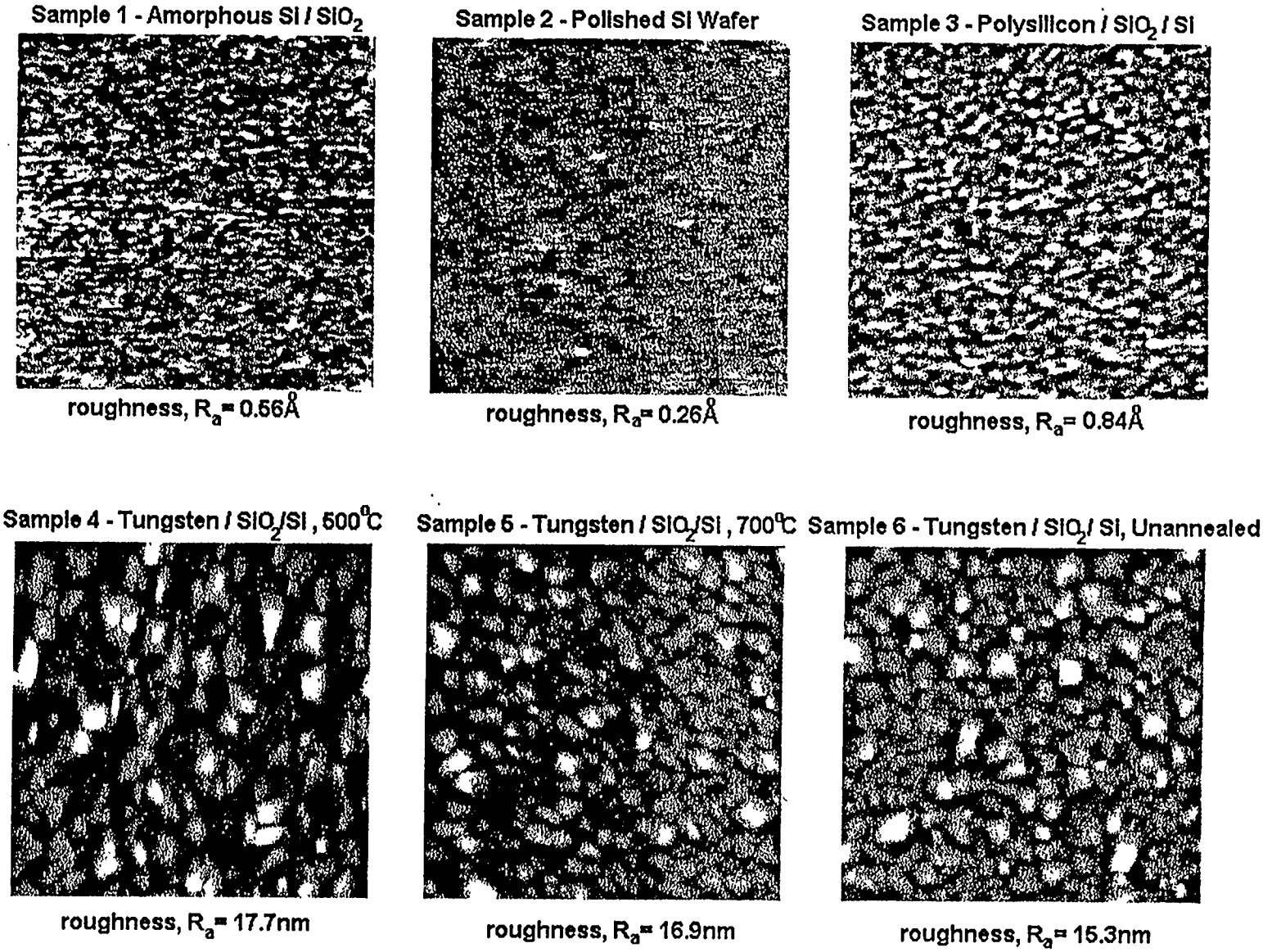

Fig.1 Surface roughness measurements of various samples.

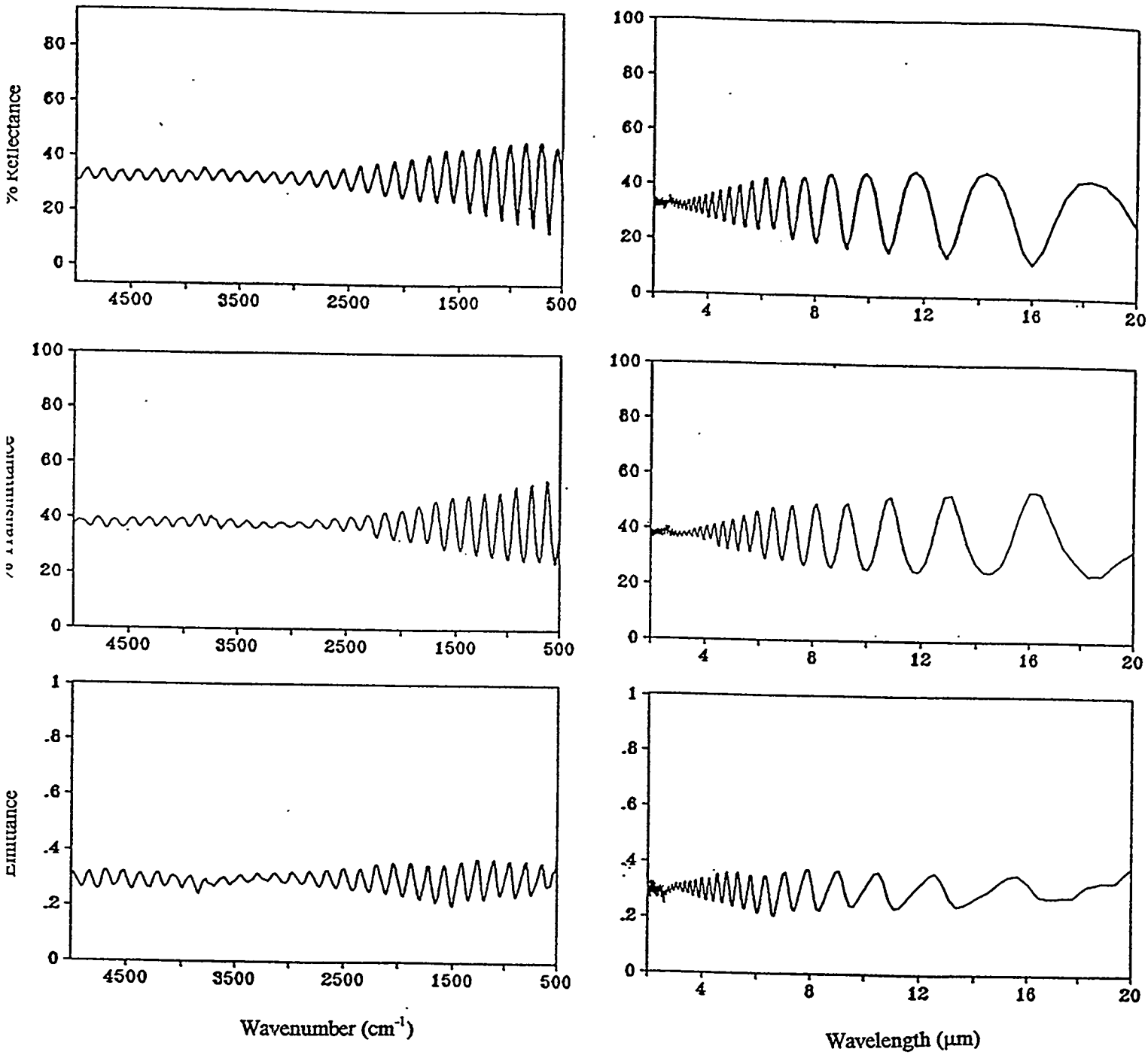

Fig. 2 Optical properties of ≈ 10μm n-type silicon sample as function of (a) wavenumber and (b) wavelength.

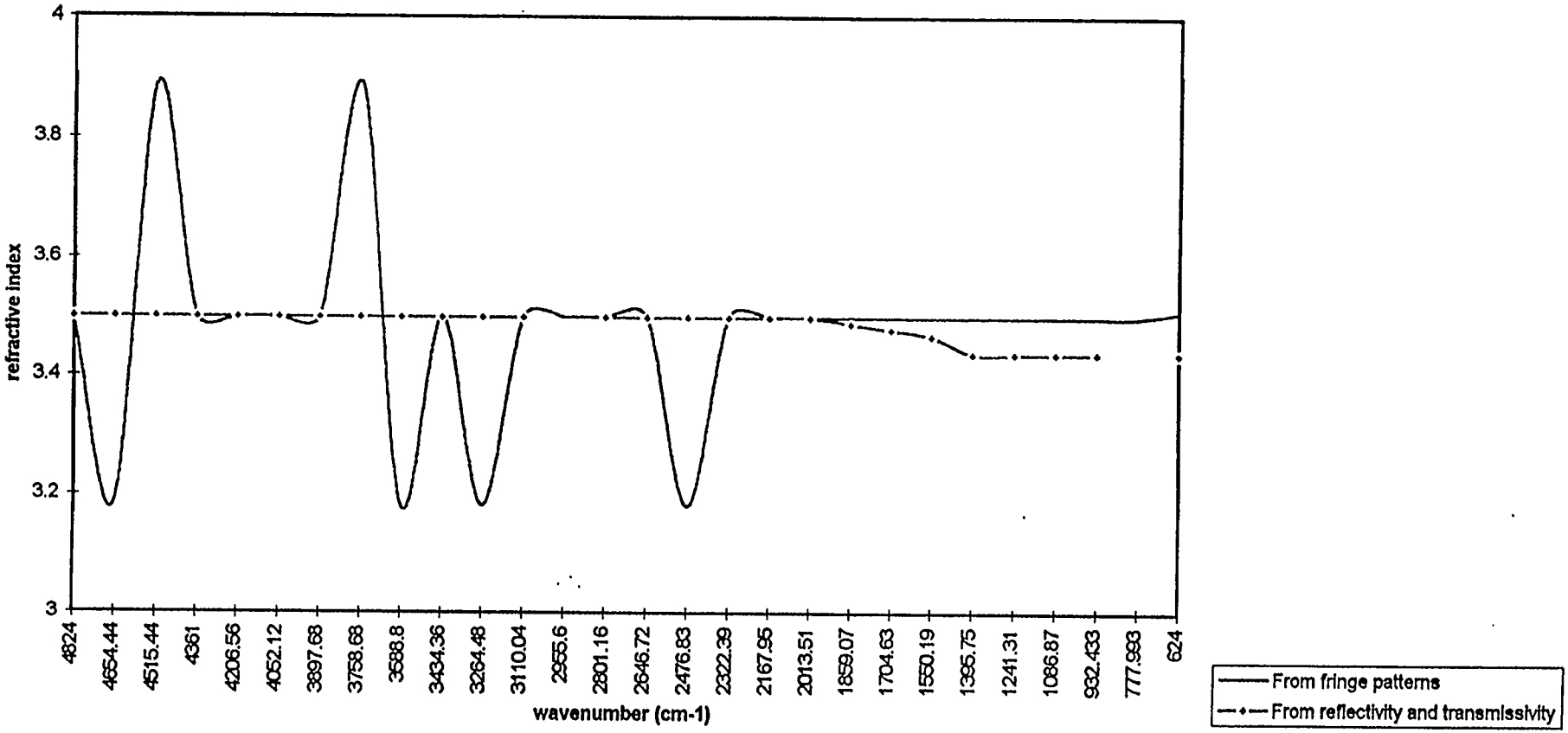

Fig. 3 **Comparison of refractive indices obtained from two different methods**

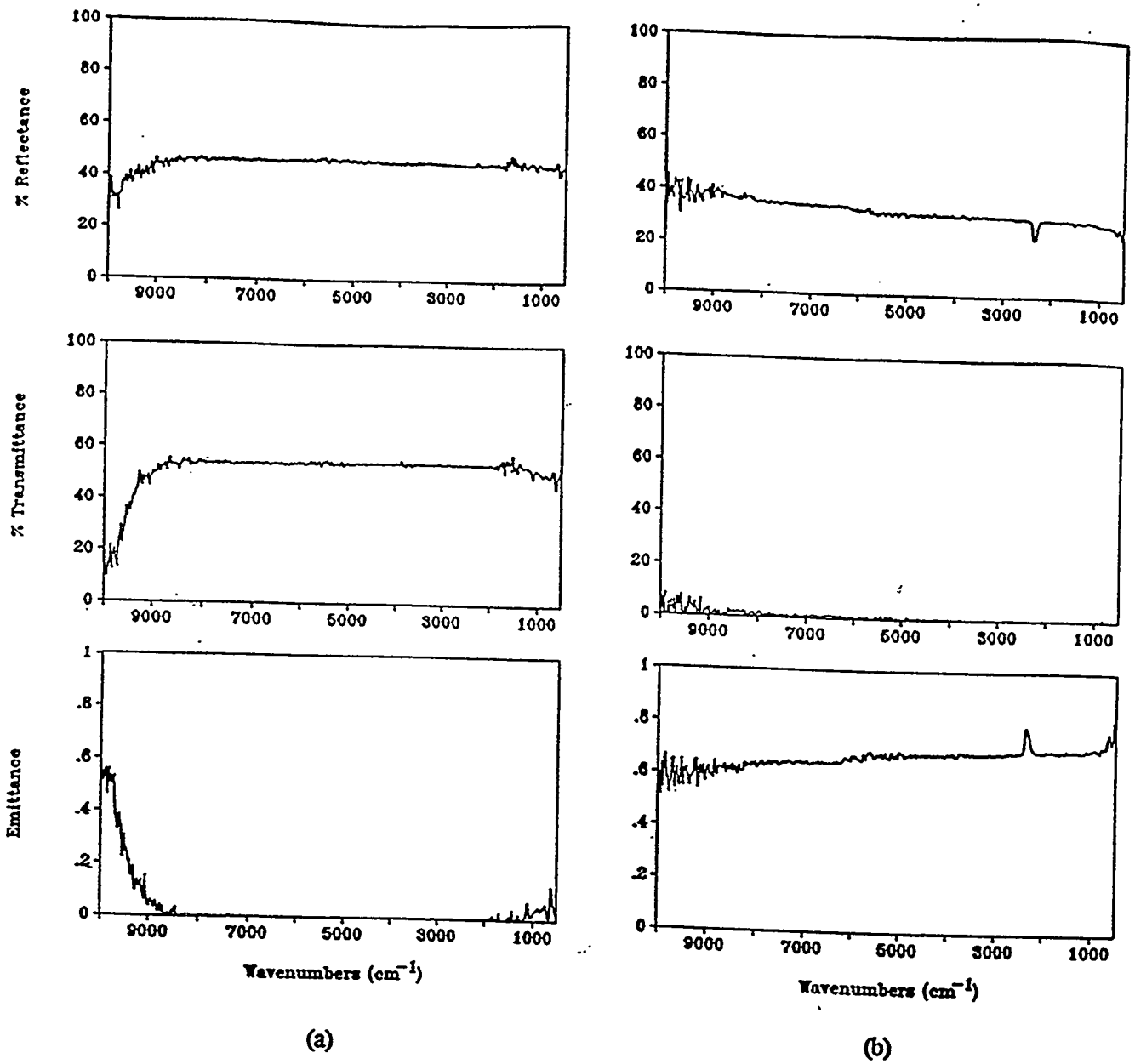

Fig. 4 Emissivity of a double-side polished silicon sample with thickness t = 250 μm at (a) room and (b) high temperature (832°C).

Precipitation of Iron in Silicon

H. Hieslmair*, A. Istratov*, S. A. McHugo‡, C. Flink*, E. R. Weber*
*Materials Science Dept. University of California at Berkeley, Berkeley, CA, USA
‡Lawrence Berkeley Laboratories, Berkeley, CA, USA

Introduction

The performance of photovoltaic polycrystalline silicon materials, edge-defined film growth (EFG) or ingot, has been hampered by regions of low minority carrier diffusion lengths. It has been shown that these regions have high concentrations of structural defects[1]. Cz PV silicon materials generally do not have such large variances in minority carrier diffusion length, but still fall far short of the diffusion lengths obtained in standard integrated circuit Cz materials, 400+ μm. It was hoped that external gettering techniques, which are part of the solar cell manufacturing process (phosphorous and aluminum gettering) would significantly improve both single and polycrystalline materials. Aluminum gettering, for instance, has been shown to significantly increase minority carrier diffusion lengths in float zone silicon which had been intentionally contaminated with high levels of iron[2]. In that study, gettering temperatures were chosen to be the same as the iron drive-in temperatures. In this manner, the iron never precipitated to any large extent. Never the less, diffusion lengths in these materials were improved from ≈17μm (iron contaminated) to ≈200 μm by aluminum gettering. Deep level transient spectroscopy (DLTS) measurements showed a drop in FeB concentration from 10^{14} to 10^{11} Fe/cm^{-3}.

Unfortunately, similar improvements from aluminum gettering were not realized in photovoltaic materials[1]. Aluminum gettering never recovered intentionally iron contaminated PV materials to the initial minority carrier diffusion lengths. As-grown PV materials exhibited varying responses to aluminum gettering. PV grade Cz silicon showed little improvement and retained its ≈100μm initial diffusion length. Polycrystalline materials generally exhibited two types of responses. The regions with high minority carrier diffusion lengths, i.e. low structural defects, generally improved by 5% to 30%. In contrast, the performance limiting regions, i.e. low minority carrier diffusion lengths, either improved slightly, by <5%, or degraded.

Since iron has been shown to precipitate rapidly in regions with high concentrations of structural defects[3] (low minority carrier diffusion lengths), these regions internally getter transition metals. Regions with low concentrations of structural defects (high minority carrier diffusion lengths), contain dissolved metals which slowly precipitate due to a lack of precipitation sites. Thus it appears that aluminum gettering is effective in gettering dissolved transition metals, but not precipitated transition metals. The difficulty of dissolving precipitates during high temperature gettering is unexpected and implies a barrier to dissolution.

Further improvement in the minority carrier diffusion length of PV materials depends upon the understanding precipitation and dissolution processes of transition metal clusters. Practical questions regarding the effects of cooling rates from growth or high temperature processes on metal impurity precipitation (and the subsequent resistance to gettering), require studies of precipitation of such metals on various well defined structural defects. Furthermore, the nature of the barriers to metal precipitate dissolution also needs to be addressed to enhance present gettering techniques or to develop new ones.

This study is a first step in studying transition metal precipitation processes. It focuses on iron precipitation in FZ and Cz materials with various concentrations of oxygen precipitates, including Cz with no oxygen precipitates. Future studies will include dislocated FZ, poly-crystalline FZ, single and poly-crystalline PV materials. Additional studies on dissolution will also begin. The methodology in both the present and future studies is based on the application of Ham's law on the precipitation or dissolution rate. This method is briefly described below before the precipitation results are presented.

Ham's Law

The precipitation rate of an impurity depends on the number of precipitation sites, n, and the effective precipitate radii, r_o. This was described by Ham with the following equation for spherical precipitates for fixed radii and for growing radii after precipitation of over 50% of the solute,[4]

$$C - C_{eq} = (C_o - C_{eq})e^{-t/\tau} \quad (1)$$

where C_{EO} is the equilibrium concentration at the annealing temperature, Co is the initial interstitial impurity concentration, and C is the time dependent concentration and

$$1/\tau = 3Dnr_o \quad (2)$$

Here D refers to the temperature dependent diffusivity and $1/\tau$ is the precipitation rate.

The nr_o product can thus be measured by how quickly the supersaturated impurity concentration drops. In previous publications, $1/\tau$ is usually derived from the slope of a line drawn through the experimental data points. This is based on the assumption that the precipitate radius does not change during the precipitation process. In fact, the solute precipitation rate increases as the precipitate grows, and does not fit a simple exponential. The slow precipitation rate during the beginning of the precipitation is primarily a result of the small precipitate surface area on to which the solute could be absorbed. Growth of the precipitate makes more surface area available, increasing the precipitation rate. Once more than 50% of the impurities have precipitated, the precipitate radius does not increase significantly, and the precipitation rate approximately follows Equation 1.

The nucleation site density can be calculated from the conservation of mass, i.e.

$$\Delta C = \frac{4}{3}\pi r_o^3 n\Omega \quad (3)$$

and Ham's law (Equation (2)), by,

$$n = \left(\frac{3}{4}\pi \cdot \frac{1}{(3D\tau)^3} \cdot \frac{\Omega}{\Delta C}\right)^{1/2} \quad (4)$$

where ΔC is the drop of interstitial iron concentration, and Ω is the density of iron in the precipitate. Implicit in Equation 4 is that τ should be obtained from data measured after more than 50% of the solute has precipitated and the precipitation rate is approximately exponential. To fit the whole precipitation curve, the fixed radius approximations, Equations 1 and 2, can be used in an iterative calculation in which the radius, r_o, is continually adjusted as the precipitate grows. In such a manner, even the early precipitation can be modeled and values for n can be obtained.

Computer Simulations

To obtain a more accurate precipitate density, an iterative finite differences computer simulation was used to fit the precipitation data. The following equations, slightly modified from Ham's original formulation, were used in the simulation.

$$\Delta C(\Delta t) = \left[C_{eq}(T) - C_o(t)\right]\left(1 - e^{-\Delta t/\tau}\right) \quad (5)$$

and

$$\Delta C = \frac{4}{3}\pi\left(r_1^3 - r_0^3\right)n\Omega \quad (6)$$

where C_{eq} (T) is the temperature dependent equilibrium solubility; C_o (t) is the impurity concentrations at the start of the time step, Δt; ΔC is the change in dissolved impurity concentration during the time step Δt; Ω is the volume density of the impurity (iron) in the precipitate (iron silicide); and r_0 and r_1 are the precipitate radii at the beginning and end of the time step, respectively. For $FeSi_2$, the density of iron is roughly 25.6 Fe/nm^3. Equation (6) is used to determine the incremental change in precipitate radius, $\Delta r = r_1 - r_0$, from changes in concentration, ΔC. It was assumed that all the metal was dissolved in the beginning of the simulation. Small steps in time were simulated. After each step a drop in solute concentration, ΔC, was calculated from Ham's law, and the precipitate radius was increased by an appropriate amount. This approach should yield more accurate results since the radius, and thus nr_o, is incrementally revised as precipitation continues. Numerous simulations were run and the precipitation site density varied to obtain a fit to the experimental data points.

Results

Samples from a FZ wafer and from Cz wafers with no oxygen precipitates, $2x10^8$, $2x10^9$, $2x10^{10}$, and $2x10^{11}$ oxygen precipitates per cubic centimeter (initial oxygen concentrations for all Cz samples 6-8x10^{17}

O/cm^3) were intentionally contaminated with iron to a concentration of ≈ 4x10^{13} Fe/cm^3. These samples were then annealed at lower temperatures for various times and quenched. After chemically etch more than 40μm from the surface, the remaining dissolved iron concentration (FeB pairs) in these samples was then measured by DLTS. Precipitate site densities were determined from computer simulations as shown in Figure 1. A low temperature precipitation at 240°C and a medium temperature precipitation at 650°C were performed on all the types of materials and precipitate site densities are shown in Figure 2. Obviously, there is a strong correlation between precipitate site density and oxygen precipitate concentration. This was also observed by Gilles et. al.[5] although he did not explicitly obtain precipitate site densities. The Cz silicon with no oxygen precipitates showed the lowest precipitate site density. In each type of material, it is observed that the precipitate site density increases as the annealing temperature is reduced below ≈500°C. Thus in each case, the site density at 240°C is greater than at 650°C. Annealing at various temperatures above 500°C yields an approximately constant precipitate site density . This is shown for one type of Cz material in Figure 3.

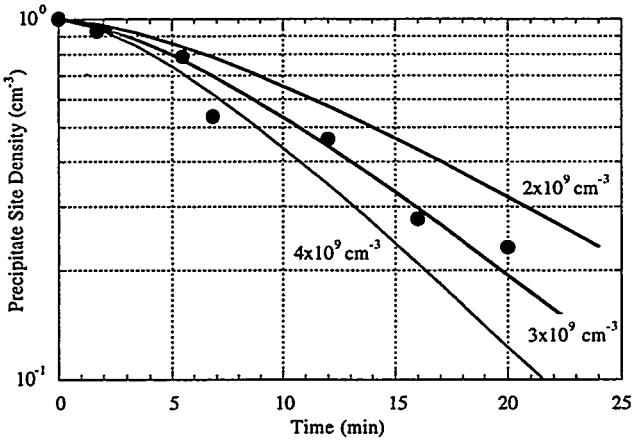

Figure 1: Example of computer simulations and experimental data for Cz material without oxygen precipitates , annealed at 650°C

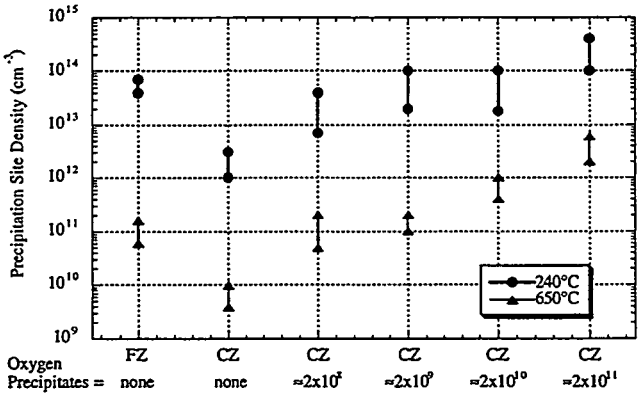

Figure 2: Precipitate site densities for various materials annealed at 240°C and 650°C

Discussion

The increase in precipitation site densities at lower temperatures, <500°C, can be easily understood in terms of nucleation at trapping sites. Since dissolved iron is detected as FeB pairs by DLTS, iron atoms need only be trapped as clusters or complexes to result in a reduction of dissolved iron. The first step in this process is a small nucleus such as an iron complex. The density of iron occupying such a trap or complex and forming a nuclei, can simply be described as ,

$$N_{precip} = N_O \, e^{\Delta E/kT} \qquad (7)$$

where N_{precip} is the concentration of iron iron precipitates, and N_o is proportional to the dissolved iron concentration and the trap density. Plotting N_{precip} as a function of 1/kT, the binding energy of the trap was estimated to be 0.49±0.14 eV. After this

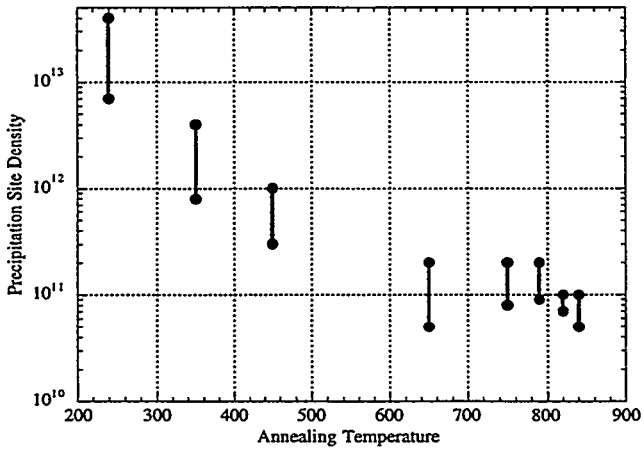

Figure 3: Precipitation site densities for various annealing temperatures in Cz silicon with 2x10^8 oxygen precipitates cm^{-3}

complex/cluster forms, further precipitation can continue as the iron atoms diffuse to these sites. If the concentration of trap sites is similar or greater than the concentration of iron sites, then the precipitation rate is essentially the rate at which iron diffuses to a trap. Since there is no growth in radius of the precipitate, the resulting precipitation curve is a simple exponential as Ham's law would predict. This is observed in samples with high site densities.

At higher temperatures, in the range of 500°C up to the iron drive-in temperature, a temperature dependence of site density on annealing temperature is difficult to resolve with the present data. The data does show that numerous precipitation sites exist even at high temperatures, indicating that the binding energy of iron to this trap is high and thus should not be easily dissolved.

Among the different materials, the lowest precipitation site density was in the Cz material with no oxygen precipitates, while the highest site density occurred in the Cz material with $2x10^{11}$ cm^{-3} oxygen precipitates. Such high densities of oxygen precipitates provide large surface areas and high concentrations of associated structural defects, punched out dislocations or stacking faults. Thus many iron nucleation sites are available per single oxygen precipitate. In the Cz material with $2x10^{11}$ cm^{-3} oxygen precipitates (smallest precipitates), each precipitate generates approximately 15 sites for iron precipitation at 650°C. In the Cz material with $2x10^{8}$ cm^{-3} oxygen precipitates, each precipitate provides 500 sites for iron precipitation. The number of iron precipitation sites per oxygen precipitate seem to correlate with the surface area of the oxygen precipitate.

However, if there are no oxygen precipitates present, as in either FZ or Cz with no precipitates, there are still iron precipitation sites present. It is uncertain what defects or impurities are present at levels of $5x10^{9}$ cm^{-3} (Cz with no precipitates). It has been recently shown that in FZ silicon, vacancies can exist in concentrations of up to 10^{14} cm^{-3} at high temperatures[6]. After the iron contamination at high temperatures, a quench is used to prevent interstitial iron from precipitating. This quench may also cause these vacancies to cluster, forming iron complexing or nucleation sites. This would result in the high site densities observed in FZ silicon. Such high concentrations of vacancies were not observed in the Cz materials which explains the lower site densities detected in the Cz material with no oxygen precipitates.

Conclusions

The precipitation behavior of iron in FZ and various Cz silicon materials was observed. Computer simulations based on Ham's law were used to fit the precipitation rates in order to obtain iron precipitate site densities. The iron precipitate site densities increase with increasing oxygen precipitate site densities at all precipitation temperatures. High precipitation rates in FZ materials is possibly due high concentrations of vacancy clusters.

A high density of traps with a relatively high binding energy was detected in FZ and Cz materials. It is suggested that a higher density of similar defects in PV materials may be responsible for resistance of these materials to gettering techniques.

Acknowledgements

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The Effects of Rapid Pre-Getter Anneal Treatments on the Performance of Cast mc-Si Solar Cells

S. Narasimha and A. Rohatgi
University Center of Excellence in PV Research and Education, Georgia Institute of Technology, Atlanta, GA. 30332-0250

Introduction

In order to improve the cost effectiveness of silicon photovoltaics, a variety multicrystalline silicon (mc-Si) growth techniques have been developed for large scale production. Solar cells formed on such materials exhibit production line efficiencies of 12-14% [1,2], whereas analogous cells made on high quality single crystalline silicon exceed 16% in efficiency. This 2-4% difference in performance is primarily due to the higher impurity levels and defect densities in mc-Si materials compared to IC grade silicon. The impact of impurities and defects can be reduced by implementing various gettering techniques. Conventional gettering processes used during solar cell fabrication (which induce the segregation of bulk impurities to phosphorus diffused junctions or aluminum regions) can lead to improvements in device performance. However, the degree of improvement is typically limited. Particularly unresponsive to conventional gettering sequences are regions of high defect density (dislocation networks or grain boundaries decorated with impurities). Impurities readily segregate to these regions and cause an increase in the local recombination rate. Additionally, if a supersaturation of impurities exists, these defects can provide nucleation sites for impurity precipitation. Past work has shown that conventional gettering treatments are rather ineffective in reducing the recombination activity in such regions [3]. In order to bridge the present efficiency gap between mc-Si and IC grade silicon solar cells, an extremely potent gettering process must be established which targets impurity decorated defect clusters.

Pre-Getter Anneal (PGA) Treatments for Impurity Release and Precipitate Dissolution

The gettering process is comprised of three steps: 1) impurity release from the active area of a device, 2) impurity diffusion out of the active area, and 3) impurity capture in a region of the device where its effects are not detrimental to device performance [4]. In regions of mc-Si wafers where the defect density is high, the gettering process is release-limited. It has been suggested that the response of such regions can be improved by incorporating a pre-getter anneal (PGA) treatment prior to the conventional gettering step [5]. If the PGA is intense enough, it can provide the energy needed to release impurities from defective regions in the device. The released impurities can then be removed from the active area by the ensuing gettering step. It is important to note, however, that each step in this two step process must be designed for compatibility. For example, if the gettering step following the PGA is of insufficient intensity (in temperature and time), there will be a net accumulation of released impurities in previously unaffected regions of the device. On the other hand, if the PGA treatment is of insufficient intensity, the impurity release from defective regions of the material will not occur.

The above concepts are depicted in the response surface model of Fig. 1 which shows the expected swing in solar cell performance as a function of both the PGA treatment and the ensuing getter. Four points labeled A-D mark the corners (or extreme cases) of this response surface. Point A represents a nominal device formed on a sample without a PGA or an appreciable gettering treatment. Point B represents a device formed on a sample receiving a strong PGA treatment but no subsequent getter. Without a means of removing the impurities released by the PGA, there occurs a degradation in device performance from point A. Point C represents a device formed on a sample receiving an intense getter but no PGA treatment. A limited increase in performance over point A is shown. As discussed above, the improvement is limited by the release of impurities from regions of high defect density. Finally, point D represents the most effective combination of the two steps: intense PGA coupled with an appropriately intense getter. It should be noted that the functional dependence shown in Fig. 1 is expected to be material specific because of the wide variation in the impurity content and structural defects in various promising PV materials.

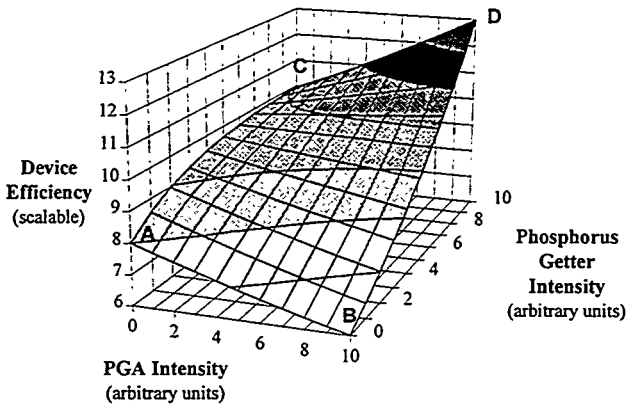

Fig. 1. Response surface model which shows the conceptual dependence of mc-Si solar cell performance on 1) the PGA intensity and 2) the ensuing phosphorus gettering efficiency.

Much insightful work in this area has been done by the group at UC Berkeley [5]. In their studies, the PGA

treatment was accomplished using rapid thermal annealing at elevated temperatures (1050-1100°C) for short times (< 1 minute). The subsequent gettering treatment consisted of a lengthy (3 hour) aluminum alloying step performed at 900°C. Different mc-Si materials (cast and ribbon) were investigated for their response to the PGA treatment, and the SPV technique was used to monitor the effective diffusion length (L_{eff}) response in the different materials. In most cases, the L_{eff} values measured for PGA samples were either the same as or slightly less than the L_{eff} for non-PGA samples. It is unclear whether: 1) the PGA treatment implemented was of insufficient intensity to increase the release of impurities from defects, 2) the aluminum gettering was not effective in removing the impurities released by the PGA.

In the present work, we have extended the application and characterization of the PGA treatment in order to determine more clearly whether this process can be successful in raising the performance on mc-Si solar cells. The approach utilized in this study contrasts that found in [5] in the following two respects. First, we have used relatively short phosphorus diffusion cycles instead of lengthy aluminum alloying for the post-PGA gettering treatment. Secondly, we have used light IV and light beam induced current (LBIC) measurements of mc-Si solar cells to characterize the effects of the PGA treatment on device performance.

Experimental

HEM mc-Si (Crystal Systems) from different ingots was used in this study. Special low-resistivity material (<0.4 Ω-cm), which is expected to yield lower performance due to higher doping levels, was specifically grown for gettering experiments. The resistivity, vertical ingot position, substitutional carbon concentration, and interstitial oxygen content in the as-grown materials were measured. These values are listed in Table 1.

Table 1. Characteristics of the HEM material used in this study.

Material/ Ingot ID	Resistivity (Ω-cm)	Position in Ingot (cm from bottom)	Carbon (ppma)	Oxygen (ppma)
HEM 1HS4	0.37	5.6	9.5 +/- 0.3	6.9 +/- 0.0
HEM 1HS7	0.38	6.4	9.2 +/- 0.1	6.7 +/- 0.1
HEM 1HS8	0.30	10.2	11.3 +/- 0.2	3.8 +/- 0.2
HEM 50-1	0.95	NA	8.9 +/- 0.2	2.0 +/- 0.0
HEM 5R8	1.20	8.5	8.0 +/- 0.0	5.8 +/- 0.2

The advantage of using cast mc-Si material for gettering studies is that consecutive wafers can be selected from an ingot. The defect structures in these consecutive samples are usually quite similar (often times nearly identical), which allows direct comparisons to be made. Two processes were compared in this study. In *Process 1*, the first four HEM samples shown in Table 1 were used. Samples were subjected to a rapid PGA (RPGA) treatment in an RTP unit for 2 minutes at 1050°C in an N_2 ambient. At the end of the 2 minute period, the samples were quenched from 1050°C to 750°C in 10 seconds by turning off the tungsten halogen lamps in the RTP unit. The ensuing phosphorus gettering treatment consisted of a short diffusion (840°C for 20 minutes) using phosphorus solid sources. Matched samples were included at this stage in the process in order to establish the response of the baseline (non-RPGA) process. The diffusion resulted in an n^+ region sheet resistance of 40 Ω/sq. Next, the emitters were etched back to roughly 85 Ω/sq. A thin layer of aluminum was then evaporated onto the backside of the wafers and alloyed at 850°C for 15 minutes to form the BSF. During this alloying process, a 100A passivating oxide was grown on the emitter surface. Multiple 1 cm^2 devices were formed on each sample. Contact metallization was applied using lift-off photolithography, and the individual devices were isolated using a mesa etch procedure. Again, the use of matched wafers allowed for the fabrication of cells with identical defect structures for both the RPGA and non-RPGA samples.

In *Process 2*, wafer splits from the first experiment as well as samples from the remaining ingot listed in Table 1 were used. Samples undergoing the RPGA treatment were first annealed in an RTP unit for 3 minutes at 1100°C. At the end of the 3 minute period, the samples were quenched from 1100°C to 750°C in approximately 10 seconds. The ensuing phosphorus gettering treatment consisted of a more intense diffusion (900°C for 30 minutes) using phosphorus solid sources. Matched samples were included at this stage in the process. This diffusion resulted in sheet resistance of 15 Ω/sq. The junctions were then etched away completely, and emitter regions re-diffused (840°C for 30 minutes) using a $POCl_3$ source. The emitter sheet resistance resulting from this diffusion was 85 Ω/sq. The rest of the process was identical to that described above. Light IV tests were done under approximate one sun conditions without the application of an AR coating. LBIC scans were done under low level injection conditions using a 905 nm laser diode source.

Results and Discussion

Process 1 - Light Phosphorus Getter

Table 2 shows the results of Process 1. Each parameter in this table represents the average value taken from 12 solar cells across the sample.

Table 2. Results of Process 1 (RPGA followed by light phosphorus getter. Solar cells were measured without AR coatings.)

	Without RPGA Treatment				With RPGA Treatment			
Sample/ Ingot ID	Voc (mV)	Jsc (mA/cm^2)	FF	Efficiency (%)	Voc (mV)	Jsc (mA/cm^2)	FF	Efficiency (%)
HEM 1HS7	577	20.3	.781	9.1	584	21.9	.792	10.1
HEM 1HS4	578	20.0	.770	8.9	580	21.9	.744	9.4
HEM 1HS8	559	21.6	.560	6.8	563	20.4	.613	7.0
HEM 50-1	574	22.2	.752	9.6	570	21.1	.784	9.4

Two altogether different results are indicated by the measured data. In the case of samples from ingots 1HS7 and 1HS4, the average J_{sc} response increases dramatically as a result of the RPGA treatment, which leads to a substantial increase in cell performance. LBIC analysis of a representative matched pair of devices from ingot 1HS4 (Fig.2) reveals that the intragrain response is considerably higher for cells undergoing the RPGA treatment. This is either due to the dissolution of precipitates in the intragrain regions, or impurity release from dislocation clusters within grains. For these samples, the light phosphorus diffusion removes the impurities released by the RPGA treatment.

In the case of samples from ingots 1HS8 and 50-1, the average J_{sc} response falls dramatically as a result of the RPGA treatment. LBIC maps of a representative pair from ingot 50-1 (Fig. 3) show that the collection efficiency in the intragrain regions is reduced as a result of the RPGA treatment. For samples which do not undergo the RPGA, LBIC maps reveal denuded zones around structural defects, which indicates that impurities have segregated to the defect sites during the ingot growth stage or possibly during cell processing. However, in matched devices undergoing the RPGA treatment, the denuded zones vanish and the regions in the immediate vicinity of structural defects exhibit reduced collection efficiency. This shows that the RPGA treatment does enhance the release of impurities away from defect sites and into the surrounding bulk silicon. However, in the present case, the ensuing light phosphorus gettering treatment does not effectively remove the released impurities. Thus, the overall J_{sc} response is reduced.

Process 2 - Intense Phosphorus Getter

Table 3 shows the results of Process 2 on the wafer splits taken from ingots 1HS4, 1HS7, and 1HS8, as well as samples taken from ingot 5R8. Again, the information in the table represents the average values of 12 devices fabricated on each wafer.

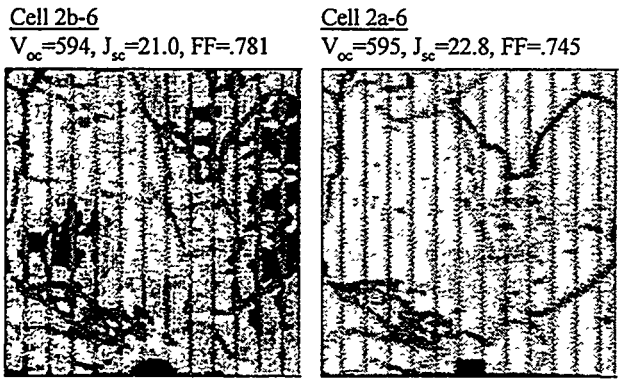

Fig. 2. LBIC response of matched solar cells fabricated from wafers from ingot 1HS4. The RPGA has improved the overall collection efficiency.

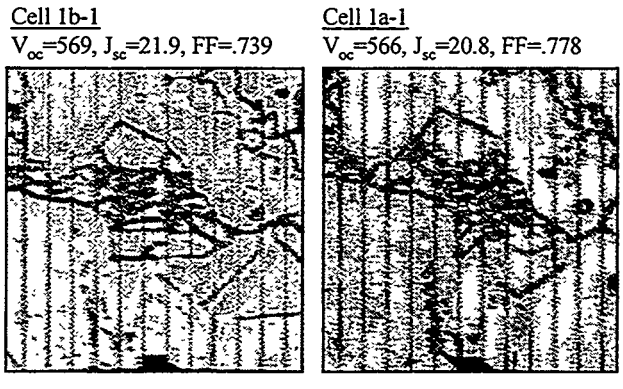

Fig. 3. LBIC response of matched solar cells fabricated from wafers from ingot 50-1. The RPGA has reduced the collection efficiency in the vicinity of the defect centers.

Table 3. Results of Process 2 (RPGA followed by intense phosphorus getter. Solar cells were measured without AR coatings.)

Sample/ Ingot ID	Without RPGA Treatment Voc (mV)	Jsc (mA/cm^2)	FF	Efficiency (%)	With RPGA Treatment Voc (mV)	Jsc (mA/cm^2)	FF	Efficiency (%)
HEM 1HS7	607	22.7	.769	10.6	613	22.9	.785	11.0
HEM 1HS4	596	22.4	.783	10.5	603	22.5	.789	10.7
HEM 1HS8	615	22.6	.763	10.6	608	22.6	.757	10.4
HEM 5R8	587	23.5	.774	10.7	591	23.5	.783	10.9

In contrast to the results of Process 1, the results of Process 2 show little effect of the RPGA treatment. The J_{sc} values for samples undergoing the RPGA treatment are essentially the same as those undergoing the baseline process. This behavior can be explained in terms of the conceptual model shown in Fig. 1 by observing the efficiency progression of cells for the four process variations implemented in this study. Again, these process variation are: 1) light phosphorus getter only, 2) RPGA followed by light phosphorus getter, 3) intense phosphorus getter only, and 4) RPGA followed by intense phosphorus getter. The efficiency progression resulting from these processes is shown in Fig. 4. Two points are evident from the data. First, when a light phosphorus gettering step is used after the RPGA, a significant efficiency improvement occurs for certain materials. Secondly, and more generally, the intense phosphorus gettering alone produces a very pronounced gettering effect for all materials. In fact, for samples from 1HS4 and 1HS8, the effect of the RPGA is masked by the intense phosphorus gettering. In terms of the model in Fig. 1, the RPGA used in this step is not intense enough to yield additional performance improvements when followed by a 900°C/30 minute phosphorus getter. This is understandable if the time duration of each step is considered. The RPGA treatments times were relatively short ($1.2x10^2$-$1.8x10^2$ seconds), whereas the time used for the intense phosphorus getter was one order of magnitude longer ($1.8x10^3$ seconds). It is evident that the RPGA cycle temperature or time must be increased in order to show an effect after the 900°C/30 minute phosphorus getter.

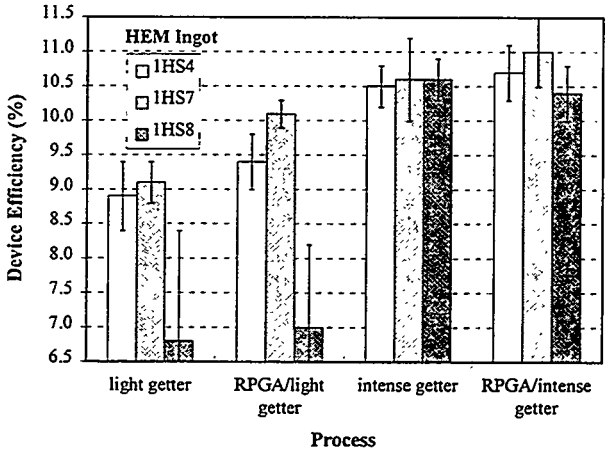

Fig. 4. Efficiency progression for HEM mc-Si solar cells for the four gettering variations implemented in this study.

Conclusions

The results in this study show that an RPGA treatment can enhance the impurity release process. However, the final device performance is strongly dependent on the combined effect of the RPGA and the ensuing phosphorus gettering sequence. If an intense RPGA treatment is followed by a weak phosphorus getter, the overall device efficiency can decrease due to an accumulation of impurities in intragrain regions of the solar cell. If the phosphorus gettering treatment is dominant, the RPGA has little impact on the device performance. This suggests the existence of an optimal RPGA/phosphorus gettering combination for mc-Si materials. Of course, the response of a given material to a specific gettering combination will depend on the type of impurities present as well as their relative concentrations. Table 2 clearly shows that an effective combination of RPGA/phosphorus gettering for one material might not be appropriate for another. Further experimental work is in progress to develop RPGA/phosphorus gettering combinations that can be applied generally to a wide range of mc-Si materials.

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The Reaction Kinetics of Iron at Silicon Surfaces and Interfaces
Aimee L. Smith, Sang H. Ahn, Song Zhao, Lynn L. Chalfoun, Gerd Norga,
Lionel C. Kimerling

(Paper unavailable at time of printing)

EFG MANUFACTURING LINE TECHNICAL PROGRESS AND MODULE COST REDUCTIONS UNDER THE PVMaT PROGRAM*

J. Cao, R. Gonsiorawski, M. Kardauskas, J. Kalejs,
C. O'Brien, M. Prince and E. Tornstrom
ASE Americas Inc., 4 Suburban Park Drive, Billerica, MA 01821

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Introduction

Manufacturing technology for photovoltaic modules based on a multicrystalline silicon wafer produced by the Edge-defined Film-fed Growth (EFG) technique became the first "new" crystalline silicon approach, i.e., not based on producing wafers using conventional Czochralski or casting methods, to enter commercialization in 1994 on a multi-megawatt level. The EFG technique is based on production of hollow octagonal-shaped tubes, 4.6 m in length and 300 μm average wall thickness, consisting of 8 faces of 10 cm width each. Since 1994, the EFG manufacturing line has expanded to a 4 MW capacity level, to become the third largest U.S. producer. This paper describes the contributions that have been made in this growth through technology development and in module cost reduction by successes under Phase 4A2 of the Photovoltaic Manufacturing Technology (PVMaT) Initiative, which started in December of 1995 at ASE Americas. They have resulted in a 7% reduction in module manufacturing cost in the first year of the program, and the cost reduction is anticipated to reach to 15% by the end of 1997.

Technology Development

The PVMaT program at ASE Americas has been structured to incrementally improve manufacturing line processes and so attain module manufacturing cost reductions on a continuing basis, as well as to develop new technology that will more radically impact on costs and change manufacturing line processing steps in the last two years of the program. An integral part of this effort involves work being done at subcontractors both in the private sector and at Universities. We outline the scope of the work here and describe the progress made in implementing new technology to reduce costs in the main areas of wafer, cell and module manufacture.

EFG wafer manufacturing. EFG wafer costs are dominated by silicon feedstock material and graphite component costs, and by process yield. Progress has been made in reducing costs in all three areas. Silicon feedstock utilization was increased by 3% by improving pellet sorting; the main contributor to reduced graphite cost, the run length, has been increased by over 50%; yield in crystal growth and laser cutting has been increased by 3% as result of reductions in stress during growth and in improvements in thickness uniformity in octagon tubes. Purification methods for graphite furnace components also have been improved, contributing to stabilization and overall improvement in EFG wafer quality, hence solar cell efficiency.

Yield improvements are targeting thinner material. A portion of the EFG growth line has now been turned over to production of 275 μm thick wafers, down from the current 300 μm thickness. The planned reduction in thickness to 250 μm will give an overall 17% decrease in silicon feedstock costs when fully implemented at the end of the PVMaT program at year end 1998. Yield issues in cutting of the thinner EFG material are being addressed. A new laser cutting technology which utilizes copper vapor lasers is in the feasibility testing stage. It has the potential to significantly reduce cutting damage to the levels required for thin wafer manufacture with high yields.

EFG cell manufacturing. Process improvements which are being studied include improved metallization, a more environmentally benign method of phosphorus glass removal, a new diffusion process using rapid thermal processing (RTP), and the study of front surface texturing schemes which can increase cell efficiency through improved light trapping. Metallization changes planned increase the number of fingers from 32 to 40, and to make them thinner. This will decrease series resistance and will increase EFG cell efficiency by 0.3-0.4% absolute. Optimization work on the EFG cell line has produced significant numbers (in the hundreds) EFG cells in the 14-14.5% efficiency range. When combined, these improvements have the potential for achieving program targets of 15%. Work is proceeding with a subcontractor, Georgia Tech, to study improved methods of processing, including RTP. To date, record small area (1 cm^2) EFG cells of over 16% have been demonstrated with RTP at Georgia Tech. A second subcontractor, Harvard University, has successfully demonstrated that a textured ZnO layer can be deposited on silicon nitride AR coating used by ASE Americas. Encapsulated EFG cell efficiencies have not improved, indicating the current EFG manufacturing line module process is already highly optimized in trapping sunlight. A subcontractor, Bright Technology, is developing a novel method to remove phosphorus doped glass. This approach has potential to reduce manufacturing line add on costs in the cell processing area by 7%, and more importantly, will reduce fluorine ion effluent by several orders of magnitude, hence almost completely eliminating a serious concern for waste disposal in this process step.

EFG module manufacturing. We have redesigned several components of the module housing and electrical protection circuits in this program. These will reduce module add on manufacturing costs by 4% when implemented later this year. We are also evaluating low-cost framing approaches. Studies of module encapsulants are under way. Several of the new EVA formulation have been evaluated, and compared to the ASE Americas' proprietary non-EVA encapsulant for potential advantages. Further improvements on the proprietary non-EVA encapsulant, as well as other new materials are also being investigated. These are aimed at improving yields and increasing flexibility in manufacturing, and in reducing costs.

Boron Gettering of Si Substrates and the Effect on Cell Performance

T. Saitoh, S. Ishikawa, N. Ohe[1], Y. Takano* and T. Warabisako**

Tokyo A&T University, Koganei, Tokyo 184, Japan
*Science University of Tokyo, Noda, Chiba 278, Japan
**Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo 185, Japan

ABSTRACT: Boron gettering effects on FZ and CZ Si substrates have been investigated by measuring effective lifetime with a chemical passivation. After removal of the boron-diffused layers, the effective lifetime increased about two times higher than initial values for p-type FZ Si substrates. However, thermal processes in O_2 and N_2 after boron diffusion degraded the effective lifetime drastically for both the substrates. These results were confirmed by DLTS measurement indicating an existence of a nitrogen-vacancy complex. The boron gettering was effective to improve short-circuit current density and cell efficiency for monocrystalline Si solar cells.

1. Introduction

High-efficiency crystalline silicon solar cells include a back surface field (BSF) structure fabricated using boron (B) diffusion to reduce recombination at the rear electrode [1]-[3]. However, B diffusion is a delicate process because sometimes B diffusion degraded cell performance by diffusing lifetime killer impurities or defects at high temperature. This is one of the reasons why a theoretical efficiency of single crystalline Si solar cell is difficult to be achieved. Furthermore, one of the ideas to reduce the cost of solar cells is to use thinner Si substrates. In the thinner cell structure, the BSF structure has to be fabricated hopefully by an aluminum alloying. However, the alloying process is difficult to apply for thin substrates due to warping. To avoid the problem, gas-phase B diffusion should be employed to prepare p^+ layers without warping.

In this research, a detailed study on effective lifetime (τ_{eff}) variation during cell processes related to B diffusion has been carried out by making the B-diffused p^+ layers for FZ and CZ single crystalline Si substrates[4]. The effect of "de-gettering" was evaluated by measuring t_{eff} for Si substrates after thermal processes in O_2 or N_2 ambient. The effect of B gettering on cell performance is also described.

2. Experimental

Two different Si substrates of p-type, FZ (2 Ω·cm) and CZ (10 Ω·cm) were used in this experiment. B was diffused at 1000°C for 60 min into both sides of the substrates to fabricate p^+ layers with a sheet resistance of 20 Ω/□ using a pyrolytic boron nitride solid source. To investigate the effect of thermal processes after B diffusion on bulk lifetimes, two types of samples were prepared. One was oxidized at 1000°C for 60 min to make a surface

[1] He is now with Sharp Corp.

passivation layer and the other was annealed in N_2 ambient at the same condition. Furthermore, to investigate gettering and de-gettering effects in detail, p-type CZ (10 Ω·cm) substrates were processed to fabricate B-diffused samples using consecutive B diffusion and oxidation. First, the B-diffused layers of three samples were removed in an HF:HNO_3 (1:20) solution. Then, the first sample was oxidized at 1000°C for 60 min, the second sample was diffused by B again and the third sample was oxidized at the same condition after the second B diffusion.

A microwave detected photoconductivity decay method using a pulse laser of 904 nm was used to measure τ_{eff}.. To examine the effect of B gettering, bulk lifetimes before and after B diffusion were measured using a chemical passivation (CP) technique. The CP technique using an ethanol solution of iodine was applied for reducing surface recombination velocity at wafer surfaces [5]. To obtain bulk lifetimes, before τ_{eff} measurements, the B-diffused layers were removed from each side of the wafer in an HF:HNO_3 (1:20) solution and then native oxide was removed in an HF:H_2O (1:10) solution.

3. Results and Discussion

The effect of B diffusion process on τ_{eff} for FZ and CZ wafers was investigated after removal of the B-diffused layers. As shown in Fig.1, the initial τ_{eff} values for FZ-p and CZ-p wafers were about 240 and 600 μs, respectively. After B diffusion, τ_{eff} for the FZ-p Si wafer increased about two times higher than the initial value although that for the CZ wafer did not vary substantially. This result showed that τ_{eff} increased due to B gettering.

On the contrary, as indicated in Fig. 2, measured τ_{eff} for both FZ and CZ wafers oxidized after B diffusion decreased drastically to as low as 3 μs. The values were two orders of magnitude lower than those for the B gettered samples. Furthermore, similar τ_{eff} decreases to about 10 to 20 μs were obtained for B-diffused wafers annealed in N_2 ambient. These mean that the drastic τ_{eff} decrease was caused by the thermal processes rather than the ambient effect.

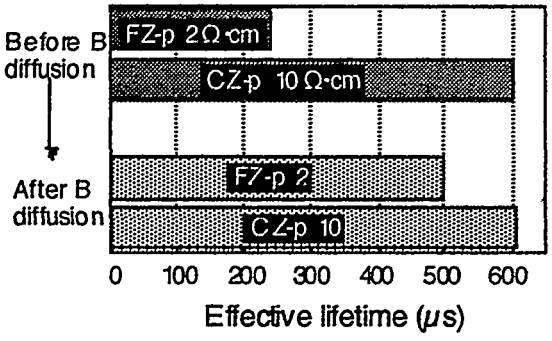

Fig. 1 Effect of boron gettering on effective lifetime for p-type FZ and CZ wafers.

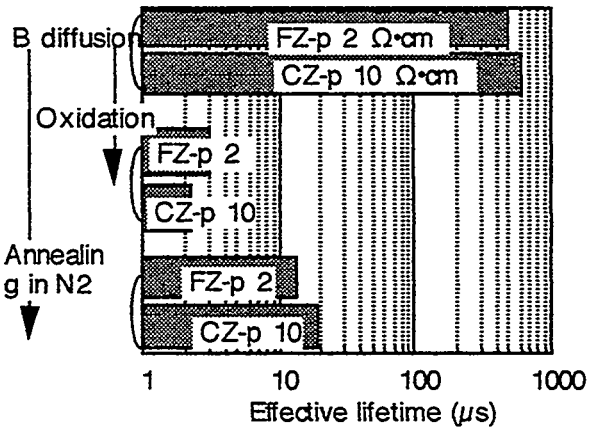

Fig. 2 Effect of thermal processes in O_2 or N_2 ambient on effective lifetime for p-type FZ and CZ wafers after B diffusion.

The effect of consecutive thermal processes on τ_{eff} was examined for CZ-p 10 Ω·cm Si wafers after removing the first B-diffused layers. After the second B diffusion, as shown in Fig. 3, τ_{eff} was about 500 μs as high as that for the first B-diffused sample, but τ_{eff} after

subsequent oxidation decreased to about 15 μs. On the other hand, in the oxidation after removal of B-diffused layers, τ_{eff} of about 150 μs was not so low as compared with the B-gettered samples and higher than samples oxidized after the first and second B diffusions. This result suggests that the twice B gettering is more effective than the once gettering and "de-gettering" occurs during thermal processes for samples with p^+ layers.

To investigate gettering and "de-gettering" mechanisms, carrier profiles before and after oxidation for the FZ-p wafers were measured by the C-V method with an electrochemical etching. Surface carrier concentration before oxidation was about 5×10^{19} cm^{-3}, which means B was heavily doped at the surface. Gettering sites were generated in the heavily B-diffused layers due to the atomic size difference between Si and B atoms. As a result, lifetime killer impurities were diffused and gettered at the sites. On the other hand, surface B concentration after oxidation decreased to 1×10^{19} cm^{-3}. Therefore, the gettering sites in the B-diffused layers became lower after oxidation. As a result, lifetime killer impurities could not be trapped at the defects and were diffused out from the B-diffused layers into bulk regions.

In order to estimate the gettering mechanism, the dependence of wafer thickness on τ_{eff} was investigated by repetitive etching of oxidized, B-diffused the CZ-p Si wafers. As indicated in Fig.4, the lifetimes degraded for whole regions of the wafers. This result indicated

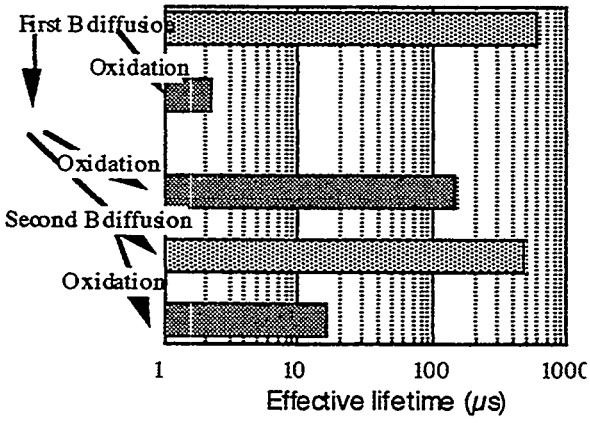

Fig. 3 Effect of consecutive B diffusion and oxidation processes on effective lifetime for p-CZ 10 Ω·cm wafers.

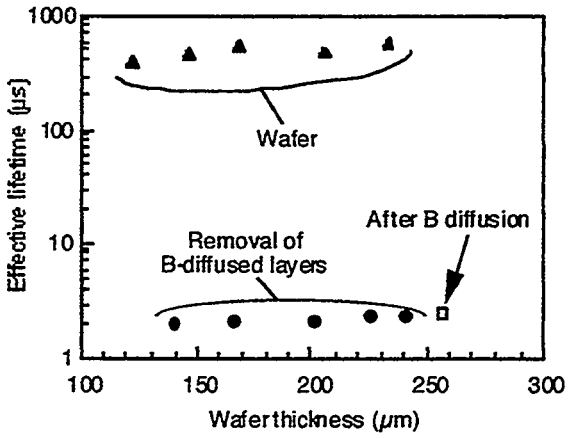

Fig. 4 Dependence of wafer thickness on effective lifetime for an oxidized and B-diffused p-type CZ.

that lifetime killer impurities diffused into almost the center of the wafer. Using an equation of $\sqrt{D}\cdot t$ where D is the diffusion coefficient and t the oxidation time, a diffusion distance of Fe was estimated to be 3 mm using the D of about 3×10^{-5} cm^2/sec at 1000°C [6]. This suggests that a fast diffuser like Fe might be related to the gettering and "de-gettering" processes. However, this assumption was not confirmed by measuring a deep level using Deep Level Transient Spectroscopy. As shown in Fig.5, a DLTS signal relating to nitrogen-vacancy complex was observed for an n-type FZ wafer oxidized after B-diffusion, whereas no signal was observed just after the boron diffusion process.

To confirm the effect of B-gettering on cell performance, cells were fabricated using p-type FZ wafers[7]. As indicated in Fig.6, cell efficiency was found to depend on B-diffused area and to attain a very high efficiency of 22.6 %. This was due to the increase of short-circuit current density by improving minority-carrier lifetime during the boron diffusion process.

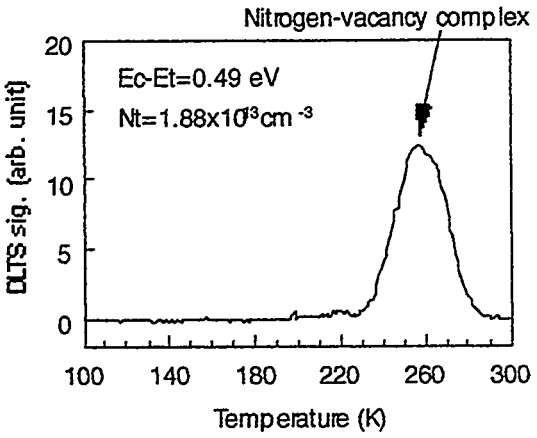

Fig.5 DLTS signal for an n-type FZ wafer oxidized after boron-diffusion.

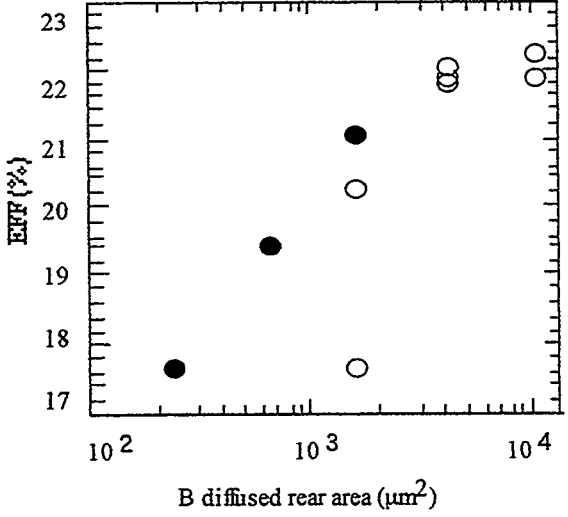

Fig.6 The effect of B-diffused rear area on cell cell efficiency for highly efficient Si cells.

4. Conclusion

After B diffusion, bulk lifetimes increased about two times higher than initial value for p-type FZ Si substrate. However, thermal processes in O2 or N2 after boron diffusion affected the drastic degradation of bulk lifetimes. These results suggest that lifetime killer impurities were gettered at defects in the heavily B-doped p^+ layers, whereas diffused out into bulk regions because of lowering surface B concentration by thermal processes. The B gettering was effective to improve cell efficiency for monocrystalline Si solar cells.

ACKNOWLEDGMENT

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ALUMINUM GETTERING OF GOLD IN SINGLE-CRYSTAL SILICON

SUBHASH M. JOSHI, ULRICH M. GÖSELE, AND TEH Y. TAN
Department of Mechanical Engineering and Materials Science, Duke University
Durham, NC 27708-0300

ABSTRACT

Aluminum gettering has been widely shown to improve minority carrier diffusion lengths in both single- and multi-crystalline Si, which has been attributed to gettering of metal impurities from silicon. In this paper, experimental results are reported which show that the Al gettering process can successfully getter away deliberately introduced Au from single-crystal Si. The Au diffusion profiles measured by the Spreading Resistance Profiling(SRP) method show that the Au is quickly gettered from Si regions near both wafer surfaces although the Al layer is present on only one wafer surface, while Au from the bulk of the wafer is gettered at a much more lower rate. This bears out previous simulation results which attribute the effect to the diffusion of Au in Si by the kick-out mechanism, by which the Au diffusion is coupled to Si self-interstitials (*I*). Out-diffusion of Au generates an *I* undersaturation which hinders further out-diffusion of Au from the bulk region whereas in the surface regions the ready supply of *I* from the surfaces prevents such an undersaturation from developing and hence the out-diffusion and gettering of Au proceed unimpeded in these regions.

INTRODUCTION

Gettering of unwanted impurities away from the device active regions is an integral part of manufacturing integrated circuits (IC) using Czochralski (CZ) Si wafers, where intrinsic or internal gettering (IG) is employed. IG utilizes oxygen precipitates and their associated defects in the CZ Si wafer bulk as gettering sites.[1,2] Gettering also shows promise for use in Si solar cell fabrication for improving the cell efficiency.[3,4] In this case an extrinsic or external gettering (EG) scheme, applied at one Si wafer surface, needs to be used since solar cells are bulk devices. Cost effective gettering schemes proposed for solar cell applications include P indiffusion gettering and Al gettering, since both P and Al are already used in solar cell fabrication for doping the emitter region and for forming contacts respectively. The gettering of contaminants, usually transition metals, to the gettering region involves the metal dissolution (if existing in a precipitated form), the diffusion of metal atoms to and their being stabilized at the gettering sites.

Al gettering is performed by annealing Si wafers with an Al layer on one wafer surface, which provides a gettering effect because the solubility of typical metal contaminant species is much higher in Al than in Si, thus creating a driving force for the metal species to segregate into the Al layer from the Si bulk. If the annealing temperatures used are above the Al-Si eutectic temperature of 577°C, then a liquid Al-Si alloy layer is formed on the surface of the Si wafer, which may have even higher solubility for metals and thus provide an even stronger gettering effect. Al gettering has been shown to successfully getter specific metal species from Si[5,6] and to result in improved minority carrier diffusion lengths.[7,8,9]

Au is not a naturally occurring impurity in Si, but its diffusion behavior in Si has been widely characterized and utilized for fundamental studies of diffusion in Si[10,11,12]. Au in Si is a substitutional-interstitial impurity, which means that it primarily resides in substitutional sites but diffuses in an interstitial form. The changeover from substitutional to interstitial form or vice versa requires interaction with native point defects in Si, which may be self-interstitials or vacancies. The diffusion of Au in Si has been widely modeled by considering interactions with self-interstitials via the kick-out reaction[13]

$$Au_s + I \leftrightarrow Au_i ,$$

where Au_s is a substitutional Au atom and Au_i is an interstitial Au atom. Au_s has a negligible diffusivity, while Au_i is very fast-moving but has a very low equilibrium concentration with respect to Au_s. Thus, diffusion of Au proceeds by a substitutional Au atom being kicked-out into an in-

terstitial site by an *I*. Therefore, the process consumes *I*, and if there is a net flux of Au atoms diffusing away from a Si region, an *I* undersaturation develops in the region. If this developing *I* undersaturation cannot be relieved by the presence of suitable *I* sources like dislocations, grain boundaries and surfaces, then further diffusion of Au is hindered.

SRP has been shown to be suitable for measuring Au diffusion profiles in Si because of the strong compensation effect of the Au mid-gap level on the shallow dopant levels in Si.[10,14] This causes a significant reduction in the carrier concentration and hence a significant increase in the resistivity when the Au concentration becomes comparable to the dopant concentration.[15] Thus, higher Au concentrations correspond to higher resistivity and hence higher measured spreading resistance.

EXPERIMENTAL

The present experiments involve deliberately contaminating Si with Au and then gettering the Au with an Al layer. 125 nm of Au was deposited on one side of a P-type, B-doped, single-crystal FZ Si wafer of 10-40 Ω-cm resistivity and 530 μm thickness, and subsequently the wafer was annealed at 950°C for 16 hr to indiffuse Au and then rapidly cooled in air. Following the anneal, 15 μm of Si was etched off from both sides of the wafer in two steps along with boiling aqua regia and RCA treatments after each step to remove all the surface Au, leaving a thickness of about 500 μm. After etching, a SRP sample was prepared by cleaving a piece of suitable size and bevel-polishing it to allow probing to a sufficient depth. This was done by lapping with 3 μm alumina abrasive in water followed by a 1 μm alumina abrasive in water and finally a polish with 0.25 μm diamond paste in oil. A SRP sample from the original wafer before Au indiffusion was also prepared. One sample from the wafer was sealed in an evacuated quartz ampoule and annealed at 1000°C for 8 hr, which served as a control. Other samples from the wafer were deposited with 1 μm of Al(99.999%) and also sealed in evacuated quartz ampoules and then annealed at 1000°C for 30 min, 2 hr and 8 hr respectively to perform Al gettering. The samples sealed in evacuated quartz ampoules were all about 9 mm wide and about 15 mm long or longer. At the end of each anneal, the ampoules were quenched in water. After quenching, the samples were removed from the quartz ampoules and SRP samples were prepared from the central part of each sample by cleaving and bevel-polishing as described above. Profiling was done in the thickness direction, i.e., one-dimensional diffusion conditions were considered. All the SRP profiles were measured from the unpolished side of the wafer, except for the 30 min Al gettering sample for which two samples were made and profiles measured from both surfaces. For the Au indiffusion as well as the Al gettering, the metal films were deposited on the unpolished wafer side.

RESULTS AND DISCUSSION

Figure 1 shows all the relevant SRP depth profiles. The SRP profile after Au indiffusion and etching shows a U-shape (Fig. 1(a)), which is characteristic of the indiffusion of Au by the kick-out mechanism.[10,13,14] In this case, the sides of the U have actually been truncated somewhat due to etching. The resistance values were noticeably increased as compared to the original SRP profile before Au indiffusion (Fig. 1(a)). The control sample which was annealed without Al for 8 hr at 1000°C shows some flattening of the SRP profile (Fig. 1(b)), i.e., the Au concentration has risen in the middle of the sample while it has dropped near the surface, but there does not seem to be any significant loss of Au. This flattening of the Au profile is expected as there is no longer an infinite source of Au atoms at the surface.[16] After Al gettering for 30 min, the spreading resistance has almost dropped to its original value near both wafer surfaces, while it remains almost unchanged in the middle (Fig. 1(b)). The 30 min profile is a composite of two separate profiles measured from both wafer surfaces and the Al gettering layer was on the left surface of the profile shown. For the 2 hr Al gettered sample, the SRP profile (Fig. 1(b)) has almost dropped to the original wafer values before Au indiffusion (Fig. 1(a)). Previous simulation results of the gettering of Au by Al from a Si wafer have indicated that initially, gettering of Au in both the surface regions is fast even though there is an Al layer on only one surface.[17] This is because outdiffusion of Au will generate an undersaturation of *I* in Si because of *I* consumption by kicking out Au_s atoms to become the

mobile Au_i atoms. Since both surfaces of the sample serve as sources of *I*, they will relieve the *I* undersaturation in the surface regions, thus allowing further kicking-out of the Au_s atoms to diffuse to the Al-Si layer where they are stabilized, i.e., gettered. In the wafer interior, the *I* undersaturation will not be relieved, thus inhibiting more Au_s atoms from being kicked-out and mobilized. Since the diffusivity of the substitutional gold atoms is negligible, they will remain practically ungettered. As the annealing proceeds, the in-diffusion of *I* from the surfaces will relieve the undersaturation of *I* in the bulk, thus allowing more and more gold substitutional atoms to be kicked-out and gettered.

After 8 hr annealing, it is expected that all the Au will be gettered and the SRP profile will thus be flat and almost equal to the original profile that was present before Au contamination. In our experiment, a reasonably flat profile is obtained after 8 hr Al gettering (not shown here) but the SRP values are not as low as the original sample but intermediate between the original sample and the contaminated sample. Since the Al gettering has been performed in evacuated quartz ampoules at high temperatures, it is expected that there will be loss of Al from the surface Al-Si layer due to evaporation, and indeed it is observed after annealing and quenching that the insides of the quartz ampoules have a thin metallic coating. This is observed for all gettering times, i.e., 30 min, 2 hr and 8 hr. However, it is reasonable to expect that loss of Al is the most severe for the 8 hr anneal, and the composition of the liquid Al-Si layer may be sufficiently changed so that the Au solubility is reduced towards the later part of the anneal. Since the relative concentrations of Au in the Si and the Al-Si layer when equilibrium is reached are dependent on the relative solubilities of Au in the two layers,[18] a reduction of Au solubility in the liquid layer would cause a decrease in the Au concentration there and a simultaneous increase in the Au concentration in the Si sample. Thus, for longer times, the gettering capacity of the liquid Al-Si layer may decrease due to evaporation loss of Al.

SUMMARY

Al gettering was successful in gettering Au from deliberately contaminated single crystal Si. Although the liquid Al-Si gettering layer is present only on one surface, the Au is initially gettered from both surface regions and then progressively to increasing depth from both surfaces. This is attributed to undersaturation of Si self-interstitials in the bulk of the sample which is gradually compensated by supply of self-interstitials from both surfaces. For long annealing times, evaporation loss of Al from the surface Al-Si layer reduces its gettering capacity for Au, thus causing some of the Au to diffuse back into the Si.

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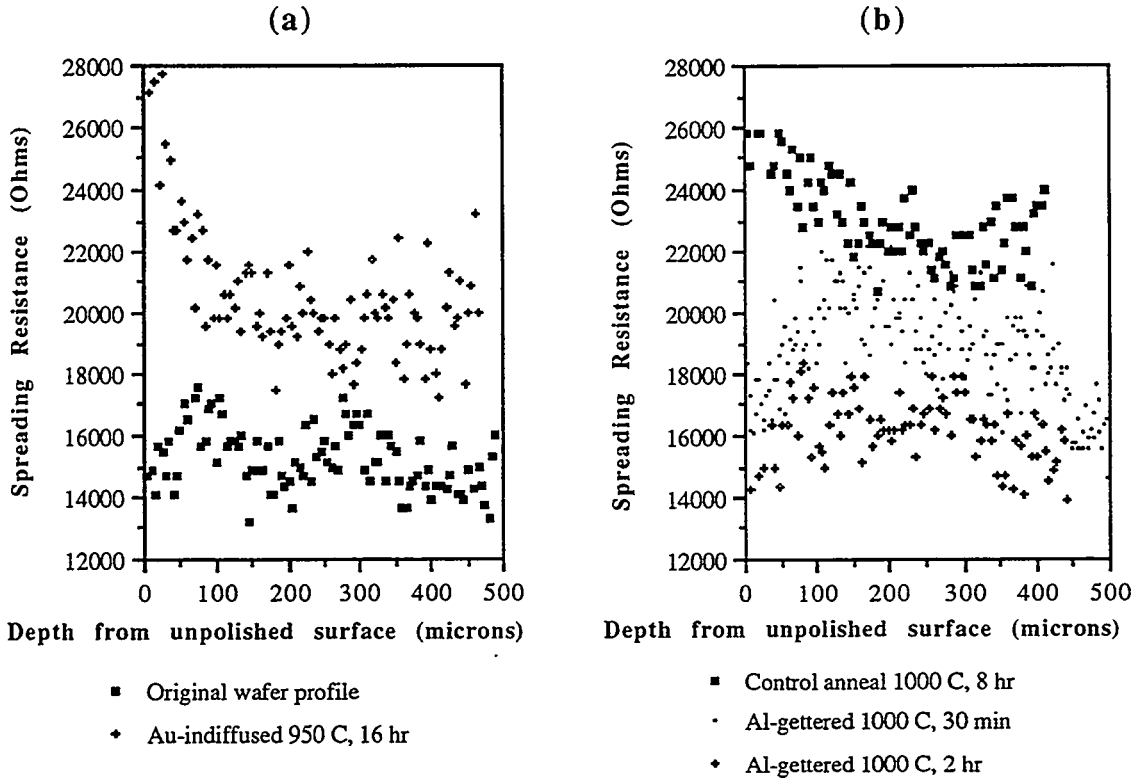

Fig. 1 Spreading resistance depth profiles of Si samples (a) from original wafer and after Au indiffusion at 950°C for 16 hr, (b) control annealed at 1000°C for 8 hr and after Al gettering at 1000°C for 30 min and for 2 hr respectively. Almost all profiles were measured from the unpolished wafer surface (at 0 micron depth). For the 30 min Al gettering, two samples were taken from adjacent locations and profiles measured from both surfaces (i.e., from 0 microns and 500 microns). The profile shown above is a composite of the two. For Au indiffusion as well as Al gettering, the metal films were deposited on the unpolished surface, i.e., on the left side of the profiles shown.

Response of Silicon-Film™ Polycrystalline Silicon to Post-Growth Quality Enhancement Treatments

Yibin Bai, David H. Ford, James A. Rand, Robert B. Hall and Allen M. Barnett
AstroPower, Inc., Solar Park, Newark, Delaware 19711-2000, USA

The baseline post-growth quality enhancement procedures used to produce high efficiency Silicon-Film™ polycrystalline silicon solar cells feature an extended-duration phosphorus/aluminum gettering and a RF hydrogenation. Effective minority carrier diffusion lengths have been increased from 30-40μm to 150-200μm as a result of the post-growth processing. During the course of investigation, the response of Silicon-Film™ materials to the quality enhancement steps was found to be material specific and site specific. Spectral response of certain devices was shown to have an unusual illumination dependence. Non-uniformity of effective diffusion lengths across the wafer correlates with this unusual illumination behavior. Initial efforts to understand these behaviors are described.

I. Experimental

Post-growth quality enhancement techniques, or defect engineering, have been investigated by many groups and are considered to be an integral part of polycrystalline silicon solar cell processing. The degree of improvement and the individual process can vary with different materials. Process sequence used to fabricate high efficiency Silicon-Film™ polycrystalline silicon solar cells involves a pre-gettering preparation, phosphorus/aluminum gettering, removal of diffused/alloyed layers, emitter diffusion, RF hydrogenation, emitter surface passivation, metallization and antireflection coating. Among these, external gettering and hydrogenation are two major steps used to improve the quality of as-grown Silicon-Film™ sheet materials.

Phosphorus diffusion and aluminum alloying, which are compatible to silicon solar cell fabrication sequences, were chosen for the investigation. Prior to gettering, the as-grown Silicon-Film™ wafers were chemically thinned to about 300μm. This allows phosphorus gettering to occur at the front surface and aluminum gettering at the back surface. Because of the synergistic and complementary effects of impurity diffusion and segregation during P/Al gettering, a four-hour gettering step performed at 890°C [1] was used and found effective in increasing the minority carrier diffusion length in Silicon-Film™ materials. The diffused and alloyed layers were removed to prevent the gettered impurities from entering the bulk during the subsequent high temperature process steps. Emitter diffusion was optimized separately.

Passivation of bulk structural defects was accomplished using RF hydrogen plasma treatments performed at 310°C for 40 minutes. This treatment was found to be additive to the gettering step in increasing the effective carrier diffusion length. The side effect of

plasma treatment is that it interferes with emitter surface passivation by damaging the solar cell surface, thereby decreasing the blue response. In order to avoid the depassivation of hydrogenated materials from a high temperature oxidation process and to achieve a good blue response, a low-temperature emitter surface passivation using a PECVD (Plasma Enhanced Chemical Vapor Deposition) oxide layer was implemented. Surface damage caused by RF hydrogenation was found reparable by an emitter etchback using a weak HF/HNO_3 based solution.

II. Result and Discussion

Figure 1 shows the effects of post-growth quality enhancements on the internal quantum efficiency (IQE) of Silicon-Film™ solar cells. Extended P/Al gettering and RF hydrogenation significantly improved the long wavelength (>600nm) response by increasing minority carrier diffusion length in the base region. The diffusion lengths obtained in finished solar cells can reach over 200μm after incorporating material quality enhancement steps. As illustrated by two dashed lines in Figure 1, PECVD oxide enables the passivation of the emitter surface, leading to an increase in the short wavelength response. Here, the good surface passivation is the result of optimized emitter doping profile, oxide deposition conditions and forming gas annealing.

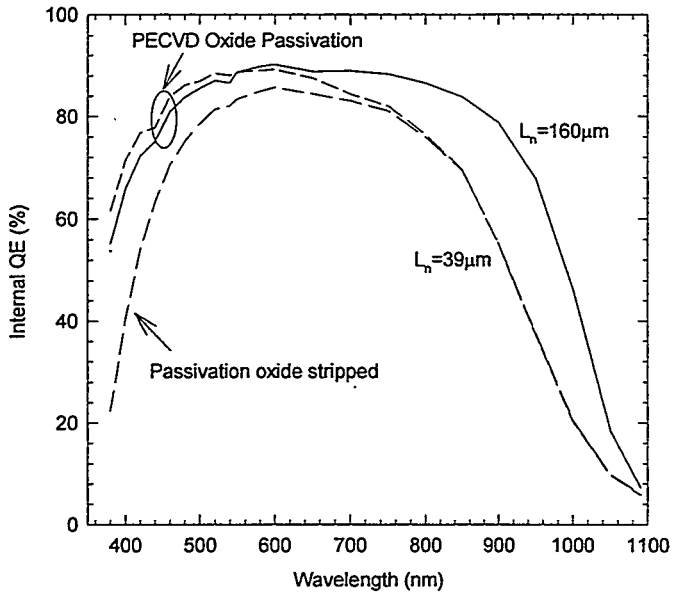

Figure 1. Effects of post-growth quality enhancements on internal quantum efficiency (IQE) of Silicon-Film™ solar cells. Solid line: gettered; Dashed lines: ungettered. All cells received identical emitter diffusion and passivation.

The degree of improvement for Si-Film™ materials was found to be material specific and site specific. This may be due to the batch differences in material growth and the inhomogeneous distribution of impurities and defects. This limits the performance of

large-area Silicon-Film^{TM} solar cells. Investigation into the process of material upgrading was required. One of the focuses was the *evolution* of carrier diffusion length along with the solar cell fabrication process, especially the post-growth quality enhancement steps. Figure 2 shows the diffusion lengths measured at three different stages during solar cell fabrication. Diffusion lengths were determined from IQE data taken on three sets of mesa diodes. The substrates used to make mesa diodes were cut from the same wafer in order to ensure a statistically significant result. Data shown in Figure 2 do not represent the best case of improvement but reflect the typical changes in diffusion length. As indicated in Figure 2, the Silicon-Film^{TM} materials investigated, in general, have a high response to hydrogenation treatment. However, the overall improvement in carrier diffusion length depends on the effectiveness of gettering step. Obviously, material-B was degraded during the gettering step. This can be related to the high oxygen concentration and/or high localized dislocation densities that can reduce the gettering efficiency [2]. This area is addressed in the material growth process.

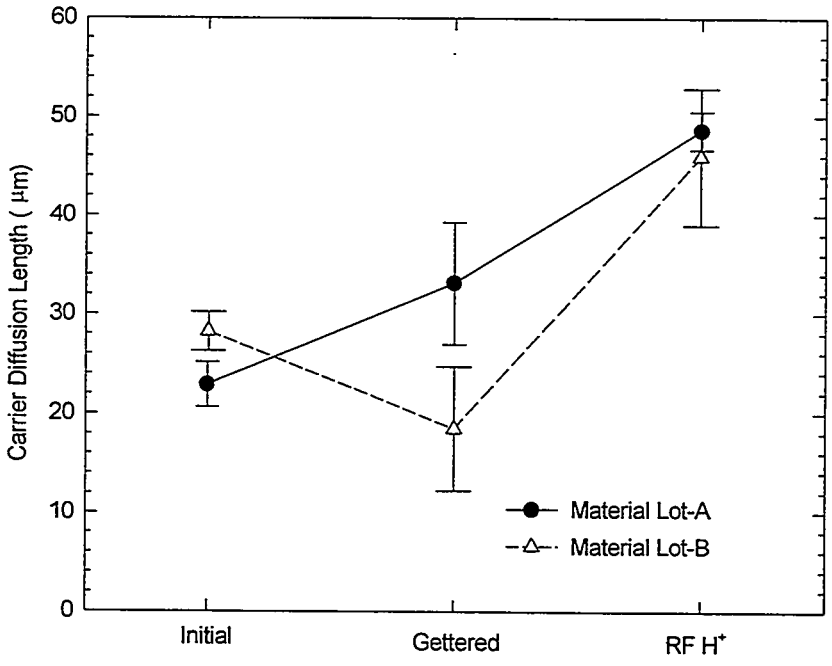

Figure 2. Evolution of measured carrier diffusion lengths along with post-growth quality enhancement steps. Two typical material lots that have different gettering responses

Localized characterization using EBIC measurements was also performed on the mesa diodes analyzed in Figure 2. The measurements were made using a beam energy of 30 KeV, which yields an electron penetration depth of about 7 μm. Results indicated that the gettering step increases the overall EBIC signal level over the whole mesa diode while the hydrogenation treatment works greatly to suppress the electrical activities at grain boundaries. Figure 3 shows a EBIC image of a mesa diode that has received both gettering and hydrogenation treatments. Prior to hydrogenation, a PECVD oxide layer (~4500Å)

used to prevent hydrogen plasma from reaching the silicon surface was deposited onto the mesa diode. Then a square-shaped window (2mm x 2mm) in the middle was opened by selective etching. Thus, only the exposed region received a hydrogen plasma treatment. The masking oxide was removed prior to EBIC measurements. As can be seen, the grain boundary recombination was significantly minimized in the hydrogenated region.

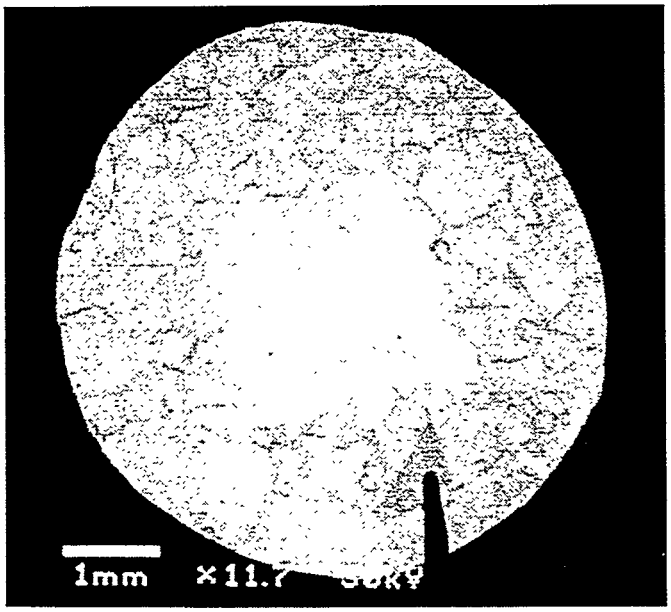

Figure 2. EBIC mapping shows the effect of extended RF hydrogenation on the electrical activities at grain boundaries. Measured in the dark and no bias.

Inhomogeneous behavior of bulk electrical properties across wafers is also related to extended defects, such as grain boundaries and dislocations. One interesting phenomenon that we have observed was an unusual illumination bulk behavior, i.e., the solar cell long wavelength response decreases as the bias light intensity is increased. This is different from what was observed previously, in that the long wavelength response increased with the bias light intensity. According to the explanation by others [3], defect clusters (or grain boundaries) in polycrystalline silicon are effectively negated by high injection levels, leading to a reduction in carrier recombination at these regions. The opposite illumination dependence indicates other mechanisms exist in the devices, either material related or process related. Based on the limited data obtained from devices processed at different stages, the unusual illumination response is likely to occur during the hydrogenation treatment. If this is the case, the illumination-dependent bulk effect would occur mostly at grain boundaries based on the result of Figure 2. As reported earlier, the dependence of recombination velocities on injection levels at grain boundaries and at the silicon surface can be modified by oxygen concentration [4] and doping concentration [5] in the materials. It is still too early to conclude that elimination of this unusual illumination dependence can lead to further increase in bulk quality. More interestingly, the diffusion lengths extracted from light biased IQE data show a better uniformity than those extracted from IQE data taken without light bias. An observation

of this is listed in Table 1. To facilitate further investigation, the light-biased EBIC or LBIC studies can be a good tool to identify any possible localized illumination behavior. This work is in preparation.

Table 1. Diffusion lengths of three adjacent one cm^2 Si-Film™ solar cells determined from IQE with and without light bias.

Effective Diffusion length (μm)	*Cell#1*	*Cell#2*	*Cell#3*
With light bias	90	88	87
Without light bias	114	148	174

III. Conclusion

Silicon-Film™ material has a high response to post-growth quality enhancement techniques through the suppression of intragrain and grain boundary recombination. Spatial behaviors of bulk electrical properties are of importance to large area Silicon-Film™ solar cells. Non-uniform bulk electrical properties are originated from non-uniform distribution of impurity species and extended defects. Non-uniformity of effective diffusion lengths correlates with the injection dependent bulk behavior.

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MAGNETIC FIELD TOPOGRAPHY FOR CURRENT DISTRIBUTION MEASUREMENTS IN SOLAR CELLS

J. Kabs and H.J. Möller
TU Bergakademie Freiberg, Institute for Experimental Physics
Silbermannstr. 1, 09596 Freiberg, Germany
phone: 49 - 3731 - 39 36 89, fax: 49 - 3731 - 39 43 14
email: kabs@physik.tu-freiberg.de

1. Introduction

The current flow in homogeneous standard solar cells is well understood. After the generation electrons and holes diffuse mainly in one direction perpendicular to the surfaces. Close to the top surface the current changes the direction and flows in the emitter region to the contacts parallel to the surface. Inhomogeneities in the conducting properties of the emitter layer or 'shunts' of the pn-junction disturb the current flow and may degrade the electrical properties of the solar cell. In order to understand the mechanisms of the degradation the localization and identification of the defects that cause the inhomogeneity is essential.

Recently we developed a new method CASQ (Current Analysis by SQuids) that allows one a very direct measurement of the current distribution in a solar cell [1]. The CASQ method is based on the relationship between the lateral current in the emitter region and the induced magnetic field that extends into the free space above the solar cell. Inhomogeneities of the current distribution are directly reflected in the magnetic field. From the topographical measurement of the field close to the surface we can calculate the current flow in the emitter and in the contacts. In addition to the localization of bulk defects and their ramifications on the current distribution, the quality of the grid fingers can be monitored as well.

2. Experimental Procedure

SQUIDs are sensitive sensors for magnetic fields and are required for current density measurements in the range considered here (down to 10 $\mu A/cm^2$). The use of high-temperature SQUIDs offers today much greater flexibility for the application compared to SQUIDs that require liquid helium. An important advantage is that the sensor can be brought close to the sample surface which increases the spatial resolution.

In our commercial CASQ instrument the SQUID probe is placed inside a specially constructed cryostat filled with liquid nitrogen [2]. The position of the SQUID can be oriented in various directions so that all three components of the magnetic field can be determined. The cryostat is mounted above a non-magnetic xy-table that can support and shift 10 x 10 cm^2 solar cells. The minimum distance between the sensor and the sample is less then 1 mm, restricted by the isolation vacuum of the cryostat. This limits the maximum lateral resolution of the measurement which is currently about 0.5 mm.

To minimize the influence of external electromagnetic fields, the system is shielded in a μ-metal / aluminium chamber with small lead-throughs for the connection to the interior (e.g. the electrical connection of the SQUID). The xy-movement of the table is realized by two step motors outside of the chamber. In addition, all the electrical connections to the sample have to be twisted and located at maximum distance to the sensor. A potentiometer allows the adjustment of the total current from the cell.

At present three different operating conditions for the solar cell can be realized:

- the application of an external voltage,
- the global illumination by four halogen lamps and
- the local illumination through an optical fibre with laser light.

After the measurements a numerical deconvolution of the magnetic field is performed that yields a topographic image of the current distribution in the top layer of the solar cell. This analysis is based on the application of the Biot-Savart-law:

$$B(x,y,z)=\frac{\mu_0}{4\cdot\pi}\int\frac{\vec{J}(x',y',z')\times(\vec{r}-\vec{r}')}{(\vec{r}-\vec{r}')^3}d\vec{r}' \qquad (1)$$

It is assumed that the conductive layer is very thin (thickness $d_{emitter}$) and carries currents only parallel to the surface, that means $j_z = 0$. In this case equation 1 simplifies and yields for instance for B_x

$$B_x(x,y,z)=\frac{\mu_0 \cdot d_{emitter} \cdot z}{4 \cdot \pi}\int\frac{\bar{J}_y(x',y')}{(\bar{r}-\bar{r}')^3}dx'dy' \qquad (2)$$

Equation 2 is a convolution integral, where the source $J_y(x',y')$ is convolved with a Green's function $G(x-x',y-y',z) = 1/(\mathbf{r} - \mathbf{r}')^3$. The determination of the current density from the magnetic field requires the inversion of the problem. In general, the inverse problem can not be solved uniquely for a three-dimensional current distribution. In the special two-dimensional case considered here the solution is, however, unique [3].

Equation 2 can be Fourier-transformed applying the convolution theorem. One obtains the following equation for the transformed B_x- component:

$$b_x(k_x,k_y,z)=g(k_x,k_y,z)\cdot j_y(k_x,k_y) \qquad (3)$$

$$\text{with } g(k_x,k_y,z)=\frac{\mu_0 \cdot d_{emitter}}{2}\cdot e^{-\sqrt{k_x^2+k_y^2}\cdot z} \qquad (4).$$

The determination of the current is thus reduced to a division of $b_x(k_x,k_y,z)$ by $g(k_x,k_y,z)$ and the reverse transformation into the real space.

As $g(k_x,k_y,z)$ decays exponentially with both **k** and z, the Green's function works as a spatial low-pass filter. In addition, g contains only discrete values of **k**, settled in the low-frequency range of the frequency spectra. For the inverse problem this loss of information means an amplification of the noise, as the current density rises for low magnetic fields and high spatial frequencies. Nevertheless equation 3 contains a fast and elegant way to compute the current density distribution from the magnetic field data.

3. Experimental Results

3.1 Solar cell with applied voltage

Although the magnetic field topography of a solar cell operated under applied voltage does not reflect the real situation, this mode can be used to detect inhomogeneities [4,5,6].

In figure 1 we focus on a part of a mc-silicon solar cell. The j_y component calculated from the measured B_x component is displayed. A 100 mV forward biased voltage is applied to the 100 x 100 mm^2 cell without anti-reflexion layer. The total current is about 6 mA. The bus bar of the cell is orientated parallel to the x-direction (at y=25 mm), the grid fingers at a distance of 4 mm are parallel to the y-direction. The electrical contact is located at the lower end of the bus; the rear contact covers the entire aluminium backside contact of the solar cell.

The topogram shows a rather diffuse current distribution and does not reflect the current flow accurately in the grid fingers. This is because of the numerical deconvolution of the magnetic field as mentioned above, which can only be performed on a discrete set of data because of the limited lateral resolution of the method. Nevertheless differences in the current flow are obtained that are unexpected.

The B_x component mainly reflects the current in the y-orientated grid fingers and is less sensitive to the bus current. The red areas always belong to a current flow in positive y-direction, the blue areas to a negative j_y (as also indicated by the arrows). The topogram clearly shows inhomogeneous current densities in several fingers in the picture. It is surprising that not only the absolute values vary but also the directions of the currents.

Figure 2 gives a detailed view of the upper part of figure 1. The enhanced current densities of two neighbouring grid fingers are clearly separated. In addition, one can see the increase of the current towards the bus and the inversion of the current flow direction in neighbouring grid fingers as mentioned above.

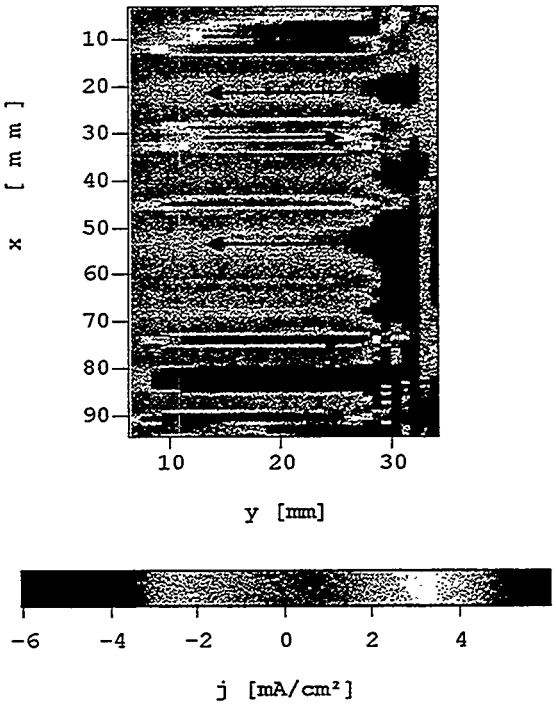

Figure 1: Calculated j_y component from the measured magnetic field B_x of a mc-silicon solar cell operated under applied voltage (100 mV, 6 mA). The external contact is positioned at (100/25). The red and the blue areas indicate enhanced current densities in positive and negative y-direction, outlined by the arrows.

These results that have been observed in other cells as well show that not all fingers contribute to the current flow equally. Furthermore there exist also loss mechanisms that lead to an inversion of the current flow.

3.2 Solar cell under global illumination

In Figure 3 the j_y component of another mc- silicon solar cell (50x50 mm^2, a single bus bar orientated in x-direction at y=28 mm) is shown. During this measurement the cell was homogeneously illuminated. A single external contact collected the total current (about 3 mA) from the cell at the lower end of the bus bar.

The current distribution is more or less homogeneous, the current increases from all parts of the cell to the collecting contact. There are current variations between bulk and grid but they are weak and can only be seen in line scans. Under these conditions any inhomogeneities in the current distribution in the grid fingers and the bulk material cannot be detected. (The narrow yellow area in the middle of the topogram belongs to the enhanced current in the bus bar which, although perpendicular to the measured B_x-component, cannot be totally suppressed probably due to misorientation.)

The same sample if observed under the same illumination conditions, but in the open-circuit-case, i.e. without external contact, is shown in figure 4. In contrast to the previous conditions there is no current flow in the grid fingers of the cell. The current flows to areas where recombination of the carriers can occur. Therefore this yields a kind of 'current-loss topography'. The topogram for this example shows enhanced current densities in the centre of the cell and a small variation in the middle of the lower edge (direction also outlined by the arrows).

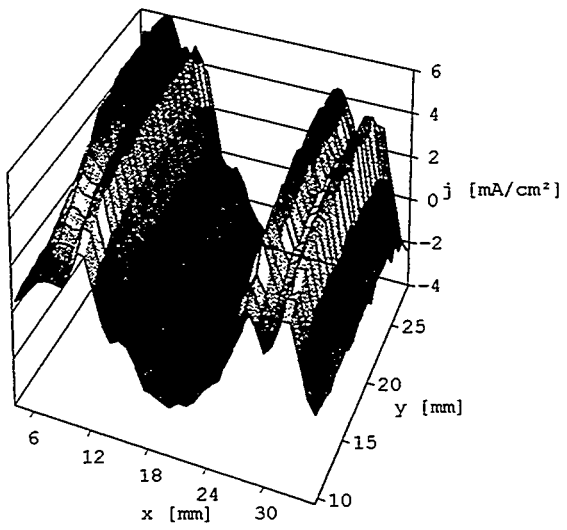

Figure 2: Enlarged view of figure 1 at the upper part. The axes labels are the same. The increasing current towards the bus of two neighbouring grid fingers (at x=7 and 11 mm and x=29 and 33 mm) can be seen. The blue area in the middle indicates a current flow in the opposite direction.

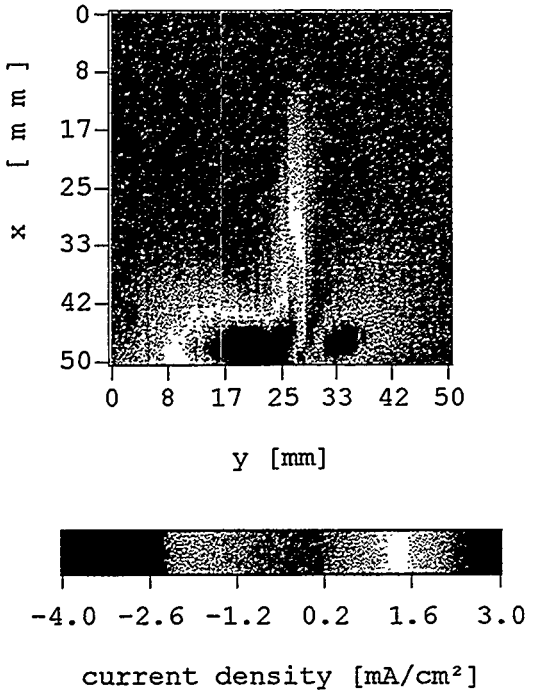

Figure 3: Calculated j_y component of a mc-silicon solar cell under global illumination. A contact is located at position (50/28). The total current from the cell is about 3 mA. The current density increases homogeneously to the contact. No variations of the current in the grid structure or the bulk are observed.

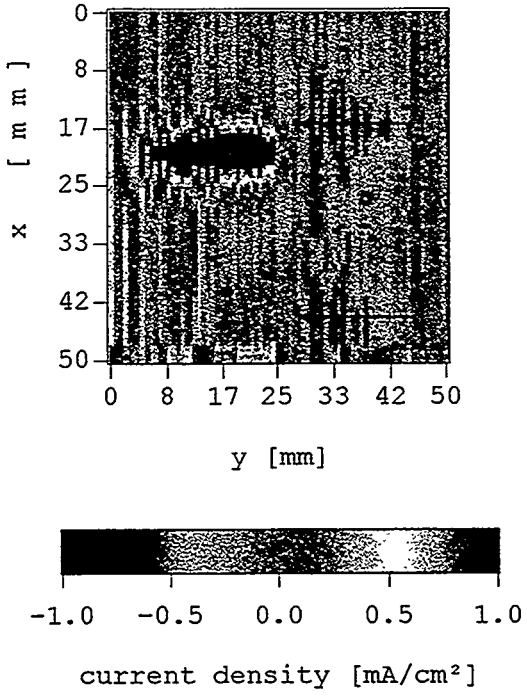

Figure 4: j_y component of a mc-silicon solar cell under homogeneous illumination in the 'open-circuit' case. Under these conditions no current flows in the grid. One can observe, however, the areas where enhanced recombination of carriers in the bulk occurs. The vertical artefacts are due to the amplification of noise in the y-direction.

These topograms clearly show the difference between the two measuring conditions. While the measurement with electrical connections leads to a magnetic field topography dominated by the main current flow in the grid, the open-circuit mode, allows one to monitor bulk areas where enhanced current losses occur.

3.3 Locally illuminated solar cell

Another operating mode for CASQ is measuring the magnetic field under spotlike illumination. In this case, illumination occurs by a laser through an optical fibre. Due to geometrical constraints of the cryostat the end of the optical fibre can only be located at a certain distance from the SQUID, as shown in figure 5.

The spatial resolution in this case is determined by the size of the illuminated area (about 0.2 mm^2). Under the assumption that the generated carriers diffuse radially from the illumination centre, the SQUID detects the difference of the current flow in positive and negative direction and works, as the distances equal each other, as a current gradiometer. It is thus particularly sensitive to the direction of the current flow in the bulk.

An example is shown in figure 6 where the j_x component of a multicrystalline silicon solar cell (same sample and equivalent axes labels as in figure 4) is depicted. The orientation of the SQUID is as in figure 5: the SQUID detects the B_y-component. The red and blue areas indicate regions where the current flows mainly in the positive or negative x-direction. The grid structure is visible because carrier generation is suppressed when the laser beam hits the contact area.

The topogram displays a current flow to the centre of the cell (the carriers accumulate at an area in the region between x = 25 - 33 mm). Only the small stripe parallel to the bus on the right hand side the current flows in the inverse direction (mainly to the edge of the cell).

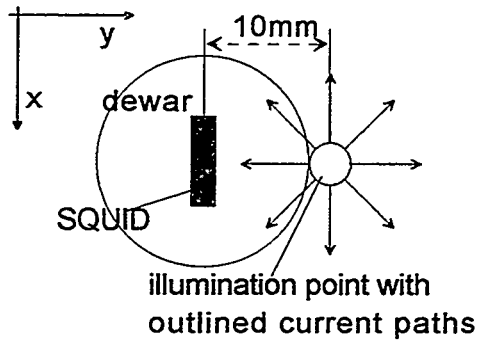

Figure 5: Geometry of the point illumination mode. Under these conditions (SQUID detecting B_y), the SQUID works as a 'current-gradiometer' for the current flow in positive and negative x-direction.

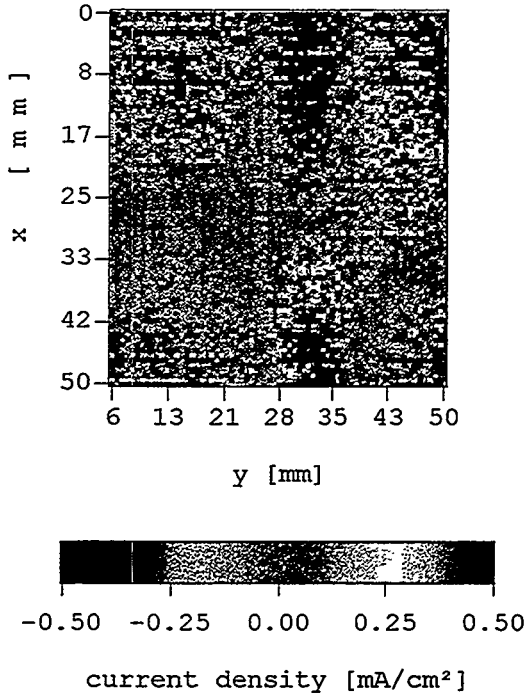

Figure 6: j_x component of a mc-silicon solar cell illuminated by a laser beam positioned at a distance of about 10 mm to the SQUID. In this mode the SQUID detects the difference of the current flow in positive and negative direction parallel to the SQUID area and works as a current gradiometer. The horizontal stripes parallel to the y-direction reflect the grid fingers (visible in the non-homogeneous areas): if the beam hits the contact carrier generation is suppressed.

4. Conclusion

CASQ is a new method for direct measurements of the current distribution in solar cells. Apart from the advantages, that it is undestroying and non-touching, CASQ is a very sensitive method for the determination of the current, not only of the absolute value, but also of the direction. First measurements have underlined the possibilities of CASQ to observe inhomogeneities in the current flow. Different operating conditions allow one to monitor the grid and the bulk currents independently.

The investigations showed already that the grid fingers of commercial solar cells often do not work efficiently. The results further demonstrated that the CASQ method is able to detect deteriorated bulk areas of the solar cell. This information can be used for further investigations with other analytical techniques which allow one to connect the electrical characteristics with defect distributions.

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THE EFFECT OF GETTERING ON AREAL INHOMOGENEITIES IN LARGE-AREA MULTICRYSTALLINE-SILICON SOLAR CELLS

James M. Gee[1] and Bhushan L. Sopori[2]
[1]Sandia National Laboratories, Albuquerque, New Mexico (USA)
[2]National Renewable Energy Laboratory, Golden, Colorado (USA)

ABSTRACT: Multicrystalline-silicon (mc-Si) materials and cells feature large areal variations in material and junction quality. The regions with poor device quality have been predicted to have more recombination current at forward bias than a simple area-weighted average due to the parallel interconnection of the good and bad regions by the front junction. We have examined the effect of gettering on areal inhomogeneities in large-area mc-Si cells. Cells with large areal inhomogeneities were found to have increased non-ideal recombination current, which is in line with theoretical predictions. Phosphorus-diffusion and aluminum-alloy gettering of mc-Si was found to reduce the areal inhomogeneities and improve large-area mc-Si device performance.

INTRODUCTION

Multicrystalline-silicon (mc-Si) materials are a commercially important photovoltaic material. This material consists of individual crystalline-silicon grains. The crystal orientation and grain size distribution depends upon the specific crystal growth method, but the orientation is generally random and the size varies between a few millimeters to several centimeters. The intragrain dislocation density, impurity precipitate density, and intrinsic stress can vary significantly between grains. The net result is that there can be significant areal variations in material and junction quality in large-area mc-Si cells.

The effect of areal inhomogeneities has been examined theoretically by several research groups [1,2,3]. These models use a network model of the solar cell – i.e., the cell is divided into many small subcells that are connected in parallel through resistors that represent the front-surface junction and grid (Fig. 1). The areal inhomogeneities are represented in the equivalent circuit parameters of the small subcells. A significant result of these studies is that the recombination current in the poor regions at open-circuit and maximum-power voltages are greater than predicted by the area-weighted average of the subcell parameters; i.e., *the low-performing regions can act as "sinks" to dissipate power internally within the cell* [2] due to the parallel interconnection of the good and poor regions.

Experimentally demonstrating the enhanced recombination due to poor regions has been difficult. For example, mapping of the recombination current at any bias except short circuit is difficult because the parallel interconnection of the junction distributes the recombination current over a large area. The theoretical models suggest an indirect means to experimentally examine the effect of areal inhomogeneities. A solar cell is frequently modeled as two parallel diodes, a current source, and a series and shunt resistance. The diodes represent "ideal" and "non-ideal" recombination current, where the diode quality factor (n) is unity for ideal and n>1 for non-ideal recombination. The models predict that cells with large areal inhomogeneities will exhibit large non-ideal recombination in the double-diode model [3].

We examined the effect of gettering on areal inhomogeneities in mc-Si substrates . Gettering refers to a process where deleterious impurities are removed from important regions of a solar cell to less important regions. As a result of the detailed device characterization for our experiments, we also make some observations on the effect of areal inhomogeneities on large-area mc-Si solar cell performance.

EXPERIMENT

Several types of large-area mc-Si cells were thoroughly characterized. The first group of cells were low-, medium- and high-performance production 100-cm^2 EFG cells from ASE Americas. This material consists of long (many centimeters) and narrow (less than 1 cm) grains, and has low oxygen and high carbon concentrations. The second group of 42-cm^2 mc-Si cells were fabricated at Sandia using HEM mc-Si from Crystal Systems. This mc-Si material has low carbon and oxygen concentrations and was used in the recent demonstration of an 18.6%-efficient 1-cm^2 mc-Si cell [4]. The Sandia cells included both control and gettered splits, where the gettering included phosphorus diffusion and/or aluminum alloy. The gettering step was performed and the gettering layer removed prior to cell fabrication. The fabrication sequence includes an aluminum-alloyed back-surface field and passivated emitter, and uses a photolithographically defined, evaporated metallization and an evaporated double-layer ARC [5].

The cell characterization included one-sun IV, dark-IV, absolute spectral response, hemispherical reflectance, and 1064-nm laser-beam-induced-current (LBIC) scans. The

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one-sun and dark-IV data was fitted to a double-diode model, and the recombination current distribution at maximum-power and open-circuit voltages were calculated. Histograms of the LBIC data provided a good graphical description of the areal inhomogeneities.

RESULTS

The histograms of the LBIC data for the ASE cells show a systematic improvement in areal homogeneity as the cell performance increases (Fig. 2). The LBIC histogram both narrows and the mean moves to higher response, which indicates that the material is both more uniform and of higher quality. The improvement in cell performance is reflected mainly in V_{oc} and I_{sc} (Table 1), while the cell parameters from the fitted dark-IV data show that there is a systematic decrease in the non-ideal recombination current with improved cell performance (Table 2).

The gettering experiment on the HEM material (Table 3) found significant improvement in device performance due to the gettering of around 2% absolute. Similar gettering experiments in our laboratory typically finds more modest improvements (on the order of 0.5% absolute) and is generally material specific. The large gettering effect for this particular experiment more clearly illustrates some of the effects of gettering on areal inhomogeneities in large-area mc-Si cell performance.

There was a dramatic improvement in non-ideal recombination with gettering for the 42-cm^2 HEM mc-Si cells. The non-ideal recombination represented around 18% and 5% of the recombination at V_{oc} and 60% and 30% of the recombination at V_{mp} for the non-gettered and gettered cells, respectively (Table 4). The histograms of the LBIC data (Fig. 3) again show an improvement in the areal uniformity for the gettered cells.

CONCLUSIONS

Gettering of mc-Si substrates was found to both reduce the areal inhomogeneities and improve large-area mc-Si cell performance. In line with theoretical predictions, we found that the non-ideal recombination current in large-area mc-Si cells is qualitatively correlated with larger areal inhomogeneities.

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Table 1. ASE 100-cm^2 EFG mc-Si production cells.

Cell	Eff	V_{oc}	J_{sc}	FF	V_{mp}
High	14.2	0.586	31.8	0.760	0.480
Medium	13.4	0.578	30.7	0.757	0.471
Low	12.8	0.567	30.1	0.752	0.460

Table 2. Distribution of recombination (%) in ASE cells. n1 and n2 refer to ideal and non-ideal recombination.

	V_{oc}		V_{mp}	
Cell	n1	n2	n1	n2
High	94.9	4.6	68.1	26.2
Medium	94.4	5.2	67.2	27.9
Low	93.4	6.3	67.0	29.4

Table 3. Gettering experiment with 42-cm^2 cells on HEM mc-Si material. Gettering using Al and P simultaneously (Al/P) was ineffective, while gettering using Al or P individually (Alum and Phos) was effective.

Cell Name	Split	Eff	V_{oc}	J_{sc}	FF
NREL-17-3	Alum	15.1	0.607	31.3	0.796
NREL-17-10	Phos	14.5	0.605	31.2	0.766
NREL-17-4	Al/P	12.4	0.580	29.0	0.737
NREL-17-5	None	12.6	0.577	30.4	0.714

Table 4. Recombination distribution (%) for HEM cells.

Cell	Split	V_{oc}		V_{mp}	
Name	Descr	n1	n2	n1	n2
NREL-17-3	Alum	95.4	4.2	75.4	22.2
NREL-17-10	Phos	93.6	5.6	51.3	40.6
NREL-17-4	Al/P	80.0	19.6	32.1	63.7
NREL-17-5	None	82.9	15.3	28.2	59.6

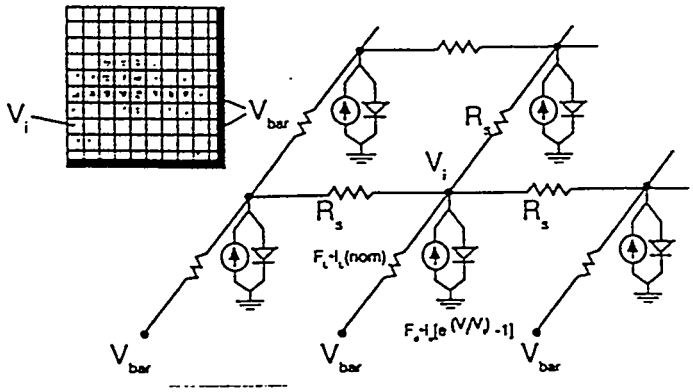
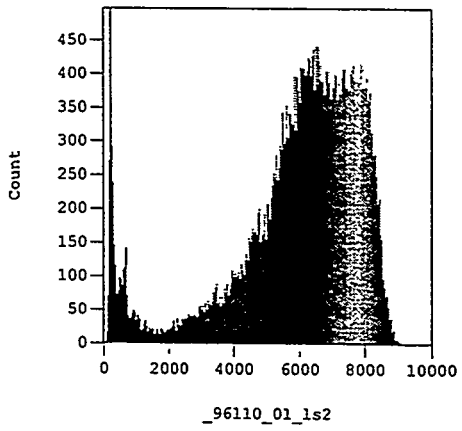
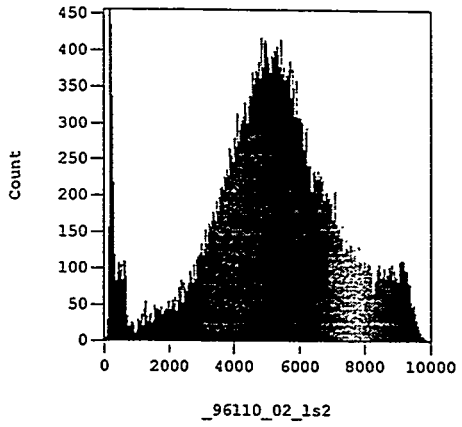


Figure 1. Network model of solar cell with areal inhomogeneities. The model assumes that the cell may be modeled as one-dimensional diodes connected in parallel by the emitter and grid on the front surface. The parameters of the one-dimensional diodes reflect the inhomogeneous properties of the solar cell. Note that only the dominant current component in the figure for clarity. From Sopori and Murphy [2].

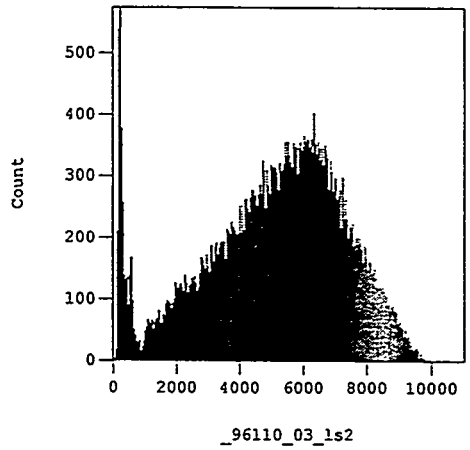
Figure 2. LBIC plots and histograms for ASE cells.



"High-performance" ASE cell.

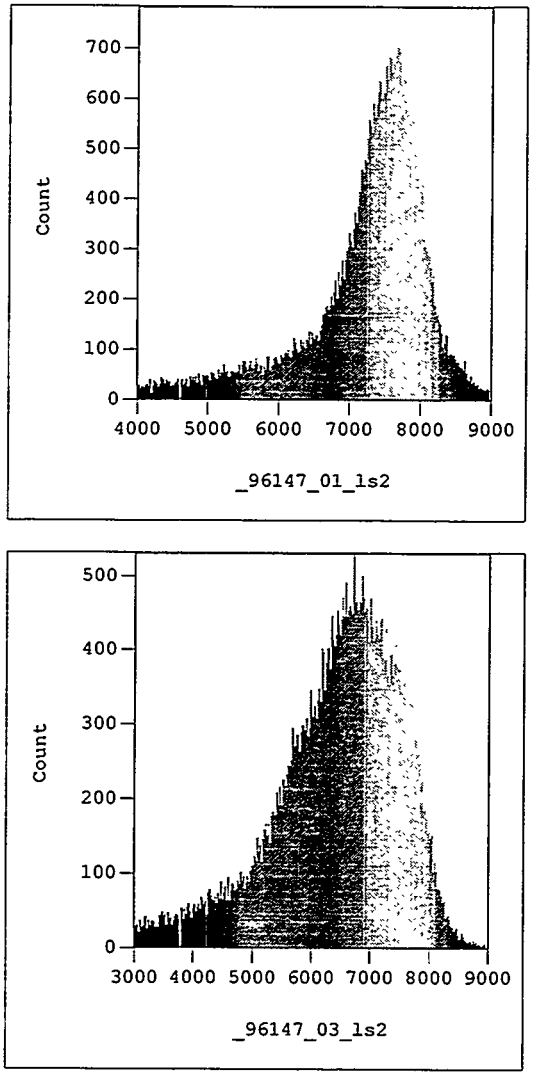


"Medium-performance" ASE cell.



"Low-performance" ASE cell.

Figure 3. LBIC histograms of gettered and non-gettered HEM cells, respectively.



BORON-DOPED BACK-SURFACE FIELDS USING AN ALUMINUM-ALLOY PROCESS

James M. Gee, Michel Bode, and Beverly Silva
Sandia National Laboratories*, Albuquerque, New Mexico 87185-0752

ABSTRACT: Boron-doped back-surface fields (BSF's) have potentially superior performance compared to aluminum-doped BSF's due to the higher solid solubility of boron compared to aluminum. However, conventional boron diffusions require a long, high temperature step that is both costly and incompatible with many photovoltaic-grade crystalline-silicon materials. We examined a process that uses a relatively low-temperature aluminum-alloy process to obtain a boron-doped BSF by doping the aluminum with boron. In agreement with theoretical expectations, we found that thicker aluminum layers and higher boron doping levels improved the performance of aluminum-alloyed BSF's.

Doped junctions on the back surface are a well-known technique to reduce back-surface recombination in silicon solar cells. These junctions are commonly known as back-surface fields (BSF). BSF's are of increasing importance because (1) manufacturers are using thinner substrates to reduce material and crystal-growth costs and (2) material quality is now high enough such that the back surface is a large source of recombination in present silicon solar cells [1].

Aluminum-doped BSF's can be formed at relatively low temperatures with easily applied aluminum paste and with a relatively low temperature alloy process. The physics of the alloy process and of the resulting junction have been studied extensively [2]. Boron-doped BSF's can potentially achieve superior results compared to aluminum-doped BSF's due to the higher solid solubility of boron compared to aluminum. A more heavily doped BSF is particularly important when using lower resistivity (<1 Ωcm) substrates (Fig. 1). Boron doping, however, has been difficult to implement cost effectively. Boron diffusions require high temperatures (>950°C) that are costly and frequently injurious to photovoltaic-grade silicon materials, while implantation of boron uses costly equipment with low throughput.

Lölgen *et al.* has described a potentially low-cost method for forming boron-doped BSF's using relatively low temperatures (<900°C) [3]. This process dopes an aluminum paste with boron. When the boron-doped aluminum paste is alloyed with the silicon, the boron dopes the regrown silicon at the higher solid solubility of boron compared to aluminum. The result is that a heavier boron doping is achieved with the low-temperature process of an aluminum alloy.

In this extended abstract, we report results of an experiment to examine aluminum-alloyed BSF's using sputtered boron-doped aluminum layers. Sputtered aluminum layers provide a more highly controlled environment (i.e., more uniform film with controlled composition) for examining the physics of the resulting junction compared to aluminum pastes. Aluminum sputtering targets that were doped with boron to 0.3 and 1% by weight were obtained from a commercial vendor. Pure aluminum layers were deposited by thermal evaporation. The alloys were performed in dry oxygen in a tube furnace for 30 minutes at 850°C. This step both alloys the BSF and grows a thin passivating oxide on the front surface of the solar cell. The cell fabrication sequence is presented in Table 1. The experiment varied both the aluminum thickness (1 and 10 μm) and the boron doping (0, 0.3, and 1%). The material was 320-μm 2-Ωcm float-zone silicon wafers.

A problem with tube-furnace alloys is the vertical configuration of the wafers. We found that the molten silicon eutectic would flow to the bottom of the vertical wafer – particularly on the wafers with the thick

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10-μm Al layers. This uneven thick Al deposit on the back surface caused problems with the photolithography processing, with the net result that the cells with the thick Al alloy have low fill factors due to discontinuous grids on the front surface. The variation in aluminum thickness also causes uncertainty in the data analysis since the precise thickness of the aluminum remaining in any particular region on the wafer is uncertain. The effect of the boron doping and aluminum thickness on BSF performance was monitored through cell V_{oc} and back-surface recombination velocity (S). S was estimated by analysis of the spectral data [4]. Table 2 presents the results.

Both increasing the thickness of the aluminum layer and the boron doping of the aluminum improved the BSF performance. The improved BSF performance is also evident in the internal quantum efficiency spectra (Fig. 2 and 3). Current experiments are performing the alloys with the wafers laid flat. The resulting alloyed layer is flat and has much improved morphology. The flat geometry might also improve the alloyed junction due to the improved morphology.

In conclusion, we performed preliminary experiments to examine boron-doped aluminum-alloyed BSF's. In agreement with theoretical expectations, the boron doping and aluminum thickness improved BSF performance.

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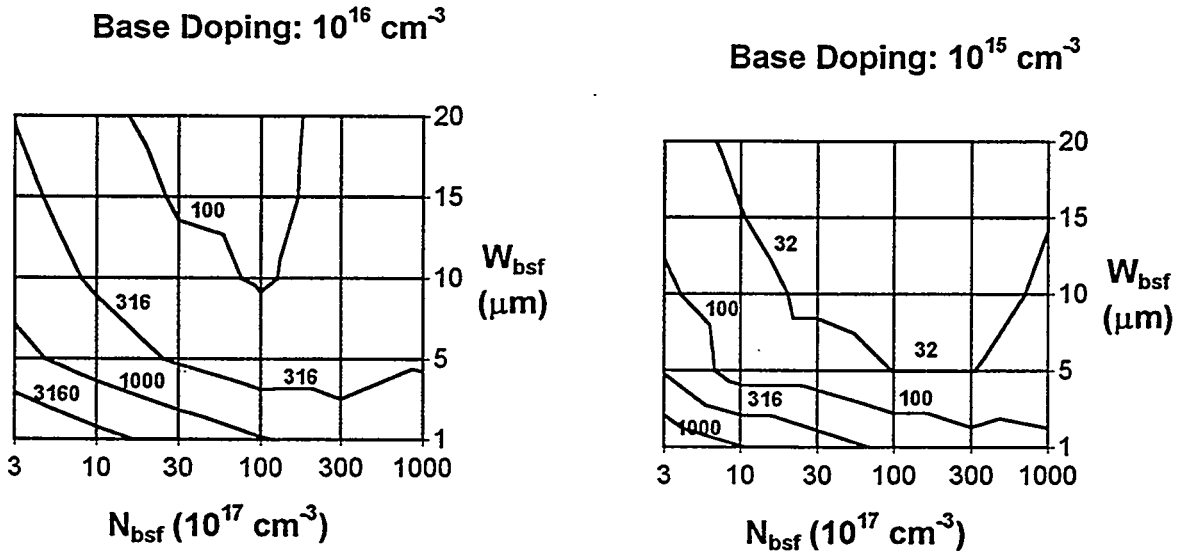

Figure 1. Calculated effective recombination velocity S at a pp+ interface as a function of the BSF thickness and doping level. The contours are S in cm/s. The calculations used PC1D and assumed a uniform doping profile for the BSF.

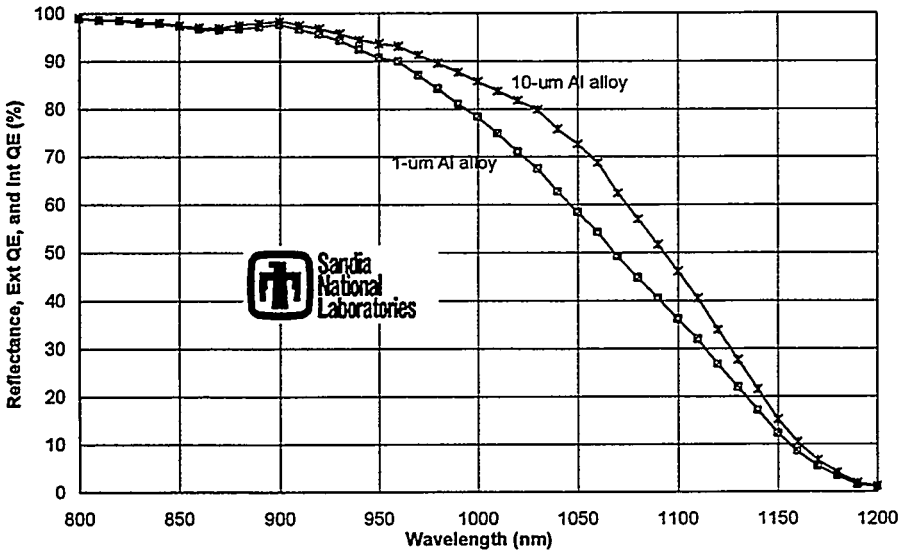

Figure 2. Internal quantum efficiency spectra illustrating the improvement of red response due to use of a thicker aluminum layer for the aluminum-alloyed BSF.

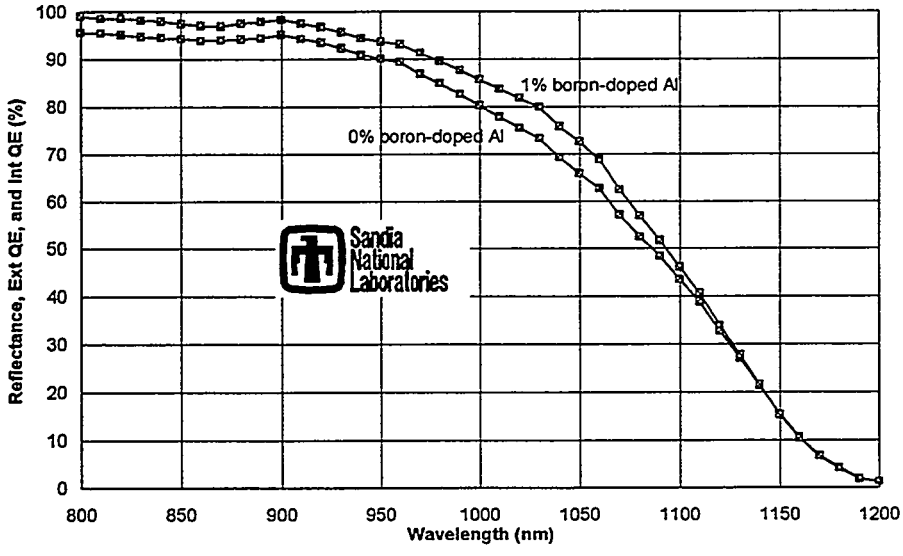

Figure 3. Internal quantum efficiency spectra illustrating the improvement of red response due to boron doping of the aluminum in an aluminum-alloyed BSF.

Table 1. Summary of cell fabrication sequence.

1. Wafer clean and etch.	8. Photoresist and expose on front.
2. Wafer label.	9. Contact etch, evaporate TiPdAg, and liftoff.
3. CVD oxide on back surface.	10. Evaporate Al on back.
4. $POCl_3$ diffusion.	11. Sinter in forming gas, 400°C, 20 min.
5. HF etch.	12. Ag plate grid on front.
6. Aluminum deposition on back surface.	13. TiO_2/Al_2O_3 double-layer antireflection coating.
7. Dry Oxidation, 850°C, 30 min.	14. Laser-scribe grooves and cleave 42-cm^2 cells from 100-mm diameter wafers.

Table 2. Results of experiment that examined aluminum thickness and boron doping on aluminum-alloyed BSF performance. The cells have planar surfaces and are 42 cm^2. The effective diffusion length and internal collection efficiency (L_{eff} and η_c) are parameters from the analysis of the internal quantum efficiency spectra, and are used for the calculation of the bulk diffusion length L and back-surface recombination velocity S [4]. R_b is the estimated back-surface reflectance. *Thick* refers to the aluminum thickness, and *Boron* refers to the boron doping. The BSF's using 10-μm Al layer doped with 1% boron improved the V_{oc} by about 24 mV and reduced S from around 1700 cm/s to below our measurement resolution compared to BSF's using 1-μm Al layer without boron doping.

Cell Name	Boron %	Thick μm	V_{oc} volts	L_{eff} μm	η_c %	R_b %	L μm	S cm/s
BorBSF17-6	0	1	0.606	338	62	74	372	1530
BorBSF17-8	0	1	0.606					
BorBSF17-28	0	1	0.604	396	64	77	536	1811
BorBSF17-16	0.3	1	0.609	428	68	74	531	
BorBSF17-19	0.3	1	0.606					1304
BorBSF17-20	0.3	1	0.604	435	67	75	603	1492
BorBSF17-13	1	1	0.610	459	68	72	668	1406
BorBSF17-27	1	1	0.607	377	62	74	361	702
BorBSF17-32	1	1	0.604					
BorBSF17-7	0	10	0.614	601	77	75	690	673
BorBSF17-18	0	10	0.614					
BorBSF17-17	0.3	10	0.608	666	81	75	551	318
BorBSF17-2	1	10	0.630					
BorBSF17-4	1	10	0.627	1055	94	70	536	0
BorBSF17-10	1	10	0.629	783	88	71	466	0
Factor Average		<1>	0.606	405	65	74	512	1374
		<10>	0.620	776	85	73	561	248
Split Averages	0	1	0.605	367	63	75	454	1670
	0.3	1	0.606	431	65	75	510	1534
	1	1	0.607	418	65	73	515	1054
	0	10	0.614	601	77	75	690	673
	0.3	10	0.608	666	81	75	551	318
	1	10	0.629	919	91	71	501	0

Industrial process for bulk and surface passivation of multicrystalline silicon solar cells.

F. Duerinckx, R. Einhaus, E. Van Kerschaver, J. Szlufcik, J. Nijs, R. Mertens.
IMEC, Kapeldreef 75, B- 3001 Heverlee, Belgium.
M. Roy, S. Narayanan
Solarex, 630 Solarex Court, Frederick, Maryland 21703, USA.

Abstract

This work presents a simple screen printing solar cell process based on firing the front contacts through a silicon nitride (SiN_x) layer deposited by direct plasma enhanced chemical vapour deposition (PECVD). This sequence of only six steps results in an excellent front surface and bulk passivation. Efficiency improvements up to 1.5% with a state-of-the art processing sequence were obtained on Solarex multicrystalline material. Independently confirmed efficiencies of almost 16% were reached. First indications of the excellent passivation quality of SiN_x deposited by direct PECVD on p-Si are given.

1. Introduction.

One of the impediments for the industrial production of high efficiency multicrystalline silicon solar cells is the lack of a cost effective method to achieve an efficient surface and bulk passivation. A possible solution lies in the use of silicon nitride deposited in direct plasma enhanced chemical vapour deposition (PECVD). A silicon nitride layer serves as an antireflection coating passivating the surface and also the bulk if an appropriate annealing step is applied[1 - 3]. In this paper the PECVD silicon nitride is incorporated in a simple and high throughput screen printing process and the effects of surface and bulk passivation by hydrogen are demonstrated and analysed. Solarex material has been chosen for this study because it is representative for present day multicrystalline silicon substrates used by the PV industry.

2. Process sequence.

The key towards a cost effective and efficient hydrogen passivation process is to fire the screen printed front side grid through the PECVD silicon nitride antireflection layer. Figure 1 describes the process as it is developed and optimised in IMEC[4].

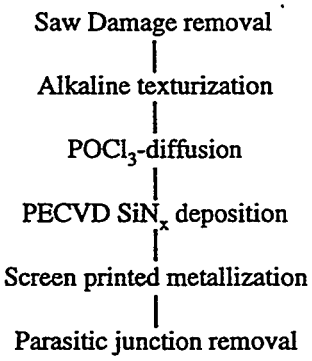

Figure 1 : 'firing-through-SiN_X' process sequence

It consists basically of only six steps: First, after a removal of the saw damage and a texturization using NaOH, the emitter is formed by POCl3-diffusion to reach a sheet resistance around

45 Ω/sq. This is followed by a silicon nitride deposition in a direct PECVD-system capable of depositing on 84 100 cm^2 wafers at once. Then the contacts are screen printed on the front side and back side of the wafer and co-fired in an IR-furnace. Hereby, the front contact is fired through the silicon nitride layer to make contact with the underlying emitter. This process results in solderable contacts since no ARC-layer is covering the busbars at the end of the process. Moreover, due to the elevated temperatures used for the firing-through process, the screen printed aluminium on the back side alloys with the silicon and forms a back surface field. The most important factor however is the fact that hydrogen is released from the SiN_x layer during the firing step of the metal contacts which results in an excellent surface and bulk passivation. The surface damage created during the SiN_X-deposition is annealed during this step. However, at the same time, the vacancies resulting from the direct deposition process can help in the indiffusion of hydrogen into the bulk of the material [5]. In general, the above process has only one high temperature step (the diffusion). This means only one cleaning step is required for the whole process. Nevertheless, this simple process incorporates a BSF and an effective surface and bulk passivation as will be shown below.

3. Process application on different material qualities

The process as described above was compared to Solarex's baseline production process which was used as a reference. The baseline process includes an homogeneous emitter, TiO_X as ARC and a back surface field. Both processes were applied on neighbouring Solarex substrates of different quality : The first batch of wafers was standard quality material while the second batch was of lower quality. The results are shown in the following tables :

Table 1 : Cells made on standard quality substrates

Process	Jsc (mA/cm^2)	Voc (mV)	FF (%)	Eff. (%)
Baseline process	30.1	596	75.0	13.5
Firing through SiNx-process	31.5	613	76.3	14.7

Table 2 : Cells made on lower quality substrates

Process	Jsc (mA/cm^2)	Voc (mV)	FF (%)	Eff. (%)
Baseline process	28.0	585	74.9	12.2
Firing through SiNx-process	30.6	600	74.5	13.7

From these results, it is clear that the substrates processed with the firing-through-SiN_X sequence give much higher efficiencies compared to the standard process. This difference becomes larger for lower quality material. The SiN_X-cells of table 2 (lower quality material) even reach a higher efficiency than the cells of table 1 (good quality material) made with the standard process.

The higher Voc and the current increase for the SiN_X-cells can be explained by the hydrogen passivation due to the diffusion of hydrogen from the silicon nitride layer into the cell during the contact firing.. Laser Beam Induced Current (LBIC) measurements performed at Sandia National Laboratories have shown the uniform passivation of the surface and the upper part of the bulk, independently of the grain orientation. The worse the starting quality of the material, the more this in-situ hydrogenation will be needed to obtain good cells. In fact, the temperature treatment of the silicon nitride can replace long hydrogenation steps which can never find a place in an industrial production line. Thanks to the in-situ annealing of the surface damage, resulting from the ion bombardment during the SiN_x deposition, it is possible to remove the thermal oxidation from the process sequence. If the silicon nitride layer would not be treated with a high temperature step, an underlying oxide would be needed as a barrier to prevent an extended damaged surface layer.

The use of SiN_X not only increases the efficiency of the cells but, since high efficient cells can also be obtained on lower quality material, it can also enhance the overall material yield. This is

important since the crystallisation cost accounts for a significant portion of the total cost of the finished product.

To indicate the extent of the passivation effect coming from the SiN_X-process, figure 2 shows the IQE of two cells made on lower quality material. Both cells were processed at IMEC using firing through ARC-processes. The ARC's were respectively TiO_X and SiN_X.

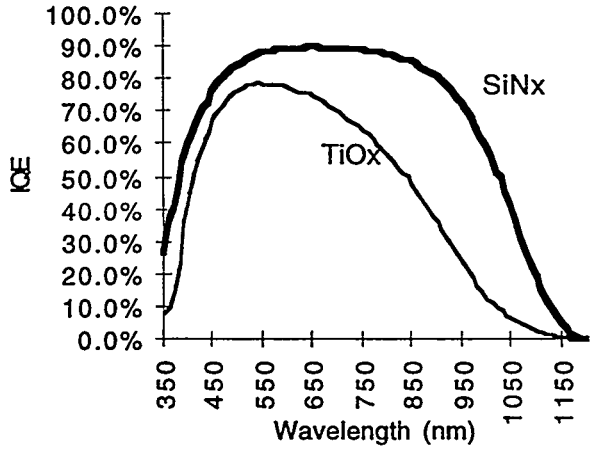

Figure 2 : IQE comparison of cells made by firing through SiN_X and TiO_X on lower quality material (cells processed at IMEC)

4. Optimised process sequence on high quality material

The firing-through-SiN_X process sequence, including the optional oxidation step, was applied on a batch of good quality Solarex material. The sheet resistance of the $POCl_3$-diffused homogeneous emitter was 50 Ω/sq. An optimised pattern for the front side contacts was used. The busbars were tabbed to decrease the series resistance. The average results of these 12 cells are shown in table 3. Two cells were independently measured at Sandia. On one of them, a second ARC (MgF_2) was applied. Efficiencies of 15.4% in the case of SLARC and 15.8% in the case of DLARC have been measured. These results are amongst the highest measured on large area, alkaline textured, multicrystalline screen printed cells.

Table 3 : Average result of 12 screen printed cells on good quality Solarex material with homogeneous emitter using the SiN_X-process (area : 96 cm^2)

Jsc (mA/cm2)	Voc (mV)	FF (%)	Eff. (%)
32.1	610	77.8	15.2

Table 4 : Results of homogeneous emitter cells on Solarex material (confirmed at Sandia) using the firing though SiN_X-process (area : 96 cm^2)

ARC	Jsc (mA/cm2)	Voc (mV)	FF (%)	Eff. (%)
Single (SiN_X)	32.3	615.7	77.9	15.43
Double (SiN_X + MgF_2)	33.0	613.4	77.7	15.79

5. Application of silicon nitride as back side passivation

The general trend in the PV industry is to reduce the wafer thickness due to the high cost of the silicon material. Till now, most cell producers use a gridded Ag/Al or an full Al back contact scheme. For thinner cells, back side recombination will become a critical issue which necessitates an adequate

back surface passivation. A screen printed Al BSF is also no solution for thin cells due to warping of the wafers.
An elegant and effective solution is the use of PECVD-SiN_x for back surface passivation. Figure 3 shows the effective recombination velocities of silicon nitride deposited by direct PECVD as a function of the applied bias light. The material used was 7 Ωcm FZ material with a bulk lifetime of 700 µs. Low recombination velocities around 30 cm/sec were obtained indicating the good surface passivation of this direct plasma technique after annealing the nitride at high temperature for a short time like for a contact firing scheme as described above. This step can also result in an effective bulk passivation from the back side. Unannealed silicon nitride gave recombination velocities two orders of magnitude higher due to the surface damage from the deposition.

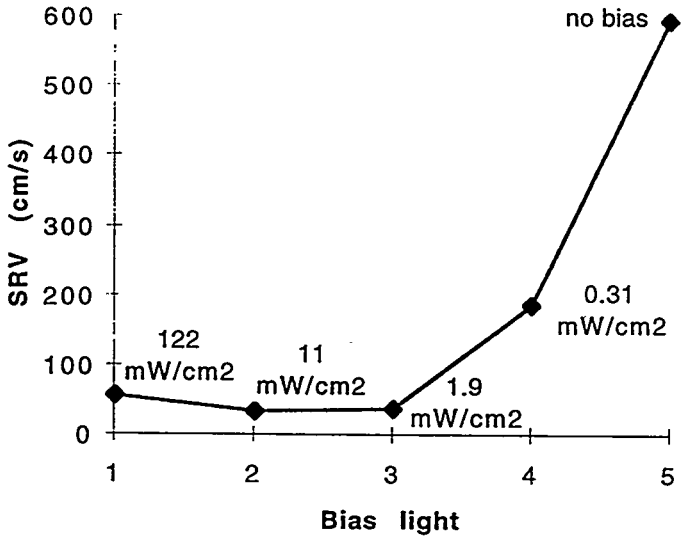

Figure 3 : Surface recombination velocities for annealed SiNx deposited by direct PECVD as a function of bias light

6. Conclusion

The advantages of the implementation of a direct PECVD SiN_x deposition in an optimised screen printing process sequence have been demonstrated. Confirmed efficiencies on Solarex material of almost 16% have been reached with a very simple process consisting of only 6 steps. This strengthens the need for high throughput PECVD systems which should be developed for industrial use since the process not only increases the efficiency but can also increase the material yield. Direct PECVD-SiNx seems the logical choice since it combines ARC, surface and bulk passivation in one step unlike other passivation techniques like plasma hydrogenation and ion implantation. Compared to remote plasma systems, it has the advantage of better uniformity and being easier to upscale while giving as good passivation properties. The development of high throughput equipment, not only for plasma passivation, but also for other innovative processing steps, will become a major topic for future solar cell R&D.

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Epilift Silicon Solar Cells

Andrew Blakers, Klaus Weber and Kylie Catchpole
Engineering Department
Australian National University
Canberra 0200 Australia
Fax: 61 6249 0506
email: Andrew.Blakers@anu.edu.au

Abstract

Silicon wafer costs are a large proportion of the cost of a commercial PV module. We have developed a technique for the preparation of single crystal silicon sheets of any size, shape or thickness that eliminates the cost of wafer slicing and reduces consumption of pure silicon by a factor of five to ten. The process, called *Epilift*, entails the growth of an epitaxial layer on a single crystal silicon wafer followed by its detachment. The substrate can be recycled indefinitely through further growth and detachment cycles.

Thin Crystalline Silicon Solar Cells

The cost of fabricating a c–Si wafer comprises the cost of pure silicon, the cost of growing an ingot and the cost of slicing the ingot into wafers. During slicing up to half of the silicon is lost as sawdust. Further silicon is wasted if single crystal round wafers are squared up. In addition, silicon wafers are generally 300–500 μm thick for mechanical strength, whereas 10–100 μm is all that is needed for optical and electronic purposes. The realisation that c–Si can be used in a thin film form (10–100 μm) with the aid of light trapping has led to considerable interest in the area.

An important choice for the fabrication of a thin film silicon cell is the choice of a suitable substrate on which to deposit the active silicon layer [1]. The substrate must be cheap, able to withstand all the temperatures to which it is exposed during processing, not cause thermal expansion mismatch cracking and permit the growth of silicon layers of sufficient quality and at a sufficient speed for photovoltaic purposes. Ideally it should enable the incorporation of light confinement into the device structure. Several different options are currently being investigated, including glass, ceramic and low cost crystalline silicon.

Thin crystalline silicon deposition processes reported to date result in silicon layers that are multicrystalline, leading to inhomogeneous material with many defects and at most moderate material quality. This limits the efficiency potential of solar cells. None of the substrates mentioned above offer the optimal combination of high material quality, low cost and effective light trapping.

A number of techniques have been developed for the separation of semiconductor layers from a substrate and subsequent reuse of the substrate. These techniques are widely used for the GaAs family of materials. One technique is to use the very large etch speed ratio of AlGaAs and GaAs. AlGaAs is grown on a GaAs wafer followed by a GaAs layer. Black wax applied to the upper GaAs layer places it under tension. The structure is then immersed in a suitable etchant, which etches AlGaAs laterally without etching either GaAs layer. The purpose of the black wax is to curl up the upper GaAs layer to allow easier exchange of etchant and reaction products. After a long period (depending on the width of the structure) the top GaAs layer floats off. The process is not suitable for silicon because no known silicon etchant has the large selectivity that is available for the GaAs/AlGaAs system. To date, no suitable non–silicon compound has been developed that can act as an intermediary layer, analogous to AlGaAs. Although CaF_2 can be deposited epitaxially on silicon, and silicon on CaF_2, the procedure is not well developed and expensive. Silicon grown on CaF_2 has a very high defect density.

In the CLEFT process, a masking layer is deposited on a single crystal substrate, usually GaAs. Line openings formed in the masking layer provide the seeds for subsequent epitaxial growth. The epitaxial layers overgrow the line seed openings laterally and eventually impinge on each other to produce a continuous epitaxial film. The masking layer is completely buried beneath the epitaxial layer. The epitaxial layer is then attached to a suitable secondary substrate. If the regions where the epitaxial layer is attached to the substrate are sufficiently narrow, and if the adhesion of the epitaxial layer to the masking layer is sufficiently weak, the epitaxial layer can be cleaved off the substrate. The process has not been successfully applied to silicon.

A practical method of single crystal wafer manufacture that involved no slicing, that produced wafers 50–100 microns thick, and that could yield square (or any other shape) wafers of arbitrary size and thickness would eliminate most wafer costs. The *Epilift* technique developed at ANU [2] is such a technique.

Epilift Growth

The *Epilift* technique is illustrated in Figure 1. One possible set of process steps are as follows:

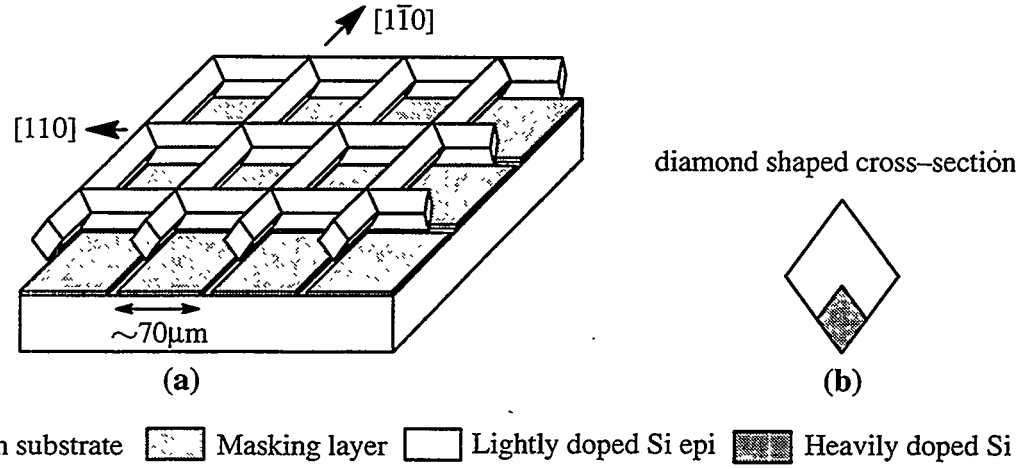

Figure. 1: The *Epilift* process. (a) The structure following deposition of the epi layer on a (100) oriented single crystal substrate; (b) Cross section through the epitaxial layer.

i) A masking layer such as Si_3N_4 is deposited and patterned on top of a (100) single crystal silicon substrate, so that the substrate is only exposed along lines (typically 5 μm wide and 70 μm spaced) which form a mesh pattern and run along the <110> directions of silicon. The masking layer prevents nucleation of silicon anywhere except along these lines of exposed silicon.

ii) An epitaxial layer is grown on the wafer by LPE. Silicon nucleates out of the lines and forms a continuous mesh. Due to the particular stability of the Si {111} planes, faces with near (111) orientation develop. As a result, the epilayer displays a diamond shape in cross section. The initial part of the epilayer can be grown heavily doped while the subsequent layer is more lightly doped, although this is not necessary.

iii) As growth is continued, the epilayer progressively overhangs the areas of the wafer covered by the masking layer, leaving a series of holes of decreasing size in the epitaxial film. Growth is terminated just before these holes have closed up. Any metallic solvent residues can be removed by immersing the wafer in a suitable acid which does not attack silicon. It is possible to texture the substrate prior to use to virtually eliminate spaces where solvent residues could gather.

iv) To detach the layer from the substrate, the wafer is immersed in an etchant which etches heavily doped silicon faster than lightly doped silicon. Due to the narrowness of the epilayer attachment points, and the fact that the initial part of the layer was grown heavily doped, the etchant rapidly detaches the layer from the substrate, This leaves the substrate ready for the growth of

another layer and the epilayer ready for processing into a solar cell. If the attachment points are sufficiently narrow and the grown layer sufficiently thick then there is no need for the initial growth to be heavily doped. Electrochemical etching based on pn junctions can also be used to undercut the attachment points while avoiding loss of silicon from the grown layer.

The *Epilift* technique is easy to perform, and, in fact, worked well first time. A 20 μm thick layer with an area of about 2 cm^2 was detached from a (100) substrate in about 20 minutes.

The big advantage of the *epilift* technique over liftoff techniques developed for GaAs is that the etchant is brought into contact with the silicon to be etched at a large number of points simultaneously through the holes in the epi layer. The substrate is not damaged by the LPE growth or subsequent processing. The Si_3N_4 masking layer can be used for many growth cycles before being renewed. If desired, the access holes for the etchant can be made in the substrate instead. This would allow growth of the epi layer to continue until it formed a continuous surface. The thickness of the epi layer can be varied by simply changing the spacing of the lines in the masking layer.

Liquid phase epitaxial growth of the silicon in the *epilift* technique has the advantage that nucleation occurs only on exposed silicon, and not on the masking layer. LPE is known to produce very pure quality silicon with low defect densities and large minority carrier lifetimes [3]. The pattern of exposed silicon created in the masking layer can be designed so that the number of holes required to give the silicon etchant access to the 'roots' of the epi layer is minimised. In fact, a suitable arrangement of mirrors and or total internal reflection from the air/glass interface of the encapsulating package can be used to avoid the need to close the holes at all while still minimising loss of light from a solar cell.

While (100) substrates are interesting for solar cell applications, (111) substrates could have very interesting applications to microelectronics. This is because lateral growth rather than vertical growth will dominate. Previous work on the LPE growth silicon on (111) substrates has concentrated on growth from individual lines [4]. Growth from a connected mesh could form a nearly continuous, thin, defect free growth over the masking layer with obvious device applications. The difference between impingement of growth fronts from disjoint nucleation areas and the filling–in of a mesh of nucleation lines is of considerable scientific interest.

A recent paper by Rolf Brendel at the 14th EC PV Conference in Barcelona [5] outlines a very good idea that resembles the *Epilift* process in that large single crystal sheets can be produced. In this process an epitaxial layer is grown on a layer of porous silicon grown on a single crystal wafer. The porous silicon is then destroyed by immersion in an ultrasonic bath, allowing the epilayer to be floated off. The quality of silicon grown on porous silicon needs to be checked. Aspects of the two processes could be combined. For example, detachment of the *Epilift* mesh could be made easier if the epitaxy was grown on porous silicon.

Epilift Solar Cells

Development of new techniques such as low temperature surface passivation and grain boundary passivation, as is required for most thin c–Si cell technologies, is costly and risky. A major advantage of the *epilift* process, in addition to the single crystalline nature of the layers, is that standard cell processing can be used. Well known techniques for diffusions, minority carrier lifetime preservation, surface passivation and metallisation are available, and there are no unusual restrictions on process temperatures or ambient. There are, however, some significant potential problems to be resolved as well as several attractive features to be exploited.

Texturing is a natural consequence of the *epilift* process on (100) substrates. The shape of the epilayer is such that there will be low reflection losses and good light trapping. The cost of texturing is eliminated from cell processing.

The presence of holes in the epilayer as a natural consequence of the growth sequence opens the way for several attractive solar cell designs. For example, an n^+ diffusion can be made into

the front surface, on parts of the rear surface and down the holes. Both the n and p contacts can then be located on the rear surface of the cell, virtually eliminating losses associated with the metal fingers. Lateral resistance loss in the emitter can also be virtually eliminated by making the holes on a spacing of 0.5 mm or less. The holes themselves need occupy only a very small proportion of the silicon surface, and can have reflectors positioned behind them to avoid loss of light. Such a design would be useful for concentrator cells. It is also attractive for the fabrication of very large area terrestrial cells (20–30 cm diameter). Finger shading and resistance losses would normally be unacceptable in a cell of this size. The idea of using holes to conduct photocurrent from the front of the cell to the rear is not new. However, the ease with which this can be accomplished using the *epilift* technique compared with using a laser or other technique makes it practical.

The large diffusion lengths observed in LPE grown silicon also allows both contacts to be moved to the rear of a sufficiently thin cell even if there are no holes to conduct photocurrent from front to back (eg if the access holes for the silicon etch used to detach the epilayer are located in the substrate rather than the epilayer). The naturally textured surface means that the substrate will be quite thin in many places. This means that the very long diffusion lengths normally needed to make a back contact cell perform well are not required.

The fact that the epilayer is thin opens the possibility of monolithic series connection of cells. The lateral resistance of a 50 micron thick wafer is ten times higher than that of a 500 micron thick cell. This means that the area of silicon lost as an isolation layer between individual subcells is reduced by a factor of ten. It is possible to alter the nucleation pattern to nearly eliminate undesired lateral conduction.

Much of the cell processing can be performed prior to detachment from the substrate in order to reduce cell breakage. For example, texturing, pn–junction formation and surface passivation can all be completed prior to epilayer detachment, leaving only metallisation to be performed after detachment. This would allow a high yield of thin cells.

Cell fabrication processes on *Epilift* substrates are being developed and solar cells should be available soon.

Conclusion

If crystalline silicon is to compete against non–silicon materials then advantage must be taken of its high efficiency potential in order to reduce Balance of Systems costs. Given the single crystallinity of the layer, a realistic goal for *Epilift* cell efficiency is 20%. The high efficiencies possible in principle using processes such as *Epilift* or the process introduced by Brendel [5] give them a major advantage over deposition of multicrystalline silicon onto a foreign substrate.

Acknowledgments

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PV Optics: Cell and Module Design

Bhushan L. Sopori, Jamal Madjdpour, and Chris Gaylord
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

We have developed an easy-to-use software package called *PV Optics* that accurately models the optics of any solar cell or module. *For example,PV Optics:*

- accommodates device design with as many as three active semiconductor layers plus a glass cover, encapsulation, antireflection (AR) coating, buffer, and metal backing
- assesses the light-trapping impact of nonplanar (textured or intentionally rough) interfaces of any of the device layers
- calculates interference effects (caused by the coherence of light) of very thin layers such as antireflection coating or thin-film semiconductor materials
- accurately calculates reflection and absorption from reflective metal backings
- selectively applies wave optics only where needed to address interference of coherent light in thin layers, using ray optics elsewhere to keep the computer calculation time reasonable
- with a Windows software system, allows you to continue to use other computer functions while the analysis is proceeding
- includes default values for refractive index and extinction coefficient for crystalline silicon, amorphous silicon, glass used for encapsulation, encapsulation materials such as EVA, and a buffer layer
- calculates maximum achievable current density (MACD in mA/cm^2) for each semiconductor layer, providing a benchmark for cell performance
- for most devices, automatically and clearly plots:
  - reflection, transmission, semiconductor absorbance, and metal absorbance, each as a function of wavelength
  - (for multijunction devices) absorbance for each separate layer plus total absorption
  - absorbance by wavelength for typical sunlight (AM1.5) - predicting short circuit current density
  - photon absorbance as a function of depth within the semiconductor layer—facilitating selection of optimum thickness
- provides output that can be directly input into graphic software such as Quattro Pro or Delta Graphs for manipulation of graphic display or electronic analysis software such as AMPS or PC1D for electronic modeling.

PV Optics Software (Version 1) for the PC comes on a single 3-1/2 floppy disk.
The software requires an IBM compatible PC/60 MHz (or a higher speed), a minimum of 8 MB RAM, windows, a VGA monitor, and a color printer (can also operate with a B&W printer).

Selection of the Device Configuration

PV Optics Version 1 starts with a generalized device configuration, from which one can select a desired device configuration. Your device may consist of glass, encapsulation, anti-reflectant coating, three semiconductors, a buffer and metal. The device configuration choice is made by simply deleting - with a click of a mouse - portion of the device configuration that does not correspond to your device.

The software provides you with default values for the interface type, thickness in microns, n and k of each region. The default values correspond to standard materials used in PV manufacturing. You can use the default values or click on the area that you wish to change. The anti-reflection page provides you with the default values for the interface type, n1, k1, thickness1, n2, k2, and thickness2 for a 2-layer AR coating. n1, n2 are the refractive indices and k1, k2 are the extinction coefficient. The selection of semiconductor page provides you with a choice of upto three-junction cell, and you can select the material "Silicon" or "Amorphous-Silicon," "Amorphous-Silicon Top," "Amorphous-Silicon Middle," or "Amorphous-Silicon Bottom." Additional semiconductor data can be incorporated at your request.

Results are displayed as Graphs

The seven types of graphs include: 1.) Reflectance / Transmittance,
2.) Absorbance, 3.) Weighted Absorbance, 4.) Photon Flux, 5.) Reflectance/Transmittance (Non-Coherent), 6.) Reflectance /Transmittance (Coherent), and
7.) Weighted Absorbance.

The graphs may be saved as a bit-map (.bmp) file by selecting "Export" from the file menu. This will bring up the files window and you will be able to select drives, directories, and filenames. The files window will also ensure that you give the graph a designated extension of ".bmp". Once you have selected or entered the filename that you wish to use click on the "OK" button. Make sure that you are in the directory where you wish to save the file. If you click on the "OK" button while the filename still shows "*.bmp", then the window will show you a list of only those files that have been saved as bit-maps.

LOW LEVEL CU CONTAMINATION STUDIED BY TRANSIENT ION DRIFT.

T.Heiser, S.Mchugo, H.Hieslmair, C.Flink, A.Istratov, and E.R.Weber
Department of Material Science and Mineral Engineering, University of California at Berkeley,
1, cyclotron road, Berkeley, CA 94720

INTRODUCTION

Although Cu is one of the major metallic contaminants in silicon, its properties in connection with gettering procedures or device failures are still a subject of intense research efforts. Numerous deep levels found in Cu doped silicon[1-3] were shown to be affected by defect reactions. The thermal history of the sample plays thus a crucial role in the electrical activity of the Cu impurity. Up to now, no data exist which could firmly establish the level of Cu contamination tolerated by most electronic or photovoltaic devices. Moreover, as the concentrations of the Cu induced deep levels are generally much lower than the total Cu amount in the material, the highly sensitive electrical characterization techniques are inadequate to monitor low Cu concentrations in silicon. Gettering studies and bulk contamination studies have thus to rely on less sensitive techniques like Secondary Ion Mass Spectroscopy or Atomic Absorption Spectroscopy.

Quantitative information about the Cu solubility and diffusion coefficient in silicon were obtained by Hall and Racette[4] already in 1964, using the radioactive copper isotope Cu^{64} as a probe. From the dependence of the copper concentration on the doping level they concluded that the ratio of substitutional to interstitial solubility at the annealing temperature is of the order of 10^{-4}, and that the interstitial copper (Cu_i) behaves as a mobile singly charged donor. The donor behavior of Cu_i is consistent with drift measurements carried out by Prescha et al[5] and Mesli et al.[6], where low temperature drift of Cu_i ions in the depletion region of a Schottky barrier was observed by capacitance voltage measurements.

More recently room temperature transient capacitance changes were observed in p-type silicon samples following copper contamination at high temperatures and quenching, and were attributed to interstitial copper drift.[7] In this work, we show that these 'transient ion drift' (TID) induced capacitance signals can be used to detect copper contamination in p-type silicon with a detection limit of the order of $10^{11}cm^{-3}$.

TRANSIENT ION DRIFT ANALYSES

The differential capacitance of a reverse biased Schottky barrier depends on the charge distribution in the depletion region. In the presence of mobile interstitial copper ions, this charge density is modified by the drift of Cu_i^+ ions in the electric field. When a reverse voltage is applied to the Schottky barrier, the initial uniformly distributed Cu_i impurities will be swept out towards the bulk affecting the barrier capacitance. If the reverse bias is applied for long enough times, no Cu_i will be left in the depletion region. After subsequent reduction of the applied voltage, Cu_i diffuses back toward the surface according to Fick's law. This leads, after an appropriate delay, to a uniform distribution. This drift-diffusion cycle can be repeated periodically as long as copper atoms remain interstitially dissolved. The capacitance time dependence can be found by solving the coupled diffusion and Poisson equations.[8] Numerical solutions of the Cu_i redistribution and the resulting capacitance signal, are shown in Fig.1, and compared to experimental data.

The calculations were performed assuming a diffusion potential of 0.6V, a reverse bias of 5 V, an initial uniform copper concentration of $10^{14}cm^{-3}$ and an boron density of $2\cdot10^{15}$ cm^{-3}. In these calculations, Cu - Boron pairing was not taken into account. The experimental signal was obtained at room temperature at a reverse voltage of 5V, after having reduced the voltage to zero for several seconds. As shown in Fig.1, a good agreement is found if we assume a Cu_i diffusion coefficient of $3\cdot10^{-8}cm^2s^{-1}$.

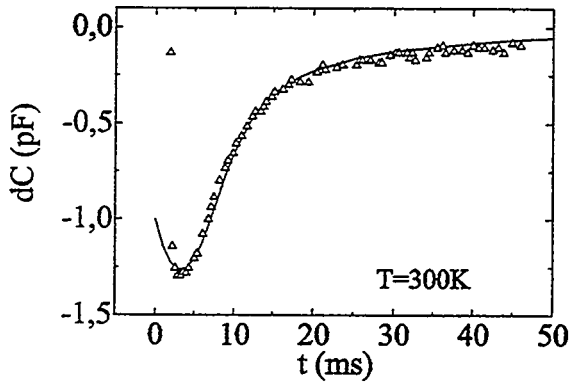

Fig.1 : Comparison between calculated (solid line) and experimental (triangles) capacitance signal.

QUANTITATIVE COPPER DETECTION

The use of TID for quantitative copper detection in silicon is only possible if the ratio of interstitial to total copper in the sample is known. This information can be obtained by comparing the TID results to the Cu solubility at the in-diffusion temperature. To investigate this question, we used both, B-doped and Al-doped samples, grown by Wacker Chemitronic with a resistivity between 2-15 Ω cm. Two types of sample preparation were performed. On the first set of samples, a 100 nm thick Cu layer was deposited by sputtering, followed by a thermal annealing at 800°C for 30 minutes. This annealing step was found to be necessary to avoid the in-diffusion barrier of native oxide and allow reproducible results. The samples were then slowly cooled to a second temperature T, and after another 30 minutes, they were quenched into ethylene glycol to prevent precipitation. The temperature T was varied between 450°C and 800°C. This step allows the copper concentration to reach the solubility limit at temperature T. The second set of samples were Cu implanted at 150 keV, with a dose of $10^{17}cm^{-2}$. Such a high dose was found to be necessary to saturate the implantation induced defects with Cu atoms.[9] The samples were then annealed for two hours at a temperature T between 450°C and 600°C and quenched to room temperature. As interstitial copper is unstable at room temperature, the signal amplitude decreases with a time constant of about several hours in B-doped material. In Al-doped material, acceptor-copper pairing increases the Cu_i 'lifetime' to above 24 hours. As a consequence, the samples were stored in liquid nitrogen before and after the Schottky barrier preparation. In B-doped material, room temperature precipitation kinetics were performed on each sample in order to evaluate the loss of Cu during the sample preparation. Fig.2 shows the as-quenched Cu_i concentration determined by TID on both sets of samples. For temperatures higher than 600°C, the concentration is temperature independent, while for lower temperatures it decreases exponentially. The same behavior is observed for all types of sample preparation and acceptors.

Also shown in Fig.2 are data on Cu solubility in silicon measured by Hall and Racette.[4] The good agreement found between Hall and Racette's data and ours below 600°C lead us conclude that most Cu atoms remain interstitially dissolved after quenching from temperatures lower than 600°C. In other words, the quenching procedure is fast enough to impede significant precipitation during cool down. Since precipitation is triggered by supersaturation , we expect that after annealing and quenching from even higher temperatures, most Cu atoms will be detected by the TID technique, if the concentration does not exceed the solubility at 600°C. It should be noted that this solubility is close to the acceptor concentration in our samples and that for higher doping levels we found an increase of the highest measurable Cu concentration.

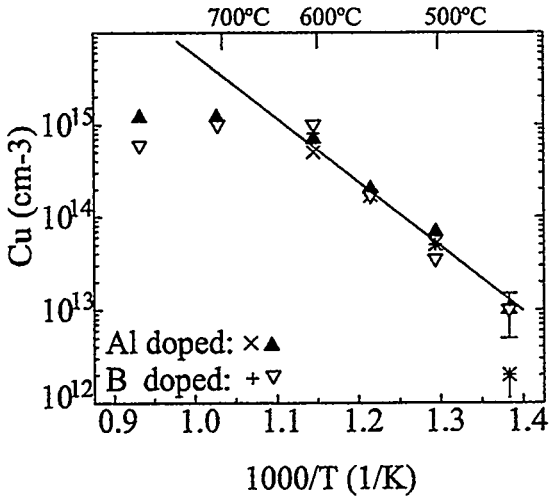

Fig.2 : As-quenched Cu_i concentration measured by the transient ion drift method, as a function of annealing temperature for Al and B doped samples. The Cu source was either from an implanted layer (+), (×), or from a sputtered Cu layer (▲), (▽). The solid line represents the solubility limit of Cu in Si.[4]

We would like to emphasize that, in spite of the considerably different diffusion behaviors at room temperature of Cu_i in both, Al and B-doped silicon, as reflected through the different capacitance time dependence, the results agree fairly well. It is also remarkable that two very different sample preparation procedures lead to similar results and thus corroborate Cu to be responsible for the observed transient capacitance signals. In particular, as the implanted samples were not subjected to the initial high temperature anneal, any contamination, which might have affected the results, can be ruled out.

LOW LEVEL COPPER CONTAMINATION STUDIES

The efficiency of the TID analyses in detecting low level copper contamination is tested by studying the amount of copper introduced into silicon during chemical treatment with a copper contaminated solution and subsequent high temperature annealing.

The present study was performed only on the Al-doped silicon. Residual metallic surface contamination was removed by cleaning the samples with a H_2SO_4 :H_2O_2 (5 :1) solution. Then, they were subsequently dipped into a 1% H_2O:HNO_3 mixture containing various densities of $Cu(NO_3)_2$, blown dry one minute later, annealed at 1000°C for 10 minutes in a vertical furnace and quenched into ethyleneglycol. The Cu concentrations, as measured by TID are shown in Fig.3 (filled circles) as a function of copper density (in atomic parts per billion or ppb) in the aqueous solution. The copper concentration in the bulk is given in atoms per square centimeter in order to take into account the various widths of the samples. The dotted line corresponds to a concentration obtained in a clean aqueous solution and indicates the contamination background level. For copper densities between approximately 10 and 500 ppb, a strong correlation is found between the Cu in solution and the Cu in the silicon bulk. For higher values, the Cu concentrations reaches the maximum measurable concentration as discussed above, while for lower densities, the contamination is equal to the background level. As few as 30 ppb of Cu in solution are enough to induce a Cu dose of about $2 \cdot 10^{12} cm^{-2}$. These results illustrate how silicon contamination by copper impurities during chemical treatment and subsequent high temperature annealing can be successfully monitored by TID analyses.

The samples were next annealed at 100°C for several hours in order to precipitate the Cu impurities. After such a treatment the TID signals vanish completely. Upon removal of the Schottky barriers, the samples were shortly etched and cleaned before being annealed again at 1000°C for 45s in a vertical RTA furnace followed by quenching. This annealing step is necessary to redissolve the Cu impurities which were previously precipitated during the low temperature anneal. The subsequent TID results are shown as empty triangles in Fig.3. A good correlation is again found between the Cu bulk concentration and the Cu density in the aqueous solution, indicating that the second anneal was

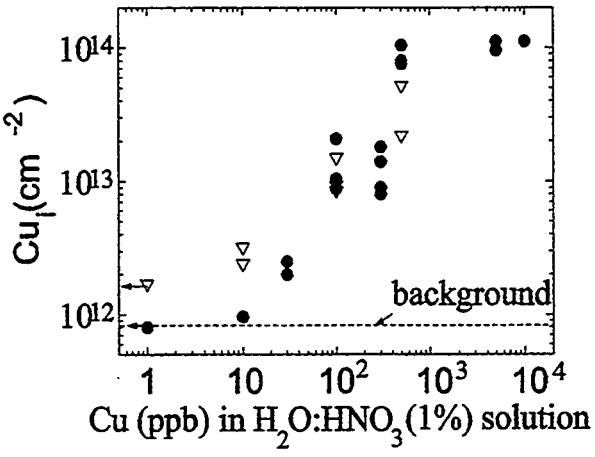

Fig.3 : Interstitial Copper concentrations measured by TID as a function of Cu density in solution after a short dip into the solution and annealing at 1000°C for 5 minutes (circles); after additional 100°C a few hours and 1000°C for 45 seconds (triangles).

long enough to redissolve most copper impurities in our samples and make them contribute to the TID signals It is worth noting that the background level is slightly increased after the second high temperature anneal.

CONCLUSION

From both experiments described in the present work we may conclude that, after a high temperature anneal followed by fast cooling, most copper atoms remain on interstitial sites and become 'visible' to TID analyses. The lowest detectable amount of Cu should be close to the detection limit of DLTS (~$10^{11}cm^{-3}$), and make TID analyses of considerable interest in fields like gettering and contamination studies. Although interstitial copper does not have a strong recombination activity and hence no significant impact on photovoltaic devices, copper precipitates may well be responsible for efficiency limitations in solargrade materials. Copper precipitation studies using TID combined with diffusion length measurements and TEM studies may be a clue to increase our understanding of the technological impact of Cu contamination.[10]

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The theme of this workshop is "R&D Issues for Cyrstalline Silicon to Support GW/yr Goal by the Year 2010." This workshop provides a forum for an informal exchange of information between researchers in the photovoltaic and non-photovoltaic fields on various aspects of impurities and defects in silicon, their dynamics during device processing, and their application in defect engineering. This interaction helps establish a knowledge base that can be used for improving device fabrication processes to enhance solar-cell performance and reduce cell costs. It also provides an excellent opportunity for researchers from industry and universities to recognize mutual needs for future joint research. The workshop format features invited review presentations, panel discussions, and two poster sessions. The poster sessions create an opportunity for both university and industrial researchers to present their latest results and provide a natural forum for extended discussions and technical exchanges.

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