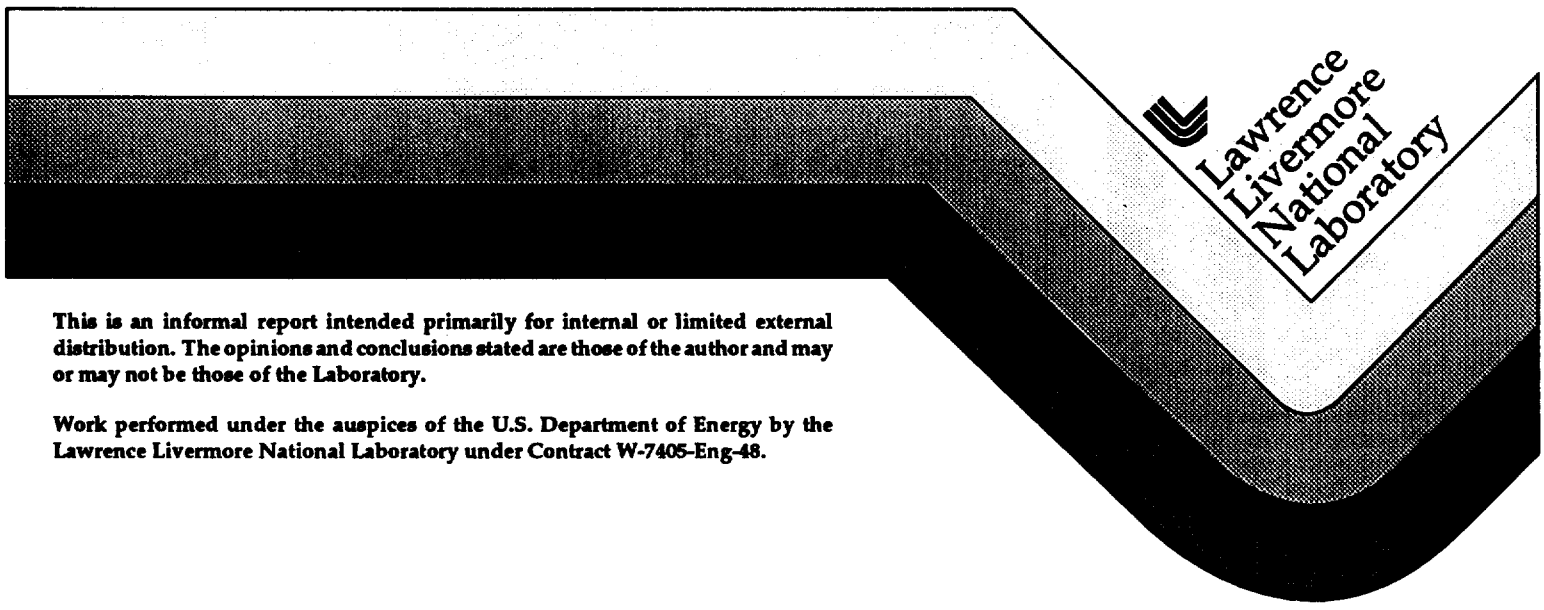
UCRL-ID-111643

High Energy Density Capacitors Using Nano-Structure Multilayer Technology

Troy W. Barbee, Jr
Gary W. Johnson
Dennis W. O'Brien

August 1992



Work performed under the auspices of the U.S. Department of Energy by the Lawrence Livermore National Laboratory under Contract W-7405-Eng-48.

DISCLAIMER

WHITE PAPER

HIGH ENERGY DENSITY CAPACITORS USING NANO-STRUCTURE MULTILAYER TECHNOLOGY

Submitted by

Lawrence Livermore National Laboratory
P.O. Box 808
Livermore, CA 94550

August, 1992

Materials Division
Troy W. Barbee, Jr. (510) 423-7796

Nuclear Engineering Systems Division
Gary W. Johnson (510) 423-0156
Dennis W. O'Brien (510) 422-5593

OBJECTIVE

Today, many pulse power and industrial applications are limited by capacitor performance. While incremental improvements are anticipated from existing capacitor technologies, significant advances are needed in energy density to enable these applications for both the military and for American economic competitiveness.

We propose a program to research and develop a novel technology for making high voltage, high energy density capacitors. Nano-structure multilayer technologies developed at LLNL may well provide a breakthrough in capacitor performance. Our controlled sputtering techniques are capable of laying down extraordinarily smooth sub-micron layers of dielectric and conductor materials. With this technology, high voltage capacitors with an order of magnitude improvement in energy density may be achievable. Well-understood dielectrics and new materials will be investigated for use with this technology.

Capacitors developed by nano-structure multilayer technology are inherently solid state, exhibiting extraordinary mechanical and thermal properties. The conceptual design of a *Notepad* capacitor is discussed to illustrate capacitor and capacitor bank design and performance with this technology.

We propose a two phase R&D program to address DNA's capacitor needs for electro-thermal propulsion and similar pulse power programs. Phase 1 will prove the concept and further our understanding of dielectric materials and design tradeoffs with multilayers. Nano-structure multilayer capacitors will be developed and characterized. As our materials research and modeling prove successful, technology insertion in our capacitor designs will improve the possibility for dramatic performance improvements. In Phase 2, we will make Notepad capacitors, construct a capacitor bank and demonstrate its performance in a meaningful pulse power application. We will work with industrial partners to design full scale manufacturing and move this technology to industry for volume production.

TECHNICAL PROBLEM

High performance capacitors are needed for many applications. Capacitor requirements for military and scientific pulse power applications are particularly acute. The rapid discharge of a significant amount of electrical energy is used to create a variety of physical phenomena. To achieve this, high voltage, high energy density capacitor banks with good circuit performance are needed. Capacitors for pulse power applications must have low loss, low inductance and be thermally and mechanically robust. Industrial applications also have unique requirements for high precision and highly reliable capacitors. Today, new pulse power and industrial applications are limited by current capacitor performance (refer to Table 1).

Pulse Power Applications	Industrial Applications
Electro-thermal propulsion	*High precision instrumentation*
Electromagnetic propulsion	*Medical instrumentation and systems*
X-ray generation	*Space and remote applications*
Electromagnetic effects	*High reliability electronics*

Table 1. By advancing capacitor technology and performance, many pulse power and industrial applications of interest to the military and industry will be enabled.

Military and space applications have uniquely difficult survivability and reliability requirements for harsh environments. Capacitor banks need to survive and function through mechanical and thermal shock without significant mechanical degradation or chemical aging. In some cases, capacitors need to survive high radiation environments. Military applications in the field must be maintainable while remote applications in space depend on highly reliable capacitors for electrical energy storage.

New pulse power applications demand better capacitor performance than that currently available. Capacitors and capacitor bank requirements include high energy density, specific energy, bank charging voltage, and efficiency. A ~1 Hz repetition rate and long shot life are also needed. Current state-of-the-art capacitors can acheive an energy density <1 MJ / m^3 and a specific energy of >6 KJ / Kg delivered. Requirements for DNA's electro-thermal propulsion program, listed in Table 2, specify the very high performance needed. Issues to be addressed in achieving these objectives include:

- Capacitor dielectric breakdown voltage, V_b
- Dielectric constant, k
- Managing electromagnetic field gradients and edge effects
- Current density and the *action integral* for the application
- Dielectric loss mechanisms (dipole relaxation and resonance, ionization, structural inhomogeneity and conduction loss) and conductor loss
- Equivalent series resistance and inductance (ESR / ESL)
- Mechanical, thermal and chemical integrity under stress
- Interconnection and integration
- Self healing (an issue with current materials and manufacturing)

Energy density:	$\geq 15\ MJ / m^3$
Specific energy:	$\geq 10\ KJ / Kg$
Bank charge voltage:	*5 Kv - to - 20 Kv*
Loss factor:	< 0.02
Pulse rep rate:	*0.1 Hz - to - 1.0 Hz*
Shot life:	*> 1000 shots*

Table 2. Some requirements for electro-thermal pulse power applications are not achievable with existing capacitor technology.

Current capacitor technologies suffer from defects and inhomogeneity introduced in the dielectric material and in capacitor manufacturing which contributes to voltage breakdown. Important voltage breakdown mechanisms include electrical or avalanche breakdown, electrochemical breakdown and thermal breakdown as dielectric loss increased under stress and with aging.

Rolled paper-conductor or polymer-conductor capacitors are characterized by high breakdown voltage but lower dielectric constant. They suffer from material and manufacturing defects, and can fail under the mechanical and thermal shock expected of pulse power applications in military environments. They experience chemical degradation with aging, temperature and shot life. They are bulky to package and aren't expected to achieve the performance required for the envisioned pulse power applications.

Capacitors with ferroelectric ceramic dielectrics such as $BaTiO_3$ typically have a much higher dielectric constant than polymer or paper capacitors. However, large geometry ceramic capacitors still have lower breakdown voltage and often high dielectric loss. Performance of today's ceramic capacitors is limited by ceramic powder quality, capacitor design and the manufacturing process.

BACKGROUND

Nano-engineered multilayers are characterized by a near atomic scale and thus, uniquely large interfacial area to volume ratios. Successful capacitor structures fabricated using multilayer technology will give us the ability to engineer high performance capacitors. We can optimize properties by materials selection, and design of the synthesis process and materials processing.

Multilayer materials are widely known in the materials community for scientific study and physics application. Their use has been demonstrated at many laboratories, including Lawrence Livermore National Laboratory. The multilayer effort at LLNL is among the strongest in the world as it is a core technology supporting many programmatic and scientific activities.

Nano-structure or nano-phase multilayer materials are dense, low contamination solids synthesized using atom by atom processes. They are characterized by a high concentration of material interfaces. The most notable of such materials are semiconductor superlattices fabricated using molecular beam epitaxy (MBE). However, multilayers may be synthesized using elements from all parts of the Periodic Table using MBE, evaporation, sputtering and electrochemical deposition technologies. At this time, multilayer structures have been fabricated by physical vapor deposition from at least 75 of the 92 naturally occurring elements in elemental form, as alloys or as compounds. The structure of multilayer materials is determined in synthesis by control of the thicknesses of the individual layers during deposition. These thicknesses vary from one monolayer (0.2 nm) to thousands of monolayers (> 1000 nm).

Until recently, the macroscopic thickness of nano-structure multilayer materials has been generally limited to less than a few microns, and more typically to 0.5μm or less. Recently, processes for magnetron sputter deposition of thick macroscopic nano-structure multilayer materials have been developed at LLNL and used to fabricate free standing high quality structures up to 300 μm thick containing up to 50,000 individual layers. Our existing research synthesis system produces samples having periods uniform to 2% of the individual layer thickness and areas of ~ 400 cm^2. These macroscopic nano-structure multilayer samples enable use of standard diagnostic techniques for material property characterization and open a path to develop devices with performance that approaches theoretical limits.

The through film and lateral perfection of these macroscopic multilayer materials have been determined using surface roughness measurements, cross-section transmission electron microscopy (TEM) and standard x-ray diffraction analysis. The surfaces of macroscopic multilayers (t > 20 μm) have demonstrated surface perfection essentially equal to the substrate roughness: multilayers deposited on super polished substrates with roughness of ~ 0.02 nm RMS and 0.14 nm peak to valley (PV) had roughness of ~ 0.04 nm and 0.29 nm PV. Cross-section TEM shows that the multilayer structure ~17 μm from a substrate is identical to that 1μm from that same surface and that this uniformity extended laterally over several microns. X-ray analysis demonstrates that the multilayer period of a 5 nm period 25 μm thick free standing structure varied by less than 1% top to bottom through 10,000 individual layers and is constant over 10 cm on single substrates. The perfection shown by these characterization results is unique in that it is **atomic in scale** but extends over **macroscopic distances.** These materials exhibit exceptional application

specific performance as a result of their nano-structures and atomic distributions. Structural flaws that characteristically limit performance are controlled so that the full potential of the nano-structure multilayer materials is achievable.

There are several potential advantages inherent to fabrication of high energy density capacitors by multilayer synthesis technologies. First, the processes used are generic in that a wide range of materials may be deposited as thin films. Therefore, it will be possible to apply new materials as they are developed potentially enhancing the dielectric properties of the insulating spacer (i.e. **technology insertion**). The designs presented here are based on a simple dielectric, amorphous SiO_2, with a dielectric constant of k=3 and a maximum standoff field of V_b = 1.2 -to- 1.4 x 10^7 V/cm. Enhanced performance can be expected if $ZrTiO_3$ (k =20 to 25), TiO_2 (k =70 to 80), or $CaTiO_3$ (k =140 to 150) are applied. Standoff fields of these materials in thin film form are not currently well known but are expected to be substantially larger than those observed for commercial bulk materials formed using powder compaction/sintering processing (~10^5V/cm). This optimistic opinion is based on our ability to fabricate fully dense layers having controlled surface roughness less than 5 Å on a routine basis. This is demonstrated in Fig. 1 where a cross section transmission electron micrograph of a molybdenum-silicon multilayer having a periodicity of 135 Å is shown at a magnification of 200,000x. Note the uniformity of the layers and the interfacial quality; the interfaces in this structure are smooth to approximately 1 to 2 atomic diameters (2 to 4 Å). Second, these structures are thermally and mechanically robust. Strengths approaching the

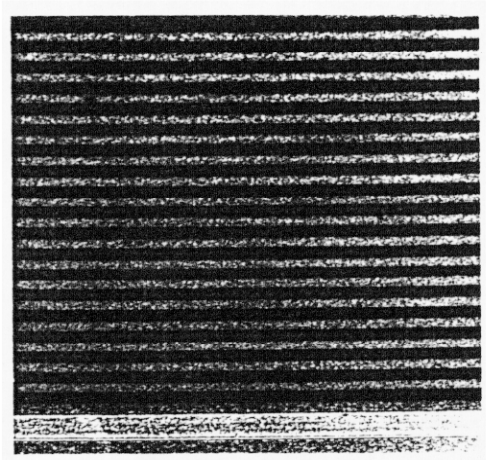


Fig. 1. Molybdenum (dark) - silicon (light) multilayer having a period of 135Å. Interface roughness is estimated to be ~2Å from this transmission electron microscope cross section (200,000 x).

theoretical limits of the component materials in metal/metal multilayers have been experimentally demonstrated for several alloy systems. Also, these materials are observed to be stable in multilayer form to temperatures in excess of 500°C in most cases. Thus, nano-engineered multilayer structures have several strategic advantages in developing high performance capacitors.

There are also manufacturing advantages. It is possible to design and fabricate a capacitor structure to *near net form*. This manufacturablity and the atom-by-atom nature of the deposition processes can facilitate engineering design. The conductor structures can be formed in a variety of configurations allowing applications-specific geometries and sizing to minimize anticipated capacitor performance limitations.

CONCEPTUAL ENGINEERING DESIGN

Our conceptual engineering design addresses a pulse power application typical for electromagnetic propulsion. The design goal is to deliver at least 5 MJ in about 15 ms to a load that exhibits significant inductive reactance. A moderate repetition rate, on the order of one shot every 10 seconds is required, along with a lifetime of a thousand shots or better. Efficiency must be high to obviate the need for an elaborate cooling system. Our calculations show that the design presented here meets these specifications.

The Notepad Capacitor

A form factor that is amenable to multilayer fabrication techniques is analogous to a thin notepad, roughly 8.5 by 11 inches, or 200 by 300 mm, and 1 mm thick (Fig. 2). Terminals at each end of the notepad are solid copper, suitable for brazing, which guarantees low contact resistance and high durability.

A cross section of a notepad capacitor element is shown in Fig. 3. We chose amorphous silicon dioxide (SiO_2) as the dielectric for this conceptual design because its properties are well known; our research would surely point towards other non-ferroelectric materials with better dielectric constants such as TiO_2 or $CaTiO_3$. Characteristics of SiO_2 used in this design are:

Breakdown voltage:	7×10^8 V / m (17.8 KV / mil)
Dissipation factor (Tan δ):	7×10^{-4}
Relative permittivity (k):	3.0

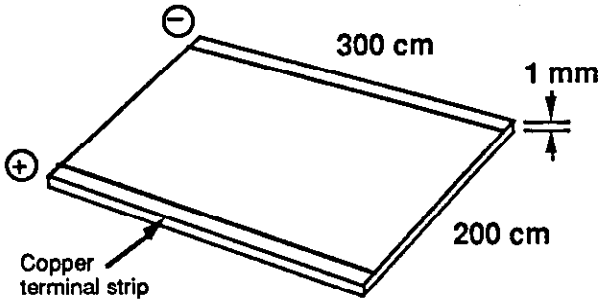


Fig. 2. Form factor of a notepad capacitor element.

The breakdown voltage, in particular, is a conservative value. Because of the very thin layers that are proposed, breakdown performance modes are expected to improve. One such effect, avalanche breakdown, should be reduced because of rapid electron recapture. The dissipation factor is about 50 times lower than that of paper/oil dielectrics found in the most commonly-used high energy capacitors. Though it is a relatively low-*k* material, SiO_2 is also free from dipole losses and the high effective inductance of high-*k* ferroelectric ceramics like $BaTiO_3$. In applications where high capacitance is the most important factor, high-*k* materials could certainly be used.

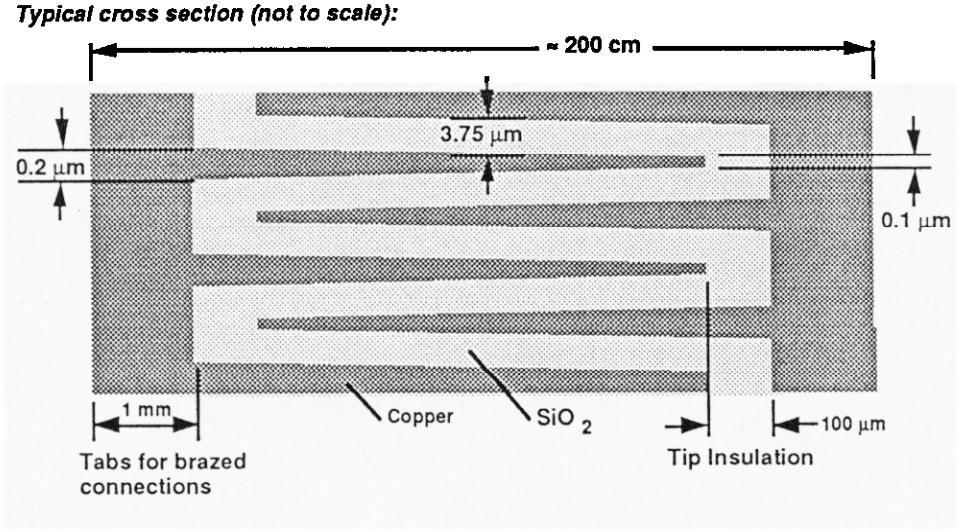


Fig. 3. Cross section of a notepad capacitor.

From Fig. 3, you will note another engineering advantage of the multilayer technique: tapered conductors. Since the current density in any plate is proportional to the distance from the tip, the required cross section of conductor can also vary proportionally. This reduces the amount of copper in the assembly, saving weight and bulk. The minimum practical thickness for copper deposition is about 0.1μm and the maximum is about 1.0μm. Other metals, such as aluminum, are also likely candidates for this design.

In ordinary foil capacitors, breakdown at the edges of the foils is a nagging problem. In our design, the edges, or plate tips, are completely buried in the multilayer dielectric. We hope to demonstrate how multilayer dielectric material can be engineered to offset the electric field gradient and reduce edge effect, improving capacitor voltage breakdown characteristics.

Capacitance for one layer of this parallel-plate capacitor is calculated from

$$C = k\varepsilon_o \frac{a}{d} \qquad (1)$$

where C is the capacitance in Farads, k is the relative permittivity (3.0 for SiO_2), ε_o is the permittivity of free space (8.854 x 10^{-12} F / m), a is the plate area and d is the dielectric thickness. Notepad structures with the dimensions in Fig. 3 and 256 layers are expected to have capacitance C = 109 μF and a breakdown voltage V_b = 2,600 V. Copper accounts for 4% of the volume and 11% of the mass of this capacitor. Minimizing the quantity of copper maximizes the volume of dielectric, improving energy density.

Energy stored in a capacitor is calculated from

$$W = \tfrac{1}{2}CV^2 = \tfrac{1}{2}k\varepsilon_o V^2 ad \qquad (2)$$

where W is the energy in Joules, and V is the voltage. One notebook capacitor can store 368 J if it is charged to its breakdown voltage. When designing a capacitor, it is apparent that dielectrics with high-k and high breakdown voltage increase energy density, but there may be other tradeoffs: dielectric absorption (loss), capacitance changes with voltage and temperature, thermal conductivity, mechanical properties, etc., all affect the choice of the dielectric material.

Performance of a Notepad Capacitor Bank

A conceptual design for a 20 KV, 6 MJ series-parallel bank of 16,800 notepad capacitors is shown in Fig. 4. Specifications are listed in Table 3.

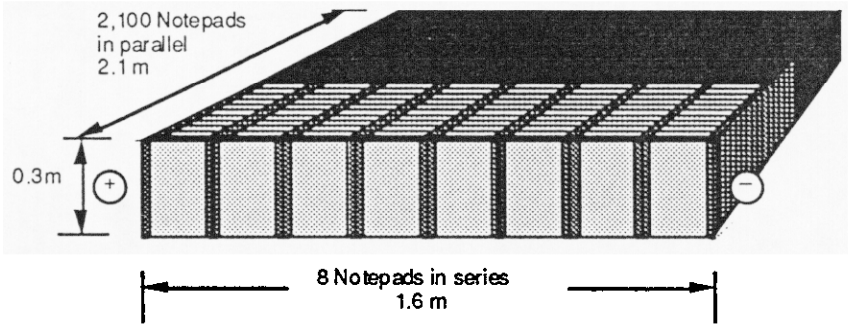


Fig. 4. Series-parallel bank of 16,800 notepad capacitors.

Volume:	*1.0 m^3*
Capacitance:	*0.03 F*
Working voltage:	*20 KV*
Energy storage:	*6 MJ*
Weight:	*3000 Kg*
Energy density:	*6 MJ/m^3*
Specific energy:	*2 KJ/Kg*
Effective Series Resistance:	*0.3 mΩ*

Table 3. Capacitor bank specifications.

To examine the efficiency of this capacitor bank, a simplified model of an electromagnetic propulsion (railgun) application was devised, represented by an *RL* load with R=0.2 Ω and L=2 mH. This initial charge was 20 KV, 6 MJ. With these conditions, the expected voltage ringdown occurred with voltage reversal at 17 ms. Losses in the capacitor bank include 3 KJ of I^2R loss in the conductors and 6 KJ of dielectric loss, for a bank efficiency of 99.85% (refer to Table 4). In a practical system, much more energy would be lost externally in a resistive *crowbar* circuit that is required to prevent voltage reversal and quench any arcing on the railgun.

Resistive loss:	*3 KJ*
Dielectric loss:	*6 KJ*
Bank efficiency:	*99.85 %*
Heating per shot:	*0.007°C*

Table 4. Expected capacitor bank performance, pulse application.

Little heating of the bank (a 0.007°C rise per shot) would occur because of its high efficiency and high heat capacity. The heat capacities of the capacitor materials relative to water (water = 1.0) are 0.54 for SiO_2 and 0.89 for copper. Use of thin layers also promotes rapid thermal diffusion, preventing internal stress. This looks very favorable for high repetition rate applications. It is feasible to build in liquid cooling channels if different geometries or materials that require cooling were used.

Design Summary

This conceptual design uses well-understood materials to engineer a design for an extraordinary capacitor. High energy density, low loss, good thermal and mechanical properties, and low inductance make the nano-structure multilayer capacitor an excellent candidate for military pulse power applications.

TECHNICAL STATUS AND ISSUES

Our nano-structure multilayer technology is well established. Facilities and equipment capable of proof-of-principal and small scale capacitor fabrication and testing is available. We are capable and prepared to retrofit and add to the existing systems to carry out Phase 1 of the proposed program. Our scientific and engineering staff is currently in place and available for this program. We are prepared to draw on the collective materials, pulse power and related expertise at LLNL needed to succeed in this program.

Some important technology issues need to be investigated. Time dependent dielectric breakdown of nano-structure multilayer capacitors need to be well understood for a variety of materials and capacitor designs. Interfacial reactions (e.g., diffusion) between dielectrics and conductors are important to understand voltage breakdown phenomena. Complex dielectric-conductor structures and multiple dielectric-dielectic interfaces that are expected to provide very high voltage holdoff will be studied. Amorphous, complex-composition dielectrics may offer advantages. Voltage breakdown resulting from electromagnetic field gradients at the edges of conductors is a concern.

Program issues include development and fabrication of the first nano-structure multilayer capacitors designed for high voltage holdoff. Substrates and substrate removal to fabricate free standing capacitors have to be developed. Full capacitor time and temperature holdoff and discharge performance characterization need to be done. We need a better understanding of engineering design of near-net-form capacitors with consideration to electromagnetic gradients and edge effects, mechanical properties and interconnection for integration in capacitor banks. Scale up of this nano-structure capacitor technology will require investment in facilities and equipment, and will present new fabrication and processing problems.

PLANNED WORK

Our efforts will be divided into two phases. Phase 1 encompasses proof of principle capacitor fabrication, materials research, device engineering, and the design of a scaled-up capacitor fabrication facility. If Phase 1 is successful,

Phase 2 will follow with the construction of the facility, design and testing of notepad capacitors for a capacitor bank demonstration, and the design of high-volume manufacturing equipment for industry.

Phase 1 (Duration: 15 months)

1. Proof-of-principle capacitor: An existing LLNL research facility will be upgraded to support fabrication of small scale multilayer capacitors. Devices will be fabricated from several materials, followed by electrical characterization and mechanical testing to establish the viability of this technology. Deliverables: Progress and test reports.

2. Materials Studies & Modeling: Throughout Phase 1, we will be improving our physical models and understanding of nano-structure multilayer dielectrics, accumulating a database of dielectric characteristics, and performing electrical system analyses. These models will effect capacitor design and improve performance. Deliverables: Database and modeling report.

3. Second-generation capacitor: Building on our knowledge gained in the previous steps, the facility will be modified as required, new capacitor designs and materials will be fabricated and extensive testing will be performed. Deliverables: Progress and test reports; characterized small scale capacitor(s) for independent evaluation.

4. Fabrication facility design: As this technology shows progress, we will design a scaled-up capacitor fabrication facility that will be used to make the proposed notepad capacitors. Deliverables: Facility design documents.

Successful completion of Phase 1 with encouraging findings would lead to approval and funding to proceed with Phase 2.

Phase 2 (Duration: 21 months)

1. Materials Studies & Modeling: Continuation of Phase 1 materials research and engineering modeling efforts. Deliverables: Database and modeling report.

2. Fabrication Facility Construction: Procurement, construction and checkout of the Notepad capacitor fabrication capability at LLNL. Deliverables: Completed facility.

3. Notepad Capacitors: Design, fabricate, characterize and test of individual notepad capacitors using various materials and geometries. These will be full-scale devices, usable in pulse power applications. Deliverables: Progress report; characterized Notepad capacitor(s).

4. Capacitor Bank: Design, fabricate, and test a demonstration pulse power capacitor bank made up of tens of notepad capacitors, including interconnection, charging and switching systems. The bank will be tested with loads that are representative of the desired application. Deliverables: Final report.

5. Manufacturing: Work with designated DoD contractors to design a commercial manufacturing facility capable of high-volume capacitor production. Deliverables: Conceptual plant design.

PROJECT FUNDING

Phase 1	Q1, FY93 -*through*- Q1, FY94	$1,500 K
Phase 2	Q2, FY94 -*through*- Q4, FY95	$3,000 K

RELATED ON-GOING WORK

LLNL is an applied physics laboratory with a well established materials and engineering technology base. We expect to draw on the collective capabilities and expertise at LLNL to better understand the pulse power application and be in the best position to meet DNA's capacitor performance goals. Core materials technologies include the nano-structure multilayers, interatomic materials diagnostics, and carbon and silica aerogels. Multilayers are currently being developed as physics diagnostic and optical devices. Research is proceeding to take advantage of their remarkable mechanical and thermal properties for DOE Weapons programs and applications in aerospace and related industries. The transmission electron microscopes x-ray diffraction and similar diagnostic capabilities at LLNL are needed tools to understand and develop nano-structure multilayer materials. Carbon aerogels are extremely low density, high surface area foams developed for DOE programs. We are currently developing low voltage, very high capacitance electrolytic capacitors with carbon aerogels to replace batteries in some applications.

LLNL also has well developed engineering thrust areas in pulse power, microwave, laser and semiconductor technologies, and electromagnetic and device modeling. Very large capacitor banks have been developed for electric gun, rail gun and x-ray applications. LLNL originated small pulse power slapper detonators for weapon initiation. Microwave broad band sources and vulnerability assessment at LLNL rely on high performance capacitor technology. Pulsed, high power lasers developed at LLNL for DOE and DoD programs similarly rely on high performance capacitors banks. Research has been done on laser and electron beam initiated fast semiconductor switches for pulse power applications. Our electromagnetic and device modeling expertise is a resource used by DOE and DoD programs.

EXPECTED PAYOFFS

We are proposing research and development of an important enabling technology. The nano-structure multilayer capacitor technology can open up many new opportunities for the military and industry. An order of magnitude or more improvement in energy density with very high efficiency can be significant. We can expect immediate use of this capacitor technology in electro-thermal and electromagnetic effects programs, and possibly rail-gun, laser and x-ray generation programs. Their applications in weapons initiation and smart penetrator fuzing is anticipated, and use in space and other remote applications will surely arise.

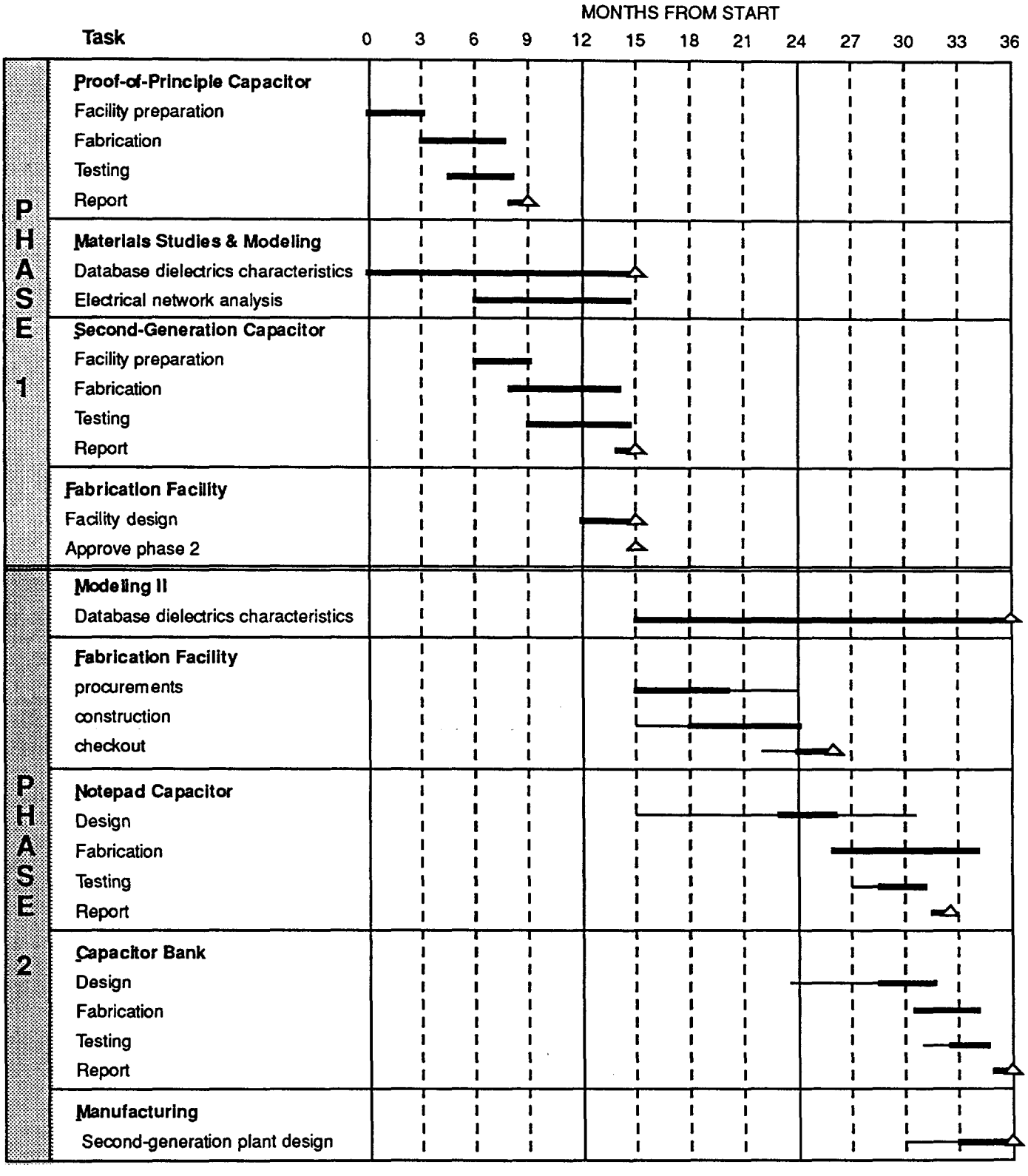
The proposed technology may enable capacitor designs that approach theoretical limits of the dielectric and conductor materials used. New capacitor design techniques are made possible to control field gradients, edge effects and current densities in the capacitor, and enable rugged, high density capacitor bank packaging for military and space applications.

We plan to move this technology to DNA industrial partners in Phase 2 of the program. We will be available to support military application commercialization this new technology with DNA and pulse power community.

The revitalization of the American electronics and industrial base is also important. The proposed capacitor technology can make a needed difference in a variety of industrial fields. Communication and transportation systems envisioned today can be enabled and made practical by high energy density capacitor technology. Electric automobiles with reasonable acceleration and effective energy recovery through dynamic breaking may become a reality with this technology. Medical systems, such as defibrillator implants, and high density electronics packaging can be made possible.

MULTILAYER CAPACITOR DEVELOPMENT SCHEDULE

REV: 8-19-92



Technical Information Department • **Lawrence Livermore National Laboratory**
University of California • Livermore, California 94551