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High Efficiency Copper Ternary Thin Film Solar Cells

Annual Subcontract Report
1 March 1987 – 30 April 1989

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SERI Technical Monitor: R. Mitchell

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1.0 SUMMARY

This is the Annual Technical Progress Report for a 24-month research program entitled " High Efficiency Cu-Ternary Thin Film Solar Cells ". This program is a continuation of a previous 22-month research effort [1,2,3].

The goal of this project is to develop a high efficiency thin film $CuInSe_2$ (CIS) solar cell using a potentially low-cost process. The technique used in this project is a two-stage process. The two-stage process involves depositing the metallic elements of CIS (i.e. Cu and In) on a substrate in the form of stacked layers and then selenizing these stacked metallic layers in an atmosphere containing Se to form a CIS film. During the first two years of this research program we concentrated our efforts on using electrodeposition techniques for depositing the Cu and In films on Mo coated glass substrates. These efforts resulted in a process in which the CIS films prepared could be used to fabricate small area solar cells with conversion efficiencies close to 10% [1,2,3]. These results established the fact that the two-stage process using electrodeposition/selenization techniques can yield CIS films with good electrical and optical properties and efficient solar cells can be fabricated using these films.

During the present phase of this program we focused our efforts on scaling up the two-stage process in order to fabricate larger area (up to $50cm^2$) solar cells and sub-modules. We designed and built large area plating fixtures and a selenization furnace suitable for processing substrates of $50cm^2$ area was fabricated. During this scaling-up effort two problems with the two-stage process emerged. These were, (i) stoichiometric non-uniformities in the large area CIS films prepared by the electrodeposition/selenization process and (ii) poor adhesion of the CIS films to the Mo coated substrates. These problems did not allow the fabrication of high efficiency devices on such large area films. Consequently, we initiated work on understanding the origins of these problems. The stoichiometric non-uniformity of large area films in the macro scale was solved by modifying the plating fixture design, however, non-uniformities in the micro-scale remained because of the surface sensitive nature of the plating process. Experiments to modify the surface of the Mo layer to promote adhesion between the Mo and the CIS films affected the plating processes for Cu and In to the point where the excellent control we had achieved in fixing the Cu-to-In ratio by the electrodeposition technique was lost. Therefore, we initiated another approach to the two-stage process,

namely, an evaporation/selenization approach wherein the elemental metallic layers were deposited by vacuum evaporation onto the Mo coated glass substrates. Using this approach, we have overcome the adhesion problem and have fabricated highly adherent solar cells with close to 11% efficiency. Our future research will concentrate more on this evaporation/selenization technique which offers the possibility of yielding cells in the 12-15% efficiency range.

2.0 INTRODUCTION

The overall objective of this project is to develop thin film copper ternary solar cells with conversion efficiencies approaching 12.0%. A two-stage process has been developed for this purpose and high efficiency solar cells have been demonstrated using this very promising technique.

The two-stage process involves deposition of some or all of the elemental components of a compound in the form of stacked layers on a substrate followed by a reaction of these elemental components to form the desired compound. In the case of $CuInSe_2$ (CIS), either Cu/In/Se or Cu/In stacked layers can be utilized in a two-stage process. If a Cu/In/Se stack is used, the reaction of the elements can be carried out in an inert atmosphere. If, on the other hand, a Cu/In stack is employed, then the reaction should be carried out in a reactive atmosphere containing H_2Se gas or Se vapor. Although, standard furnace annealing is the commonly used method for forming CIS by the two-stage process, there has also been some work on reacting ultra-thin layers of Cu, In and Se by pulsed laser radiation.

The elemental layers in a two-stage process can be deposited by various techniques. However, the technique chosen should have a demonstrated ability to deposit layers with tightly controlled thicknesses. Such control is important for obtaining material of proper stoichiometry especially for the case of Group I-III-VI_2 semiconductors.

The two-stage process employed by our group in this research program consists of two basic processing steps:

(a) deposition of a thin Cu/In metal stack on a substrate;
(b) selenization of this metal stack in an atmosphere containing H_2Se gas.

During most of the present program we concentrated our efforts on the electrodeposition/selenization process which uses electrodeposited Cu/In stacked layers. We have previously demonstrated devices with around 10% conversion efficiency using this approach [3]. Samples used in these early experiments had small areas of about 1-2 cm^2 and the films were grown using small area plating fixtures. However, our efforts in this program focused more on scaling-up the electrodeposition technique. We designed and constructed large area (up to 50 cm^2) plating fixtures and selenization facilities for processing these large area samples.

We also studied the mechanical characteristics of the CIS films grown on Mo coated substrates by the electrodeposition/selenization approach. In the course of scaling up the electrodeposition process two problems with the CIS films emerged. Firstly, because of plating on a large planar substrate, stoichiometric non-uniformity was observed in these CIS films. Secondly, because of the large volume expansion of the films during selenization the CIS/Mo interface was subjected to high degrees of stress. This frequently gave rise to peeling of portions of the films from their substrates. The stoichiometric non-uniformity problem was solved by a design modification of the plating fixture and this is discussed in section 3.2.3. The peeling problem has been studied and is discussed in section 3.2.4. It is well known that electroplating is a very substrate sensitive process, therefore, any modification made to the surface of the Mo substrate for the purpose of enhancing the Mo/CIS bond affected the control that we could exercise in maintaining the Cu/In ratio in CIS films. This problem compelled us to examine other ways of depositing the metallic films for the two-stage process.

During the last six months of this program we investigated the use of vacuum evaporation technique in a two-stage process to obtain high efficiency solar cells. In this work Cu and In layers were evaporated onto Mo coated substrates and they were then selenized in the same manner as the electrodeposited films. This effort led to very encouraging results and highly efficient solar cells with excellent mechanical integrity were fabricated using this new approach. Work on the evaporation/selenization approach is presented in section 3.3 of this report.

3.0 TECHNICAL DISCUSSION

3.1 Substrate Preparation

The majority of the substrates used in this work were Mo coated 7059 glass. Mo layers were E-Beam evaporated on 6"x6" glass substrates using an Airco Temescal FC 1800 evaporator coupled with a Sloan Six/Ten power supply. The details of the Mo deposition technique have been previously published [3] and they will not be repeated here. The thickness of the Mo was typically 2.0-2.5 microns and the sheet resistance of the substrates was typically 50-100 milliohms per square. Low sheet resistance was especially important for substrates used in the large area electrodeposition work to minimize I-R drops. The Mo films were stress free and they adhered well to the glass substrates. The Mo surface was subjected to chemical and electrochemical treatments prior to depositing the Cu and In layers. Some of these treatment steps were discussed in our previous reports [1,2,3].

3.2 Electrodeposition/Selenization Process

Electroplating work on small area samples was performed in plating cells similar to the one shown in Fig. 1. In this fixture the electrical contact to the glass/Mo substrate was made by contacting the Mo surface with flexible contact strips buried behind a gasket. All plating experiments were carried out at room temperature using copper and indium anodes and without any electrolyte stirring and electrolyte filtration. Most of the plating work was carried out under constant current conditions, although some experiments were performed using constant potential conditions using a reference electrode in a three electrode plating cell.

3.2.1 Copper Plating

Although several different plating parameters and electrolytes were investigated in this work, the best results were obtained using the electrolytes and procedures given below:

Copper plating was carried out using acidic copper sulfate electrolyte with 0.8 M $CuSO_4{:}5H_2O$ and 2M H_2SO_4. The electrolyte contained approximately 50 ppm of chloride (from HCl) to obtain smooth films of uniform morphology. The anode consisted of a 5 9's pure Cu sheet and the plating current density changed from

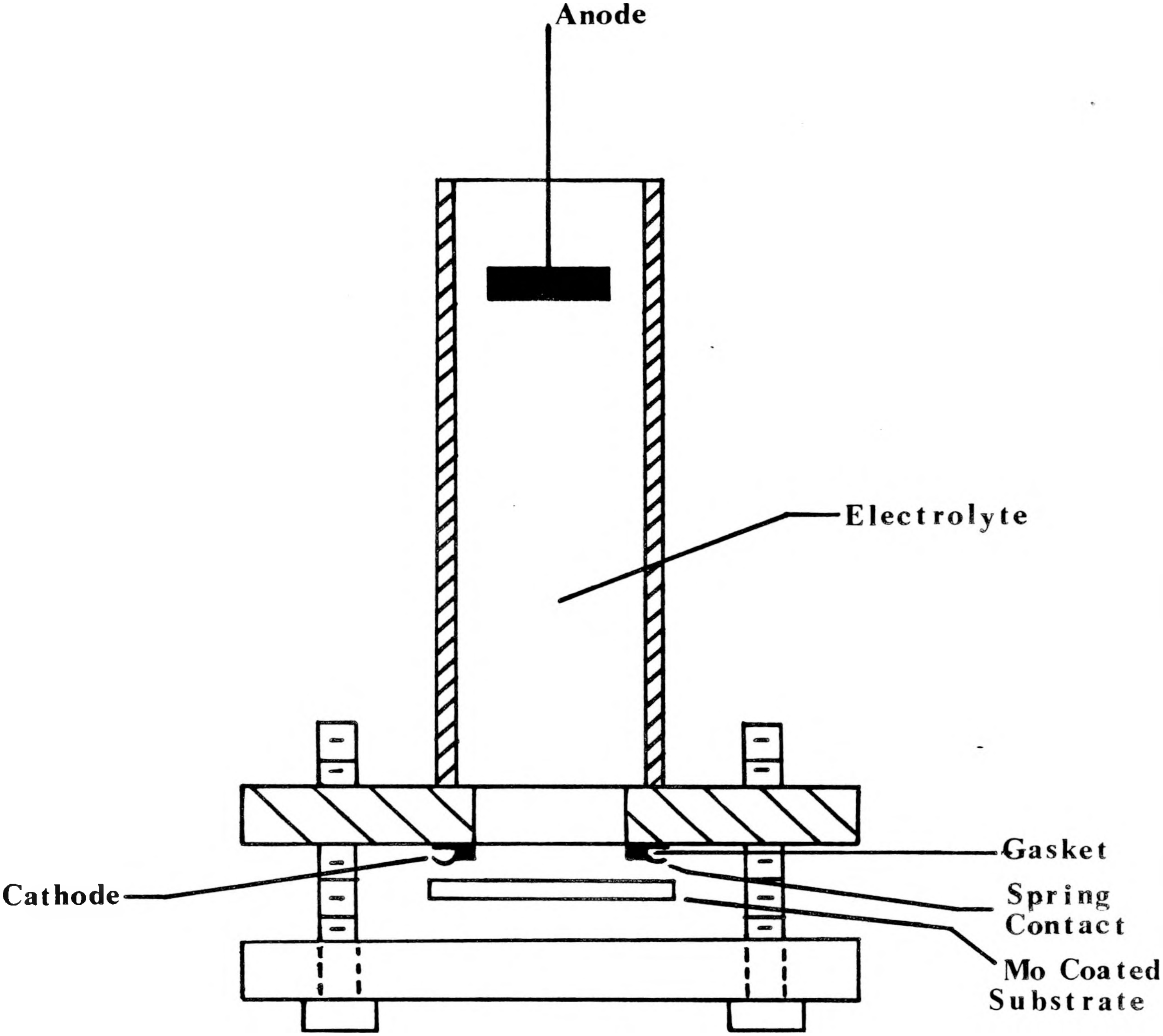


Fig. 1. A small area electrodeposition fixture used in this work.

40 mA/cm^2 to 120 mA/cm^2. The best coverage of the Mo coated substrate was obtained by using an initial high current pulse (120 mA/cm^2) followed by a low current (40 mA/cm^2) plating step. Good coverage of the Mo film by the Cu layer was found to be essential for obtaining uniform In layers of high quality. Indium plating over non-uniform Cu layers was problematic and excessive hydrogen evolution was observed for such samples during the In deposition step.

3.2.2 Indium Plating

Indium plating was carried out using commercially available acidic indium sulfamate electrolyte and indium anodes. Platings were performed at room temperature at a typical current density of 20 mA/cm^2. The quality of the electroplated In films was found to be a very sensitive function of the nature of the underlying Cu film. Indium plated very well over uniform, small grained and shiny Cu layers. Large grained discontinuous Cu films, however, caused hydrogen evolution during the In plating step and the control over the thickness of the In layer and thus the stoichiometry was lost. This issue became more important when working with large area samples as will be discussed below.

3.2.3 Large Area Plating

It is well known that the electronic properties of a CIS film are very much affected by its stoichiometry. To control the stoichiometry, the deposition of the component layers i.e. Cu and In has to be carried out precisely. Electroplating techniques offer a good possibility of obtaining controlled amounts of materials on selected substrates. We have very clearly demonstrated this for the case of Cu and In depositions on small area samples and we have obtained good quality CIS films with controlled stoichiometry using the electrodeposition/selenization technique. However, as the plated area in an electrodeposition process increases, the issue of uniform deposition becomes more and more important.

During this phase of the project, a plating fixture was designed and built for the purpose of depositing Cu and In films with up to 50 cm^2 area on glass/Mo substrates. This fixture consisted of a substrate holder, an anode holder plate and a plastic container holding the plating electrolyte. The plastic container had vertical grooves formed on its two walls. These grooves were used to place the anode plate and the substrate holder at various fixed distances from each other in the plating electrolyte. A picture of this plating fixture is shown in Fig. 2. Fig. 3 is a picture of the substrate holder and the anode holder of the set-up depicted in Fig. 2.

Before constructing the plating fixture of Fig. 2, a computer program was used to determine the near-optimum geometry for such a fixture. The program took into account the primary current distributions for Cu and In but the effects of possible IR drops, electrode kinetics, and mass transfer were not included in the calculations. The exchange current density values used in the calculations for Cu and In were 3.9 mA/cm^2 and 2.3 mA/cm^2 respectively. Figures 4a through 4e show the cross sectional view of various plating fixture geometries used in the computer calculations. These figures are for Cu plating. Similar results were obtained for the In plating process. The shaded areas drawn over the anode and cathode surfaces in Figs. 4a-4e are the plots of the relative values of the calculated current densities for different plating fixture geometries. It should be noted that the geometry of the plating fixture (anode size, the shape and the dimensions of the well in which the cathode is placed) has a pronounced effect on the current density distribution across the cathode. In Fig. 4a, for example, the substrate is placed in a well with smooth and vertical walls. The current density for this case is clearly higher along the two edges of the cathode and such a current density distribution would result in thicker Cu plating along these edges. Addition of 0.25 cm size obstructions in front of the cathode in the plating well (Fig. 4b) dramatically changes the current density distribution and the thickness distribution of the plated Cu is changed in a way that would cause the middle of the sample to receive a thicker coat. The results of the computer calculations of Figs. 4a-4e can be summarized as follows:

For an average current density of 10 mA/cm^2, and a cathode to anode distance of 6cm:

a) The Current density distribution varies by 18% across the cathode for the plating fixture geometry of Fig. 4a. The corresponding variation in voltage distribution is 12%.
b) With 0.25 cm wide obstructions along the two edges of the substrate and with a total of 1.5 cm deep well, a 6 cm wide anode is expected to give a 5% variation in current density distribution (Fig. 4c). This variation is increased to 5.5% for a 4 cm wide anode (Fig. 4b).
c) For a geometry where a total well depth of 2 cm is used, a 4cm wide anode gives a 2% variation in the current density distri-

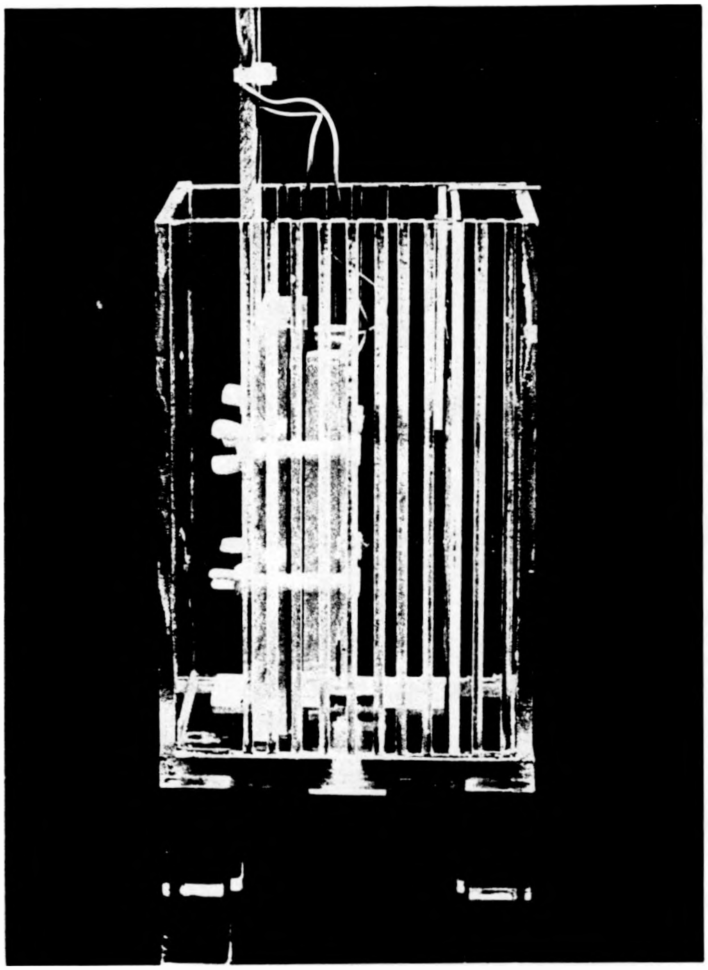
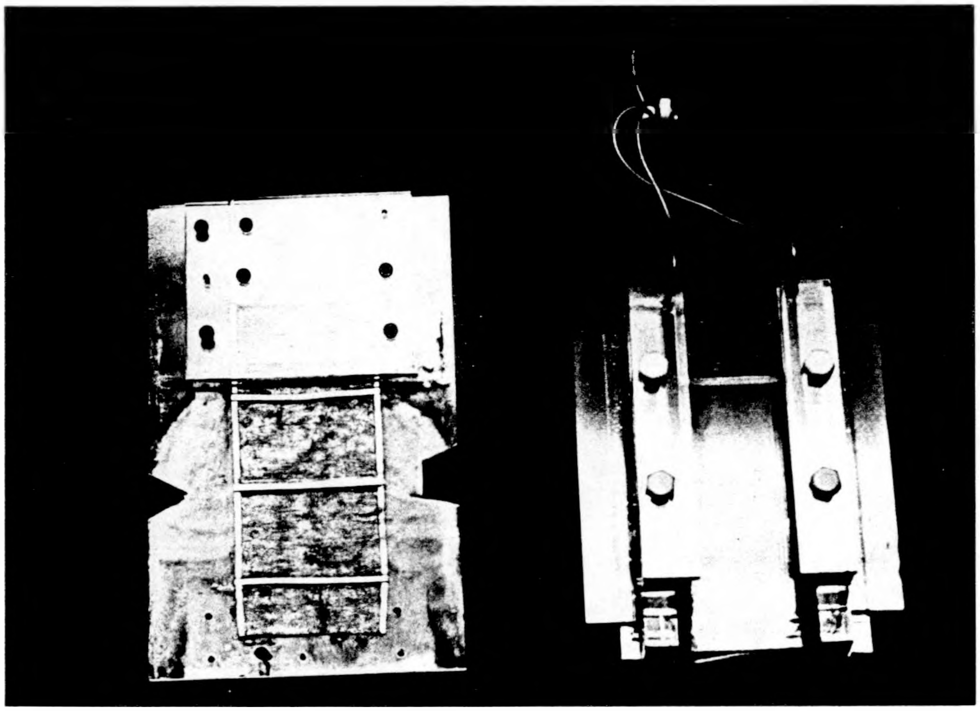
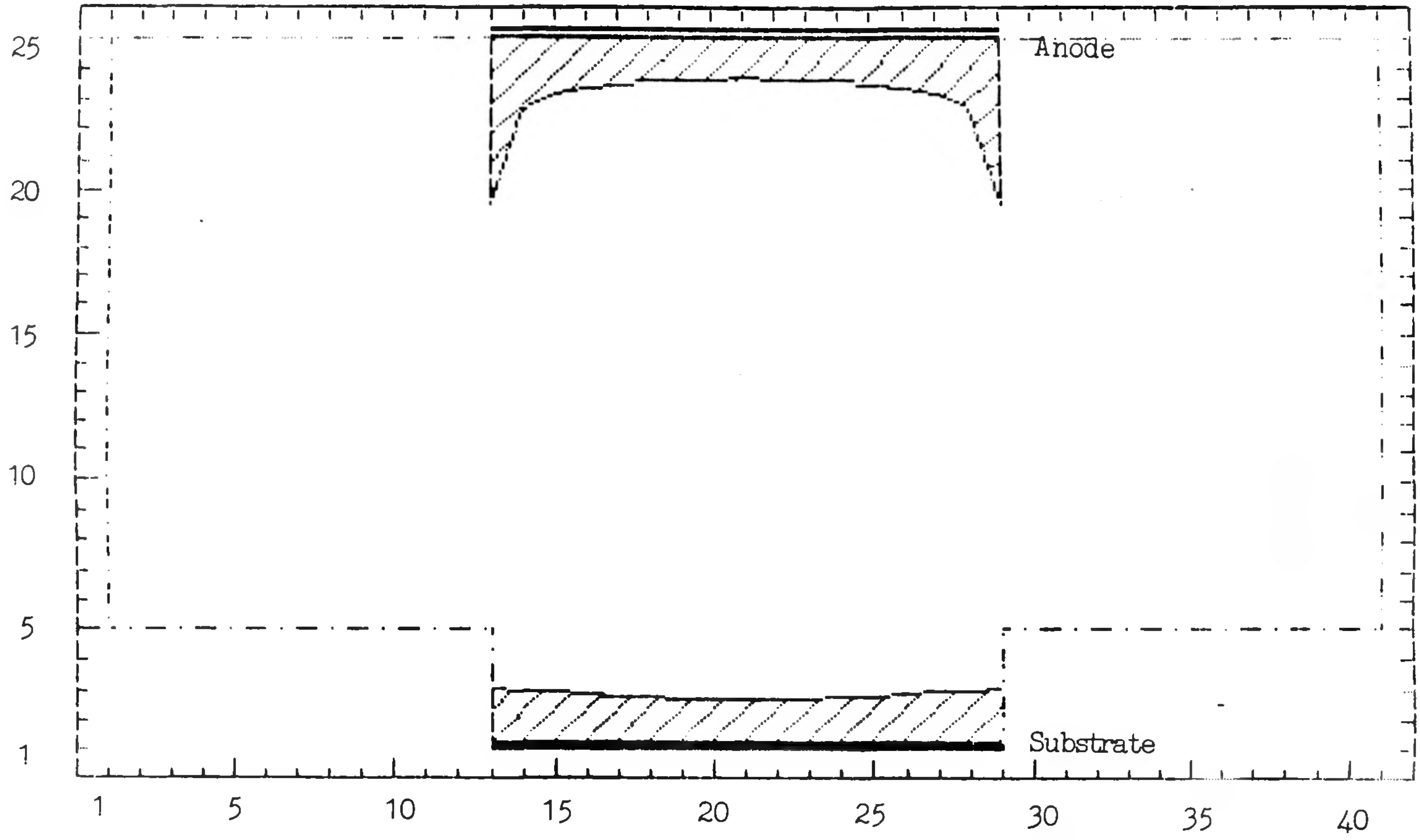


Fig. 2. A large area electrodeposition fixture used in this research. This fixture handles substrates with areas up to 50cm².



ANODE HOLDER SUBSTRATE HOLDER

Fig. 3. The substrate and anode holders of the fixture shown in Fig. 2.



Each division is 0.25 cm.

Fig. 4a. Result of computer calculations of current density distribution in a plating fixture. Electrolyte is in the region bounded by the dotted (-.-.-) line.

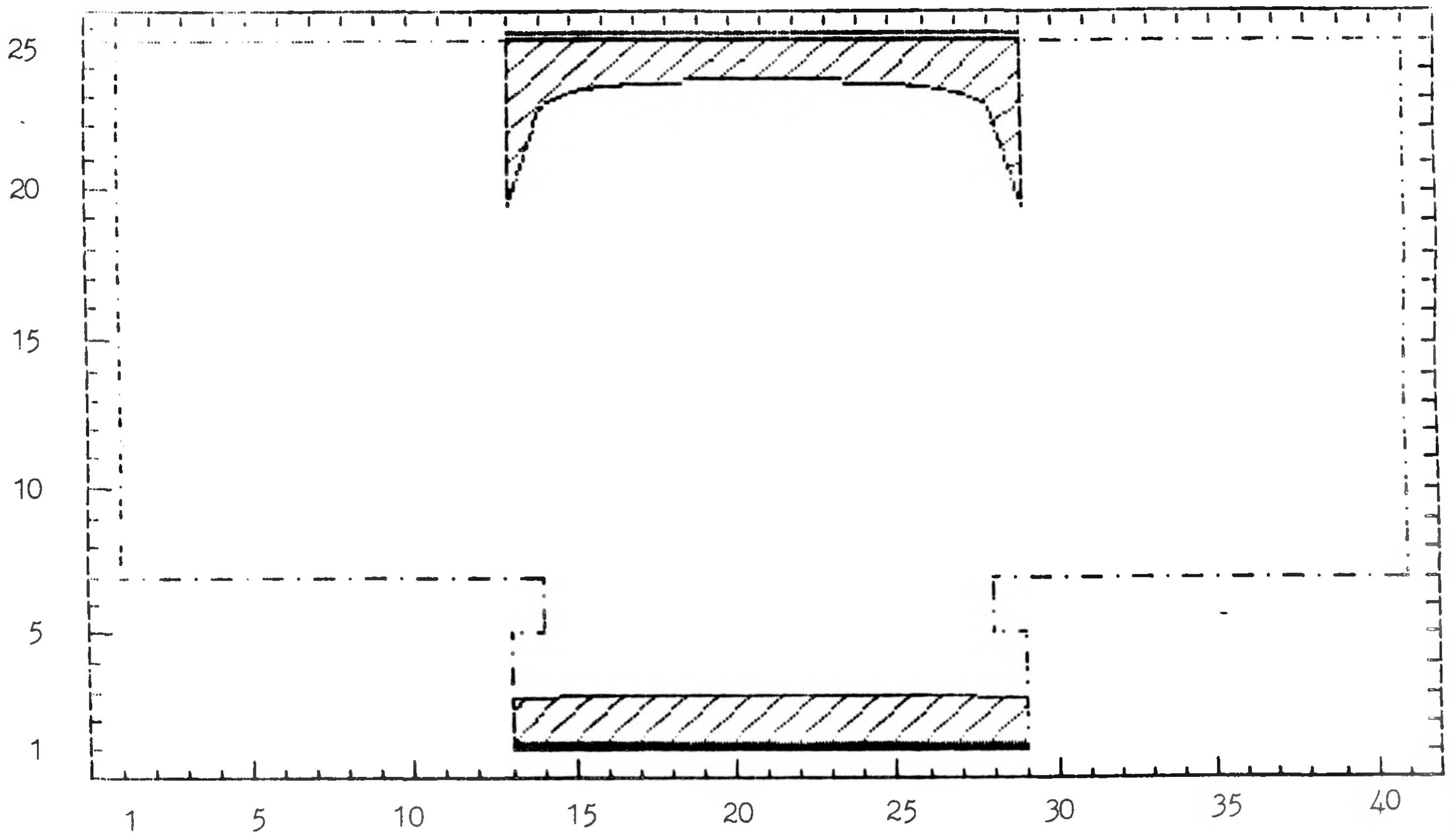


Fig. 4b. Result of computer calculations of current density distribution in a plating fixture.

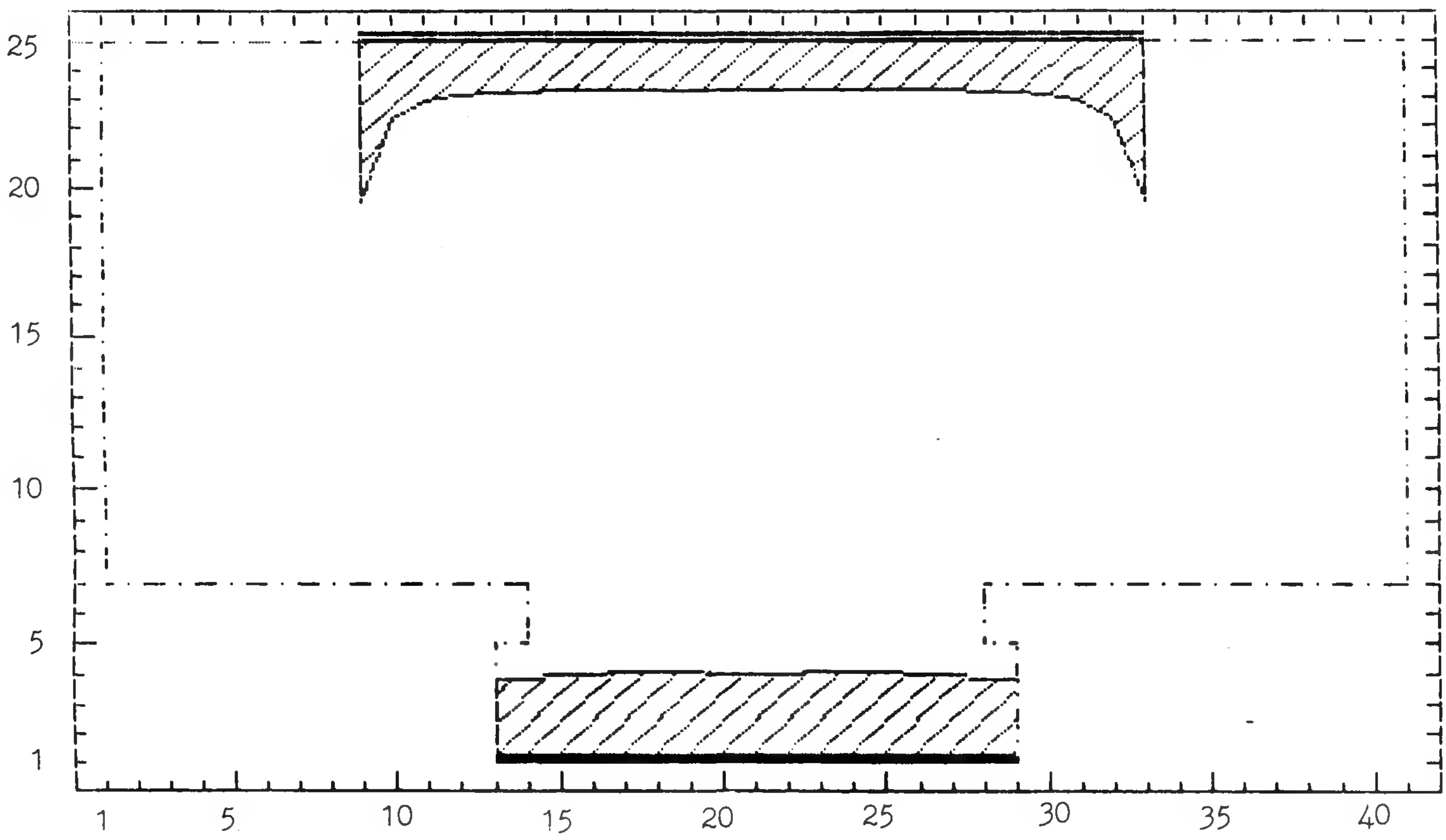


Fig. 4c. Result of computer calculations of current density distribution in a plating fixture.

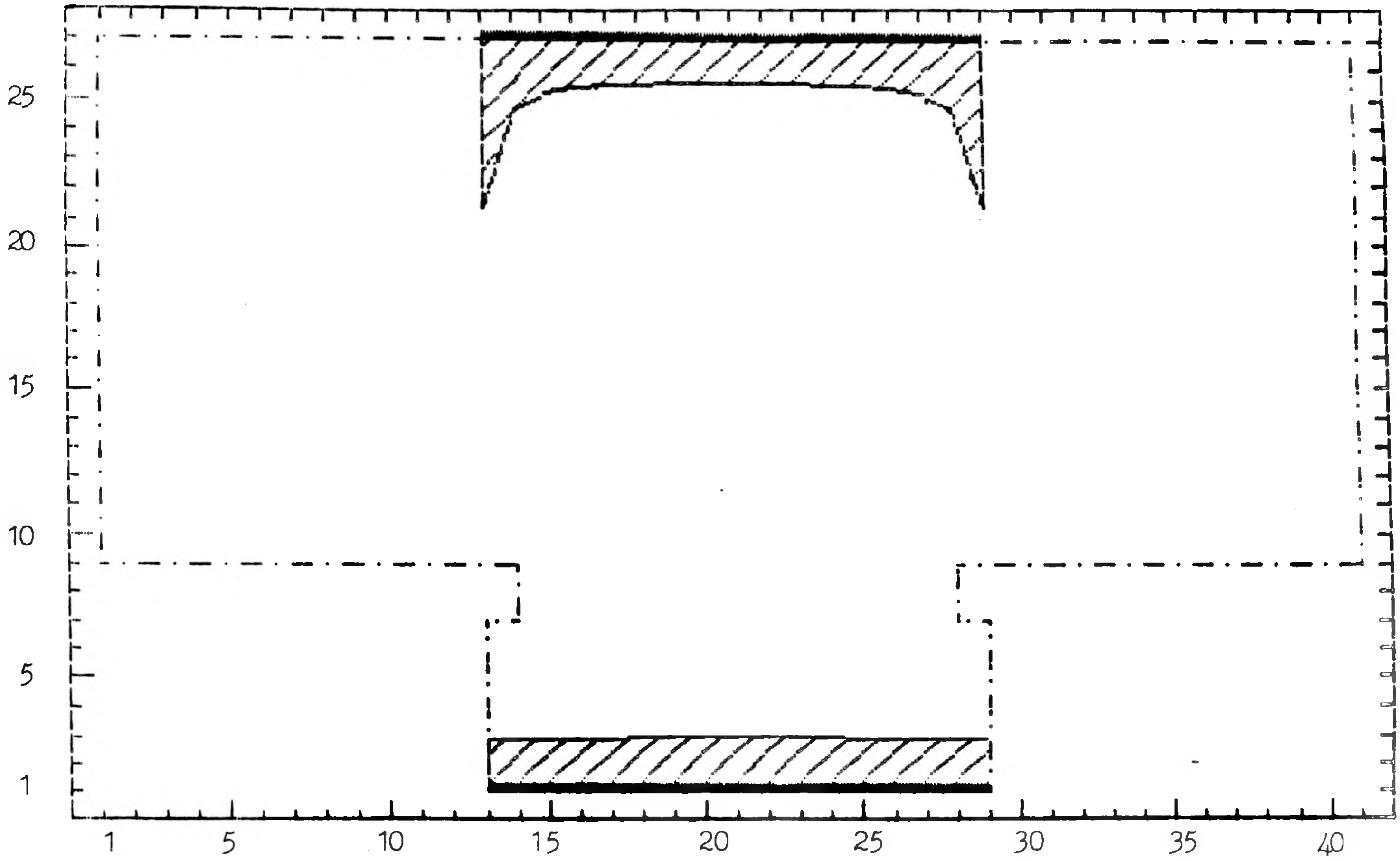


Fig. 4d. Result of computer calculations of current density distribution in a plating fixture.

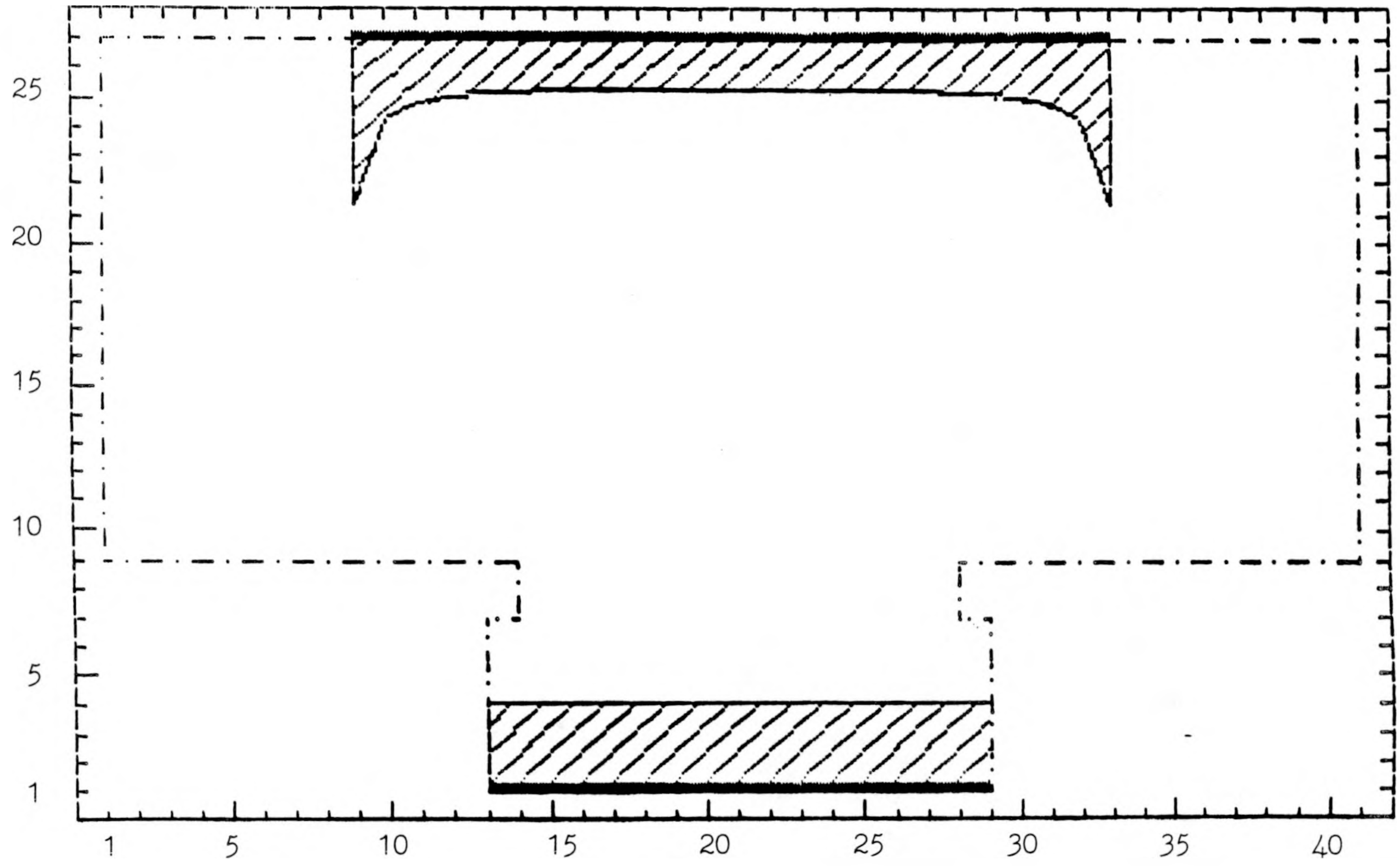
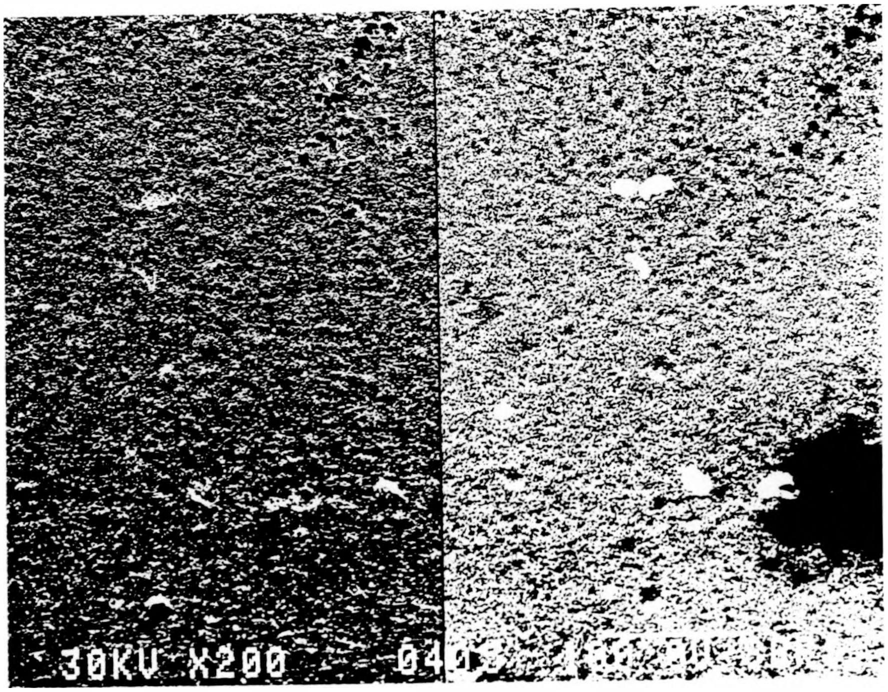


Fig. 4e. Result of computer calculations of current density distribution in a plating fixture.

bution (Fig. 4d). This value is very similar for a 6 cm wide anode as depicted in Fig. 4e.

These calculations offered us a starting point to build a proper fixture for large area plating. The substrate holder was machined in a way that allowed us to change the size of the obstructions which were placed along the two edges of the substrate where the electrical contacts to the Mo surface were made. The effect of the IR drops on the uniformity of the plated films was studied using the Atomic Absorption Spectrophotometry. In these experiments large plated substrates were cut into small pieces of equal area and the thicknesses of the films were calculated using AAS results. This way thickness maps of large area films were obtained. As a result of these experiments the plating fixture design of Fig. 4e with 2cm deep well was adopted. This design gave us a uniformly plated area of about 30 cm^2 in the middle of 40 cm^2 area samples.

With the above design of the plating fixture we were able to overcome the macro-scale thickness non-uniformity problems for the electroplated layers at least in a defined area in the middle of the sample. Occasionally observed micro-scale non-uniformity and especially the poor adhesion of the CIS films to Mo substrates, however, did not allow us to make high efficiency large area devices on these films. The micro-scale non-uniformity originated from the substrate-sensitive nature of the electrodeposition process. Cu plating, for example, is a very sensitive function of the Mo surface. In a large area substrate, local differences in the surface of the Mo layer were found to affect Cu plating in the vicinity of that area. This non-uniformity was then reflected into the In deposition step because In plates very well on uniform Cu layers whereas the plating efficiency drops drastically if there are any non-uniformities in the Cu film, exposing the Mo substrate to the In plating solution. Fig. 5. shows the SEI and EBIC images of an electrodeposited/selenized CIS film. The black spots in the EBIC image, especially the dark area on the lower right hand side, are indicative of local non-uniformities in the material. Y-modulated EBIC map of the junction area of a device made on this film is shown in Fig. 6. A large variation in the device response can be observed in this figure, again indicating micro-scale non-uniformities in the stoichiometry of the CIS layer. It should be noted that these problems are largely alleviated when working with small substrates because the control of the surface uniformity of the Mo substrate as well as the Cu and In layers is much easier for such samples.



SEI

EBIC

Fig. 5. SEI and EBIC images of an electroplated/selenized CIS film showing local defects (dark areas in the EBIC picture).

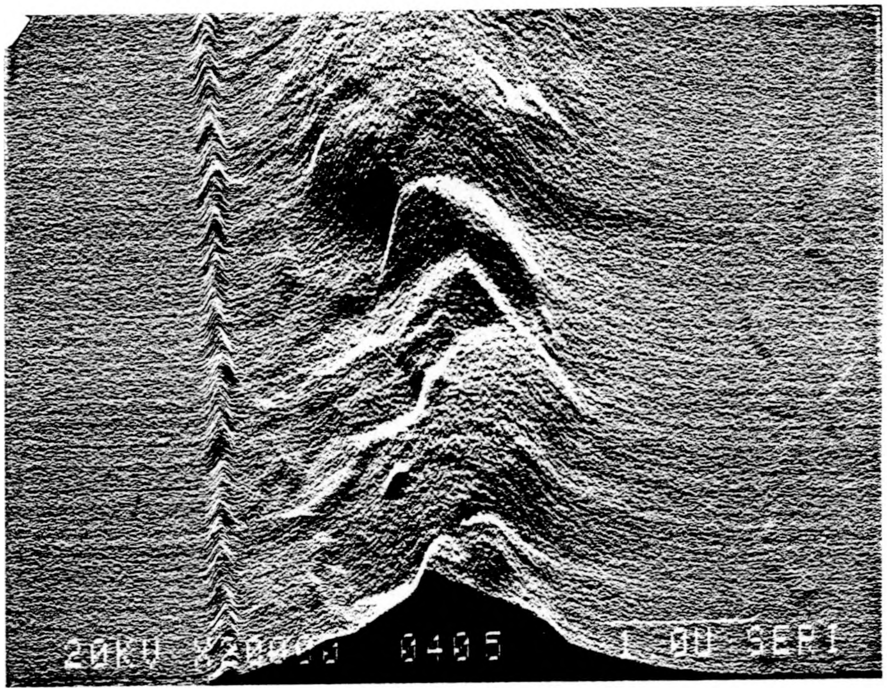


Fig. 6. Y- modulated EBIC map for a CdS/CIS device made on the film of Fig. 5 showing non-uniform response.

3.2.4 Adhesion

As we have previously reported, electroplated and selenized Cu/In stacked layers frequently suffer from poor adhesion between the CIS film and the Mo coated substrate. This can clearly be observed from Fig. 7 which shows a cross sectional SEM picture of a typical CIS film prepared by the electrodeposition/selenization technique. The dark line between the CIS film and the Mo substrate is indicative of poor adhesion between the two films.

During this period of the research program we have conducted studies on the nature of this adhesion problem and tried to develop methods to improve the adhesion between the CIS films and their Mo coated substrates. Based on general observations that we have made during the course of our studies, causes for the poor adhesion of the CIS film can be explained as follows:

In the device structure of glass/Mo/CIS/CdS, a layer of copper is first electrodeposited onto the Mo surface. The copper layer is then followed by an electrodeposited layer of indium. The stacked layers are then selenized in an H_2Se atmosphere. Copper and Mo do not alloy under the conditions of this reaction. Therefore, there is not any bonding interface that could promote the adhesion of CIS to the Mo after selenization. Thus the Mo/Cu interface is a weak one to begin with and this interface is subjected to stresses originating from various sources in the process of forming films. The possible stress generating sources are:

a) Stresses and pin holes in the Mo film as deposited on the glass substrate.
b) Differing thermal expansion coefficients of the glass substrate, Mo, Cu, In and CIS films.
c) At least three fold volume expansion of films due to the formation of CIS.
d) Oxygen and moisture in the glass/Mo/Cu/In stack.
e) Stresses caused by the reaction of hydrogen selenide with the Cu/In stack.

We will now examine each of these possible sources of stress to the film in more detail.

a) The glass/Mo substrate is prepared by depositing Mo on glass either by sputtering or by evaporation (electron beam evaporation). In either case the deposited Mo film can be under stress and contain pinholes if the deposition conditions are not properly optimized. When CIS films are fabricated on stressed Mo films,

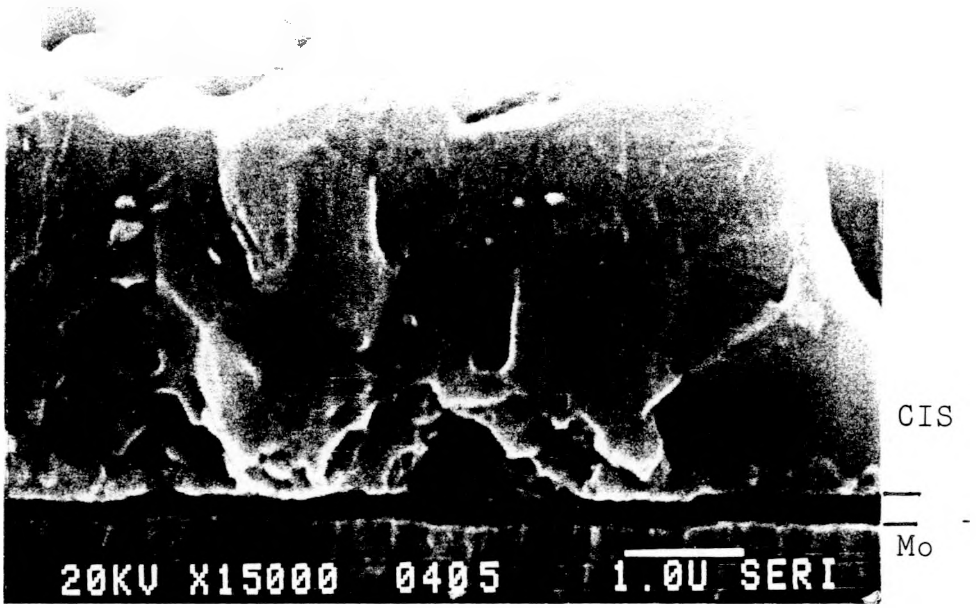


Fig. 7. Cross sectional SEM of a CIS/Mo structure. The gap between the Mo and CIS films is indicative of poor adhesion.

peeling of CIS films is a common occurrence. In the ISET labs we prepare the glass/Mo substrate by the electron beam evaporation technique. We have optimized our deposition process to obtain glass/Mo substrates free of stresses and defects and thus results presented in this report have not been affected by any problems associated with the poor mechanical properties of the Mo layer.

b) The linear thermal expansion coefficients of the various layers used in the present process are:

Soda Lime glass	9.2 X 10^{-6}/ deg. C
"7059" glass	4.9 X 10^{-6}/ deg. C
Molybdenum	5.0 X 10^{-6}/ deg. C
Copper	16.6 X 10^{-6}/ deg. C
Indium	24.8 X 10^{-6}/ deg. C
(However, Indium melts at 156.6 deg. C)	
CIS	8.0 X 10^{-6}/ deg. C

The thermal expansion coefficients of copper and indium are quite high compared to that of Mo and glass. However, since most of the films are very thin and since there is a liquid phase (due to In) in the films at temperatures of selenization it is thought that the contribution of stresses caused by the differences in thermal expansion coefficients is not the major factor causing poor adhesion.

c) During the formation of CIS films by the two-stage process, the volume of the Cu/In stack increases by at least a factor of three. We believe that this rather large change in volume is the major source of stress in CIS films and therefore is the major cause of poor adhesion. It is hypothesized that if selenium were to be present, simultaneously with copper and indium, during the deposition process, the stresses generated due to the volume expansion would be much less severe. This hypothesis is supported by the fact that CIS films deposited by the method of co-evaporation are reported to be free of stresses caused by volume expansion and that they are relatively free of adhesion problems. In the two-stage process that we use, this stress generating source is unavoidable, but it can be tolerated by promoting the bond strength of the Mo/CIS interface.

d) We have observed that if the stacked metal films are heavily oxidized or contain moisture (physically adsorbed water from the aqueous plating process) or if there is a leak in the selenization system, blistering begins to appear in the CIS films after selenization. The blisters are the result of the CIS film lifting from the substrate. This source of poor adhesion can be eliminated by properly drying the stacked metal films, by avoiding excessive oxidation of the metallic films, and by removing the sources of air leakage into the selenization reactor.

e) H_2Se gas reacts with copper and indium to form CIS. This reaction is quite exothermic. It is possible for the final CIS film to be stressed because of the kinetics of this reaction. This source of stress can also be reduced by optimizing the partial pressure of H_2Se gas in the reaction gas mixture. This way the kinetics of the selenization reaction can be slowed to minimize the stresses that may result from an accelerated reaction.

After minimizing the stress generating sources in the selenization reaction to the extent possible the next step in trying to improve the adhesion of the CIS film to the Mo layer was to enhance the bond strength at the Mo/CIS interface. Various experiments were carried out for this purpose:

i) In some of the earliest experiments we tried alumina substrates with somewhat rougher surfaces than the glass substrates. Alumina/Mo substrates were prepared in a similar fashion to the glass/Mo substrates and the CIS films were fabricated by the usual two-stage process. The idea behind this experiment was to use mechanical interlocking of the CIS film with the relatively rougher morphology of alumina to promote adhesion. CIS films fabricated on the Alumina/Mo substrates, however, showed no improvement in adhesion.

ii) Another observation made during the course of these experiments was that CIS films that were off-stoichiometric in either the copper-rich or indium-rich directions seemed to adhere well to the glass/Mo or the Alumina/Mo substrates. In fact it was discovered that pure copper selenide or pure indium selenide films had very good adhesion to the glass/Mo substrates. But these adhering films did not result in devices that performed well. Whenever we fabricated stoichiometric CIS films the films showed poor adhesion. This observation indicates that either the magnitude of stresses in stoichiometric CIS films is higher than that in non-stoichiometric CIS films or that the presence of the binary phases (Cu-selenide and In-selenide) in off-stoichiometric films improves the bonding between the Mo layer and the CIS film. We believe that the latter is the case.

iii) In our attempts to strengthen the Mo/Cu-In interface we have carried out experiments where the Cu/In stacked layer was alloyed for long periods of time in hydrogen atmosphere or in vacuum before the film was subjected to selenization. The aim of these experiments was to enhance any chemical bond between the Mo layer and the Cu-In alloy. But no repeatable adhesion improvement was observed in samples processed this way.

iv) We have attempted to prepare a bi-layer CIS film structure by first obtaining a well adhering Cu-rich CIS film on a Mo coated substrate and then electroplating over this Cu-rich layer a second set of Cu and In films corresponding to a low Cu-to-In ratio and then selenizing the whole structure once again. The difficulty faced in this case was that the second set of Cu and In platings were out of control because especially the Cu plating was very much affected by the nature of the underlying low-resistivity CIS film. This is a result of the surface-sensitive nature of the plating process.

It should be noted that the adhesion problem discussed in this section has now been solved in evaporated and selenized films. In the evaporation/selenization approach, we were able to improve the bond strength between the CIS film and the Mo substrate in a way that allowed the fabrication of extremely well adhering films. The evaporation/selenization approach will be discussed later in this report in section 3.3.

3.2.5 Film Characterization

The mechanical characteristics of electroplated/selenized films have been described in the previous section. The structural characteristics of these films were examined by SEM. The general observation was that the films with Cu-to-In ratios close to stoichiometry had a rough surface morphology and a grain size that was larger than 1 micron (see for example Fig. 7). Indium rich compositions (especially those with Cu-to-In ratio of less then 0.9) had a shiny surface with sub-micron size grains. The resistivity of the films were measured by peeling and transferring them onto insulating substrates. Resistivity values for films that yielded the best devices were found to be around 50-500 ohm-cm range. Several microprobe measurements made at SERI indicated that the stoichiometric uniformity was good for samples that were prepared using the small area plating fixture. Stoichiometric non-uniformities were detected, however, on large area samples that were prepared by the 50 cm^2 plating fixture. The reader is referred to our previous reports [1,2,3,4,5,6] for details of measurements made on electroplated/selenized CIS films.

3.2.6 Solar Cells

Majority of the devices were fabricated by evaporating CdS window layers over the CIS surfaces. There was no special treatment of the CIS surface before the CdS evaporation and the CdS layers had the commonly used bi-layer structure. First a 0.4-0.6 micron thick high resistivity undoped CdS film was evaporated on the CIS surface. This was then followed by a 0.6-0.9 micron thick In-doped layer which brought the overall sheet resistance of the composite film to 20-40 ohms/square range. Evaporated aluminum fingers were used as the top contact to these devices.

During this phase of the program we have also carried out some experiments on the use of chemically deposited CdS window layers in CdS/CIS solar cells. Chemical deposition (also known as dip-coating or solution growth) is a technique that is known to yield thin layers of near-stoichiometric, highly transparent CdS films. In our work we have used a solution with the following composition to obtain thin films of CdS on CIS.

Cd^{++} as 1.0 M $CdSO_4$,		15 ml
NH_4OH	14.5 M	40 ml

These two reagents were mixed with 85 ml of D.I. water and warmed to 75°C. A CIS coated substrate was placed in the container with the above solution mixture and 30 ml of 1.0M thiourea solution was then added into the container with vigorous stirring. After 45 minutes, a coating of CdS that appeared to be powdery at the surface was obtained. On brushing away the powder, an underlying smooth and continuous film of CdS about 2,500Å was obtained. The device fabrication was completed by evaporating another layer of doped CdS to make a total thickness of CdS to be 1.5 microns. Similar devices were also fabricated using identical plating conditions but without the solution coated CdS. On comparing the performance of devices with or without the solution coated CdS, it was observed that, in general, the open circuit voltages (V_{oc}) in the CIS/CdS devices increased when solution coated CdS was used. The V_{oc} increase in such devices ranged between 12% to 19% over those with evaporated CdS layers. The short circuit current density values decreased when the thickness of the solution coated CdS was either >0.3 microns or < 0.05 microns.

It should be noted that the devices made on electroplated/

selenized CIS films had areas ranging from 0.1 to 1 cm^2. These devices were fabricated on 1-2 cm^2 area films. Fabrication of larger area devices on the 50 cm^2 substrates was difficult because of the adhesion problems and stoichiometric non-uniformities as discussed in the previous sections. However, we have made many small area cells with 7-8 % efficiency without A/R coating using the electroplating/selenization approach. These devices were very similar to those previously reported [4,5,6]. We have also fabricated a cell with an efficiency exceeding 10 % as was reported in our previous report [3]. The highest cell parameters measured on electroplated/selenized cells under 100 mW/cm^2 ELH illumination were around 0.45 V, 35 mA/cm^2 and 0.68 for the V_{oc}, J_{sc} and FF respectively. Typical values, however, were in the range of 0.4 V, 30 mA/cm^2 and 0.60.

3.3 Evaporation/Selenization Process

During the last six months of this project we redirected our research effort to obtain CIS films of various stoichiometries by the two-stage process using vacuum evaporation technique for metal deposition instead of electroplating [7]. In this method, Cu and In layers were first evaporated onto Mo-coated glass substrates in the form of stacks, and then they were selenized in an H_2Se atmosphere at 400°C to form CIS films. Heterojunction solar cells with a structure of Transparent Conductive Oxide (TCO)/CdS/$CuInSe_2$ were fabricated on these films and conversion efficiencies close to 11% were obtained.

3.3.1 Deposition of CIS Films

Mo-coated glass substrates were used in this work. Most of the glass substrates were Corning 7059, although some soda-lime glass samples were also used. Mo films were deposited in an E-beam evaporator to a thickness of 2-2.5 microns. The nominal sheet resistance of a glass/Mo substrate was 0.08 ohms/square. Substrates were degreased and prepared for Cu and In evaporation.

In the early experiments metal depositions were carried out in a thermal evaporator at a pressure of $5x10^{-5}$ Torr. A Mo dimple boat with alumina barriers was employed as the evaporation source. Cu and In layers were deposited on the Mo coated substrates and glass witness slides using 4-9's pure Cu and In charges. Substrates were not intentionally heated during the evaporation. Deposition rates were monitored by a crystal rate monitor and they were kept at around 30 Å/second. The thicknesses of the Cu and In layers were varied to obtain CIS films of differing stoichiometries. During the last 3 months of the research program we have prepared our E-beam evaporation system for Cu and In evaporations. The existing tooling was modified to permit the addition of a thickness monitor into this system. The rotating mechanism of the four-pocket hearth was also repaired and activated so that the Cu and In evaporations could be carried out in one pumpdown. Cu films were typically 0.2 um thick. The thickness of the In layers changed from 0.45 to 0.5 um depending upon the desired stoichiometry of the compound.

After the evaporation, the substrates were removed from the vacuum chamber and placed into a tube furnace for selenization. Selenization was carried out for 1 hour at 400 °C in an 95% Ar + 5% H_2Se atmosphere. In some of the experiments an attempt was made to simulate the double-layer structure of the Boeing cells. In these experiments, first a 2 um thick Cu-rich CIS layer was deposited onto the Mo coated glass substrate. This was achieved by evaporating and selenizing Cu and In layers corresponding to a Cu-to-In ratio of around 1.1. After the selenization step, another elemental layer with Cu-to-In ratio of 0.7 was deposited over the first selenized film and then the whole structure was again selenized briefly for about 10 minutes. The thickness of the second layer in these samples was 0.8 um.

3.3.2 Film Characterization

Selenized films were analyzed by SEM and X-ray diffraction techniques. Resistivity measurements were made on witness samples prepared on glass slides. Fig. 8 is a X-ray diffraction pattern for a CIS film prepared by the two-stage process utilizing E-beam evaporation. The intense peaks observed at 2θ values of 40.52 and 73.7 degrees are due to the Mo coated substrate. Table 1 gives the "d" values and the relative intensities of the CIS peaks of Fig. 8 and compares them with the previously published data. It should be noted that all of the characteristic peaks associated with the chalcopyrite phase of this material (i.e. <211>, <103>, <101> and <105><213> peaks) have been observed in this diffraction data.

The grain size of a CIS film prepared by the co-evaporation technique is known to be a function of its stoichiometry. Films with Cu-rich compositions have larger grains than those with In-rich compositions. Although the two-stage method is quite

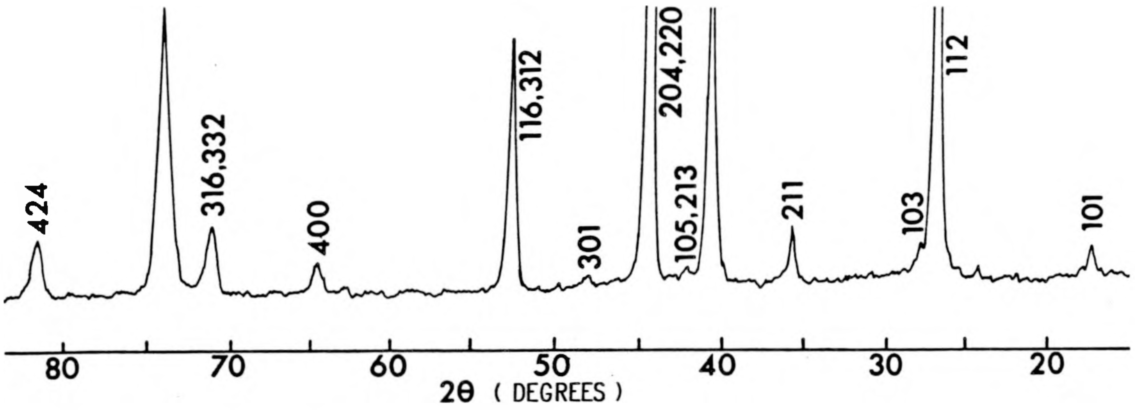


Fig. 8. X-ray diffraction pattern of a CIS film obtained by the evaporation/selenization method.

Table 1. X-ray diffraction data for a CIS film prepared by the evaporation/selenization process. Calculated values are from [9].

hkl	Calculated I/I_0	Calculated d	Observed d	Observed I/I_0
101	4	5.2	5.16	2
112	100	3.34	3.34	100
103	4	3.22	3.21	3
200	2	2.89		
211	8	2.52	2.52	4
105,213	4	2.15	2.15	1
204,220	65	2.04	2.04	55
301	5	1.9	1.9	1
116,312	43	1.74	1.74	20
305,323	5	1.48		
400	10	1.44	1.44	2
217,411	4	1.39		
316,332	15	1.32	1.32	5
325	5	1.32		
415	4	1.2		
424	21	1.18	1.18	5
501,431	4	1.15		
336,512	8	1.11	1.11	3 (possible Mo)

different from the co-evaporation technique, we have observed a similar phenomenon in our evaporated/selenized films. The near-stoichiometric or Cu-rich films displayed grain sizes of the order of 1 um (Fig. 9a), whereas, the grain size decreased to around 0.1 um in films with In-rich compositions. Fig. 9b is a cross-sectional SEM of a CIS film with a Cu-to-In ratio of about 0.9.

Resistivities of the films were measured using samples prepared on witness glass slides. Early films obtained by evaporation from Mo boats showed resistivity values changing from 0.1 ohm-cm to over 10^4 ohm-cm as their Cu-to-In ratio changed from 1.1 to 0.7. Our later work concentrated on the E-beam evaporated samples and on a Cu-to-In ratio of about 0.9 where the typical film resistivity on glass substrates was 50-500 ohm-cm. Although these measurements give a general idea about the dependence of the resistivity on stoichiometry, the absolute values of the measured resistivities may not be readily applicable to samples grown on Mo coated substrates because CIS film characteristics are expected to be substrate dependent.

3.3.3 Device Fabrication

Both evaporated and chemically deposited CdS layers and evaporated CdZnS films were used for heterojunction device fabrication. The evaporated CdZnS layers were In-doped. They were 1.1 microns thick and they contained 15% Zn. The sheet resistance of the CdZnS films was 175 ohms/square. A 2000 Å thick Indium Tin Oxide (ITO) layer was sputter deposited over the CdZnS film to bring the sheet resistance down to about 20 ohms/square [8]. The evaporated CdS films had the commonly used two-layer structure that was obtained by first evaporating a 0.5 um thick undoped layer and then depositing on top of it a 0.8 um thick In-doped region. The substrate temperature and the deposition rate for CdS evaporations were 200 °C and 60 Å/sec respectively and the nominal sheet resistance of the composite CdS layer was 30 ohms/square. Aluminum was used as the top contact material in devices with evaporated CdS window layers. Chemically deposited CdS layers were 500-1000 Å thick and they were obtained by the solution growth method. Devices with the solution grown CdS layers also employed a Transparent Conductive Oxide (TCO) window which was sputter deposited onto the CdS layer. Both ITO and ZnO/ITO were used for this purpose and the nominal sheet resistance of the TCO window was 20 ohms/square [8]. Nickel was used as the top contact material for these devices.

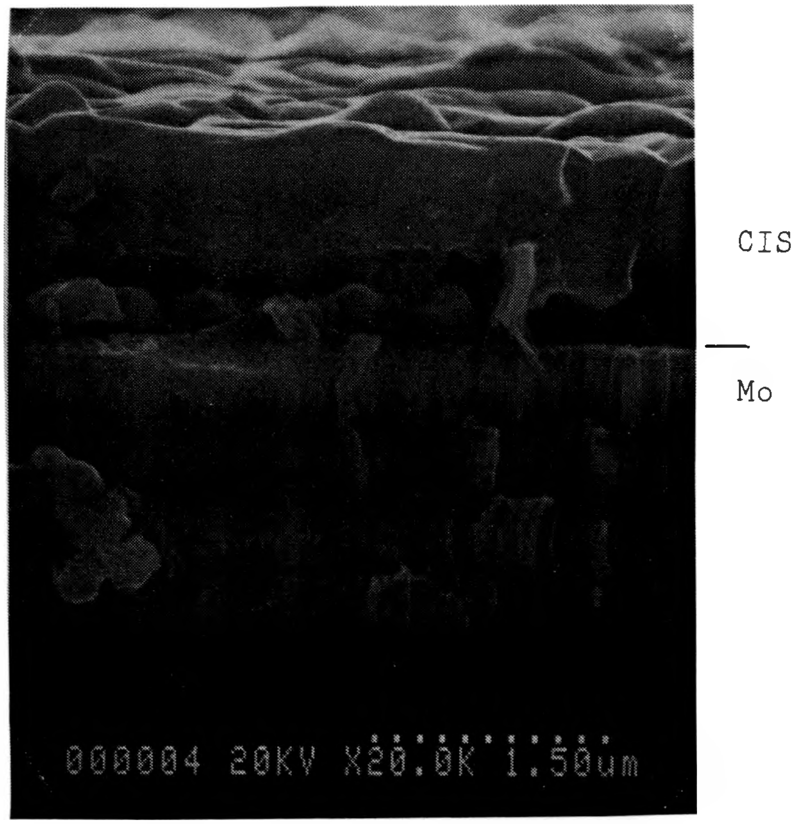


Fig. 9a. Cross sectional SEM of a near-stoichiometric CIS film prepared by the evaporation/selenization method.

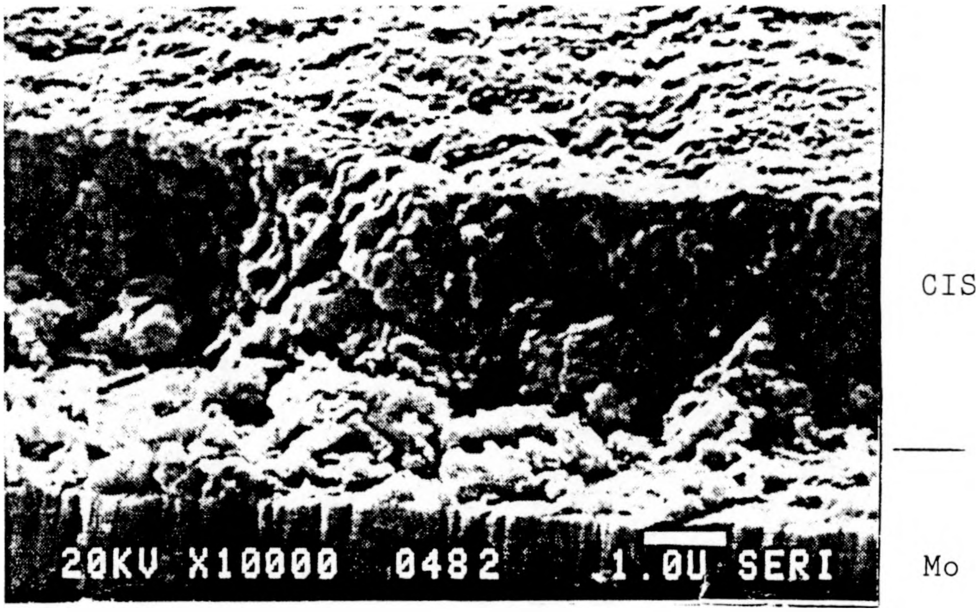


Fig. 9b. Cross sectional SEM of a CIS film prepared by the evaporation/selenization method. Cu-to-In ratio is around 0.9.

Fig. 10 is the illuminated I-V characteristics of a ITO/CdZnS/CIS solar cell measured at IEC under ELH simulation of 87.5 mW/cm^2. This device was fabricated on a CIS film with a Cu/In ratio of about 0.92 and the Cu and In films were evaporated out of a resistively heated boat. The photovoltaic parameters of the device are V_{oc}=0.332 V, J_{sc}=32.24 mA/cm^2, FF=56.91% and Eff. = 6.96%. The spectral response of the device of Fig. 10 is shown in Fig. 11. The response is seen to extend to 1.3 microns on the long wavelength side. The cutoff at the short wavelength region corresponds to the band-edge of CdZnS. The illuminated characteristics of another device with an evaporated CdS window layer is shown in Fig. 12. The CIS film of this device was prepared by selenizing E-beam evaporated Cu/In layers. The efficiency of the cell in Fig. 12 is around 7.4% as measured under 100 mW/cm^2 ELH illumination at ISET.

A solar cell was prepared with a double-layer absorber structure similar to that of Boeing's. A resistively heated Mo boat was used in evaporating the Cu and In layers for this device which also employed an evaporated CdS layer. The cell parameters were measured under 100 mW/cm^2 ELH illumination. The V_{oc} (0.45 V) and the FF (63 %) values of this solar cell were quite good. However, the J_{sc} (25 mA/cm^2) value limited the active area efficiency of the device to 7%. Poor long wavelength response of this cell led us to believe that the break introduced into the film growth process for the purpose of simulating the double layer structure also caused a break in the grain structure of the material and possibly introduced recombination sites which effectively limited the current collection to the top 0.5-0.8 um of the absorber layer.

The highest efficiency cells produced during this period employed a thin chemically deposited CdS layer and a Transparent Conductive Oxide film. Fig. 13 is the illuminated I-V characteristics of a solar cell which had a 0.1 um thick solution grown CdS layer and a sputter deposited ZnO/ITO window [8]. This device had a total area of 0.1 cm^2. Thicknesses of the ZnO and ITO layers were 0.8 um and 0.2 um respectively. The active area of the device was 0.075 cm^2. The solar cell parameters of Fig. 13 are: V_{oc}= 0.4627 V, J_{sc}= 35.36 mA/cm^2, FF= 66.59% and Eff.= 10.89 % (active area). Another group of cells fabricated on a similarly prepared film has yielded devices with active area efficiency values of 10.47%, 10.68%, 10.74% and 10.74% as can be seen in Table 2. The external quantum efficiency of the cell of Fig. 13 is shown in Fig.14. Good collection in the blue region of the spectra as compared to the

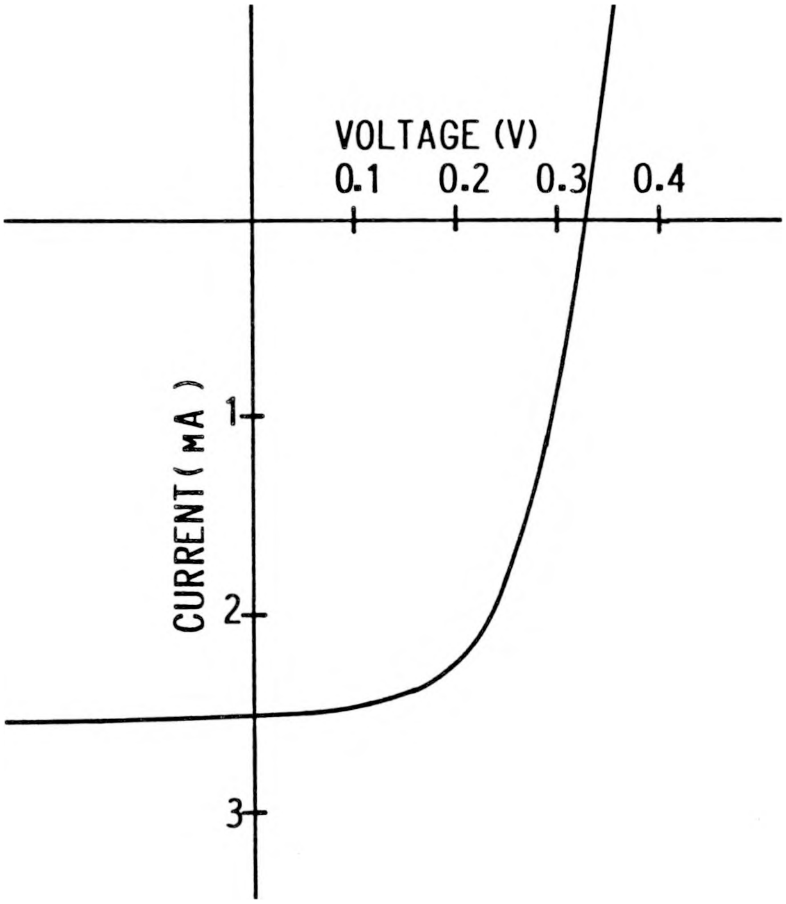


Fig. 10. Illuminated I-V characteristics of a ITO/CdZnS/CIS cell. 87.5 mW/cm² ELH illumination, 0.08 cm² area. V_{oc}=0.332 V, J_{sc}=32.24 mA/cm², FF=56.91 and Eff.=6.96%. (IEC measurement).

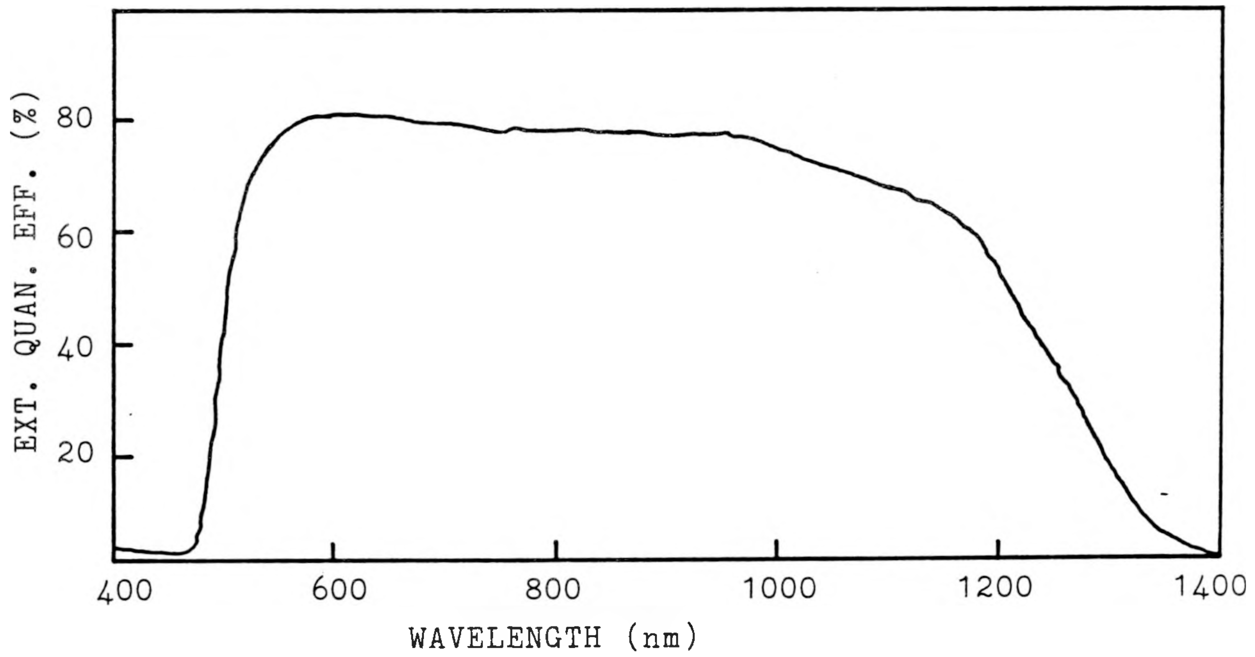


Fig. 11. Spectral response of the device of Fig. 10.

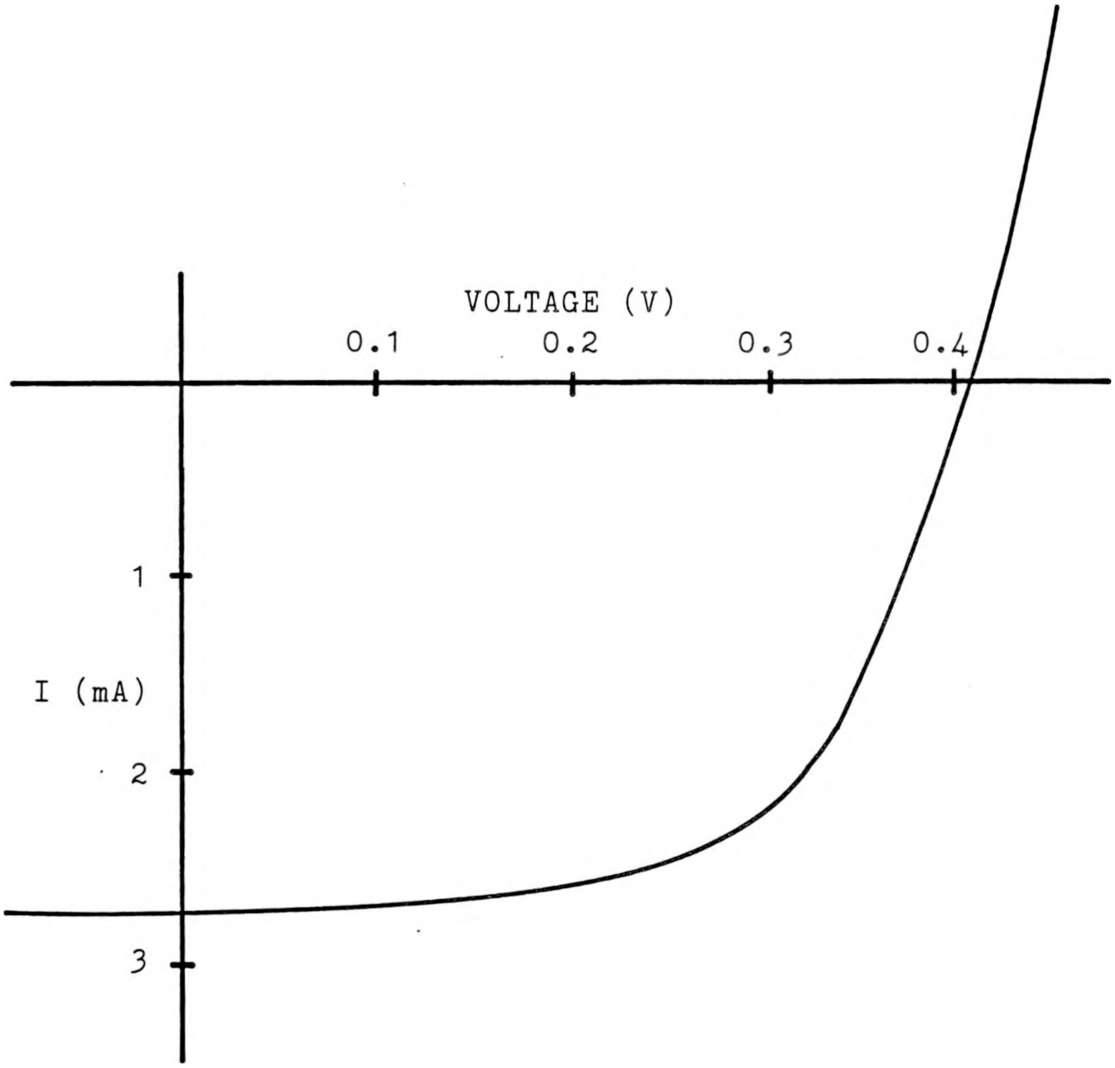


Fig. 12. Illuminated I-V characteristics of a CdS/CIS device. 100 mW/cm² ELH illumination, 0.09 cm² area. V_{oc}=0.41 V, J_{sc}=30.1 mA/cm², FF=60% and Eff.=7.4%. (ISET measurement).

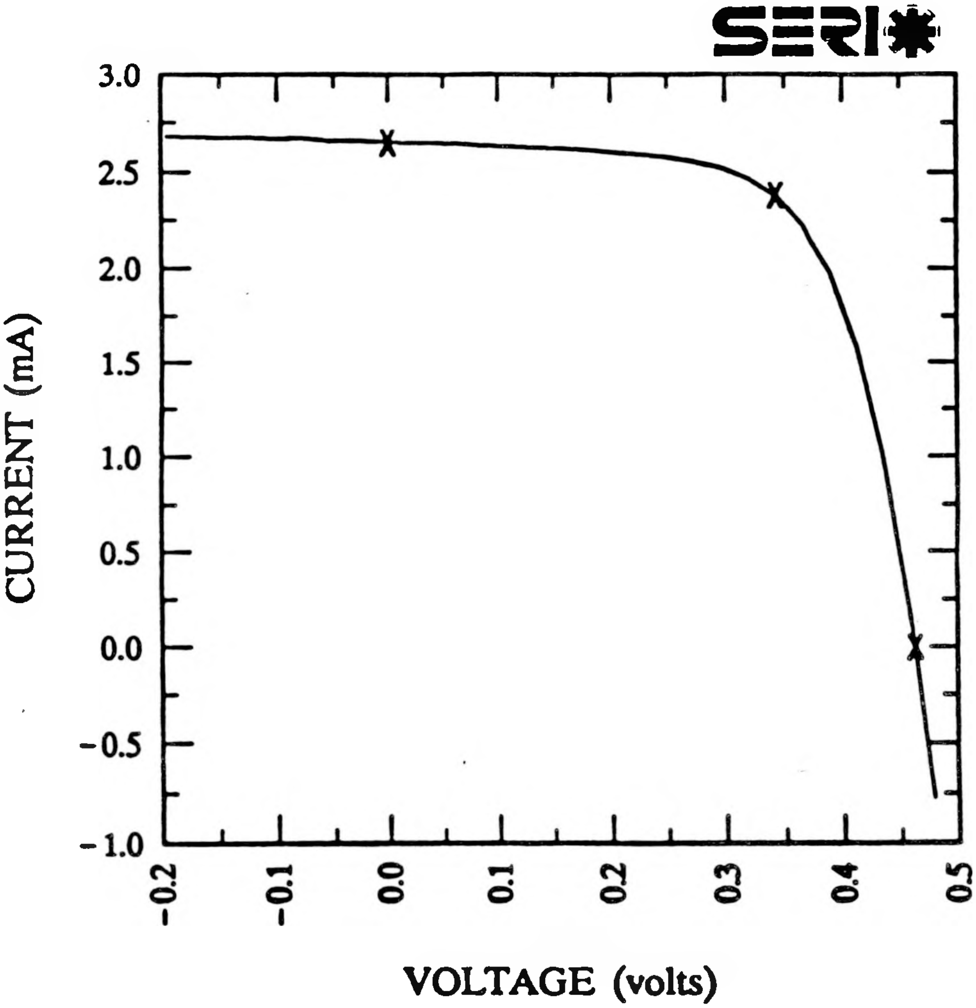
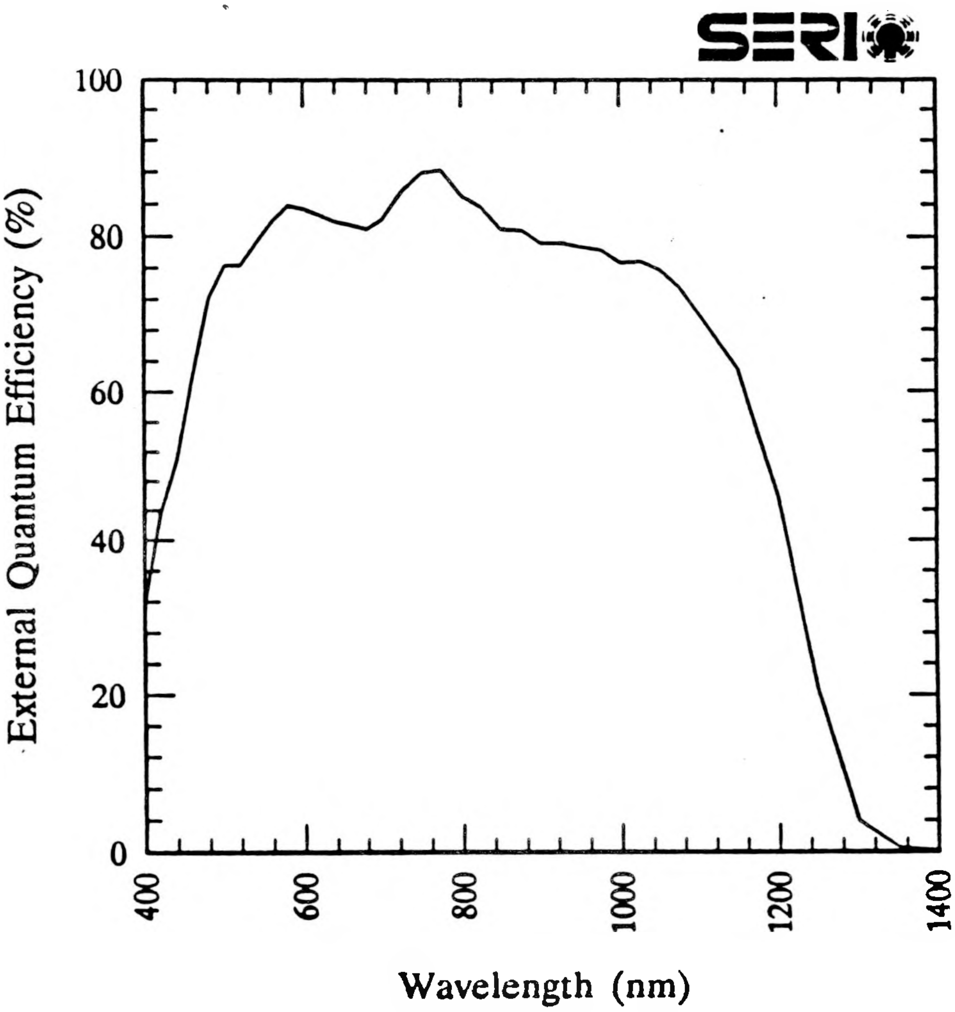


Fig. 13. Illuminated I-V characteristics of a 0.1 cm^2 device with 0.075 cm^2 active area. Device structure is CIS/solution grown CdS/ZnO/ITO. SERI Global AM1.5 spectra. Active area parameters: $V_{oc}=0.4627$ V, $J_{sc}=35.36$ mA/cm^2, FF=66.59 and Eff.=10.89%.

Table 2. Solar cell parameters of a group of CIS/solution grown CdS/ZnO/ITO devices.

Device No.	V_{OC}(V)	J_{SC}(mA/cm^2)	FF (%)	Eff. (active area)
CI-56-5	0.4650	35.48	63.50	10.47
CI-56-8	0.4589	34.5	67.46	10.68
CI-56-11	0.4656	34.29	67.28	10.74
CI-56-12	0.4585	36.0	65.06	10.74

Active Area = 0.075 cm^2



Light bias = 2.50 mA
Zero voltage bias

Fig. 14. Spectral response of the cell of Fig. 13.

device of Fig. 11 is due to the use of highly transparent CdS/ZnO/ITO window layer. Response at long wavelength region again extends to 1.3 microns as expected from a CIS cell.

4.0 CONCLUSIONS AND FUTURE PLANS

The two-stage process is a very promising and versatile technique for depositing polycrystalline thin films of I-III-VI_2 compounds for solar cell applications. In this work we have used the two-stage process to prepare high quality CIS films. Solar cells with active area efficiencies around 10% have been fabricated on films prepared by the selenization of electrodeposited Cu/In stacked layers. Evaporation/selenization approach has yielded devices with efficiencies approaching 11%. Further improvements especially in the short circuit current density values of these cells are expected to increase the conversion efficiencies to the 12-15% range in the near future. In our future work we will concentrate on the evaporation/selenization technique and fabricate large area devices and modules using this approach. This technique does not suffer from the adhesion problem which was the major obstacle for making large area solar cells on electroplated/ selenized CIS films.

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16. Abstract (Limit: 200 words)

This report describes a project to develop a high efficiency thin film $CuInSe_2$ solar cell using a low-cost process. The two-stage process involves depositing the metallic elements of Cu and In on a substrate in the form of stacked layers, and then selenizing this stacked metallic film in an atmosphere containing Se. Early research concentrated on the electrodeposition technique for depositing the Cu and In films on Mo-coated glass substrates. This resulted in small-area cells with around 10% efficiency, indicating that the technique could yield $CuInSe_2$ films with good electrical and optical properties. The program then involved scaling up the electrodeposition/selenization technique; fixtures for large-area plating were designed and built, but poor adhesion of the $CuInSe_2$ films to the Mo-coated substrates and the stoichiometric non-uniformities encountered in the large-area films hindered the efficiency of the devices. The latter part of the program explored a new approach to the two-stage process. An evaporation/selenization approach, where the elemental layers were evaporated onto the Mo-coated substrates for selenization. Solar cells have been produced with efficiencies approaching 11% using E-beam evaporated/selenized $CuInSe_2$ films.

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