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VACUUM DEPOSITED POLYCRYSTALLINE SILICON FILMS FOR SOLAR CELL APPLICATIONS

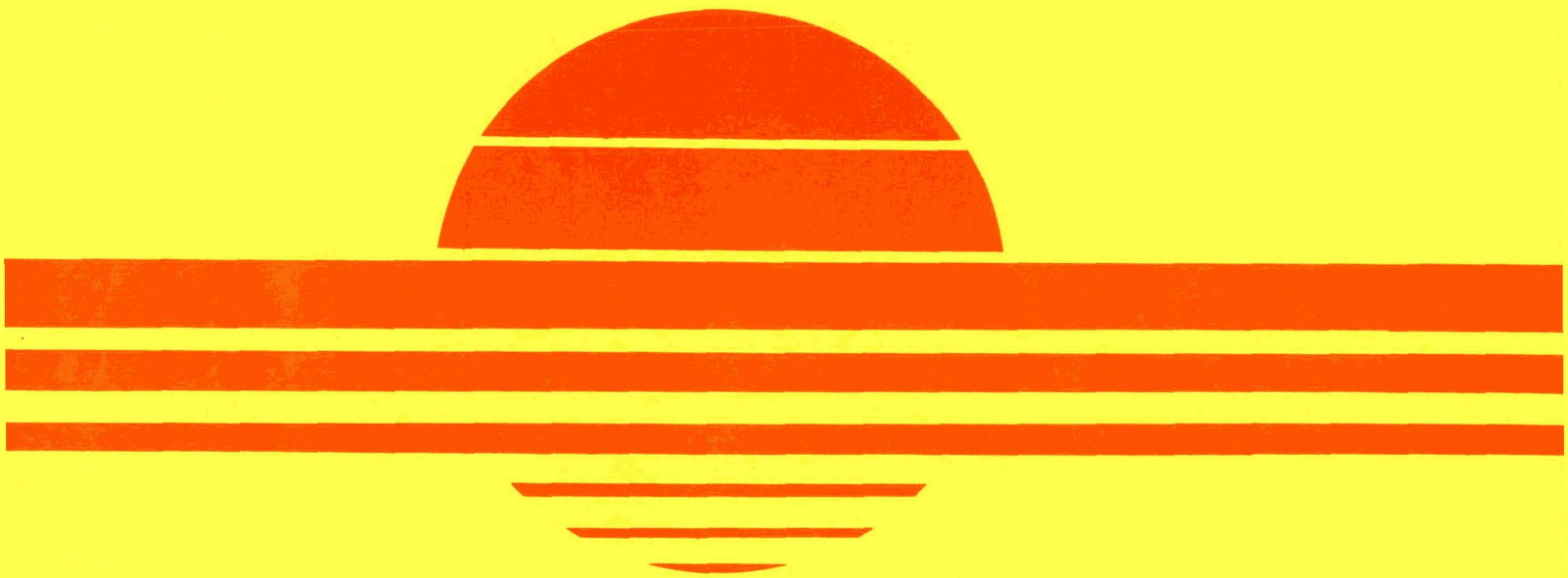
Quarterly Report for April 1—June 30, 1980

By
Charles Feldman
Charles H. Arrington, III
Norman A. Blum
Frank G. Satkiewicz

August 1980

Work Performed Under Contract No. AC02-77CH00178

The Johns Hopkins University
Applied Physics Laboratory
Laurel, Maryland



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THE JOHNS HOPKINS UNIVERSITY
APPLIED PHYSICS LABORATORY
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PREPARED FOR THE SOLAR ENERGY RESEARCH INSTITUTE
PHOTOVOLTAIC PROGRAM OFFICE
UNDER SUBCONTRACT XS-9-8278-1

This Quarterly Technical Progress Report covers the period April 1 - June 30, 1980, and describes work performed by the Johns Hopkins University, Applied Physics Laboratory for the Solar Energy Research Institute under Subcontract No. XS-9-8278-1. The Subcontract with SERI continues work previously supported for one year by DOE under Interagency Agreement No. ET-78-A-03-2208. C. Feldman is the Principal Investigator. Other professional staff members participating in this investigation are C. H. Arrington, III; N. A. Blum; H. K. Charles, Jr.; and F. G. Satkiewicz. Technical assistance was provided by R. B. Givens, K. G. Hoggarth, E. W. Koldewey, and R. Neuwiller.

DESCRIPTION OF PROJECT

This study addresses the goal of fabricating low-cost, 10% efficient solar cells through the use of vacuum deposited, thin film, polycrystalline silicon. Work areas include methods of growing large grains, exploration and optimization of suitable substrate/bottom electrode material, improvement in photovoltaic efficiency, formation of n-layer by vacuum deposition rather than by diffusion, and analysis of film and junction properties. Emphasis is placed at each stage of the program on understanding and elucidating the pertinent physical and electrical phenomena through the judicious use of analytical tools such as secondary-ion mass spectrometry for impurity and compositional analysis, and x-ray diffractometry and scanning electron microscopy for structure analysis.

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ABSTRACT

Polycrystalline p-type silicon films were vacuum deposited onto TiB_2 coated alumina and sapphire substrates. Epitaxial layers were also formed on single crystal silicon substrates. Junctions in the layers were created by both gaseous diffusion in a tube furnace and by vacuum deposition. The TiB_2 vacuum deposited bottom electrodes have resistivities between 30 and 40 $\mu\Omega$-cm.

All-vacuum-deposited solar cells were fabricated for the first time. Efficiencies approaching those in the diffused junction devices were achieved. The n-layers were deposited on the previously deposited p-layer/TiB_2/ceramic sandwiches by vacuum deposition of silicon in a phosphine (PH_3) atmosphere. Photovoltaic data in diffused junction samples, including efficiency and spectral response measurements, indicate that crystallite size may no longer be the limiting factor in achieving high efficiency; rather, performance is now being limited by the presence of impurities in the vacuum deposition silicon base region.

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1. INTRODUCTION

This is the Third Quarterly Technical Progress Report describing investigations on vacuum deposited thin-film polycrystalline silicon solar cells. The work was performed under Solar Energy Research Institute Subcontract XS-9-8278-1.

The study addresses the DOE goal of fabricating low-cost 10% efficient solar cells through the use of thin-film polycrystalline silicon. It is visualized that each step of the solar cell fabrication would be performed in a vacuum chamber and that the complete process could be carried out in a large scale mass production facility. Investigations being conducted at present correspond to the separate fabrication steps in the formation process.

Prior studies[1] under contract have led to the thin-film structure illustrated schematically in Fig. 1a. The high substrate temperatures lead to interactions between the layers, resulting in the structure illustrated in Fig. 1b. The formation of the titanium diboride bottom electrode has proceeded according to schedule so that consistently low resistivity, stable electrodes are now being formed on a more or less routine basis. The titanium silicide phase between the TiB_2 and the p-type silicon layer as shown in Fig. 1b. aids in the crystallite growth process. Diffusion of Ti from $TiSi_2$, and of Al from the substrate, however, appear to be occurring and will be discussed in Section 2.2.2.

No changes were made this quarter in the p-type deposition procedure. During the latter part of the quarter, a 12-position tantalum substrate holder was substituted for the 6-position holder. A description of the p-type layers formed is given in Section 2.1.

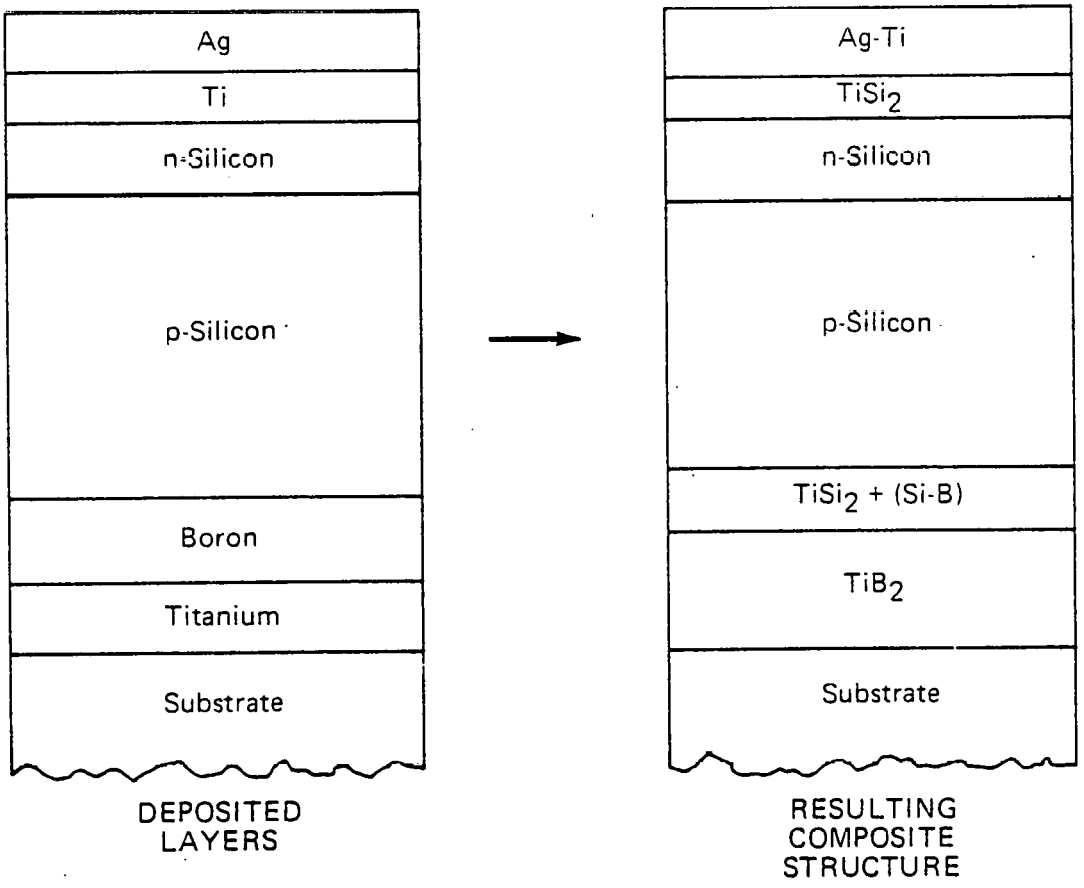

Fig. 1 Schematic layer diagram of vacuum deposited polycrystalline silicon thin film solar cell.

The n-type layers are being placed on the p-type layers to form the necessary junction by either diffusion or direct deposition. Variations in the diffusion process were carried out to explore possible differences between shallow and deep junctions. This will be described in Section 4. Research on vacuum deposition of the n-type layers, as described in Section 2.3, has led for the first time to an all-vacuum deposited cell with efficiencies approaching those achieved in the diffused devices. The top electrodes in the cell are now routinely being formed by evaporation of titanium and silver through the deposition masks.

As mentioned in previous quarterly reports, photovoltaic device efficiency appears to be limited by impurities within the p-type layer rather than by grain size. In order to determine the sources of the impurities, studies were conducted on those impurities which may arise from (1) the bottom electrode and substrate; (2) the vapor phase during deposition; and (3) the surface of the deposited layer due to cleaning (Section 2.2).

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2. SILICON FILM FORMATION

2.1 p-Type Silicon Films

Studies on both the p-type and the n-type vacuum deposited silicon layers continued this quarter. The n-type layers will be described in Section 2.3. The p-type silicon layers are listed in Table I. As can be seen from the table, silicon depositions on silicon substrates, at the substrate temperatures used, always result in epitaxial layers. Silicon on sapphire substrates frequently, but not always, result in epitaxial layers. This appears to depend on the particular deposition conditions. The samples deposited on substrates coated with TiB_2 electrodes and those deposited on silicon crystal slices were suitable for forming into complete devices. Some of these were used to form diffused junction devices while others were used in the study of the vacuum deposited junction devices. The samples used in device formation are indicated in the "Remarks" column of Table I. The last deposition (Si*250) listed in Table I employed a new tantalum substrate holder which contains twelve substrates plus an "N" substrate which is supported outside the heating zone for thickness measurements. Unfortunately, during this run (Si*250) the water-cooled crucible developed a leak and caused a thermal runway, briefly increasing the rate of deposition by an unknown amount before cut off. During each deposition two thermocouples were used instead of the usual single one. One thermocouple is inserted through the radiation shields in the top of the heater and the other is inserted in the side of the heater. Both thermocouples rest on the back of the substrates. The readings of both thermocouples are indicated in Table I. Variations in the substrate temperature and deposition rates are also indicated in the table. These variations were carried out to improve the purity in the films. Higher deposition rates should serve to reduce the concentration of impurities arriving in the film from the vapor phase, while reduction in the substrate temperature during deposition should

TABLE I

SILICON FILM DEPOSITION PARAMETERS

Sample	Substrate	Sub. Temp. (°C)	Thickness (μm)	Deposit Rate Å/Min	Remarks
Si*245A	Alumina				
B	Sapphire/$TiB_2$279C	1290(2)			Diffused Junct.
C	Sapphire/$TiB_2$297D			615,1st hr/(3)	Diffused Junct.
D	Alumina			705,4 hrs	Etch Test
E	Alumina/$TiB_2$297B	1250			
F	Sapphire				
G(1)	Sapphire		19		
Si*246A	Si X-tal				Epi. Diff. Junct.
B	Alumina/$TiB_2$300B	1300(2)			Deposit Junct.
C	Alumina/$TiB_2$303F				Deposit Junct.
D	Sapphire/$TiB_2$303M				
E	Alumina/$TiB_2$303E	1270			Diffused Junct.
F	Sapphire/$TiB_2$303B				
G(1)	Sapphire		21	683,5 hrs.	
Si*247A	Sapphire/$TiB_2$302L				
B	Alumina/$TiB_2$304J	1220(2)			
C	Si X-tal				Epitaxy
D	Alumina/$TiB_2$301B				Peeled
E	Sapphire/$TiB_2$304E				Deposit Junct.
F	Sapphire				
G(1)	Sapphire		13	446,5 hrs.	
Si*248A	Sapphire/$TiB_2$305K				
B	Sapphire/$TiB_2$305A	1207(2)			
C	Alumina/$TiB_2$305D				
D	Si X-tal			615,1st hr/(3)	Epitaxy
E	Alumina/$TiB_2$305C	1243		1600,4 hrs.	Diffused Junct.
F	Sapphire				
G	Sapphire		42		
Si*249A	Alumina/$TiB_2$304A	1250,1st hr/(2)			
B	Sapphire/$TiB_2$303D	1050,4 hrs.			
C	Si X-tal				
D	Si X-tal				Epitaxy
E	Sapphire/$TiB_2$305B	1244,1st hr./			
F	Sapphire	1050,4 hrs.			
G(1)	Sapphire		19	627	
Si*250A	Alumina	1257,1st hr./(2)			(Crucible Leak)
B	Alumina/$TiB_2$305G	1047,1 hr,20m			
C	Si X-tal				Epitaxy
D	Alumina/$TiB_2$305J				
E	Alumina/$TiB_2$306E				Deposit Junct.
F	Sapphire/$TiB_2$307H				
G	Alumina				
H	Sapphire/$TiB_2$307L				
J	Sapphire/$TiB_2$301J				
K	Si X-tal	1276,1st hr./			Epitaxy
L	Sapphire	1050,1hr,20m			
M	Sapphire/$TiB_2$301K				
N(1)	Sapphire		12	700,1st hr./ (?), 1 hr. 20 min(3)	

(1) Substrate located outside hot zone for thickness measurements.

(2) Thermocouple inserted from side of heater rather than through top.

(3) Approximate rates estimated from beam power.

aid in reducing the diffusion of impurities from the $TiSi_2/TiB_2$ layers. The temperature variations are carried out so that the titanium silicide is formed in the first three to five microns, the temperature is then reduced to prevent further formation of the silicide while maintaining the large crystal growth already formed due to the presence of the titanium silicide.

2.2 SIMS Impurities Analysis of p-Type Samples

It was pointed out in the last quarterly report, and re-emphasized in Section 4 of this report, that the impurities rather than grain size seems to be limiting the efficiency of the thin-film devices. Efforts to achieve large grains have required the deposition of silicon onto TiB_2 at a relatively high temperature (1250°C). This is a higher temperature than was used in the beginning of the study, and as a consequence there must be a careful reevaluation and subsequent elimination of the sources of impurities. The results of impurity analyses of several films were presented in Table II of the last quarterly report. The impurities of interest listed in that table were carbon, aluminum, titanium, chromium, and molybdenum. Each one of these impurities, with the exception of carbon, has recently been shown to be detrimental to the efficiency of silicon photovoltaic devices at the levels observed in the samples. Ti and Mo are particularly bad, even at low concentrations. The most detrimental reported was tantalum; however, the amount of Ta in the film is not known since tantalum is used extensively in the SIMS equipment and there is, therefore, always a Ta^+ background in the ion spectra. Some sources of Mo were discovered and eliminated during the last quarter. It is possible that one source of chromium is the same flaked Cr-plated screwdriver blade discussed in Section 3. During this quarter efforts were made to distinguish between impurities which arise from the substrate and/or TiB_2 and those which arise from the vapor phase during deposition. These studies will be described below.

2.2.1 Qualitative SIMS Analysis of a Si/TiB_2 Interface from a Peeled Sample (Si*247D/$TiB_2$301B/Ceramic)

On a rare occasion, the silicon layer peels or parts from the TiB_2/Al_2O_3 substrate; advantage is taken of these situations in order to carry out analysis at interfaces. It is believed that the reason for the lack of adherence and parting of the silicon is the presence of excess boron on the surface of the TiB_2 that was not removed by the usual vacuum heating. This might have occurred, for example, when the layer of excess boron was too thick to be removed in the time required or when the water vapor background was perhaps not sufficient. In this particular sample excess boron was verified by both the polyatomic and elemental spectra. Observed in the spectra were Al^+, Si^+ along with AlB^+ and SiB^+. In addition, the alkali metal ions, Cr and Mn were present. The sources of chromium and manganese on the TiB_2 may be related with some certainty to the heating arrangement used during the TiB_2 formation process. This will be discussed in Section 3. The aluminum observed in the spectra may arise from the Al_2O_3 substrate and is not desirable since it is clearly available at this interface for diffusion into the silicon. After sputter removal of approximately 3,000 Å the spectrum revealed stoichiometric TiB_2.

2.2.2 Impurity Profiles in Silicon Films

A comparison of the profiles of detectable impurities were made between a sample deposited on sapphire alone (Si*250A) and a sample deposited on TiB_2-coated sapphire (Si*250J). Since the Si*250 samples were deposited under different conditions than usual due to a thermal runaway of the source, the impurity concentrations of another sample (Si*248A) which was deposited without changing temperature or deposition rate were also examined. A defocused beam of 10 keV argon was used to sputter the samples. This was done in an atmosphere of oxygen in order to extend the detection limits. A correction factor from the

background contribution and from the added oxygen was determined from Wacker single crystal silicon and applied to the carbon peak intensity. In addition, the ion yield of carbon using the focused beam without oxygen was used. While the levels indicated in the profiles may not be exactly correct, the trends with depth and comparison between samples are expected to be valid.

The profiles for carbon, aluminum, titanium, and chromium as functions of depth from the surface are shown in Figs. 2 to 4. An examination of the aluminum profile in Fig. 2 indicates that the silicon deposited on a bare substrate has no detectable aluminum beyond 1.5 μm from the surface, while silicon deposited on the TiB_2 substrate has an aluminum signal going far beyond this point. This tends to indicate that aluminum is coming from the TiB_2/Al_2O_3 complex and is consistent with the study described in the previous paragraph on the peeled sample where aluminum was observed at the TiB_2 surface. Evidently an Al_2O_3-TiB_2 interaction occurs during the TiB_2 formation step.

A study of the chromium profile in Fig. 2 shows that the profiles in samples with and without TiB_2 are essentially the same indicating that, at this depth at least, most of the chromium is coming from the vapor phase during the deposition.

Fig. 4 shows the carbon profile in the three samples under study. These profiles seem to indicate that the source of carbon is neither related to the TiB_2 nor to the substrate, but must be related to the vapor phase.

An examination of the titanium profile in Fig. 3 shows that most of the titanium arises from the back TiB_2 electrode; however, the rise of titanium at the surface indicates that there is a contribution from a vapor source. This is supported by the results of last quarter's work, as indicated in Table II of that report.[1]

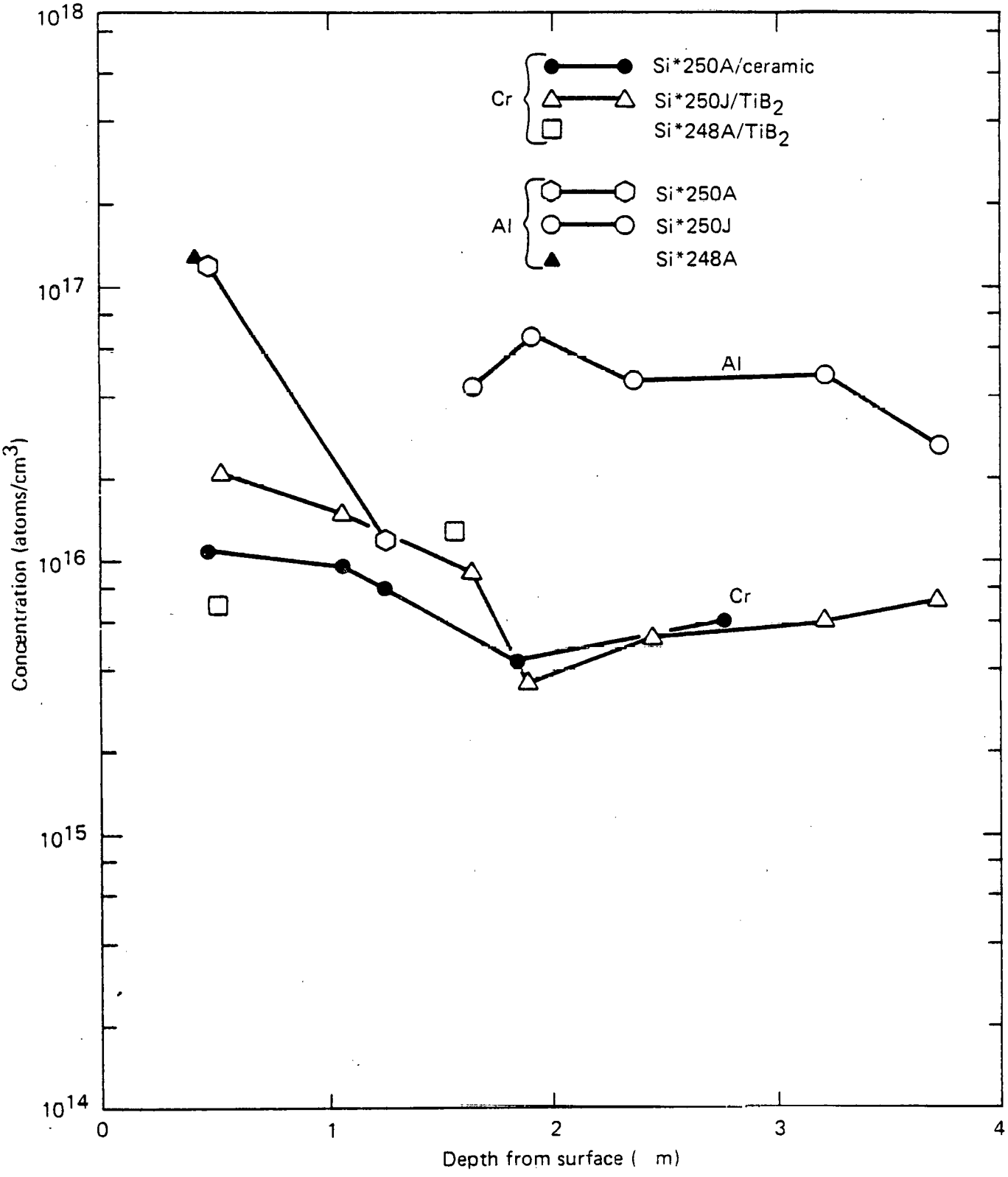

Fig. 2 **Concentration-depth profiles for Al and Cr from the sputtering of samples with and without a TiB_2 layer.**

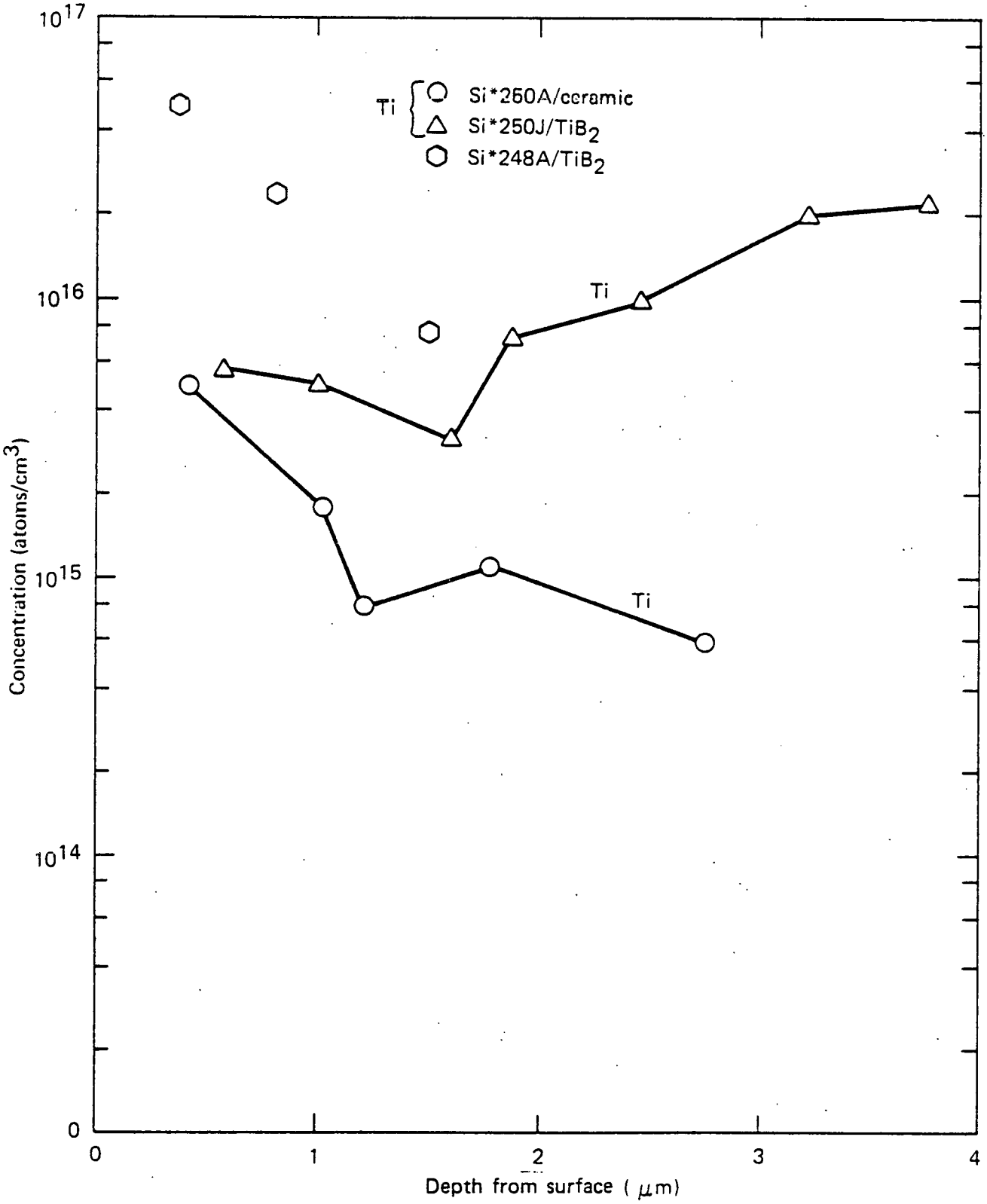

Fig. 3 Concentration-depth profiles for Ti from the sputtering of several samples.

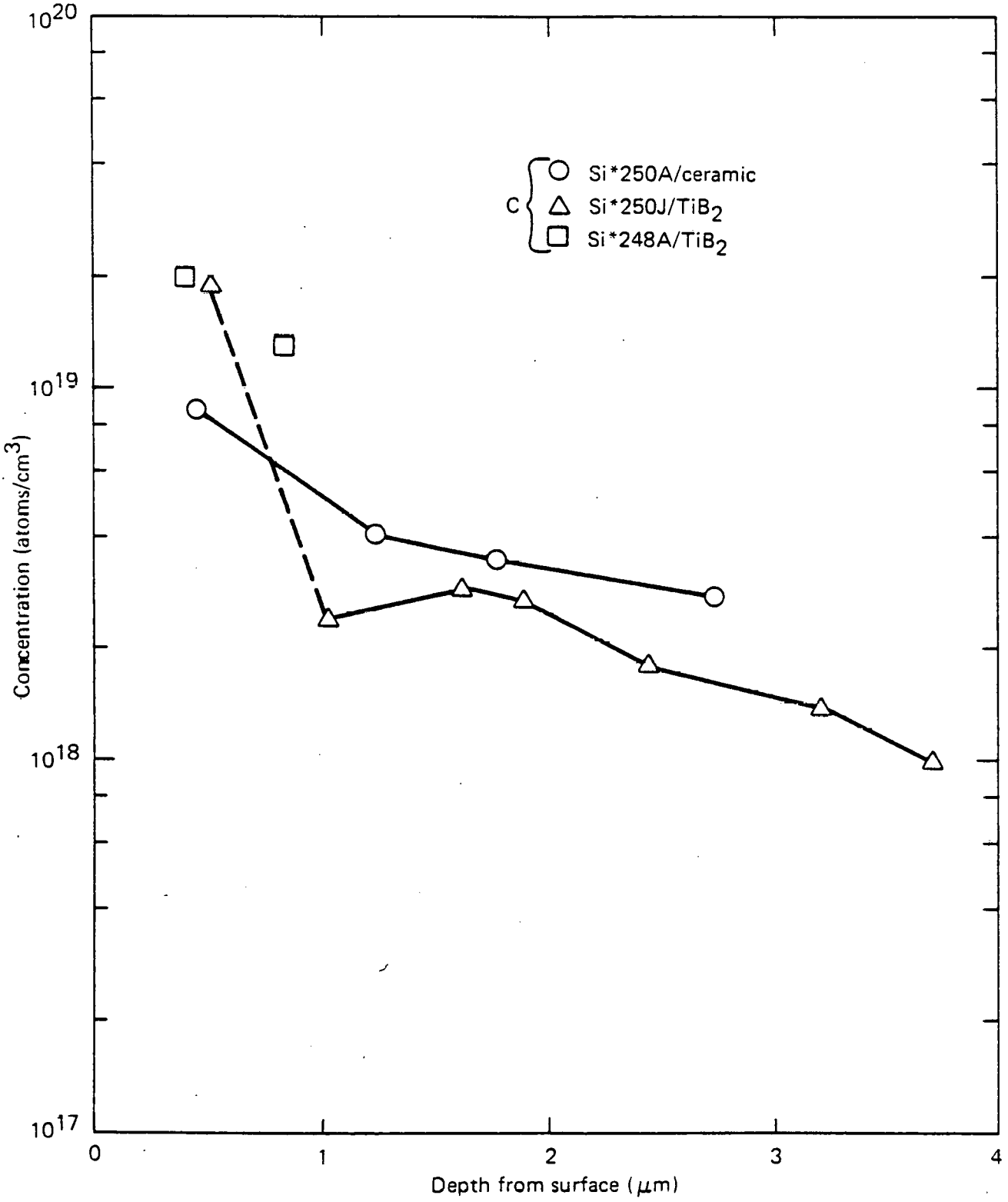

Fig. 4 Concentration-depth profiles for carbon from the sputtering of several samples.

An attempt was made to estimate the amount of titanium observed in the film due to diffusion from TiB_2. The diffusion coefficient of Ti in Si @ 1200°C was estimated from the previously determined value of

$$D_{Ti,\ 975°C} = 7.6 \times 10^{-13}\ cm^2/sec.$$

Assuming that the temperature dependency is approximately parallel to that for Al, the resulting value is

$$D_{Ti,\ 1200°C} = 6.5 \times 10^{-11}\ cm^2/sec.$$

Using this $D_{1200°C}$ value for titanium, a value of C_o (for Gaussian dependency) was calculated which would give the SIMS measured value of Ti concentration 3.5 μm below the surface for Si*250J; this was

$$C_o = 3 \times 10^{16}/cm^3.$$

The C_o and $D_{1200°C}$ were then used to calculate the Ti level expected in Si*248A. For 1.5 μm below the surface this was 1.2×10^{15}, a value less than found by SIMS, viz. 8×10^{15}. This provides further evidence that there is a contribution from a vapor source. Si*250A was deposited directly on sapphire and the Ti concentration observed in that profile may be characteristic of the amounts attributable to the vapor source during deposition. This is approximately the stated solubility limit of Ti in Si, viz. 10^{15} atom/cm^3.

In all of the profiles shown in Figs. 2 to 4 there appears to be a pile-up of impurities on the surface of the films. This may be due, in part, to a rejection of impurities as the silicon crystallites are growing.

2.2.3 Evaluation of Silicon Surface Cleaning Procedures

The procedures for cleaning surfaces prior to diffusion are indicated in steps 1 through 5 (Section 4, Table VII). During this procedure it was felt that some residue may remain on the surface by becoming embedded at the grain boundaries.

In order to check this possibility a SIMS analysis was made on the surface of a sample before and after cleaning. The procedure used for this test omitted photolithography (Step #3, Table V, Section 4). The ratio for impurity intensities before and after the cleaning process are given in Table II. Ratios greater than unity can be interpreted as contaminants introduced by the treatment and less than unity as being removed by the treatment. From this limited sampling, it appears that the surface concentrations of C, Na, and K were increased by the treatment, and Al, Cr, and Ni were reduced by the treatment. Because of the possible introduction of alkali metals, this surface cleaning procedure may be open to question.

TABLE II

Comparison of Surface Spectra Before and After Etching Procedure, Sample Si*245D

Species	I_a/I_b	
	0-1000Å	1000-2000Å
B	1.9	1.1
C	1.1	5.0
Na	1.8	15
Al	0.3	0.7
Cl	2.9	0
K	9.3	6
Ti	1.1	0.8
Cr	1.0	0
Ni(+SiO_2^+)	0	0.9
Si	1.0	1.0

Sputtering of the sample before and after the treatment was continued in the presence of oxygen to obtain the "bulk" impurity levels shown in Table III. The conclusion is that bulk concentrations remained the same within limitations of sampling statistics and experimental error.

TABLE III

Comparison of "Bulk" Impurities in Si*245D (∿ 0.9μ from Surface)

	C, atoms/cm^3		
	Before etch		After etch
B	1.6×10^{16}	d	3.3×10^{16}
C	3.9×10^{17}	f	NS
Al	1.2×10^{17}	d	ND
Ti	2×10^{15}	d	1.4×10^{15}
Cr	1.6×10^{16}	d	4×10^{15}
Na	ND		Present (∿ 4×10^{16})

ND - not detected d - defocused; O_2 enhancement
NS - not sought f - focused; no O_2

2.3 n-Type Silicon Deposition

It was reported last quarter that n^+ silicon films had been formed by evaporating silicon in a phosphine (PH_3) atmosphere. This quarter n^+-p junctions and solar cells were successfully produced by this technique.

Table IV list the deposition runs made to date in this investigation. As in the case of the p-type depositions, each run was made on seven 1" X 1/3" substrates. The various substrates included blank sapphire and alumina, single crystal silicon wafers, and previously-deposited polycrystalline p-type silicon films with and without TiB_2 bottom electrodes. In runs nSi6, 8 and 9 a thick silicon film was deposited without introduction of PH_3 and then (in 8 and 9) a thin film was deposited with the PH_3 atmosphere.

The various deposition parameters which were used in each run - substrate temperature, deposition rate, phosphine pressure, and total thickness of the deposit - are also listed in the table. The resistivities, as measured on polycrystalline films deposited on sapphire, are also listed. It is believed that the resistivities are high since (1) they are measured perpendicular to the columnar crystal grains, and (2) some

TABLE IV

n-TYPE SILICON DEPOSITION PARAMETERS

Sample	Substrate Temp (°C)	Deposition Rate (Å/min)	PH_3 Pressure (X 10^{-6} Torr)	Thickness (μM)	ρ (poly) (Ω-cm)	ρ (Epitaxy) (Ω-cm)
nSi 1	966	160	2.0	1.0	.06	
2	1163	110	2.0	2.0	8	
3	953	70	2.0	0.4	0.1	0.1
4	940	275	30	3.3	.02	.003
5	933	600	2.0	0.9	.06	
6	941	880	-	p 15.9	73	
7	925	300	2.4	0.3	0.8	
8	932	250	2.2	p 5.7/n 0.5	6	
9	936	410	2.2	p10.0/n 0.5		
10	825	450	2.0	5.0	.04	.008
11	830	380	2.8	1.7	.06	.009

phosphine may migrate to grain boundaries reducing the number of active domains. Measurements on epitaxial films grown on high resistivity (15 Ω-cm) silicon substrates gave resistivities consistent with the impurity concentrations measured by SIMS ($\sim 3 \times 10^{19}$ atoms/cm^3). These values are listed under ρ (epitaxy) when available.

In the first five runs the vacuum chamber was outgassed by using the substrate heating lamps to heat the whole chamber to approximately 200°C for several days. It was discovered, however, that the resulting high temperature of the substrate (1100°C) led to the formation of carbides and oxides on the surface due to reactions with the residual gases. An analysis of the interface between n and p type deposits is presented in Section 2.4. In the remaining runs the chamber was heated with external tapes, and the substrates were not heated above 200°C until just before the deposition. A SIMS analysis of these samples has not yet been carried out.

In all runs the substrates were first heated to about 1150°C and 50-100 Å of silicon were deposited to remove the room temperature oxide. (The efficiency of this process needs to be examined in view of the results described in Section 2.4.) The substrates were then lowered to the desired deposition temperature before the PH_3 was introduced for the n^+ deposit, since at the higher temperatures the phosphine diffuses into all exposed silicon surfaces.

Successful junctions were formed on both polycrystalline and single crystal silicon using the above procedures at a substrate temperature of 940°C. The junctions exhibit large reverse current densities, however, and open circuit voltages were only 0.13V. It is likely that current is being lost either through surface leakage or is due to recombination in the junction caused by impurities at the $p\text{-}n^+$ interface. The last two runs of the quarter were, therefore, made at only 830°C, to reduce doping of the surfaces by the phosphine. It was found that epitaxial growth could still be obtained at that temperature. When tested, however, these junctions were practically ohmic and had no photovoltage! The samples were then heated in an open tube furnace to 975°C for one hour.

When tested again they proved to be much better than any produced in the previous runs, with much lower reverse current densities. When probed, the polycrystalline samples showed regions with open circuit voltages of up to 0.22V and the single crystal devices showed areas with $V_{oc} = 0.50V$. When electroded, the polycrystalline samples gave $V_{oc} = 0.18V$ ($J_{sc} = 14$ mA/cm^2) and the single crystal gave $V_{oc} = 0.38V$ ($J_{sc} = 12$ mA/cm^2). As this technique has just recently been developed, these figures should improve as the optimum deposition and heating parameters are evolved. Photovoltaic properties of nSillA are given in Section 4.2.

Tentative conclusions are that even with only a brief heating before deposition, too many impurities are formed on the surface of the p-type substrates. When the n-type region is then deposited at the lower temperatures, those impurities at the interface occur directly in the junction depletion region. Deposition at higher temperatures or post-deposition heating diffuses the phosphorus down into the substrate far enough to form the junction below the impure interface. The impurities are left in the n^+ region, where they are much less critical.

An alternate method of avoiding the impurity problem on the surface of the p-type polycrystalline substrate is to perform the p deposition and the n deposition in the same chamber, without breaking the vacuum between depositions. This process was tested in runs nSi6, 8 and 9, but without success. The residual phosphorus in the chamber generally compensated the boron doping of the silicon, which was obtained from the boron contained in the source.

2.4 SIMS Analysis of nSi4F/Si212F

A SIMS analysis of the interface between a vacuum deposited n-type film (nSi4F) and a thicker vacuum deposited p-type film (Si212F) was carried out. The two depositions were performed in separate vacuum chambers. The deposition parameters for the n-type layer are given in this report. Parameters for the 16 μm-thick p-type film are given in an earlier quarterly report.

The phosphorous level in the deposited layer was determined to range between 3.6×10^{19} atoms/cm^3 and 2.6×10^{19} atoms/cm^3 from 0.2 μm below the surface to the p-type layer. As the interface between the two silicon layers was approached, several impurity species were

observed. These include B, C, O, Al, Ni, and Mo. All showed a maximum at the interface suggesting an origin prior to the deposition of n-silicon. Assuming that O and C are tied to SiO_2 and SiC, intensities were converted to concentration. Times to depths were also obtained by using the neutral sputtering rate for Si, viz. 150 Å/min. The result is shown in Fig. 5. The lack of coincidence of the maxima for SiC and SiO_2 suggests that the formation of SiO_2 was the dominant reaction in the earlier stages of outgassing followed by the accummulation of carbide as outgassing proceeded. Graphical integration gave the following estimates for the respective thicknesses: 0.49 μm SiO_2 and 0.12 μm SiC. The observed pile-up confirms previous experiments and indicates that surface cleanup prior to deposition is necessary to obtain pure interfaces, or that deposition should take place only on substrates that have not had extensive exposure at elevated temperatures.

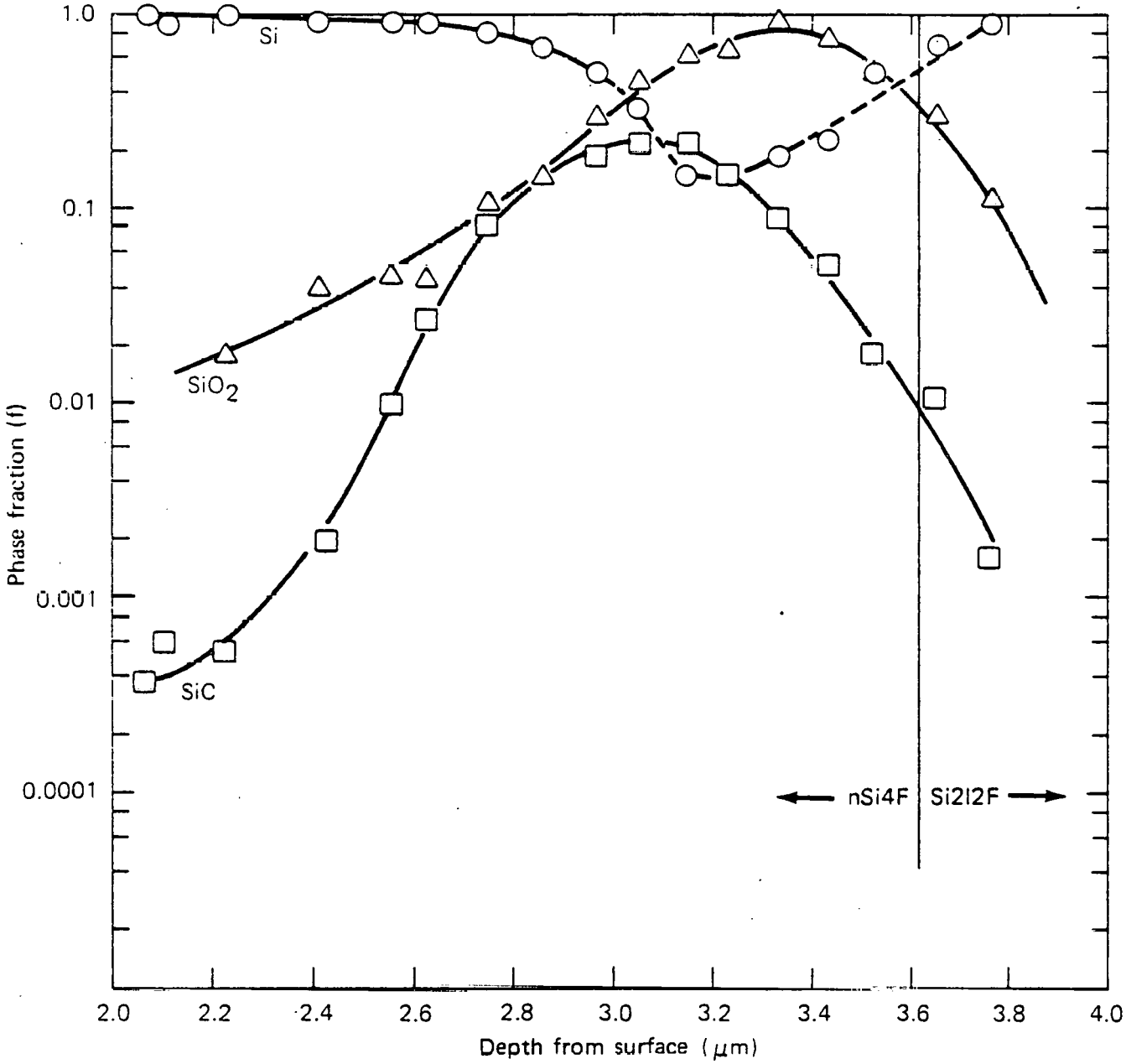

Fig. 5 Concentration-depth profiles near the n/p interface from the sputtering of sample nSi4F/Si212F.

3. THE BOTTOM ELECTRODE (TiB_2)

Studies on TiB_2 conductive layers as bottom electrodes have led to a sufficient understanding of the process so that low resistance coatings are now produced more or less routinely. The kinetics of the formation of titanium diboride from titanium/boron couples and the loss of boron due to reaction with a partial pressure of water vapor in the vacuum were discussed in previous quarterly reports.

An improvement in the heating arrangement made this quarter has resulted in more uniform and consistent resistivities than were achieved in the past. The new heating procedure consists of removing the samples from their substrate holder and placing them on a heavy tantalum plate. The plate is then covered by tungsten filament lamps and tantalum reflectors in such a way that all samples can be heated uniformly in the vacuum. In the previous heating technique samples were kept in the deposition substrate holder which was open in the front. Breaking the vacuum prior to reacting the couples does not appear to influence their resistivities. The effect of oxygen impurity on resistivity has, however, not been fully explored.

The result of a typical run ($TiB_2$305) is presented in Table V. In this run, substrates were maintained at approximately 500°C. The titanium was deposited at 1170 Å/min from a joule-heated tungsten boat, and the boron was deposited at 760 Å/min by electron beam heating. Total deposition time was 23 minutes. The samples were heated for approximately 3 hours at 950°C in a vacuum to react the layers. This vacuum heating step may possibly be eliminated by forming a more intimate mixture of Ti and B by simultaneous deposition of the two materials. An exploration of this technique, however, would be too time consuming to be carried out under the present contract.

TABLE V

TiB_2 PARAMETERS IN A SINGLE RUN

$TiB_2$305 Sample	Substrate	Thickness μM*			ρ μΩ-cm
		Ti	B	TiB_2	
A	Alumina			(1.2)	37.3
B	Sapphire	0.825	1.12	1.2	33.5
C	Alumina			(1.2)	34.1
D	Alumina			(1.2)	34.1
E	Sapphire	0.825	1.03	1.2	34.1
F	Alumina			(1.2)	40.0
G	Alumina			(1.1)	33.0
H	Sapphire	0.736	0.913	1.1	30.0
J+	Alumina			(1.1)	34.0
K	Alumina			(1.1)	35.6
L	Sapphire	0.766	0.884	1.1	34.0
M	Alumina			(1.1)	40.7

*Thicknesses measured on sapphire substrates only.
+The letter I is omitted as it may be confused with the numeral 1.

The use of the new heating arrangement had the secondary effect of eliminating a mysterious source of chromium, and perhaps also iron, which had been observed on the surface of some of the reacted films, but not on the unreacted ones. The new heating arrangement did not require the use of tantalum screws (which were subsequently removed), and the source of chromium and iron was traced to a chipped chromium plated screwdriver. Chromium and iron may have become embedded in the slots of the screws. The vapor pressure of chromium at 950°C, (approximately 5×10^{-7} Torr), is sufficient to deposit an impurity on the surface of the films. In addition, suboxides of Cr may also have high vapor pressure. An analysis of the impurities in the interior (1500 Å from surface) of a TiB_2 film made while using the tantalum screws is given in Table VI. Removal of the screws

TABLE VI

Impurities in Titanium Diboride Film
($TiB_2$305L) 1500Å from Surface

Species	Impurities (ppma)
H	NS
Li	ND
C	600
N	500
F	30
Na	I
Mg	ND
Al	430
Si	530
Cl	90
K	ND
V+(TiH^+)	310
Cr*	100
Mn	ND
Fe	470

ND - Not detected
NS - Not sought
I - Interference
* - Cr higher on the surface

reduced the Cr and Fe to 12 ppma and 130 ppma, respectively. Tracking down the source of the excess chromium on the surfaces of the samples may also lead to improvements of purity in the silicon films themselves. New screwdrivers of hardened stainless steel with aluminum handles have been fabricated. The use of aluminum handles rather than plastic permits cleaning by solvents.

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4. PHOTOVOLTAIC DEVICES

4.1 Photovoltaic Device Formation

The p-type polycrystalline layers on TiB_2 coated substrates, the epitaxial layers on silicon substrates, and the single crystal monitors were processed into complete devices using the procedures described in prior reports. The processing schedules used during this quarter are listed in Table VII. Variations in the usual schedule were carried out in order to yield different junction depths. Thus, Sample Si 245B, and its crystal monitor were diffused for 7 hours in place of the usual 1 hour, while Si 244C and its single crystal monitor were diffused for only 4.5 minutes. The three variations in diffusion drive-in, Step #8 of Table VII, yield junctions approximately 0.5 μm, 1 μm and 2 μm deep. These depths were determined by calculation from the diffusion coefficient.

The n-type layers required only the last step (Step #11, Table VII) in the process: deposition of electrodes through a mask. The n-type depositions were carried out through tantalum masks as described in the last Quarterly Progress Report. The only difficult procedure encountered in processing the n-type deposited layers was in the alignment of the electrode masks to match the n-type areas. The n-type deposit is barely (or sometimes not at all) visible on the p-type layers. This difficulty in alignment is avoided with samples whose junctions are formed by diffusion, because the colored oxide layer clearly defines the n-type regions. To avoid this problem in the future, appropriate oxide patterns will be placed on some samples prior to the n-type deposition.

TABLE VII

THIN FILM SILICON PHOTOVOLTAIC DEVICE PROCESSING STEPS

Process/Samples	Si*246A + Xtal, Si*246E, Si*245E	Si*245B + Xtal	Si*244C + Xtal
1. Clean	Boil acetone		
2. Etch	BOE 10 min → 30 min H_2O		
3. Oxidation	4 hrs. @ 975°C		
4. Photolithography	Level 1 mask	no change	no change
5. Pre-diffusion etch	2.5% HF, 10 sec → 20 min H_2O		
6. Diffusion - n-type	6.5 min. @ 975°C		
Flow rates: N_2	3300 ml/min		
O_2	44 ml/min		
PH_3	16.5 ml/min		
7. Post-diffusion etch	2.5 HF 45 sec → 20 min H_2O		
8. Oxidation, drive in	1 hr. @ 975°C	7 hrs @ 975°C	4.5 min @ 975°C
9. Photolithography	Level 2 mask		
10. Pre-electrode etch	2.5% HF 10 sec → 20 min H_2O	no change	no change
11. Electrode deposition	Through mask		

The electrode masks used for the titanium/silver deposition are identical in both the diffused junction samples. The over-etched 1 mil masks, as reported in the previous quarter, were made more precise, and the vacuum-deposited electrodes match the designed areas to approximately 10% or less. Since the electrodes form a small portion of the total device area, the error introduced by depositing through masks as compared to the precise photolithography process is small ($\sim$ 2%).

4.2 Photovoltaic Device Properties

Table VIII lists representative photovoltaic parameters together with surface grain diameters $\bar{d}$ for a selection of samples with different grain sizes. The table also includes results for two samples with deposited n-layers, two epitaxial layer devices and a single crystal monitor.

Relative spectral quantum efficiency curves for several devices are shown in Figs. 6 and 7. None of the devices have anti-reflection coatings. The values of L_D (minority carrier diffusion length) given in Table VIII were obtained from the spectral quantum efficiency curves as explained in the First Quarterly Report. In this report (unlike earlier reports) the values of L_D were obtained by assuming that all samples have optical absorption coefficients α close to the single crystal values. This assumption is certainly valid for the epitaxial samples and the single crystal monitor. Polycrystalline silicon absorbs more strongly in the visible than single crystal due to scattering at the crystallite boundaries. Optical absorption data are available only for fine grained polycrystalline and single crystal silicon. The samples with $\bar{d} >> \lambda$ are believed to have absorption properties closer to single crystal than to the fine grained polycrystalline material. The measurements of L_D for the polycrystalline films may be, therefore, larger than the true values by an amount depending on

TABLE VIII

PHOTOVOLTAIC PARAMETERS OF SELECTED DEVICES

Sample (Device)	Surface Grain Size $\bar{d}$ (μm)	M.C. Diff. Length L_d (μm)	η (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	ff	A_{eff} (cm^2)	Remarks
Si 209E (C3)	5.2	4.3	2.1	284	12.8	.58	2.6 X 10^{-1}	
Si 237D (C2)	15	3.0	2.2	346	10.1	.63	5.2 X 10^{-1}	
Si 238D (D2)	14	5.4	2.2	295	12.6	.59	5.3 X 10^{-1}	
Si 238E (E1)	40	4.1	< 1	90	10.6	-	5.2 X 10^{-1}	
Si*244C (D1)	11	4.0	1.6	286	10.1	.56	2 X 10^{-1}	Shallow junction
Si*245B (D2)	14	7.8	1.6	286	9.8	.56	5 X 10^{-1}	Deep junction
Si*245C (D2)	14	4.5	2.2	290	13.3	.57	5 X 10^{-1}	Normal junction
Si*246E (E)	7	4.0	1.3	227	15.1	.38	0.16	
Si*243B (D5)	epitax.	7.5	3.6	361	18.8	.53	2 X 10^{-2}	
Si*246A (D1)	epitax.	8.5	2.7	338	15.3	.52	2 X 10^{-2}	
XSi*246A (D1)	single xtal	35	6.6	545	18.7	.65	2 X 10^{-2}	
nSi3D/Si*244E (B)	11	22	0.24	105	8.0	.29	0.16	All vacuum dep.
nSi11A/Si*250E (D2)	8	14	1.2	172	14.8	.47	5 X 10^{-1}	All vacuum dep.

grain size: the larger the grain size, the more accurate the values of L_D. For the eight polycrystalline films in the table, with surface grain diameters from 5.2 to 40 μm, there is observed no significant increase in L_D with increasing grain size. The greatest L_D was observed in Si*245B (7.8 μm) which was fabricated so as to have a deep junction (see Table VII). The spectral quantum efficiency peak (see Fig. 6) of this sample is shifted towards the longer wavelengths ($\sim$ 600 nm) compared with the "normal depth" junctions (peak $\sim$ 500 nm). This causes the entire spectral response curve to shift to the right (increasing λ) and probably leads to a larger value of L_D than would be obtained by other techniques (e.g. lifetime measurements). The model on which the determination of L_D is based assumes that an abrupt junction is essentially at (or very near) the physical top surface.

The epitaxial layers (Si*243B and 246A) have spectral response curves which peak around 600 nm and have a fall off which indicates that L_D is approximately 8 μm (Fig. 7). This is significantly longer than L_D (poly), but much smaller than L_D (s.c.). This is probably due to recombination and trapping at impurity sites or defects in the epitaxial layer.

The evaporated n on p samples (nSi*3D and nSi*11A) exhibit anomalously long "tails" in their spectral quantum efficiency curves (Fig. 7). This results in unrealistically large values for L_D, since the p-type base regions for nSi3D/Si*244E and Si*244C were deposited together and the devices made on them should have similar minority carrier diffusion lengths. The peaks in the spectral quantum efficiency curves for these all deposited devices lie in the 600 to 650 nm region, indicative of maximum collection efficiency from a depth between 4 μm (single crystal material) and 2.5 μm (very fine grained polycrystalline material). This is a good place to have the peak in the spectral response, since the terrestial photon flux peaks at about the same wavelength.

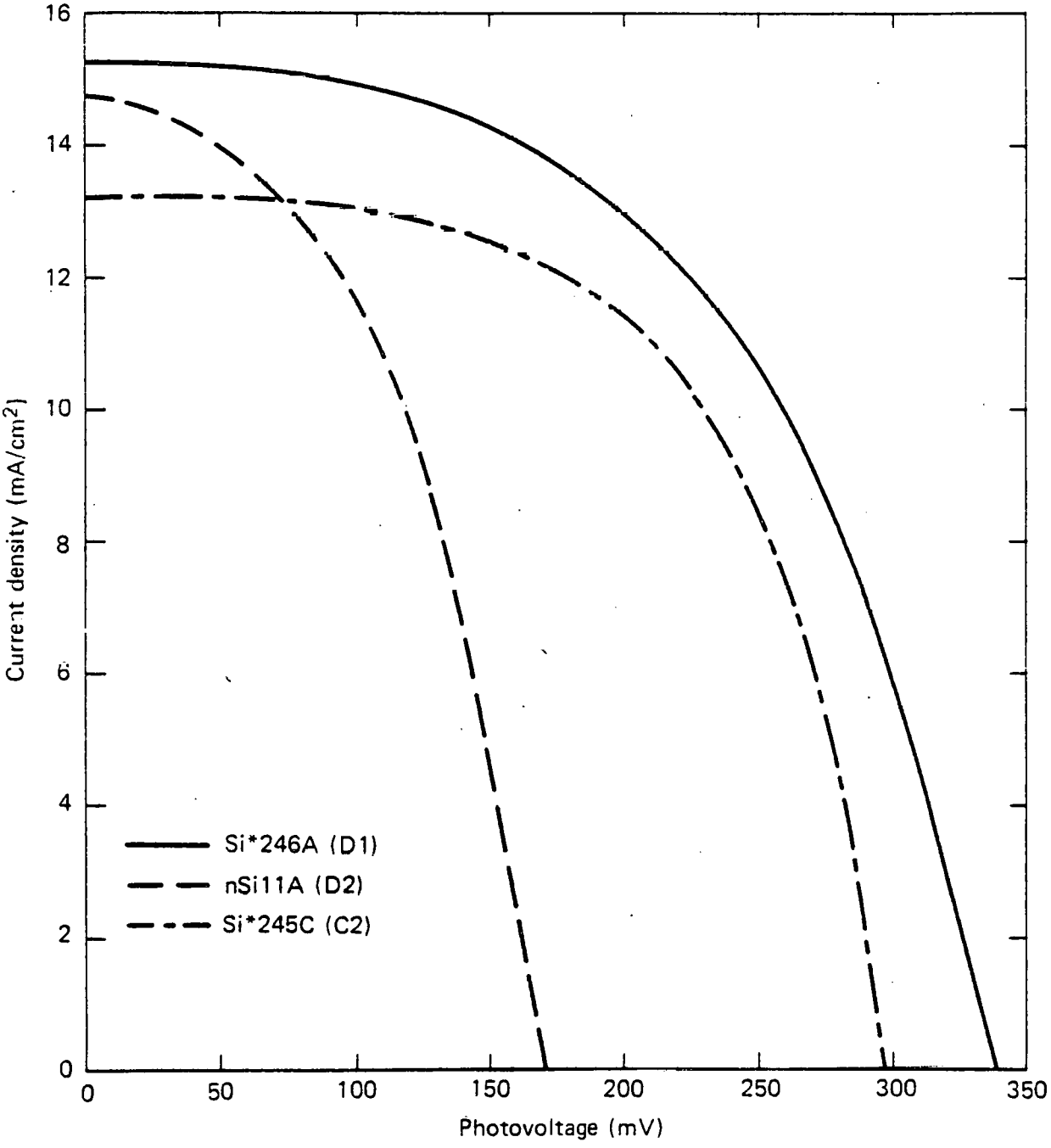

Fig. 6 Illuminated (AM1) I-V characteristics of epitaxial film (246A), vacuum deposited n on p (nSi11A), and diffused junction (245C) photovoltaic devices.

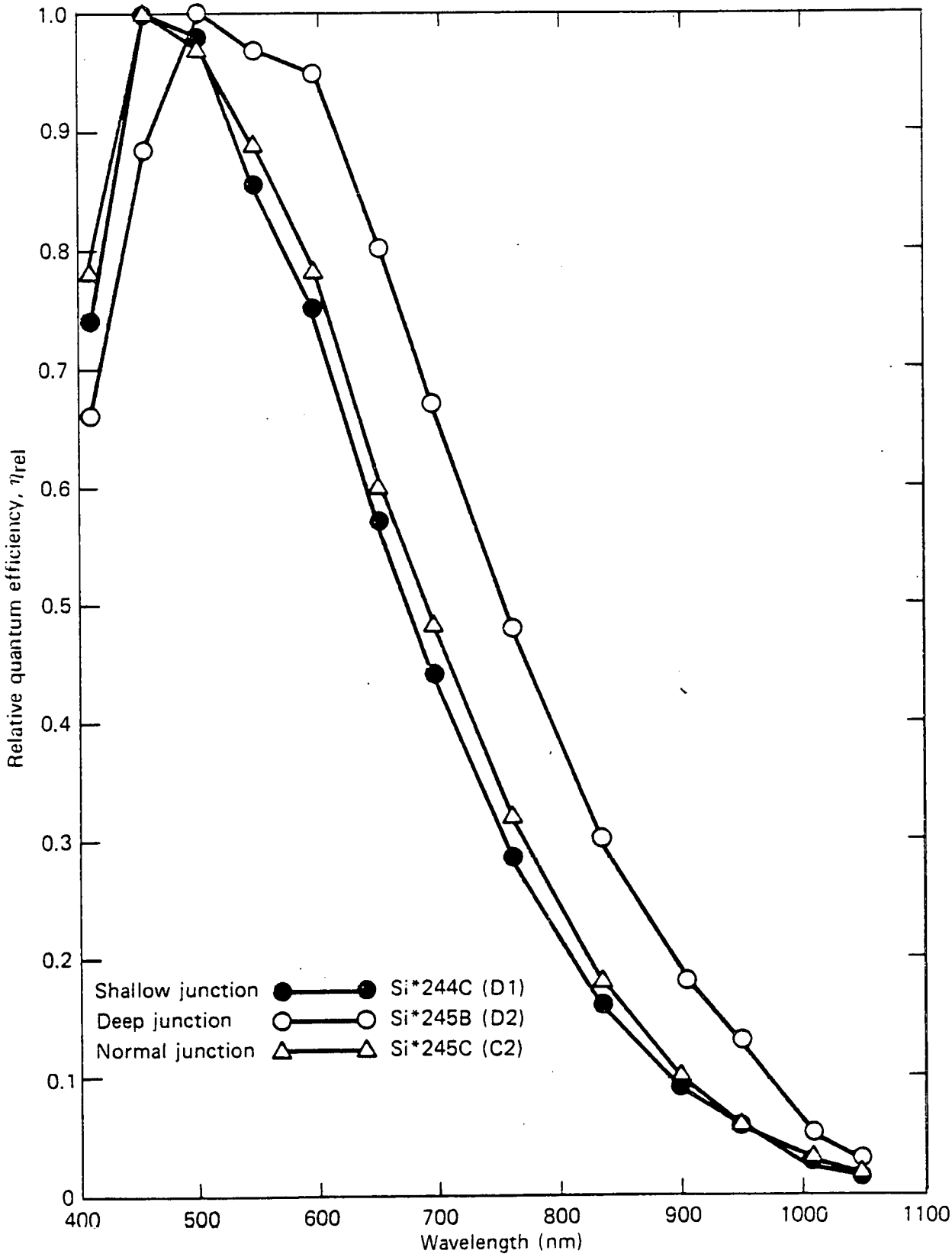

Fig. 7 Relative spectral quantum efficiency of shallow, deep, and normal depth diffused junction, thin film solar cells.

The deep, shallow, and normal junction depth cells of similar grain size and thickness (Si*245B, 244C, and 245C, respectively) show surprisingly similar photovoltaic behavior. The peak in the spectral response curve moves towards longer wavelengths with increasing diffusion time (junction depth), as would be expected (Fig. 6). The deep junction (Si*245B) has a long tail on the spectral response curve, as mentioned earlier, and this leads to an anomalously large value of L_D. Since the photovoltaic efficiency is the same as in the shallow junction device (Si*245B), no importance should be attached to the apparent larger value of L_D in this case. The AM1 I-V characteristics for a diffused polycrystalline junction device Si*245C-C2, an epitaxial layer Si*246A-D1, and an all-evaporated device nSillA-D2 are shown in Fig. 8.

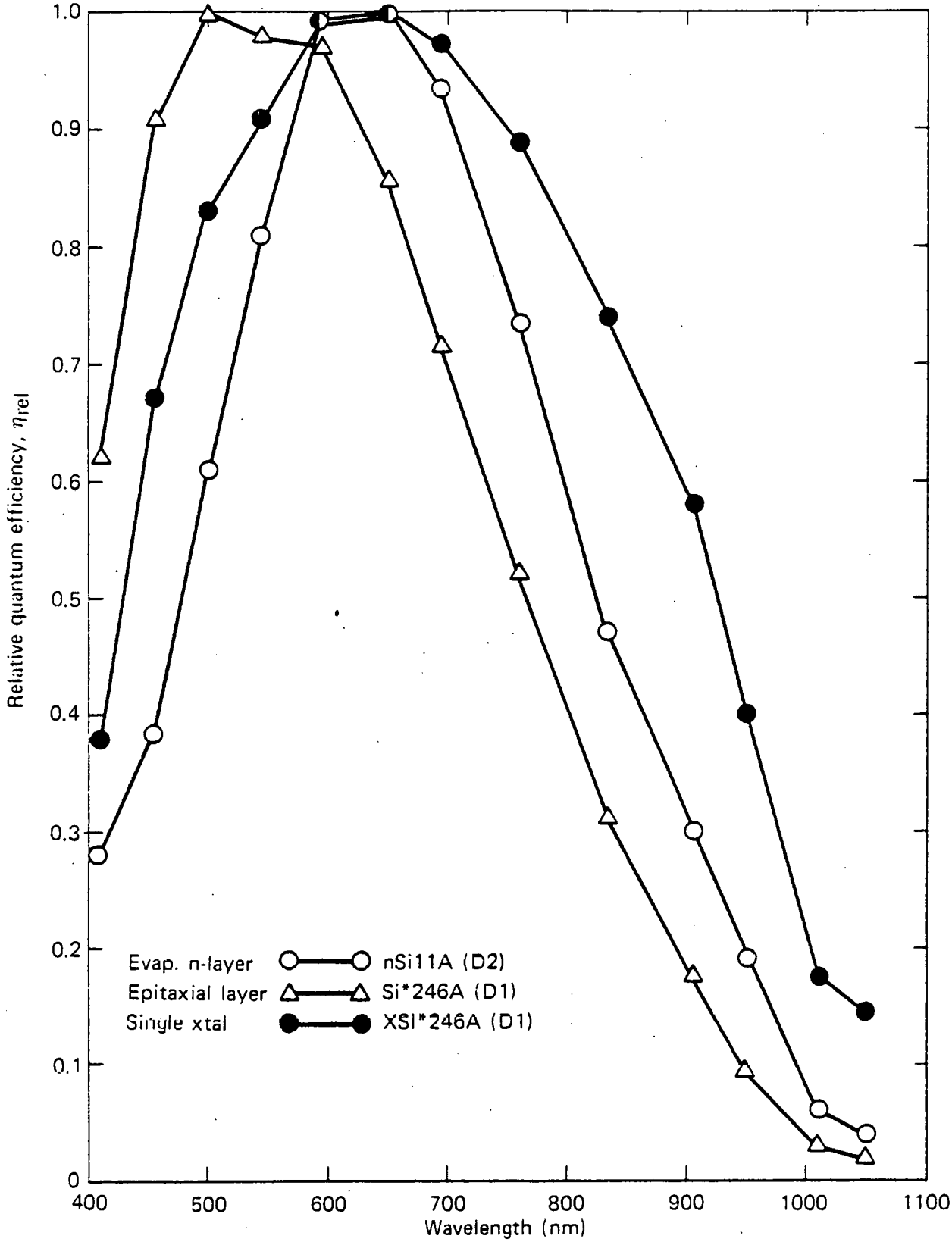

Fig. 8 Relative spectral quantum efficiency of evaporated n-layer, epitaxial thin film, and single crystal solar cells; the absolute maxima, η_{abs}, are 0.51, 0.59, and 0.63, respectively.

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5. DISCUSSION AND PLANS FOR NEXT QUARTER

This quarter, several polycrystalline silicon photovoltaic devices were formed for the first time entirely by vacuum deposition techniques. While the techniques for forming junctions by vacuum deposition have not been completely developed, it is apparent that, with additional work, devices with efficiencies equal to those obtained by diffusion in the tube furnace could be formed. From the standpoint of large scale processing, these results are encouraging.

Investigations on the photovoltaic responses of samples having different grain sizes, including epitaxial layers on silicon, indicate that crystal size may not now be the limiting factor in achieving high efficiencies. At the beginning of these studies, increases in average grain diameter led to increases in device efficiency. Curves of efficiency vs grain size followed theoretical expectations [2,3]. As the surface grain diameters increased beyond about 5 μm, however, device efficiency generally stopped increasing. The data, such as shown in Table VIII of this report, indicates that devices with grain diameters of 5 μm and 15 μm as well as epitaxial layers have essentially the same efficiency. The single common element in all of these deposited layers that may explain this lack of improvement in efficiency is their high impurity content. It is even possible that the high temperature (1250°C) used to gain an improvement in grain size resulted in the further introduction of impurities. The impurities observed in the layers by SIMS analysis are in the range reported to cause severe degradation of efficiencies [4]. It is not known, however, whether the concentrations for degradation observed in single crystals will be the same as those observed in polycrystalline films. Grain boundary impurity segregation [5] and passivation of impurities by oxygen and hydrogen etc. during the growth may ameliorate the effects of impurities in polycrystalline samples. The variations in diffusion times conducted this quarter

did not essentially lead to changes in device efficiency indicating that surface impurities are not, at present, a limiting factor.

Work on the bottom electrode (as far as this contract is concerned) is about complete. Details, such as the effect of oxygen on the resistivity and the exact rate of loss of boron in the vacuum system, still need to be investigated. The fabrication of the bottom conducting electrodes required for this present work is now more or less routine, and sufficient quantities of low resistivity samples can be produced to supply the needs of both n-type and p-type silicon studies.

The emphasis during the next quarter must be on finding means to decrease the level of impurities in the samples. This will be explored by making variations in the deposition and surface cleaning procedures, as well as working in an improved vacuum environment. Unfortunately, a faulty high-vacuum valve and delayed delivery on a cryogenic pump have hindered research in a clean, high-vacuum. The high-vacuum valve has been returned to the factory once more for repair. The present laboratory procedure of changing vacuum systems between the p-type and n-type deposition which leads to the introduction of element impurities at the n-p interface should be altered. (A production type process would not, of course, have this problem.) The surface cleaning procedures used in both diffused and deposited type junctions must be reevaluated. The formation of the n-type layers by depositing antimony, antimony oxide, or phosphorus oxide will be explored this coming quarter. The use of solid doping sources rather than a phosphine atmosphere may simplify processing and allow better area control and higher vacuum conditions.

6. REFERENCES

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