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ABSTRACT

A series of controlled experiments has been performed in Sandia's Photovoltaic Device Fabrication Laboratory to evaluate the effect of various chemical surface treatments on the recombination lifetime of crystalline silicon wafers subjected to a high-temperature dry oxidation. From this series of experiments we have deduced a relatively simple yet effective cleaning sequence. We have also evaluated the effect of different chemical damage-removal etches for improving the recombination lifetime and surface smoothness of mechanically lapped wafers. This paper presents the methodology used, the experimental results obtained, and our experience with using this process on a continuing basis over a period of many months.

INTRODUCTION

Sandia's Photovoltaic Device Fabrication Laboratory (PDFL) is funded to facilitate the transfer of laboratory-scale advances in silicon cell design and processing to large-scale processing in industry. Consistency in processing is essential to this mission. To accomplish this, we have established baseline processes which are run on a continuing basis to insure that all equipment is functioning properly and is free of contamination.

This paper describes our development and subsequent experience with a baseline process for the cleaning and dry oxidation of silicon wafers. The primary measurable quantity is the carrier lifetime as measured by microwave-detected photoconductance decay [1]. Maintaining carrier lifetime through high-temperature processes like oxidation is the single most important factor in the fabrication of high-performance solar cells, and it is also the

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This work supported by the U.S. Department of Energy under contract DE-AC04-76DP00789.

MATERIALS

Our goal in the PDFL has been to develop cleaning sequences that are adequate for a wide variety of silicon materials, while maximizing the simplicity, safety, and economy of the process. We have performed experiments using a variety of crystalline and polycrystalline materials from several major photovoltaic production companies. We report here only those results obtained using 300-Ωcm n-type float-zone (FZ) and 10-Ωcm p-type Czochralski (Cz) wafers.

The FZ wafers were purchased from Wacker and SEH with mechanically lapped surfaces, and the Cz wafers were purchased from Monsanto and SEH America with the front surface mirror-polished and the back surface chemically etched. The wafers were <100>-oriented, 100-mm diameter, and 500 - 625 μm thick.

All of the cleaning solutions used in the PDFL are mixed from concentrated semiconductor-grade liquid chemicals. Our primary suppliers are General Chemical and Ashland Chemical, although we occasionally purchase from other companies. The water used in these solutions is ultrapure 18-MΩcm deionized (DI) water produced on-site, continuously circulated through an ultraviolet sterilizer and 0.05-μm filter, and cultured monthly for bacteria. This DI water is also used for dump-rinsing the wafers after each step, and in the final rinse/dry, which is performed in an Estek SRD-1000 spinning rinser/dryer.

The baths used for the chemical etching and cleaning solutions are constructed of metal-free materials, ranging from polypropylene for low-temperature processes to Halar™ for high-temperature caustic solutions. Several of these baths are equipped with recirculation pumps and active temperature control, which can maintain the solution temperature to within 1°C throughout a

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Our quartz single-wall furnace tubes are installed without chemical cleaning, then cleaned overnight at 1100°C using in-situ oxidation of trichloroethane (TCA) to form HCl vapor. One-hour TCA cleans are then implemented on an as-needed basis,

which thus far has been only a few times per year. Silicon carbide paddles are used to transport dedicated quartz boats into the furnace, using digital programming for push, pull, temperature ramp, and gas flow control. Vacuum wands with high-temperature plastic tips are used to load and unload wafers from the furnace boats.

MAIN EFFECTS EXPERIMENT

Our initial effort involved a statistically designed main-effects experiment to explore the effects of 18 parameters associated with 8 different chemical treatments: freon-acetone-alcohol (degrease), 7:1 buffered oxide etch (BOE), nitric-hydrofluoric silicon etch, sulfuric-peroxide clean (piranha), caustic choline clean (Summa), hydroxide-peroxide clean (RCA1), hydrofluoric acid dip (HF), and hydrochloric-peroxide clean (RCA2). Four additional parameters were introduced: initial wafer contamination, time delay between cleaning and oxidation, oxidation temperature, and forming-gas anneal temperature. The results of this main-effects experiment have been presented previously [2]. The most important factor that emerged from the main-effect experiment was the inclusion of an HF-dip/rinse/spin-dry as the last step before oxidation. Other potentially beneficial factors were the inclusion of a degrease, nitric:HF, and piranha clean. The effectiveness of nitric:HF in removing metal ions, especially iron, has been reported previously [3]. The nitric:HF also proved beneficial in improving the overnight stability of the lifetime. We found no basis for choosing the relatively complex and expensive RCA process [4].

We have recently re-examined the data and found that the recombination lifetimes measured by photoconductance decay in each of the 24 trials for FZ and Cz are well correlated, as illustrated in Fig. 1. This result suggests that each impurity introduced during the cleaning sequence is much more effective as a recombination center in the low-resistivity p-type Cz material than in the high-resistivity n-type FZ material. Even the worst cleaning sequence only introduced enough impurities in the FZ wafers to reduce their lifetime to 100 μs. The Cz wafers, with a starting lifetime of about 100 μs, should have only been reduced to 50 μs if the impurities had the same effect; yet the observed reduction in lifetime is more than an order of magnitude greater.

SURFACE DAMAGE REMOVAL

In conjunction with the cleaning optimization, we have also studied two different techniques for removing the surface damage on unpolished wafers. We first used 1:1 potassium-hydroxide and water

ether (degrease), ... buffered oxide etch (BOE), nitric-hydrofluoric silicon etch, sulfuric-peroxide clean (piranha), caustic choline clean (Summa), hydroxide-peroxide clean (RCA1), hydrofluoric acid dip (HF), and hydrochloric-peroxide clean (RCA2). Four additional parameters were introduced: initial wafer contamination, time delay between cleaning and oxidation, oxidation temperature, and forming-gas anneal temperature. The results of this main-effects experiment have been presented previously [2]. The most important factor that emerged from the main-effect experiment was the inclusion of an HF-dip/rinse/spin-dry as the last step before oxidation. Other potentially beneficial factors were the inclusion of a degrease, nitric:HF, and piranha clean. The effectiveness of nitric:HF in removing metal ions, especially iron, has been reported previously [3]. The nitric:HF also proved beneficial in improving the overnight stability of the lifetime. We found no basis for choosing the relatively complex and expensive RCA process [4].

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SURFACE DAMAGE REMOVAL

In conjunction with the cleaning optimization, we have also studied two different techniques for removing the surface damage on unpolished wafers. We first used 1:1 potassium-hydroxide and water (KOH) at 85°C for 5-10 minutes to remove about 40 μm (20 μm per side) from the wafers, consistent with published data [5]. This process proved to be rather messy, generating a lot of particulate residue on and around the etch bath because it was necessary to remove the lid to agitate the wafers continuously to insure uniform etching. Even then, the wafer surfaces were rough enough to interfere with fine-line photolithographic alignment and

Fig. 1. Correlation of float-zone and Czochralski wafer recombination lifetimes for a wide variety of preoxidation cleaning sequences.

ellipsometry. The KOH process was used to prepare all of the FZ wafers used in the main-effects experiment.

Attempts to use lower-temperature (50-70°C) KOH etching solutions in a recirculating bath to eliminate the particulate residue were not successful, resulting in very rough wafer surfaces with poor uniformity.

Ten months ago, we switched to a 15:1 nitric:HF room-temperature silicon etch, performed in a recirculating bath. Ten minutes in this solution removes about 60 μm (30 μm per side) of silicon, consistent with published data [6]. This treatment leaves the surfaces fairly smooth. Additional thinning in this solution produces nearly specular surfaces, but tends to feather the wafer edges, making them very fragile. This solution also produces orange nitrogen dioxide fumes that may need to be scrubbed in an industrial setting. Although waste disposal costs for this solution are rather high due to the mixing of an acid and oxidizer, it should be possible to neutralize the solution on-site to produce an effluent that is free of metal ions. We have found that we can reuse the same 12-liter bath of nitric:HF mixture for many wafer batches if we replenish 1.5 ml of HF for every wafer-minute of etching. Otherwise, the silicon etch rate decreases with each use of the solution.

Two months ago, we discovered that a ten-minute etch in a 70°C KOH solution (1:2 KOH:H_2O) following the nitric:HF polishing etch yields a nearly specular surface and improves the post-oxidation PCD lifetime of high-resistivity float-zone wafers. Table 1 lists the results from two lots in which

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these PCD measurements, we presume that the KOH improvement is due to reduced recombination at the smoother surfaces.

Table 1
Evaluation of KOH after Nitric:HF
Average PCD Lifetime (μs)
95% confidence limits ±15%

Lot ID	Light Bias	Nitric:HF	Also KOH
Life55	None	1909	3679
Life55	100%	475	853
Life56	None	2639	3316
Life56	100%	482	675

THE LIFETIME BASELINE

Based on the results of the main-effects and damage-removal experiments, a relatively simple baseline process has been established to monitor contamination in the chemical baths and furnace oxidation tubes. The lifetime baseline process involves damage-removal, cleaning, dry oxidation, annealing, and measurements. The damage-removal process involves HF, nitric:HF, and KOH etches. The cleaning process involves only HF and nitric:HF solutions. Oxidation is at 1000°C, followed by an in-situ inert-gas anneal, then a forming-gas anneal at 450°C. The PCD lifetime is measured both with and without light bias, after waiting at least one hour for the surfaces to stabilize. The oxide and wafer thickness are also measured.

Parameter variations have been explored in an attempt to simplify the process and reduce chemical consumption. After applying a damage-removal etch to any unpolished wafers, the cleaning sequence requires only a 15-second 10:1 H_2O:HF dip, 10 minutes of 100:1 nitric:HF etch, and a final 50:1 H_2O:HF dip. All of these chemicals are at room temperature and can be reused, although the final 50:1 HF dip should be replaced frequently to prevent plating contaminants onto the wafers.

The baseline oxidation is performed with the wafers split between two different furnace tubes so that contamination can be traced to either the chemical baths or one of the furnace tubes. Tube 2 is normally used for phosphorus diffusion, and tube 3 is normally used for dry oxidation. Two clean baffle wafers are placed on each end of the wafers in the furnace boat, to minimize end effects. The wafers for each tube are pushed at 800°C in a nitrogen ambient. The temperature is ramped to 1000°C at 5°C/min using nitrogen in tube 2 and argon in tube 3. The ambient is then switched to oxygen for 30 minutes. After this time, the ambient reverts to either nitrogen or argon for a

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Fig. 2 shows the post-oxidation PCD lifetimes obtained in the PDFL over the past year using the baseline cleaning process on high-resistivity n-type FZ wafers. Lifetimes are shown both with and without light bias, with each value representing the average of 30 measurements spread across six wafers from both furnace tubes. Although the light and dark results tend to follow one another, there are some significant deviations that have been traced to variations in the damage-removal etch, to be discussed at the end of this section.

Fig. 2. PDFL lifetime baseline experience using nitric:HF for damage removal and cleaning of high-resistivity n-type float-zone wafers.

With the exception of four lifetime "crashes," the dark PCD lifetime of these wafers has remained above 1 ms. Recovery from the first three of these crashes was obtained by acid-cleaning the chemical baths using HCl. Beginning in February 1991, we started using a fresh solution of 50:1 H_2O:HF for all lifetime baseline lots, and this has improved the consistency somewhat. The recent lifetime crash in June 1991 was traced to nickel contamination on the plastic-tipped vacuum wand used to load and unload the wafers from the furnace boat. This same wand had been used to load some nickel-plated wafers into the forming-gas anneal tube. Fig. 3 illustrates the lifetime as a function of position for one particular wafer from this lot. The lifetime was adversely affected only in the lower-left portion of the wafer, which is where the wafers were grasped by the vacuum wand.

The lifetime baseline also provides a means to monitor the oxide growth rate as measured by ellipsometry [7] and the surface damage-removal etch rate as measured by a digital micrometer. We have observed that the oxide thickness grown in tube 3 is quite consistent, with a standard deviation from run-to-run of ±4%. However, a large

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Fig. 3. Lifetime map for one wafer in lot Life52, illustrating contamination restricted to the lower-left corner of the wafer.

By measuring the wafer thickness at both the start and finish of the baseline process, it is possible to monitor the damage-removal etch rate. We found that the etch rate in the 15:1 nitric:HF solution was very inconsistent, but that it could be stabilized by replenishing the HF after each use. Until this procedure was implemented, the lifetime baseline lots served as an unintended experiment comparing the PCD lifetime against the amount of silicon removed by the etch. Fig. 4 illustrates the light-biased PCD lifetime obtained for furnace tube 3. The light-biased PCD measurement is used for this purpose because it is more sensitive to the surface condition, presumably because in the absence of light bias there is enough energy-band bending to repel carriers away from the damaged near-surface region.

Fig. 4. Correlation of light-biased PCD lifetime with amount of silicon removed from unpolished

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Fig. 4. Correlation of light-biased PCD lifetime with amount of silicon removed from unpolished high-resistivity n-type FZ wafers.

Fig. 4 shows a clear increase in lifetime as silicon is removed, up to about 40 μm (20 μm per side), with somewhat less effect apparent beyond that point. Note that most of these lots used only a nitric:HF polishing etch, but a few of the more recent lots included an additional KOH etch to

produce a smoother surface. The lot that was contaminated by the vacuum wand was excluded from this data set.

CONCLUSIONS

A series of controlled experiments has been performed in our Photovoltaic Device Fabrication Laboratory to evaluate the effect of various chemical surface treatments on the recombination lifetime of crystalline silicon wafers subjected to a high-temperature dry oxidation. Both float-zone and Czochralski materials were evaluated, and correlations between the two materials were presented. We also evaluated the effect of different chemical damage-removal etches for unpolished wafers and found that a nitric:HF etch followed by a mild KOH etch gives the best lifetime and surface smoothness. From this series of experiments, we deduced a simple preoxidation cleaning sequence based on nitric:HF solutions that yields recombination lifetimes consistently greater than 1 ms in high-resistivity float-zone wafers.

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PREOXIDATION CLEANING OPTIMIZATION FOR CRYSTALLINE SILICON

Paul A. Basore and M. Elaine Buck

Sandia National Laboratories

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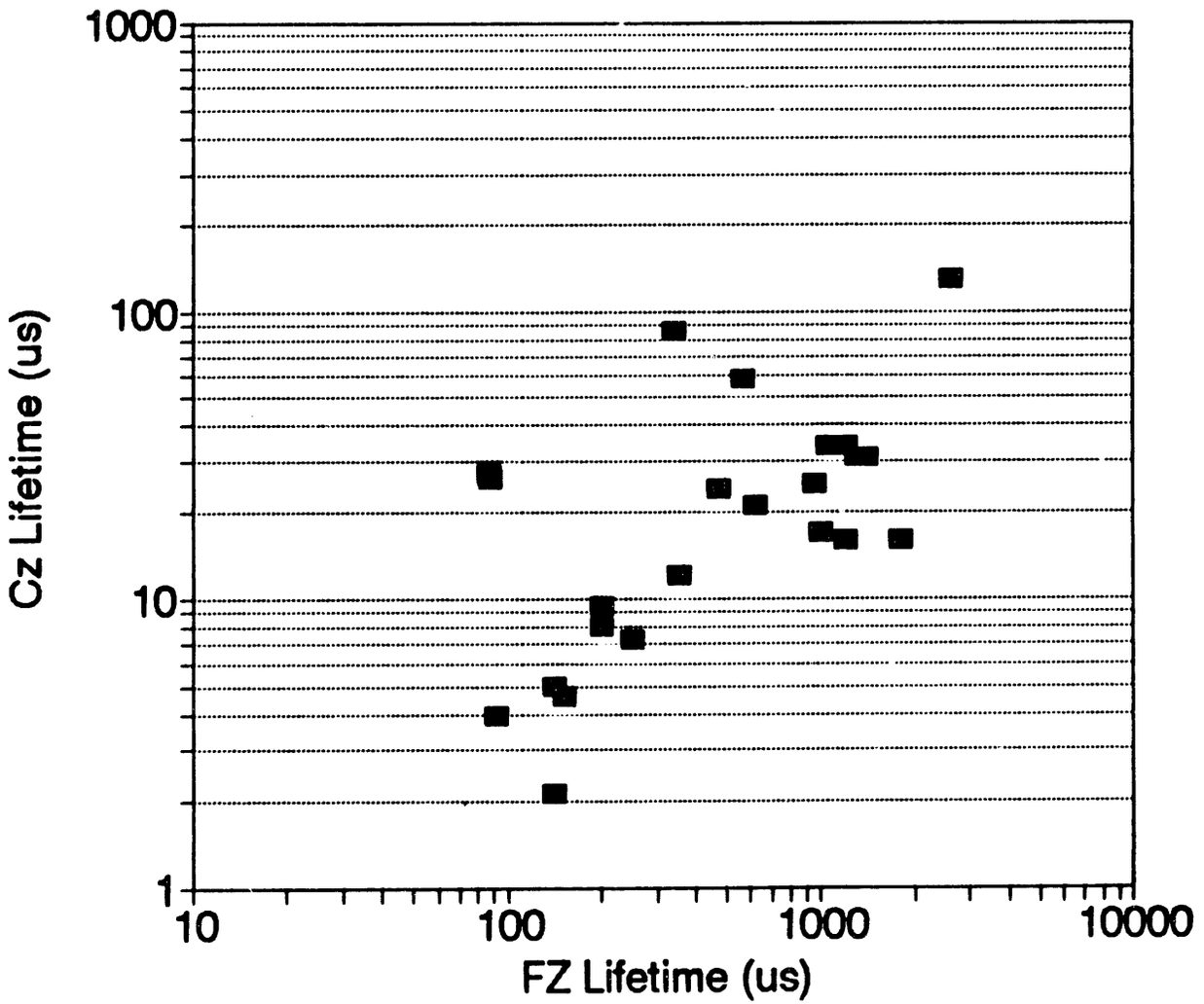
Comparison of Cz and FZ Lifetime



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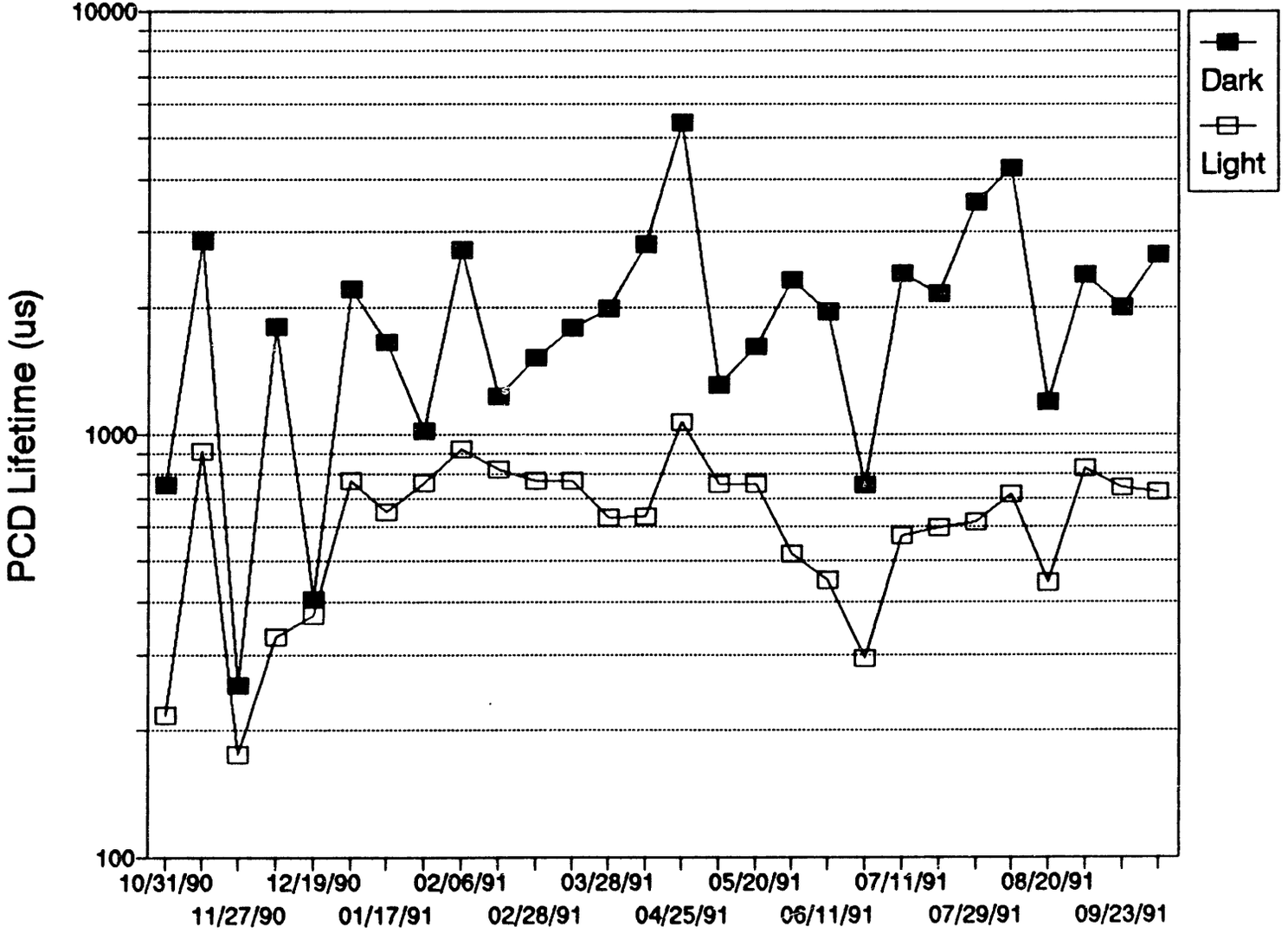

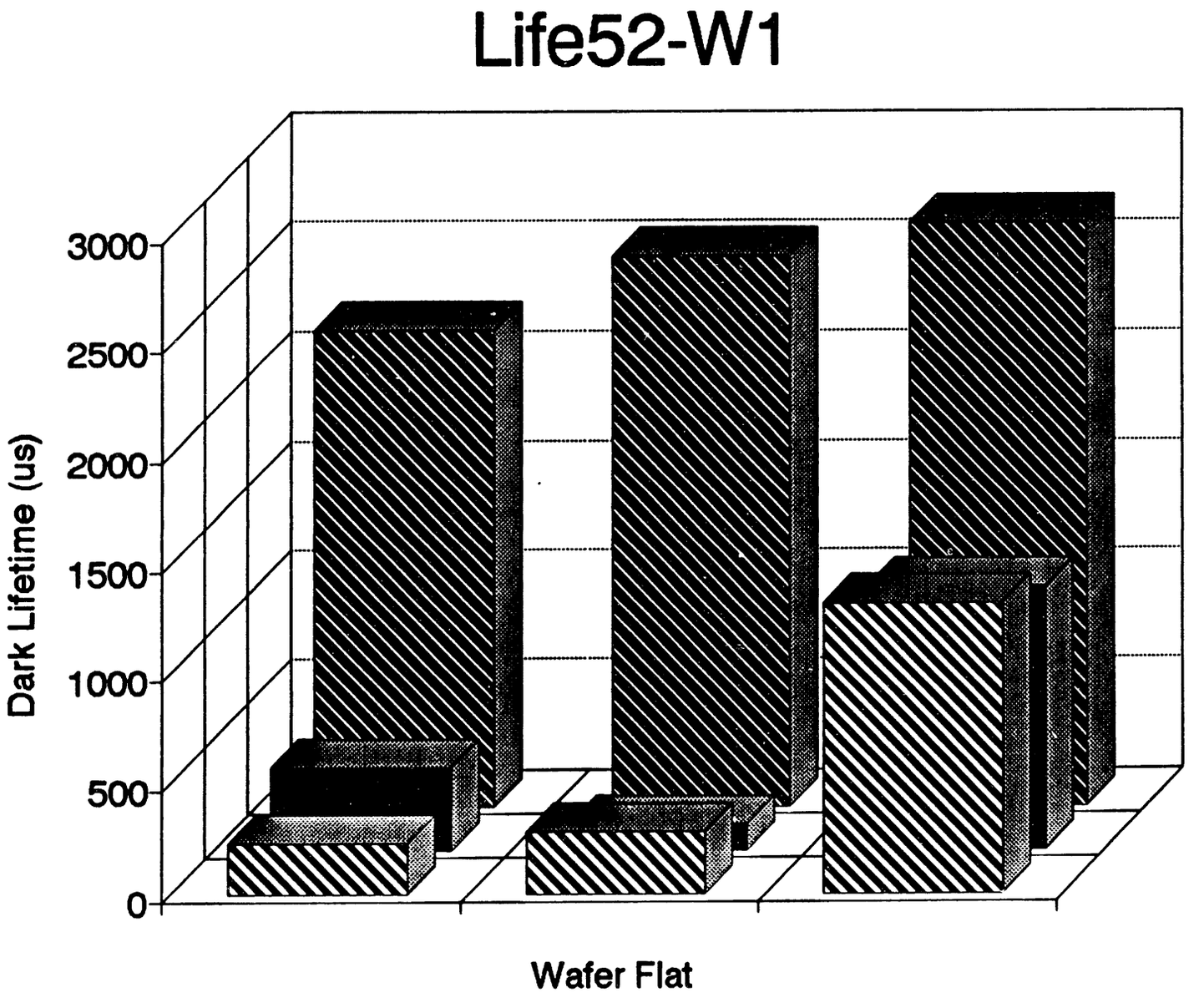
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Dark Lifetime (us)
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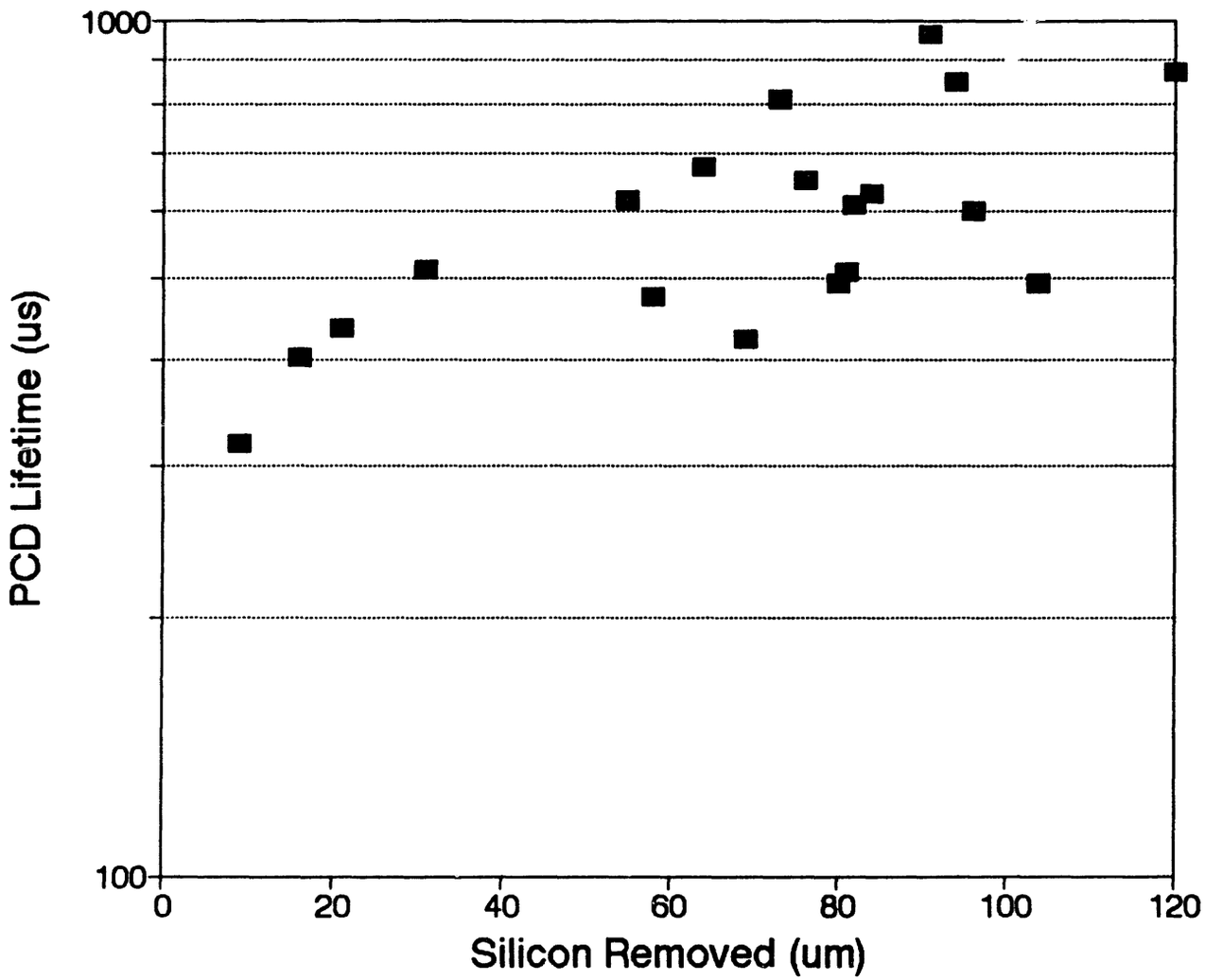
2500
2000
1500
1000
500
0
Wafer Flat

Effect of Silicon Etch on Lifetime



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