IMPACT OF AGING ON RADIATION HARDNESS*

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ABSTRACT

Burn-in effects are used to demonstrate the potential impact of thermally activated aging effects on functional and parametric radiation hardness. These results have implications on hardness assurance testing. Techniques for characterizing aging effects are proposed.

INTRODUCTION

Over the past few years, we have shown that the radiation response of MOS devices can change dramatically if devices are exposed to a pre-irradiation elevated-temperature stress [1,2]. Pre-irradiation stresses have been shown to significantly affect the radiation response of transistors and ICs for both radiation hardened and commercial CMOS technologies. Pre-irradiation stresses, e.g., burn-in, can lead to larger increases in IC static power supply leakage current during irradiation, and to a lesser degree increases in timing parameters. Others [3] have also observed results similar to those in Ref. [1] for ICs packaged in ceramic and plastic packages. This later work showed that pre-irradiation stresses significantly enhance radiation-induced changes in parametric response of CMOS ICs packaged in plastic packaging as opposed to those packaged in ceramic packages. In addition, it has recently been determined that pre-irradiation stresses can also affect the radiation response of some bipolar linear technologies [4]. These studies [1-4] indicate that changes in radiation response due to pre-irradiation elevated temperature stresses may be observed in a wide range of technologies (CMOS and bipolar).

Based on these results [1-3], the U. S. test guideline MIL-STD-883, Method 1019, which defines total-dose testing for the U. S. Department of Defense, has been modified as illustrated in Fig. 1. Before the modification, the test guideline permitted manufacturers to qualify the total-dose radiation response prior to elevated temperature reliability screens. This raises the possibility that the total-dose radiation response of ICs sensitive to burn-in effects could be significantly different than the radiation response of ICs used for qualification testing. Thus, Test Method 1019 was modified to require manufacturers to perform

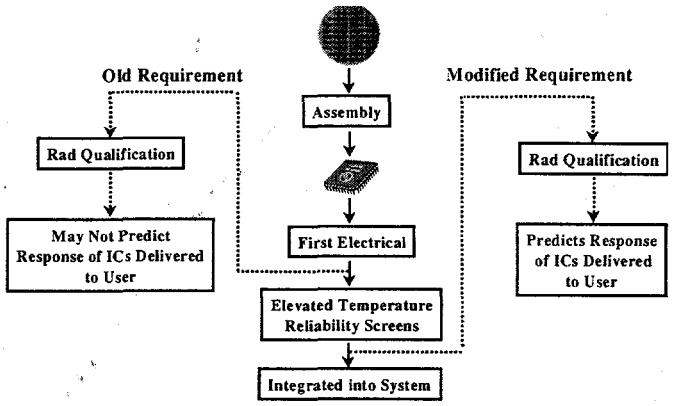

Figure 1: Modifications made to MIL-STD-883, Method 1019 to account for burn-in effects.

radiation qualification testing on sensitive ICs following all required elevated temperature stresses in order to ensure that the ICs passing radiation qualification would function as intended during system operation.

Other system scenarios can potentially produce effects similar to those of burn-in on radiation response. One of these scenarios is "aging." Aging is a change in device response that occurs from the time the device is qualified for system use to the end-of-life in a system. Aging is becoming increasingly important as national policies have mandated that military systems remain in the stockpile for longer periods of times, thus extending the lifetime of components beyond their original intended use period.

In this work, we examine the potential effects of aging on ICs through a discussion of accelerated aging effects using high temperature stresses (e.g., burn-in). Results indicate that for some device types aging can lead to increased radiation-induced device degradation that is not presently accounted for in Method 1019. Techniques for characterizing thermally activated aging effects are recommended.

ACCELERATED AGING EFFECT

We first illustrate high-temperature accelerated aging effects by examining the radiation response of three commercial static random access memories (SRAMs) in total dose environments with or without an elevated temperature stress. All SRAMs were obtained from the

manufacturer without a previous burn-in or other high-temperature reliability screen. Some of the SRAMs were then bias stressed (i.e., burned-in) for 1 week at 150 °C with nominal values of V_{DD} applied during the elevated temperature biased stress. Chip enables and output enables were tied inactive, and all other inputs were tied in a non-conflicting manner to either high or low. SRAMs (at least 4 burned-in and 4 non-burned-in) were irradiated using a 10-MeV electron linear accelerator (LINAC) located at the Boeing Aerospace Corporation Physical Sciences Laboratory, Seattle, Washington. Multiple 9 μs width pulses were used during prompt total ionizing dose (TID) testing. During these tests, it was necessary to keep the individual pulse dose-rate below the device upset level to ensure that the exposure pattern written to the memory was maintained.

Both a 5-V (PDM41256LA) and 3.3-V (PDM31256L) SRAM manufactured by Paradigm Corporation were examined. These devices are non-hardened high-performance CMOS SRAMs organized as 32k x 8 bits and produced in a 0.8-μm, proprietary bulk CMOS technology. The 3.3-V devices were fabricated in Japan and the 5-V devices were fabricated in San Jose, CA. The ICs operate from a single power supply and all inputs are fully TTL compatible. The low-current version were evaluated. The 5-V and 3-V SRAMs were packaged in plastic 28-pin 300-mil surface mount J-leaded (SOJ) packages. In addition to the Paradigm devices, we also examined the response of the Cypress CY7C1399. It is a 3.3 V high performance SRAM which is organized as 32k x 8 bits. This device is fabricated using a 0.5 μm technology with 14.5-nm gate oxides, and non-epi p-substrates. The Cypress devices studied in this work were packaged in 300-mil 28-pin dual-in-line (DIP) ceramic packages.

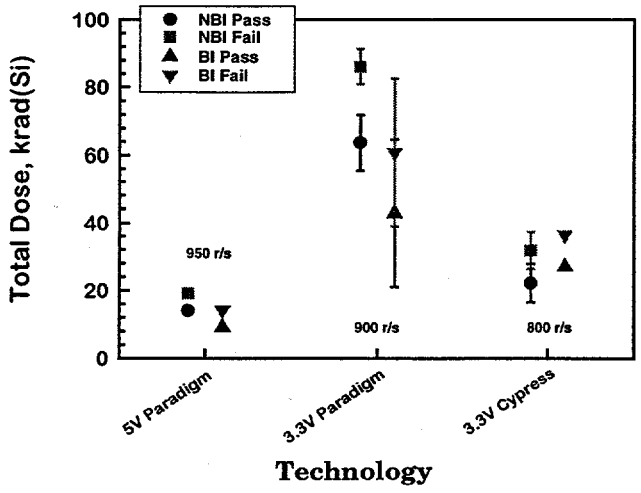

Figure 2: Prompt TID results show a pronounced burn-in dependence for some of the SRAMs. (NBI – SRAMs without burn-in, BI – SRAMs with burn-in)

Figure 2 summarizes radiation results for the three part types. This figure gives the spread in the highest total dose levels where SRAMs were still functional and the spread in the total dose level where the SRAMs first failed functionally. Data are shown for SRAMs with and without a pre-irradiation burn-in. Of the three SRAMs examined, the 3.3 V Paradigm SRAMs showed the most sensitivity to the burn-in effect. Examination of the Paradigm 3.3 V data shows a significant burn-in effect with non-burned-in devices first failing functionally at ~80 krad(Si) vs. ~40 krad(Si) for burned-in devices. Thus, the total-dose radiation hardness of these SRAMs has been reduced by ~50% following only a 1-week burn-in. *This is the first time that burn-in has been shown to affect functional failure as well as parametric degradation.* Only a ~33% reduction in functional failure level due to burn-in was observed for the Paradigm 5 V devices. These SRAMs first failed functionally at 12 krad(Si) compared to non-burned-in parts, which failed at 18 krad(Si). The Cypress SRAMs showed no significant reduction in total-dose response as a result of burn-in. This supports earlier work that shows that not all technologies exhibit a burn-in effect.

These results confirm that burn-in can be a significant problem for some technologies. An elevated temperature burn-in is often used to accelerate temperature activated aging processes. For instance, burn-in is routinely performed on all deliverables to reduce the possibility of "infant" mortality in ICs, while 1000 hour elevated temperature life tests are used to address long term reliability problems. The burn-in response of Fig. 2 indicates a potential aging problem due to a thermally activated process. Thus, both Paradigm SRAMs may be prone to long-term aging effects, while the Cypress SRAMs may not exhibit aging effects. Note that aging includes burn-in, other reliability screens (including additional burn-ins required by system use), as well as long term storage and actual system conditions. Depending on system conditions, long-term storage could require some types of devices to be maintained at elevated temperatures over extended periods of times. Indeed long-term storage and actual system use can be considerably more severe for a thermally activated process than a 1-week burn-in, depending on the activation energy of the process and the specific use conditions. This is especially troublesome because previous results have shown the burn-in effect does not saturate for some device types with increasing burn-in time for times up to three weeks at 150°C [2]. It is currently unknown if the burn-in effect saturates at longer times. Whether system related aging or burn-in is more severe may depend on many factors including device properties and system application. Note that the burn-in effect has been shown

to be bias independent [2], important for aging effects due to the fact that many parts may be unbiased during storage or system use. The possibility that aging may be more severe than burn-in indicates that Method 1019 may not be sufficient to ensure ICs will meet intended system requirements. Representative techniques for ensuring radiation hardness in a long-term aging environment are discussed below.

Thermally activated effects of aging at long times can often be estimated with short-term elevated temperature anneals. Figure 3 is a plot of the radiation-induced voltage shift at a current level of 10 nA for n-channel field-oxide transistors irradiated to 50 krad(SiO_2) versus pre-irradiation stress time. Transistors were stressed at 150°C with a 5 V bias on the gate. The field-oxide transistors were fabricated at Sandia in the CMOS IIIA technology. The field-oxide thickness was approximately 800 nm. Previous work has shown for these devices that the activation energy for the burn-in mechanism is approximately 0.38 eV [2]. Assuming this activation energy also governs the long-term aging response (which is the same type of assumption used to relate life testing to system reliability prediction), one can estimate the voltage shift at other storage times and temperatures for a given irradiation dose level. For example, listed in Fig. 3 are times corresponding to different periods of room temperature aging. Thus, a 1-week burn-in corresponds to approximately a 2.23-year room temperature aging and will produce approximately a 9 V change in radiation induced field oxide voltage shift following a 50 krad(SiO_2) exposure for these devices. Extrapolating the voltage shift to longer times, it is observed to take approximately a $2x10^7$ s (231 days)

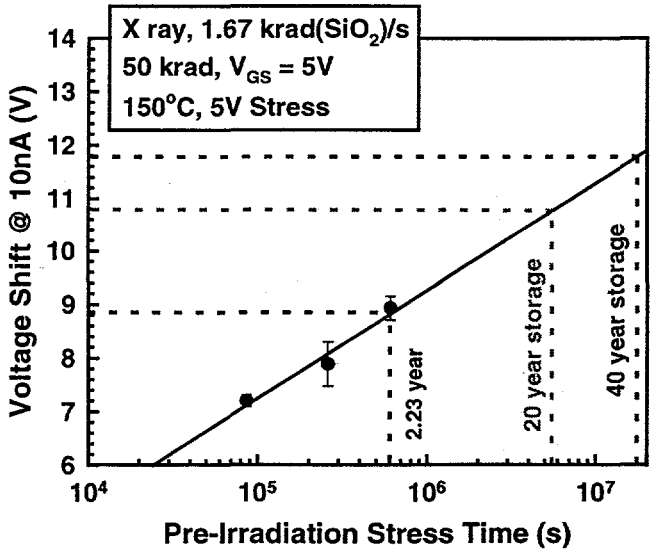

Figure 3: Significant increases in stress time needed to simulate aging impact.

150°C burn-in to simulate a 40-year room temperature aging process with a 0.38 eV activation energy. This extrapolation assumes a constant activation energy and that the burn-in effect does not saturate at longer times. Considerably longer pre-irradiation stress times will be required to estimate changes in radiation response for ICs that are stored or must function at elevated temperature in system use.

Naturally, long pre-irradiation stresses required to simulate long term aging processes at either room or elevated temperatures are not practical for routine radiation qualification, but at some point must be performed to validate extrapolations based on shorter-term tests like those in Fig. 3. Note that, instead of transistor voltage shift, other transistor and/or IC parameters (e.g., IC functional failure level or changes in static supply leakage current) could have been used to estimate changes in radiation response due to aging.

HARDNESS ASSURANCE METHODOLOGY

To date, test methods have not been developed to account for the potential effects of device aging during system use on radiation hardness. Note that conservatively assuring radiation hardness is different than estimating radiation hardness. For example, Fig. 3 shows a technique to estimate radiation-induced changes in thermally activated aging effects from elevated temperature short-term stresses for a case in which the activation energy is known. Extrapolating the elevated temperature response to longer times assumes the elevated temperature radiation response does not saturate or that the rate of increase in parametric response does not decrease with increasing stress time. If the parametric response is not linear with time (e.g., saturates), then one will not be able to accurately *estimate* long-term aging effects from short-term elevated temperature stresses. However, as long as the parametric response is the same or increases at a slower rate with time (i.e., there are no latent buildup effects [5]), one can *assure* that estimated degradation will always be more than the actual degradation due to aging. Thus, under these conditions, the estimated degradation will conservatively estimate the worst-case aging degradation.

Based on these results, we next suggest a technique for characterizing aging effects. Developing a characterization technique for technologies that show aging effects requires a thorough understanding of the response mechanisms. At this time, we are only considering thermally activated processes. There also may be field or stress activated mechanisms. Unfortunately, our understanding of these thermally activated response mechanisms is quite limited at this

time for most devices. So these recommendations are a way to gather sufficient characterization data to support future possible changes to hardness assurance test methods.

We now illustrate how characterization tests for aging response might fit within a hardness assurance method based on Method 1019. Phase 1 of Method 1019 is a conservative test for functional failure caused by n-channel gate oxide or parasitic field-oxide transistor shifts due to radiation-induced oxide-trapped charge. Phase 2 of Method 1019 (rebound test) is a conservative test for failure due to long-term buildup of interface traps. Characterization of aging effects can be integrated into the 1st phase of Method 1019. This is because burn-in has been shown to increase the amount of radiation-induced oxide-trapped charge, but suppresses the amount of radiation-induced interface-trap charge [1-4].

Figure 4 is a flow diagram of an aging/burn-in characterization technique based on Phase 1 of Method 1019. Because the type of package can significantly affect burn-in and aging, devices must be packaged in the same type of package used in the system application. If more than one type of package is required, characterization tests may be required on each type for a burn-in sensitive part. Following packaging, half of the test samples should be exposed to a 1-week, 150°C burn-in. If 150°C is higher than the specification limits for the package, then the highest temperature allowable for the package should be used. This is especially important to consider for plastic packages which are seldom rated for use at temperatures as high as for ceramic packages. The second group of samples should not see any elevated temperature stress. All devices should be irradiated to the total dose specifications at a dose rate of 50 to 300 rad(Si)/s followed by electrical test. If the change in parametrics for the burned-in devices is significantly larger (e.g., more than 20% after allowing for device-to-device variations) than the change in parametrics for non-burned in devices, then the device should be considered to have a burn-in effect. If there is no burn-in effect, one proceeds with Method 1019 and no further burn-in or aging characterization testing is required. However, if there is a burn-in effect, one must next determine the activation energy for the mechanisms responsible for the burn-in effect. Once an activation energy has been determined, the change in parametrics can be estimated, as shown above, for a given aging requirement to determine if the parts will meet system requirements. Lot acceptance of such burn-in/aging sensitive parts would then require that parts be subjected to an elevated temperature preconditioning treatment that appropriately simulates

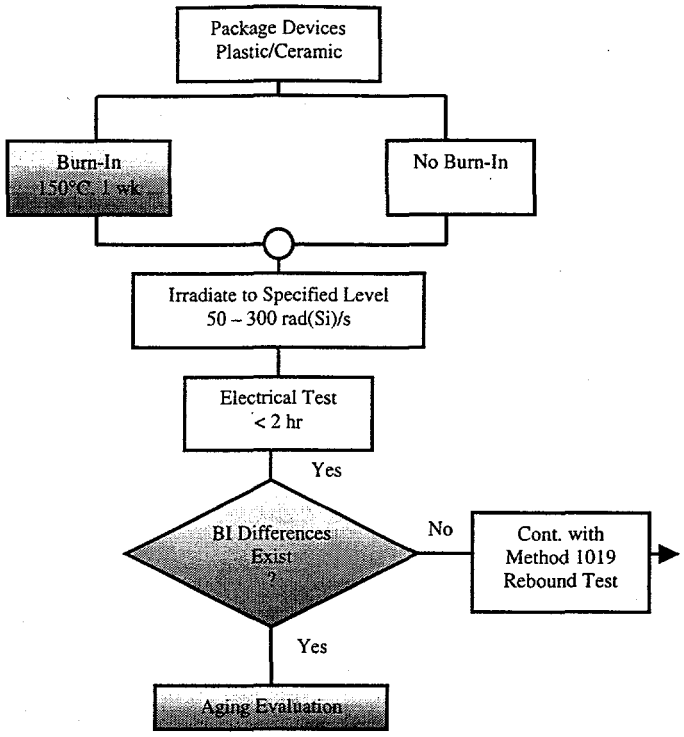

Figure 4: Techniques for integrating characterization of thermally activated aging effects in a hardness assurance plan based on Method 1019.

device aging in system qualification and use, as will be described in the full paper.

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