SURPRISING PATTERNS OF CMOS SUSCEPTIBILITY TO ESD AND IMPLICATIONS ON LONG-TERM RELIABILITY*

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Abstract

CMOS ESD failures in a product where, by design, the device input terminals are not accessible to ESD led to this study of device susceptibility and an analysis of the long-term reliability of devices in assemblies from that production line. This paper shows some surprising patterns of device susceptibility and shows that the probability of long-term failure of devices whose electrical characteristics have been degraded by electrostatic discharge is small.

Introduction

The use of sound ESD preventative procedures in design and fabrication of fire sets for weapons systems is an obvious requirement to achieve the required reliability. Techniques for providing protection from electrostatic discharge (ESD) have been learned by experience and are in continuous use in the design and fabrication of such systems. Therefore, it came as a surprise when CMOS integrated circuit failures which appeared to have been caused by ESD occurred on a fireset production line.

In a period of about three months, several fireset units failed a final functional test at the completion of the last stage of assembly. The cause of failure was traced to the failure of five CMOS 4021A eight-stage shift registers in potted subassemblies. Detailed failure analysis disclosed gate oxide ruptures in three of the 4021A circuits. The failure mode of the other two 4021A circuits was a high current in one input terminal. The failure mechanism was not found.

Each subassembly had been given a complete functional test, with no failures detected, just prior to final assembly. Further, the gate oxide ruptures occurred at gates of the 4021A for which inputs are not directly accessible by way of the terminals of the subassembly. At the subassembly or final assembly stage no CMOS input leads come to terminals or connectors that are accessible to inadvertent ESD. In addition, all CMOS inputs are protected by resistance networks in the circuit external to the IC package.

Several immediate questions arose:

- What caused the failures?
- If they were caused by ESD, did the stress occur at component level (supplier test or incoming inspection) with resultant failure at a later time?
- What is the risk that other devices in the final assemblies have been exposed to ESD and will become failures in time?

Although considerable information is available on the susceptibility of individual integrated circuits to ESD,[1,2] little information is available on the susceptibility of circuit assemblies containing CMOS devices. Previous work[1,2] on latent failures of devices exposed to ESD has been inconclusive because of the difficulty in accessing the damage done by the ESD and determining if failure mechanisms related to the damage and leading to failure exist. Perhaps the most puzzling instance is the case of gate oxide rupture where the rupture does not cause functional failure. The damage site has associated with it an unknown potential for latent failure.

The goal of the work described in this paper is to duplicate with intentional ESD the type of failures found in the fireset, thus isolating a possible cause of failure, and to investigate the possibility of latent failures after long-term use of a device degraded by ESD. This paper will also demonstrate the susceptibility to ESD of the 4021A and other CMOS devices in a circuit simulating the actual circuit in which the failures occurred.

Experimental Plan and Results

Since the source of the ESD causing the failures was unknown, no effort was made to simulate a particular ESD. Instead, a standard human body equivalent circuit was used.[3] A schematic of this circuit is shown in Figure 1. The circuit features a 100 pf capacitor which is charged to the desired ESD voltage. The charge is then dumped through 610 ohms to the circuit under test. The current through the device under test is recorded on a storage oscilliscope by measuring the voltage across a 50 ohm sensing resistor.

Resistance networks approximating the actual resistance seen by each device terminal in the circuit were added to the ESD circuit. The resistance network used for the 4021A is also shown in Figure 1. Twenty kilohms are in series with each parallel input transmission gate, 5 megohms are in series with each standard inverter

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input, and 10 megohms are in series with each output. The power supply terminals (V_{DD} and V_{SS}) go directly to the power supply.

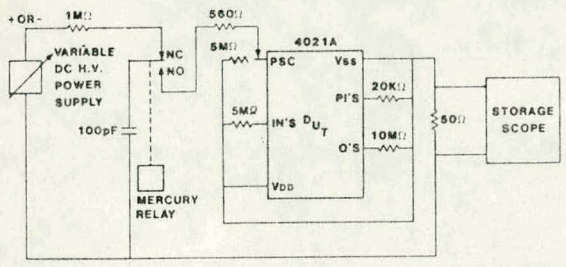


Figure 1. Simulated "In Circuit" EST Test Circuit.

The experimental plan is as follows:

1. Initial device selection and characterization.
2. Step stress with ESD on various input, output, and supply terminals to establish the threshold for parameter degradation and for catastrophic failure.
3. Perform an accelerated life test on selected units stressed in Step 2 to determine possible latent failure mechanisms.
4. Simulate the fireset failures using controlled ESD.
5. Continue step stress on selected units to establish stress levels causing catastrophic failure.
6. Perform sufficient detailed failure analysis to establish failure modes and failure mechanisms.

Each of these steps will be discussed in detail.

Device Characterization and Selection

One hundred Mil M 38510/05704 Class A, 4021A units, date code 7537, were purchased. These devices were tested 100 percent against the 38510/05704 DC and functional tests using a Fairchild 5000C integrated circuit tester. All tests were data logged. Input leakages were all less than 5 nA and static I_{SS} was less than 50 nA. In contrast, the units used in the fireset assemblies where the failures occurred were purchased as RCA Class B equivalent (CD4021A/3), then given an additional burn-in (72 hours at 175°C) and tested 100 percent to the 38510/05704 DC and functional tests. Care was taken in all testing and handling to ensure that no unintentional ESD occurred.

Step Stress

The 4021A shift register has eight parallel input transmission gates, PI_{1-8}, a parallel serial control input, PSC, a serial control input, SI, a clock input, CL, and three outputs, Q_{6-8}. The schematic is shown in Figure 2.

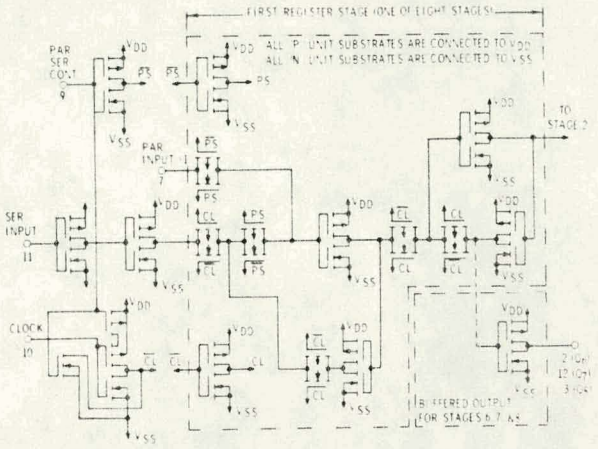


Figure 2. Schematic Diagram of 4021A.

Both positive and negative ESD pulses were applied to selected terminals. For each device only one terminal was stressed and the polarity was always the same. Table 1 is the test matrix. The ESD was initiated at 500 volts on two units for each terminal and polarity. The stress was increased in 500 volt steps up to a maximum of 1500 volts. The units were tested with the same test equipment and program as the initial tests after each stress. As soon as susceptibility was identified, more units were added to the matrix as shown in the table. These additional units were stressed at only one voltage. In order to verify that unintentional ESD was under control, all of the 100 units were tested after each step. Thus initially there were 80 control units. Then as additional units were stressed, the number of control units dropped to 47.

The results of initial step stress tests on 20 units showed that initial susceptibility to ESD was primarily in the supply terminals and the output terminals. Based upon these results 33 additional units were step stressed on supply and output terminals at the lowest ESD stress level found to cause degradation.

The overall step stress results were surprising and pointed the way toward duplication of the fireset failures. In the total of 53 units stressed, four were functional failures. Three of these had been stressed with a negative ESD pulse on an output terminal and the other had been stressed with a negative ESD pulse on the V_{SS} terminal. Twenty-two units showed an increase in static I_{SS} with values ranging from 1 μA to greater than 16 μA. These units were stressed either on supply terminals (18 each) or output terminals (four each). Nine units showed an increase in input leakage with values between 5 nA and 100 μA. These results are shown in Table 2.

TABLE 1
Step Stress Matrix, 4021A

NUMBER OF UNITS	TERMINAL STRESSED	ESD POLARITY	STRESS FOR ADDITIONAL UNITS
2+4	V_{DD}	+	1500V
2	V_{DD}	−	
2	Q_8	+	
2+10	Q_8	−	1200V
2	V_{SS}	+	
2+12	V_{SS}	−	1500V
2	PSC	+	
2+2	PSC	−	1500V
2	PI_7	+	
2+5	PI_7	−	1500V
80 FIRST, 47 LAST	CONTROL	NO ESD	

TOTAL TEST UNITS 53
TOTAL CONTROL UNITS 80 THEN 47

TABLE 2
Step Stress Results

NUMBER OF UNITS	DEGRADED PARAMETER	PRE LIFE TEST VALUE	POST LIFE TEST VALUE
19+15	I_{SS}	1 μA TO >16 μA	145 nA TO 1.3 μA
6	I_L	5 nA TO 100 μA	NO CHANGE
17+2	NONE	I_{SS} <50 nA I_L < 5 nA	NO CHANGE
12	CONTROL	I_{SS} <50 nA I_L < 5 nA	NO CHANGE
1	I_{SS}	98.57 μA	FUNCTIONAL FAIL AT 1.0 HOURS I_{SS}: 28 mA ALL INPUTS HIGH I_{SS}: 7.8 mA ALL INPUTS LOW

Accelerated Life Test

Forty-two of the 53 units that were subjected to the step stress and found to have a significant increase in static I_{SS} or input leakage were put on an accelerated life test. Twelve of the 47 control units were included in the life test. The accelerated life test consisted of operating the units in the circuit shown in Figure 3 at 150°C. At time intervals of 1, 4, 10, 30, 100, and 308 hours the units were removed from the test and electrically tested at room temperature. The test was terminated at 308 hours with no functional failures. Some minor increase in input leakage (less than 25 nA) was noted in some control units and some test units.

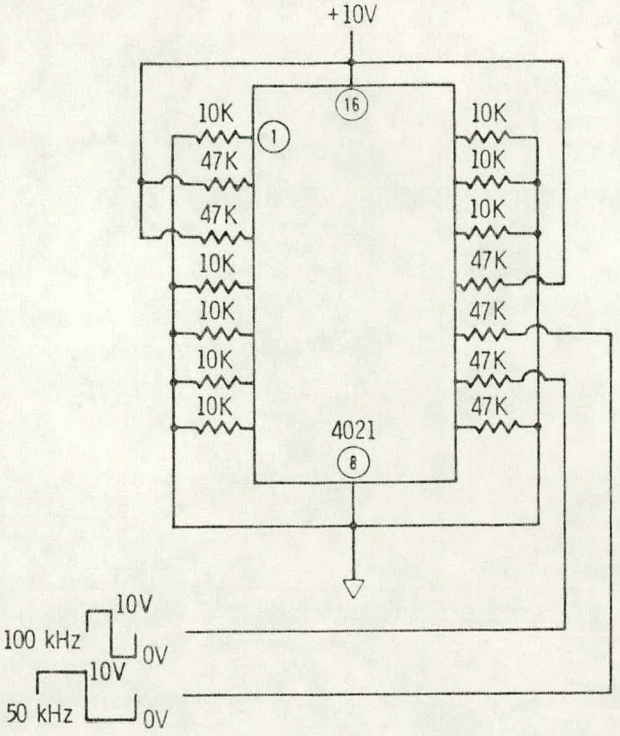


Figure 3. Operating Life Test Circuit.

The rest of the test units showed no change in input leakage during the life test. However, the units that had high I_{SS} improved during the life test. This improvement is shown in Figure 4.

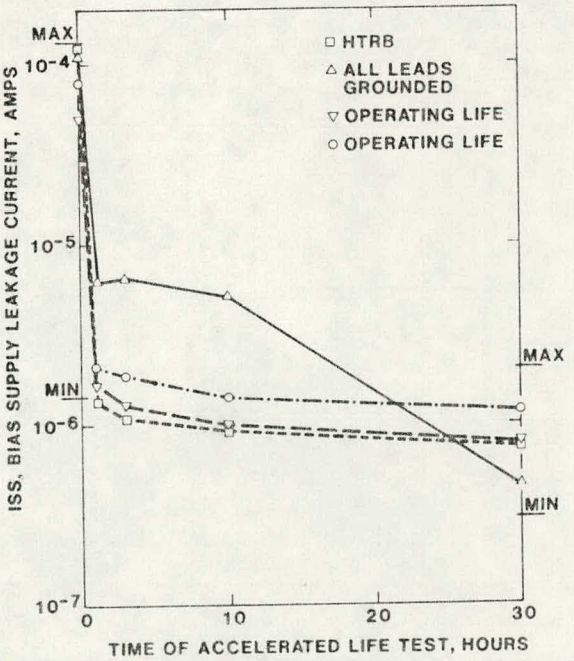
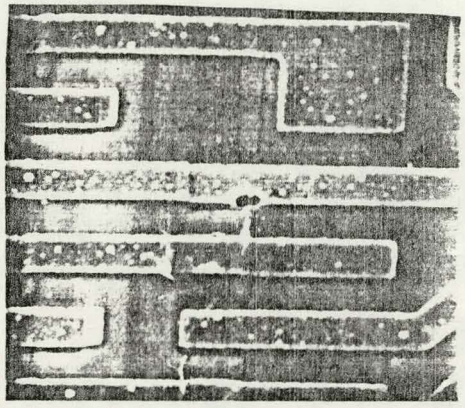


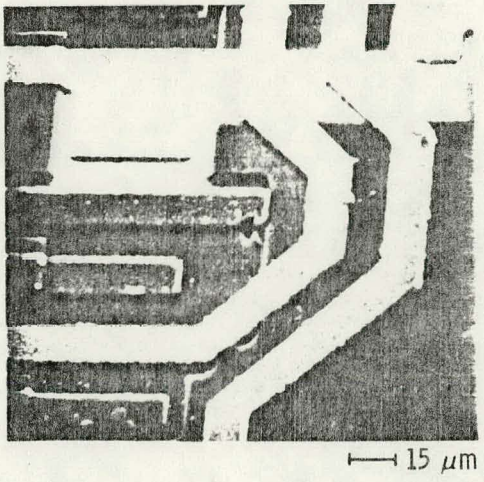
Figure 4. Improvement in I_{SS} During Operating Life.

Most of the improvement occurred during the first hour. At the termination of the test, no unit had an I_{SS} greater than 2 μA. No satisfactory explanation for this improvement in I_{SS} with time and temperature has been found.

One of the life test units that had an I_{SS} of over 16 μA as a result of the step stress was given a detailed failure analysis after the accelerated life test. Electrical data indicated that the leakage was associated with the PSC line to one of the parallel input transmission gates. The failure analysis disclosed that the cause of the high I_{SS} current was a rupture in the gate oxide of the p-channel transistor of the PI_g transmission gate. As stated previously, the unit was still functional before failure analysis. An SEM photomicrograph of the rupture is shown in Figure 5(a).



(5a) Gate Oxide Rupture on the N-Channel Transistor in the PSC Input. Unit Failed Functional Test.



(5b) Gate Oxide Rupture on the P-Channel Transistor in the PI_g Transmission Gate. Functional after Life Test.

Figure 5. Comparison of Two Units with Gate Oxide Rupture.

For comparison, Figure 5(b) is an SEM photomicrograph of a gate oxide rupture in a unit that was found as a functional failure in incoming inspection. The failure analysis verified that the failure was at the site of the rupture. It appears that a gate oxide rupture does not necessarily cause functional failure and that a unit with a gate oxide rupture does not necessarily become a failure in an accelerated life test. Instead, because of the improvement in I_{SS} with time and temperature, an accelerated life test may hide units whose I_{SS} leakage has increased because of ESD. As a further investigation of the possibility of failure of a degraded unit, particularly one with an oxide rupture, 18 additional units were subjected to one ESD pulse of -1000 volts on the V_{SS} terminal and put on the life test.

The results of the life tests are shown in Table 3. One of the 18 additional units was a functional failure at the end of one hour. Figure 6 is an SEM photomicrograph of a rupture in the gate oxide of a n-channel transistor in the PSC input of this unit. This unit had an I_{SS} leakage current of approximately 100 μA after the ESD stress. Thus, in contrast with the unit mentioned previously that did not fail in life test, this unit with a gate oxide rupture caused by ESD but still functional did fail in the accelerated life test. The unit that did not fail was stressed with -1500 V on the V_{SS} terminal whereas the unit that did fail was stressed with -1000 V on the V_{SS} terminal. The photomicrographs show that more energy was expended at the rupture site on the unit that did not fail.

TABLE 3
Accelerated Life Test Results

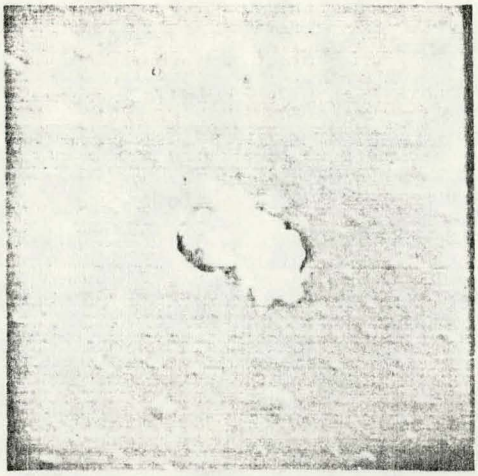
NUMBER OF UNITS	DEGRADED PARAMETER	VALUE	NUMBER FOR LIFE TEST
22	I_{SS}	1 μA TO >16 μA	19
9	I_L	5 nA TO 100 μA	6
4	FUNCTIONAL FAILURE	I_{SS} > 1mA	0
18	NONE	——	17
53			42

Figure 6. Accelerated Operation Life Test Failure. Gate Oxide Rupture on the N-Channel Transistor in the PSC Input.

Failure Simulation

While the accelerated life test was in progress, we made a successful attempt to duplicate the fireset failures. Four units were obtained from the fireset production line. Two of these units had the same date code (7622) as the failed units. The date code on the other two was 7750. Two of these units were step stressed with negative ESD pulses on the Q_8 output terminal and two were stressed with negative ESD pulses on the V_{SS} terminal. Stress started at 500 volts and was increased in 250 volt increments until functional failure. Detailed failure analysis on both units stressed on the V_{SS} terminal showed that the failure was caused by a gate oxide rupture on the n-channel input transistor of the PSC inverter input. Figure 7 is a comparison of one of these units to one of the fireset production line failures. Figure 8 is SEM photographs of the gate region of two units from the 7622 date code lot used as failure analysis control units. Comparison of the failing units to these control units led to the conclusion that the failure occurred at a point of high voltage stress and was not the result of device design or processing.

(7a) PRODUCTION UNIT. Gate Oxide Rupture on the N-Channel Transistor in the PSC Input.



(7b) ESD TEST UNIT. Gate Oxide Rupture on the N-Channel Transistor in the PSC Input.

Figure 7. Comparison of Production Line Failure and ESD-Created Failure.

(a)

3 μm

(b)

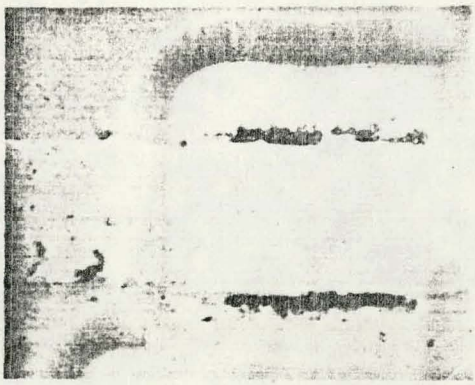


Figure 8. Control Units Analysis. Both Pictures Show the Gate Region on the N-Channel Transistor in the PSC Input.

Detailed failure analysis on one of the test units stressed on the Q_8 output terminal showed that the failure was caused by a rupture in the gate oxide on the n-channel transistor of the PI_8 transmission gate. Electrical data on the other test units stressed on Q_8 indicated the same failure mechanism. Two of the production fireset failures similarly were gate oxide ruptures of a PI transmission gate input. This simulation correlated with the fact that in the fireset production the V_{SS} terminal is always accessible to unintentional ESD and unused output terminals were not terminated with resistance or protected during assembly and potting. This correlation shows the probable cause of the production line failures to be ESD on V_{SS} and output terminals.

Step Stress to Functional Failure

Following the life test, 49 devices including 40 of the life test units were step stressed at 500 volt increments up to 5500 volts. Once a device became a functional failure it was removed from the test. Figure 9 shows that the V_{SS} and Q_8 terminals are the most susceptible to ESD. The greatest susceptibility is to negative pulses. The figure shows that, even though the ESD stress was applied directly to the inputs, there were no failures due to input stress below 3000 volts. Note that there were no failures on the transmission gate input below 4000 volts. Two of the 49 units did not fail. These two were stressed on transmission gate inputs.

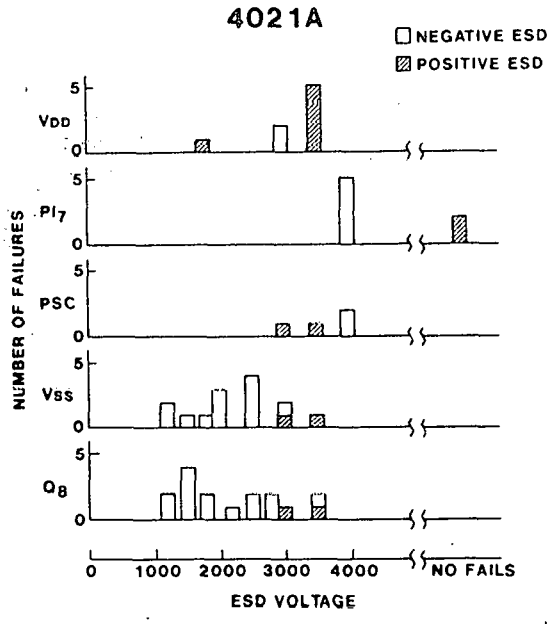


Figure 9. Step Stress to Functional Failure.

Susceptibility of Other Types of CMOS Integrated Circuits

We applied an identical (except that the maximum stress was 4000 volts) step stress to 29 silicon gate technology 4021B units for comparison of the metal gate technology with silicon gate technology. Figure 10 shows that the silicon gate units did not have the high ESD susceptibility on supply and output terminals. However, the input susceptibility was greater.

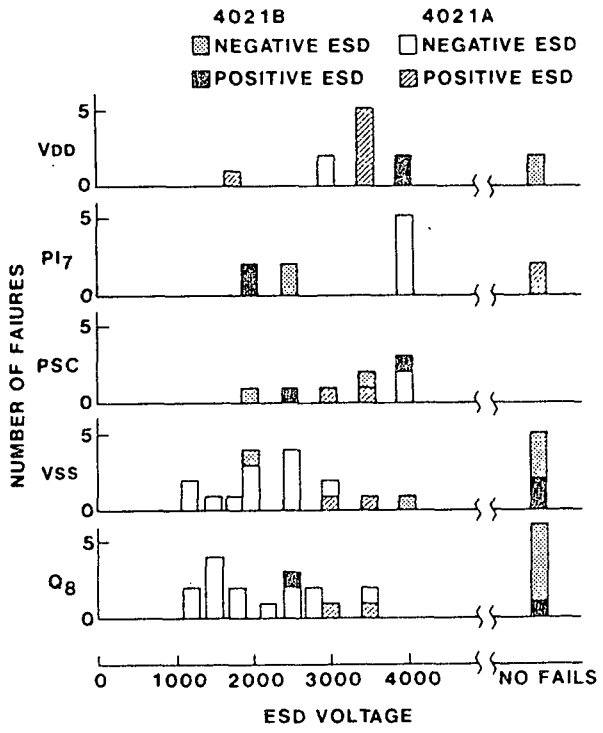


Figure 10. Comparison of 4021A and 4021B Devices.

The results of an identical step stress on a mix of eight each 4011A, eight each 4013A, and 20 each 4081B metal gate circuits are compared with the results of the 4021A in Figure 11. Except for the 4021A, supply terminals, output terminals and input terminals show comparable susceptibility. Note that, as expected, the B series is much more resistant to ESD than the A series as evidenced by the 4081B.

Failure Analysis

The detailed failure analysis in support of this work consisted of some or all of the following steps as required but not necesssarily in the order given.

1. Complete electrical characterization.
2. Delidding.
3. Visual inspection.
4. Removal of the phosphosilicate glass.
5. High magnification optical microscopy.

6. Voltage contrast, SEM.
7. Isolation of failure by opening metal paths with an ultrasonic probe.
8. Probe electrical measurements.
9. Removal of metallization.
10. Topographical analysis with SEM.
11. Selective removal of oxides and further SEM as required.
12. Energy dispersive SEM to identify contaminants.

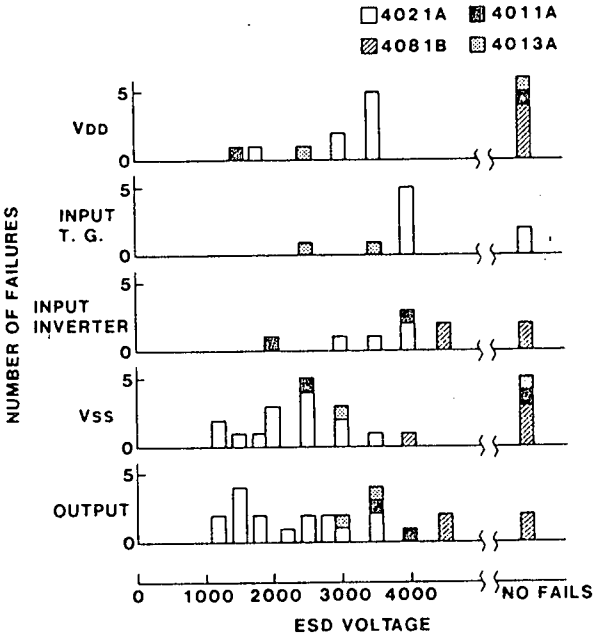


Figure 11. Comparison of 4000A and 4000B Device Types.

Fourteen gate oxide ruptures were found in the 18 detailed failure analyses completed on 4021A units. Eleven of these ruptures occurred on n-channel transistors and three on p-channel transistors. Eight occurred at transmission gate inputs, five at other inputs, and one at an output. Stress at supply and output terminals caused most of these input gate oxide failures. ESD stress on the Q_8 output resulted in ruptured gate oxide at three transmission gate inputs. ESD stress on the V_{SS} terminal resulted in ruptured gate oxide on three transmission gate inputs and three PSC inverter inputs.

Summary and Conclusions

This paper reports work done to determine the cause of apparent ESD failures on a weapon fireset production line and to determine if this cause represents a significant reduction in the long-term reliability of fireset units from this production line.

In the experimental procedure, 136 each 4000 series CMOS integrated circuits were subjected to ESD step stress tests. Sixty of these units showing a significant increase in input leakage or static I_{SS} current but still fully functional were put on an accelerated operating life test at 150°C.

The cause of the production line fireset failures was found to be a surprising susceptibility of the 4021 supply and output terminals to ESD. The fireset design and production provided protection for the input terminals but not the output or supply terminals.

One unit, a 4021A whose static I_{SS} current had increased from less than 50 nA to greater than 16 μA as a result of ESD step stress tests, survived 308 hours of operating life at 150°C and was still functional in spite of a gate oxide rupture. Another unit, a 4021A whose static I_{SS} current had increased from less than 50 nA to 100 μA as a result of ESD step stress tests, failed the operating life test after only one hour. This unit also had a gate oxide rupture. This unit was the only failure in the 60 units on life test. There is a small risk of long-term failure of ICs which have been subjected to ESD and have suffered degradation but not to failure.

A ruptured gate oxide on an input terminal does not necessarily mean an ESD stress was applied to that input terminal. In the case of the 4021A, input transistor gate oxides were ruptured as result of ESD on output and supply terminals.

Data from the operating life test showed that rapid improvement in static I_{SS} current occurs with time and temperature. Thus a unit degraded by ESD in supplier or incoming handling or test may be hidden because of the I_{SS} improvement during Hi Rel burn-in or bake. However, the data shows that screening at low values of I_{SS} and input leakages will be successful in screening out units degraded by ESD and thus will improve long-term reliability.

Although other 4000 series types tested did not show the high susceptibility to ESD on the supply and output terminals as did the 4021A, they show supply and output terminal susceptibility about equal to input terminal susceptibility. The supply and output terminals of completed assemblies must be protected from ESD.

Silicon gate 4021B units are less susceptible to ESD than 4021A metal gate units, and as expected, 4000B series units are less susceptible than 4000A series units.

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