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A SERIAL NONVOLATILE 1024 BIT MNOS MEMORY

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Introduction

This paper describes the characteristics and operation of a nonvolatile MNOS sequential memory designed and built by Sandia National Laboratories for DOD. First, a general description and block diagram are presented, followed by the power, voltage, clock and address requirements, and then operating descriptions for the control and data signals.

General Description

This chip was fabricated on <111> n epi-silicon. P diffusions give the needed isolation between memory substrate and control transistors. APCVD nitride 500 Å thick and tunneling native oxide were used for the memory transistors.

The 1024-bit nonvolatile MNOS memory is organized into eight words of 128 bits each. Fig. 1 is a block diagram of the memory. On-chip peripheral circuitry is metal gate PMOS and uses both enhancement and depletion mode transistors. All address, control, clock, and data pads are CMOS compatible and also TTL compatible if resistor pull-ups are used on the input pads. The chip will operate over the temperature range of -55°C to 125°C and dissipates approximately 140 milliwatts at room temperature. The chip measures 188 x 217 mils and has 16 pads.

Each of the eight words may be individually erased and written or the entire memory may be block erased in one operation and then each word written subsequently. Data are entered and read from the memory serially and can be retained for at least one year with no power applied. Data may be written at a rate of up to 125 kilobits/second and read back at a rate up to 500 kilobits/second.

Power and Voltage Requirements

Power is supplied to the chip mainly through three pads--Vss, Vdd, and Vw. Vss is the reference potential for all other voltages and is the potential of the n-type epitaxial substrate layer for the PMOS peripheral transistors. The drain voltage for most of the logic circuits require a higher voltage for erasing and writing the memory which is supplied by Vw=Vss-25 volts. At room temperature the Vdd pad draws about 3.0 mA and the Vw pad draws about 2.5 mA. To preserve the memory contents, power is first applied to Vdd and then to Vw during turn-on and vice versa during turn-off.

Voltages must also be applied to two additional pads--Vr and Vout. Vr is the read voltage applied to the gates of the memory transistors and is normally the same as Vdd. Vr was brought out separately to facilitate testing. The voltage applied to Vout determines the more negative potential of the DATA pad during readout. The DATA pad swings between Vss and Vout when reading.

Table I illustrates two examples of voltages to be applied for interfacing with 10-volt CMOS and with standard TTL circuitry.

Table I. Two examples of chip voltage requirements.

	10V. CMOS	TTL
Vss	+10.0	+ 5.0
Vdd=Vss-12.5	- 2.5	- 7.5
Vw=Vss-25.0	-15.0	-20.0
Vr=Vdd	0	- 7.5
Vout	0	0

When 10-volt CMOS is chosen, all input signals and the output will swing between 0 and +10 volts (Vss and Vdd). When 5-volt TTL is chosen, all input signals and the output will swing between 0 and +5 volts (not Vss and Vdd).

Clock Requirements

Two clock pads are provided for operating the memory--a read clock CKR and a write clock CKW. Normally, both clocks are supplied continuously to the chip. The write clock frequency is the

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rate of data entry into the memory and determines the write time of the memory transistors. A row of the MNOS memory is written for 32 CKW periods. Normally, 250 microseconds writing time per row is required so the maximum CKW frequency is 125 kHz. Some memories have been successfully written at higher frequencies (300 kHz), but there may be a reduction in retention time at frequencies above 125 kHz.

The read clock CKR frequency is the rate of data exit from the memory. Some memories have been successfully read at frequencies up to 500 kHz. Much lower frequencies may be used for reading, but exceptionally low frequencies may result in read disturb problems in the memory. If the read and write frequencies are the same, the CKR and CKW pads may be tied together and only one clock supplied.

Address Requirements

The three binary address inputs select one of eight 128-bit words for erasing, writing, or reading. For layout reasons each 128-bit word is partitioned into four rows of 32 bits each. These rows are addressed sequentially by the on-chip counter and cannot be selected by the user. The counter continuously cycles through four rows and is reset at the beginning of a READ or WRITE signal. Address inputs must be stable during WORD ERASE, WRITE and READ operations.

Control and Data Signals

Chip Select

The CHIP SELECT enables the ERASE, WRITE, and READ pads and permits selection of one or more chips from a bank of several chips wired in common.

Erase and Mode

The ERASE pad when high will erase either the entire memory or just one word depending upon the state of the MODE pad. Word erase occurs when the MODE pad is high and block erase occurs when the MODE pad is low. Erasing the memory is a necessary precondition to writing the memory. Erasing does not set the memory to all 0's or all 1's. Reading the memory after erasing but before writing generally results in random data. Similarly, writing data into a word that has not been erased will also result in random data.

Write

When the WRITE pad is high, data first enters serially into a 32-bit shift register. These 32 bits are then transferred in parallel to a memory row and written into the MNOS transistors while the next 32 bits are entering the shift register. This process continues as long as the WRITE pad is high. Since 32 CKW periods are required to fill the shift register and another 32 CKW periods are required to write one row, there is always a delay of between 32 and 64 CKW periods from when a bit first enters the chip to the completion of the bit's nonvolatile writing. Consequently, filling one word completely will require 128 + 32 CKW per periods. In this case, data entering the shift register during the last 32 CKW periods can be either dummy data or data for the next word. If the next word is to be written then the address must be changed at the end of the 160-CKW period. Any number of bits up to 128 may be stored in a word.

Read

Raising the READ pad high initiates the read process. During the first eight CKR periods the data in one row of the memory transistors is sensed in the sense amplifiers. During the next eight CKR periods, the data are amplified and then transferred in parallel to the shift registers. Consequently, there is always an initial delay of these several clocks at the beginning of any read operation before valid data appear. The first valid data bit occurs during the 17th CKR period. After the beginning of the read operation, serial data will continue uninterrupted from the memory as long as the READ pad is high. The address must be changed to cycle through the words. Failure to change the address will result in the data from the addressed word being continuously repeated.

Radiation Tests

The fabrication process for this chip was not radiation hardened. Nevertheless, radiation tests have shown that the memory will operate after 5×10^4 rads exposure at about half the normal speed and fails after 10^5 rads.

Conclusion

Several hundred chips have been successfully processed, packaged, and tested, demonstrating the viability of MNOS technology for nonvolatile serial memories.

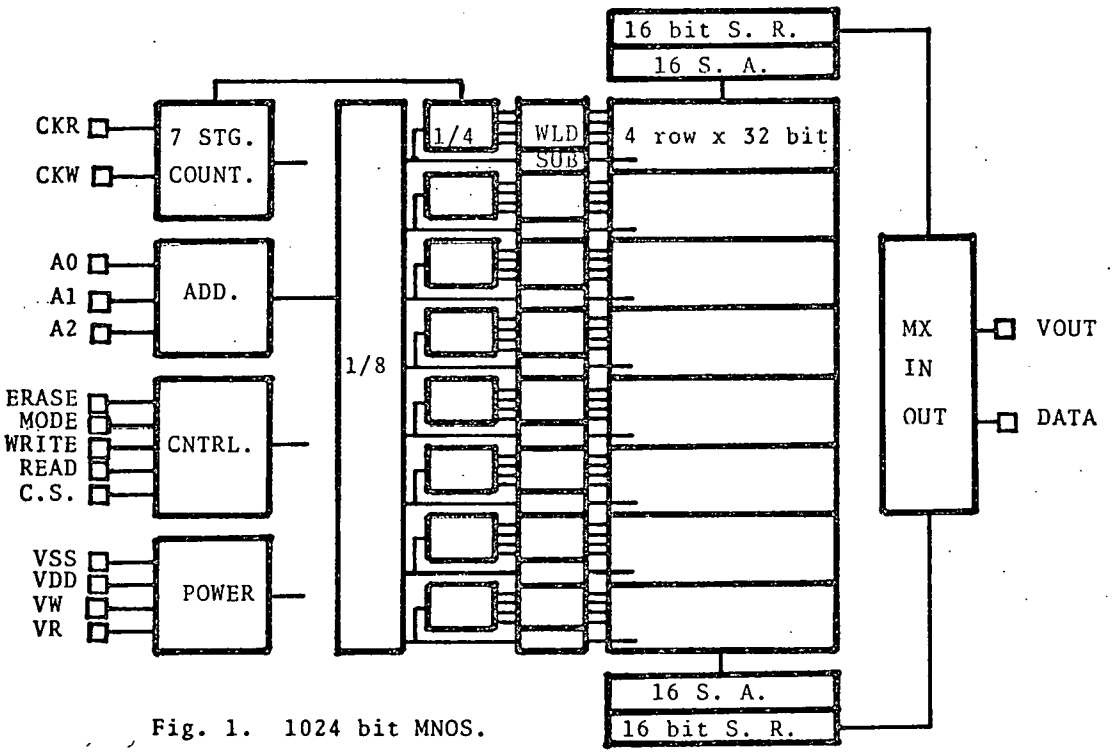

Fig. 1. 1024 bit MNOS.

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