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Soft-Error Susceptibility of a CMOS RAM: Dependence Upon Power-Supply Voltage

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Abstract

Two types of delidded CMOS 1024 x 1 RAM (Harris HM 6508-RH and Sandia TA597) have been tested for susceptibility to soft bit errors caused by 150-MeV krypton ions. Bit-error susceptibility was measured as a function of bias voltage and exposure angle with respect to the chip normal. Comparison of measured bit-error rates and thresholds with those computed by use of a simple device model and manufacturer-supplied data shows good agreement in some respects while raising questions in others. In the case of the HM6508-RH RAMs, measured values of critical charge of 1 pC and 2 pC at 5V and 7V, respectively, indicate that the devices can be expected to show bit-error rates in space of approximately 1 x 10^{-4} per chip per day at 5V bias and 1 x 10^{-5} per chip per day at 7V bias.

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Soft Error Susceptibility of a CMOS RAM: Dependence Upon Power Supply Voltage

Introduction

Soft errors induced by charged-particle radiation in integrated-circuit memories have become a topic of considerable interest in the past several years (see References 1-3 and literature quoted therein). Problems associated with these "single event upset phenomena" are of particular concern to designers of space-borne systems which encounter radiation environments much more severe than those found near the ground, where the primary source of soft errors are alpha particles from naturally occurring radioactive substances. (Secondary cosmic rays, consisting for the most part of relativistic muons and electrons do not affect systems currently in general use.) In space, on the other hand, primary cosmic-ray particles range in mass from that of protons to those of nuclei in the iron group and higher. Since the ionization charge produced by one of these particles when passing through a RAM is proportional to the square of the particle atomic number, we can expect bit errors to appear in devices which show none on the ground. Furthermore, energetic protons of galactic and solar flare origin as well as those encountered in the Van Allen belts can produce bit errors via nuclear reactions within the RAM.[1] Thus, development of techniques for reducing or circumventing device susceptibility to upsets, as well as those for modeling and predicting specific device performance in the space environment are important to future progress in the development of space instrumentation.

Whenever the maximum ionization generated in the sensitive volume of a RAM by a given radiation environment is above but close to the threshold amount needed to produce bit errors, an increase in bias voltage should reduce or even eliminate the occurrence of such errors. Since tests carried out previously have shown certain devices to possess bit-error thresholds corresponding to a critical charge not far below the maximum charge expected from galactic cosmic rays, the present work was undertaken to verify the hypothesis that operation at increased bias can make a drastic difference in device bit-error susceptibility in space.

Experimental Technique

The rad-hard, epitaxial substrate version of the Harris Semiconductor Company HM6508-RH CMOS (1024 x 1) RAM was one of the two device types selected for these tests. This particular type of device had been tested on several previous occasions by bombardment with krypton ions from the Lawrence Berkeley Laboratory (LBL) 88-in. cyclotron and found to be immune to latchup, with a $V_{DD} = 5V$ bit-error threshold appropriate for this study. In addition to the above, several neutron-irradiated Sandia National Laboratories TA597 CMOS (1024 x 1) RAMs were tested alongside the HM6508 devices in the present work. All of the work was performed with a beam of 150 MeV krypton ions from the LBL 88-in. cyclotron.

A detailed description of the test method has been published elsewhere[2] and hence only a brief outline relevant to the present work will be presented. The experimental hardware is depicted schematically in Figures 1 and 2, reproduced from Reference 2 for the convenience of the reader. Figure 1 shows in schematic form the test chamber with the hardware used for monitoring the incident particle flux for uniformity, intensity and energy.

Figure 2 is a schematic representation of the hardware used in operating the devices under test. As the bias on the devices was changed, corresponding changes in signal levels were accomplished by means of the circuit labeled "Level Translator." The loading and interrogating of the memories was accomplished by means of a micro-computer depicted by the block labeled "μC." Connections to only one of several samples are shown in Figure 2.

Individual chips were irradiated with a known total fluence of particles at several angles between the beam and the direction perpendicular to the chip surface. Prior to each irradiation, the bias (V_{DD}) was adjusted to a predetermined value ranging between 3.5V and 9V and a checkerboard bit pattern was loaded into the RAM. Following irradiation with a known particle fluence, the chip was interrogated for errors and the procedure repeated at other angles and/

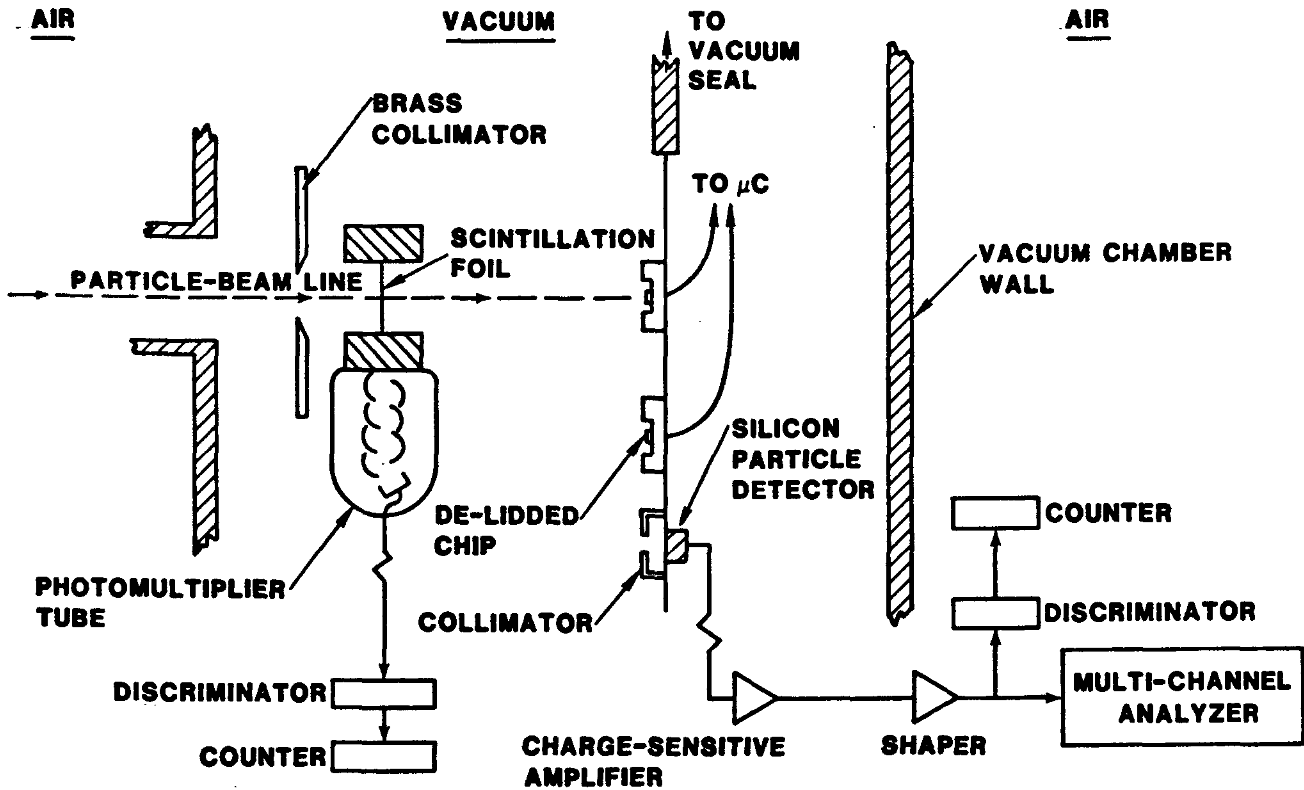

Figure 1. Schematic Representation of Test-sample Hardware and Beam Monitoring System

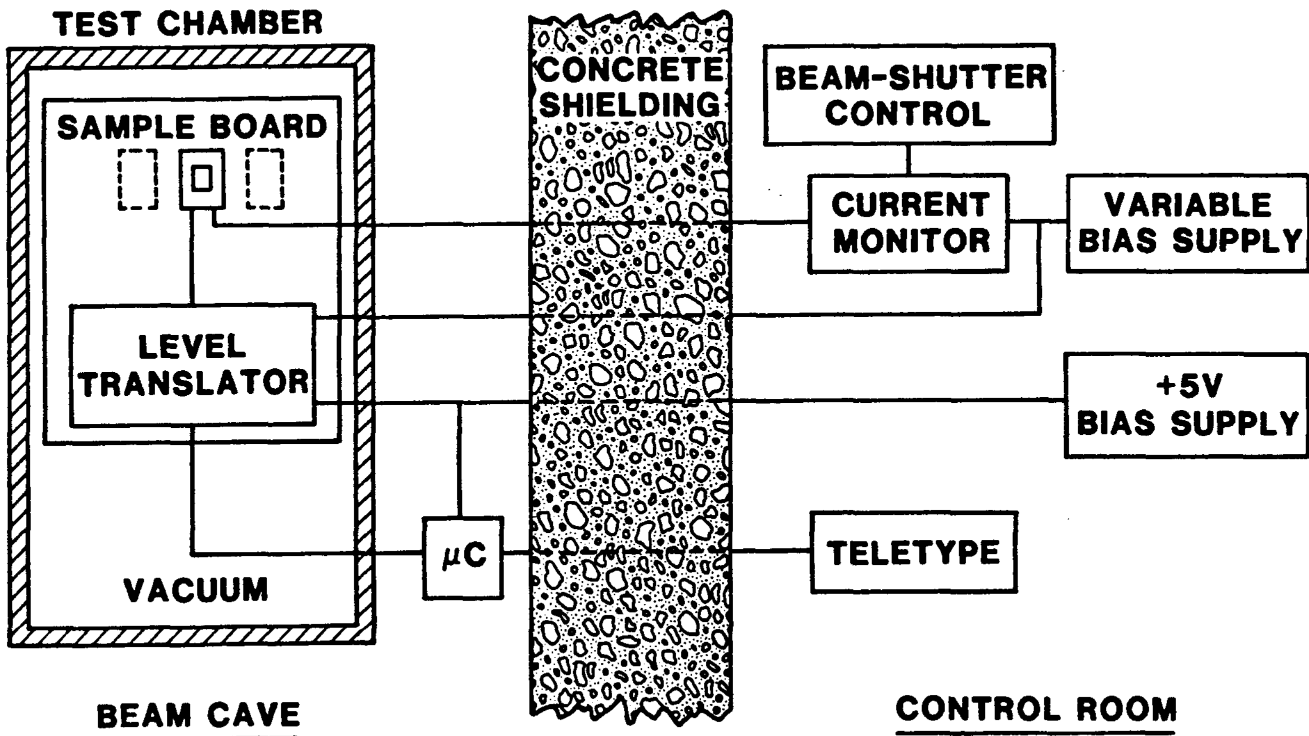

Figure 2. Simplified Block Diagram of Circuits Used to Operate Test Memory Chips

or bias values. In each case the bit error probability expressed as a cross-section (σ) for bit error was calculated using the expression

$$\sigma = (N/F) \sec \phi \qquad (1)$$

where N and F are the number of bit errors and beam fluence respectively, observed during the particular exposure, while ϕ is the incidence angle of the beam measured with respect to the chip-surface normal.

Results and Discussion

Figures 3 and 4 are summaries of the experimental data obtained in this work for the HM6508 and TA597 RAMs, respectively. The soft error cross-section (σ), defined by Eq. (1), has been plotted as a function of $\sec \phi$ for several values of the bias voltage (V_{DD}). As a first approximation, the abscissa can be viewed as the relative amount of charge produced in the depletion region of a node struck by a charged particle; hence the choice of $\sec \phi$ as the dependent variable for displaying the trends in the data.

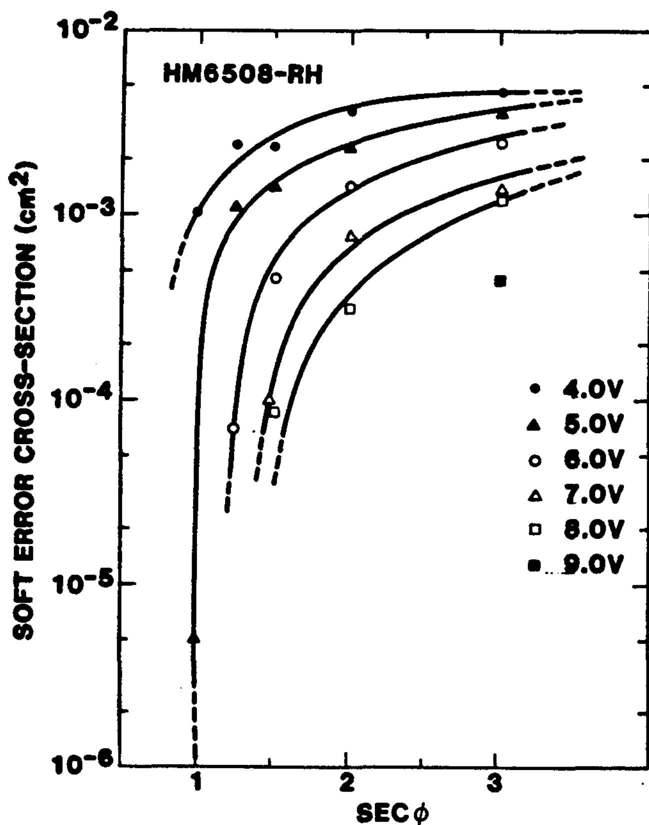

Figure 3. Plot of HM6508-RH Bit-error Cross-section as a Function of the Secant of Chip Orientation Angle (ϕ) Relative to the Incident Beam, for Various Values of the Device Bias (VDD)

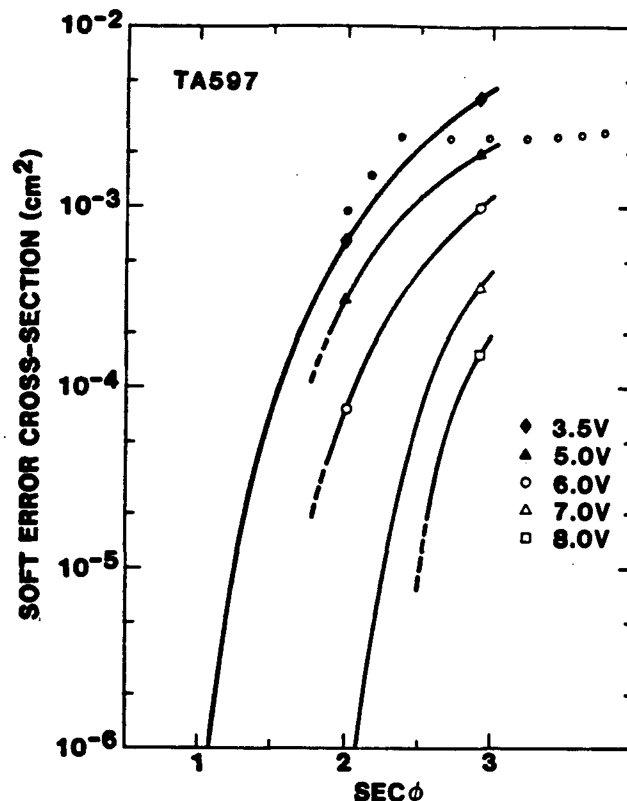

Figure 4. TA597 Data Displayed in the Same Form as Those of Figure 3

Some more or less definite trends in the data of Figure 3 are apparent. First of all, as expected, the bit-error cross-section decreases with increasing V_{DD} at all values of $\sec \phi$. Second, at low values of V_{DD} there is an abrupt change in the slope of the cross-section curve when $\sec \phi \approx 1$ and $\sigma \approx 1 \times 10^{-3}$ cm^2. At larger values of $\sec \phi$ the cross-section increases slowly to an asymptotic value of approximately 5×10^{-3} cm^2. The observed transition in slope appears to become less and less pronounced as V_{DD} increases above 5V. At these higher values of V_{DD}, the cross-section increases more slowly with increasing $\sec \phi$. While there is insufficient data to draw definite conclusions, there appears an indication that the high V_{DD} curves may approach a lower value of the cross-section than is the case for curves with V_{DD} below 6V.

The data displayed in Figure 4 for the TA597 RAM indicate that the device susceptibility to bit errors becomes significant for $\sec \phi \approx 2$. Despite the small number of data points, the cross-section curves of Figure 4 show a less pronounced flattening at high values of $\sec \phi$ than shown by the curves of Figure 3. While it is impossible to deduce an asymptotic value of the cross-section from the existing data, that value clearly must be above 5×10^{-3} cm^2.

Before discussing the results in terms of a device model, it will be useful to review briefly the single memory-cell circuit as shown in Figure 5. This circuit applies to both device types under discussion. Whenever a particle hits the drain of an inverter transistor in the *off* state and produces sufficient charge in the depletion region, a bit error will occur. A hit on the drain of one of the access n-channel transistors NA and NB can in principle also produce a bit error. However, in the devices under consideration, the access transistor drains are physically identical with the corresponding inverter n-channel drains and are not to be considered separately in the analysis.

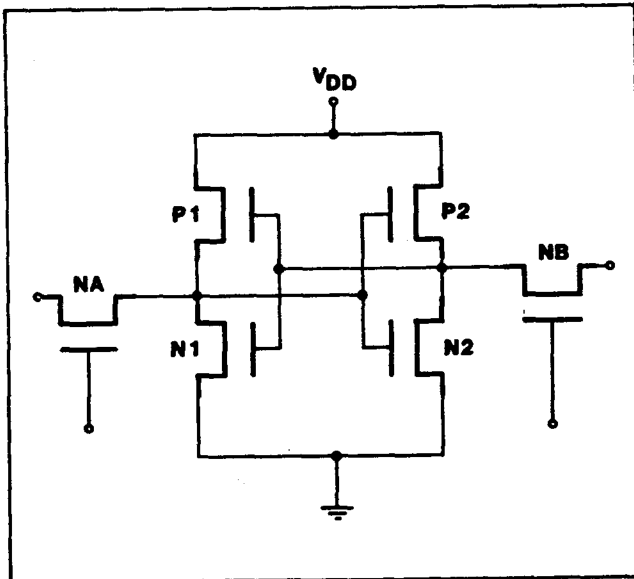

Figure 5. Simplified Schematic of RAM Cell, Applicable to HM6508 and TA597 RAMs

Interpretation of trends in the experimental data is complicated by the fact that there are considerable differences between the p- and n-channel drain characteristics. As a result, significantly different device response may be expected, depending on whether a p-channel or n-channel drain is struck by a charged particle. In particular, differences in impurity level concentrations and drain areas lead to large differences in sensitive volumes, which in turn affect the charge produced by a hit and the resulting instantaneous change in the node potential. Furthermore, the circuit response to this change will depend on a large number of device characteristics whose elucidation and incorporation into an accurate device model is beyond the scope of this work. For reference, Tables 1 and 2 contain some relevant device parameters derived from information supplied by the device manufacturers.

Within the limitations mentioned above, some semi-quantitative insight into the device performance can be obtained by examining the experimental results in the light of a simple model. Figure 3 shows that for $V_{DD} = 5V$, the bit-error threshold occurs near $\sec \phi = 1$. On the basis of Table 2, this translates to 0.9 pC and 0.06 C critical charge in the case of hits on the p- and n-channel drains, respectively. The resulting threshold change in potential (ΔV) at the node in each case can be estimated by adding the appropriate drain capacitance to the total gate capacitance and dividing the result into the critical charge. From Table 1, the total capacitances in the case of hits on the p- and n-channel drains, respectively, are 0.1 and 0.3 pF when $V_{DD} = 5V$. These values translate into $\Delta V = 9V$ and $\Delta V = 0.2V$ for hits on the p- and n-channel drains, respectively. The above numbers result from

Table 1. Relevant Device Characteristics at 5V

	HM6508-RH		TA597	
	n-channel	p-channel	n-channel	p-channel
Total Drain Area Depletion-Region Capacitance Per Memory Cell	3×10^{-3} cm^2 .2 pF	2×10^{-3} cm^2 .01 pF	5×10^{-3} cm^2 .1 pF	2×10^{-3} cm^2 .01 pF
Total Gate Capacitance Per Memory Cell	.1 pF		.2 pF	

Table 2. Charge Deposit (pico-Coulomb) in the Off-Drain Depletion Region as Function of Bias and Angle

	HM6508-RH								TA597							
	n-channel				p-channel				n-channel				p-channel			
bias	Incident Angle				Incident Angle				Incident Angle				Incident Angle			
(volt)	0°	48°	60°	70°	0°	48°	60°	70°	0°	45°	60°	70°	0°	45°	60°	70°
3.5	.05	.08	.10	.14	.7	1.1	1.4	1.9	.2	.3	.4	.5	.9	1.2	1.6	2.2
4.0	.06	.09	.11	.15	.8	1.1	1.5	2.0	.2	.3	.4	.6	.9	1.3	1.7	2.3
5.0	.06	.09	.12	.17	.9	1.3	1.7	2.3	.2	.3	.5	.6	1.0	1.4	1.9	2.6
6.0	.07	.10	.13	.19	1.0	1.4	1.8	2.5	.3	.3	.5	.7	1.1	1.5	2.1	2.8
7.0	.08	.11	.14	.20	1.0	1.5	1.9	2.6	.3	.3	.5	.8	1.2	1.6	2.2	3.0
8.0	.08	.12	.15	.22	1.1	1.6	2.1	2.8	.3	.4	.6	.8	1.3	1.8	2.4	3.2
9.0	.09	.12	.16	.23	1.2	1.7	2.2	3.0	.3	.4	.6	.9	1.3	1.9	2.5	3.4

calculations which neglect factors like stray capacitance, Miller effect, charge recombination, etc., which would lend to lower the estimated values of ΔV. The disparity in the values of ΔV caused by p- and n-channel hits indicate that near the observed bit-error threshold, only p-channel hits produce bit-errors. Since the total p-channel drain area is 2×10^{-3} cm^2 (see Table 2), this conclusion is consistent with the data of Figure 3, where for $V_{DD} \leq 5V$, $\sigma \leq 2 \times 10^{-3}$ cm^2 whenever $\sec\phi < 1.5$.

For higher values of $\sec\phi$, the cross-section increases beyond 2×10^{-3} cm^2 and eventually reaches a value equal to the sum of the total p- and n-channel drain areas (5×10^{-3} cm^2), implying that hits on the n-channel drains may produce errors at large angles. Unfortunately, an estimate of ΔV produced by an n-channel drain hit at $\sec\phi = 3$ and $V_{DD} = 5V$ yields a value of 0.7V. It is hard to see how such a low value of ΔV could cause a flip, even with the neglect of charge decay via the conducting p-channel. A possible way out of this difficulty might be to invoke a large contribution to ΔV from charge diffusion or from a mechanism like the funneling effect, recently discussed in the literature[4]. However, if such mechanisms indeed do play a role, it is not clear why their effect should only appear at large angles and primarily in cases of hits on n-channel drains, as the data of Figure 3 for $V_{DD} > 5V$ appear to imply. Here, the decrease in flattening of the cross-section curves and overall decrease in the cross-section magnitude at $V_{DD} > 5V$ indicate that the critical charge needed to produce bit-errors is barely exceeded in the case of hits on the p-channel drains, while no errors are observed due to hits on the n-channel drains.

Tables 1 and 2 show that differences between the characteristics of the p- and n-channel drains are not nearly as large for the TA597 RAM as they are for HM6508. Figure 4 shows that for $V_{DD} = 5V$, it is not unreasonable to assume that bit-error threshold occurs at $\sec\phi = 2$. In that case, Table 2 shows that values of critical charge are 1.9 and 0.5 pC, for hits on the p- and n-channel drains, respectively. Dividing by total node capacitances (drain plus gate) from Table 1, one obtains corresponding ΔV values of 9.5V and 1.7V. Again, while in the right ballpark, the numbers show the need to refine the device model, particularly where n-channel hits are concerned.

An approximate empirical relationship between the critical charge (Q_c) in pico-Coulombs and the device bias (V_{DD}) in volts, given by the expression

$$Q_c = 0.04\, V_{DD}^2, \qquad (2)$$

has been derived for the HM6508 RAM from data in Figure 3. The derivation arbitrarily assumes that threshold occurs at the value of $\sec\phi$ where the cross-section for a given V_{DD} reaches one tenth of the asymptotic value of 5×10^{-3} cm^2. According to Eq. (2), $Q_c = 1$ pC for $V_{DD} = 5V$ and $Q_c = 2$ pC for $V_{DD} = 7V$. Calculations previously described[3] were provided by

J. C. Pickel for a device with drain sizes comparable to those of HM6508. Using these calculations, bit-error rates for a single chip in a galactic cosmic-ray environment were estimated to be $\approx 1 \times 10^{-4}$ bit errors per day at $V_{DD} = 5V$ and $\approx 1 \times 10^{-5}$ bit errors per day at $V_{DD} = 7V$. Thus, a relatively modest increase in bias can produce an order of magnitude change in observed bit error rate. Both devices can be expected to be completely immune to upsets due to proton- and neutron-induced nuclear reactions, in view of their high threshold measured with krypton.

Summary and Conclusions

Two types of delidded bulk CMOS 1024 x 1 RAMs were tested in a beam of 150 MeV krypton ions. The probability of single-event upsets was measured as a function of the chip orientation in the beam as well as the bias voltage (V_{DD}). The measurements have made it possible to make an assessment of the device performance in a space cosmic ray environment and have provided insight into some aspects of the bit error mechanism while raising questions about others. The current interpretation of the results leads to the following conclusions:

1. Bit errors are caused by charged particles striking the drain regions of the p-channel inactive transistors in the inverter pair of the memory cell.
2. Much less charge is always produced in the depletion layer of the n-channel drain than the minimum amount required for production of bit errors due to hits on the p-channel depletion layer. Despite this fact, n-channel hits appear to cause bit errors.
3. In space, increasing the bias on a device by 50% can decrease device susceptibility to bit error by an order of magnitude.
4. More accurate device models, particularly in terms of circuit response to fast transients, are needed to predict soft error rates. Development of such models will in large measure eliminate the need for particle beam tests which are expensive and extremely time consuming.

References

[1]C. S. Guenzer, R. G. Allas, A. B. Campbell, J. M. Kidd, E. L. Petersen, N. Seeman and E. A. Wolicki, *IEEE Trans. Nucl. Sci.*, NS-27, 1485 (1980).

[2]W. A. Kolasinski, J. B. Blake, J. K. Anthony, W. E. Price and E. C. Smith, *IEEE Trans. Nucl. Sci.*, NS-26, 5087, (1979).

[3]J. C. Pickel and J. T. Blandford, *IEEE Trans. Nucl. Sci.*, NS-27, 1006 (1980).

[4]C. M. Shieh, P. C. Murley and R. R. O'Brien, *IEEE Electron Devices Ltrs.*,Vol II, 103 (1981).