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AN AlGaAs-GaAs PATTERNED Ge TUNNEL JUNCTION CASCADE CONCENTRATOR SOLAR CELL

Annual Technical Progress Report for the Period October 15, 1983—December 14, 1984

August 1985

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Solar Energy Research Institute
Golden, Colorado

and

Research Triangle Institute
Research Triangle Park, North Carolina

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A Subcontract Report

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Research Triangle Park, North Carolina

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ABSTRACT The goal of this research is to demonstrate a two-junction cascade solar cell, 0.5 cm^2 in area, in the AlGaAs-GaAs material system that has a power conversion efficiency of more than 30 percent at a cell temperature of 50°C. Objectives for the first year of the program included growth of $Al_xGa_{1-x}As$ on $Al_yGa_{1-y}As$ exposed to air for at least one hour; growth of Ge by vapor phase epitaxy on a GaAs substrate; fabrication of a p/n patterned Ge tunnel junction grown on n-GaAs and demonstration of a current density larger than 80 A/cm^2; growth and characterization of a top cell on a patterned Ge tunnel junction; and fabrication and demonstration of an AlGaAs-GaAs cascade solar cell using the patterned Ge tunnel junction. A patterned Ge-tunnel junction connecting the n-type base region of a GaAs cell to a p^+-GaAs substrate was demonstrated for the first time.

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1.0 INTRODUCTION

1.1 Background

A major goal of the National Photovoltaics Program is to demonstrate a power conversion efficiency of 30 percent for a small-area, multi-junction solar cell. A variety of semiconductor materials and approaches have been proposed and partially developed to achieve this goal. The materials include the group IV and several group III-V compound semiconductors. The approaches range from a 4-terminal, mechanically-stacked configuration containing two separately optimized individual cells to a 2-terminal, fully-monolithic integration of two photovoltaic p-n junctions.

Monolithic growth of two photovoltaic junctions of different energy bandgaps and possessing the same polarity creates a third intermediate junction of opposite polarity. This third junction must be fabricated such that it does not generate a photovoltage, and it does not present a high-value resistance in electrical series with the 2 photovoltaic junctions. In addition, this third junction needs to be transparent to the light transmitted through the wide bandgap top cell to the narrower bandgap bottom cell to minimize optical losses.

One attractive approach to the monolithic cascade cell is the AlGaAs/GaAs system, in which the top cell is $Al_{.38}Ga_{.62}As$ (Eg = 1.89 eV) and the bottom cell is GaAs (Eg = 1.43 eV). While this approach does not offer the absolute maximum theoretical efficiency, it does offer several attractive features. The structure is nearly perfectly matched in lattice constant and thermal expansion

coefficient to the GaAs substrate. A substantial technology base exists for these compound semiconductors, and the potential efficiency for a concentrator cascade cell may exceed 30 percent.

Initial attempts at RTI and at other laboratories to develop the AlGaAs/GaAs monolithic cascade multijunction cell centered upon use of an n^{+}/p^{+} $Al_{.35}Ga_{.65}As$ tunnel junction as the intermediate third junction, or the intercell ohmic connection (IOC). This approach is handicapped by several fundamental and technological problems.

Because of the large bandgap of this tunnel junction (Eg = 1.86 eV) and its relatively low maximum attainable n- and p-type doping concentrations, tunnel junctions exhibiting high peak current densities, J_p, have never been demonstrated. The maximum value of J_p obtained for $Al_{.14}Ga_{.86}As$ is 18 A/cm^2; as a reference, the maximum value of J_p reported for GaAs is 40 A/cm^2 [1]. The minimum current density an $Al_{.35}Ga_{.65}As$ planar tunnel junction must conduct, with only a small voltage drop for 400 suns concentration, is 4 A/cm^2. Typical $Al_{.35}Ga_{.65}As$ n^{+}/p^{+} tunnel junctions exhibit peak current densities much less than 1 A/cm^2.

Another problem is that heavily-doped $Al_xGa_{1-x}As$ alloy layers, particularly the n^{+} Te-doped layer, exhibit a fairly rough surface morphology, which tends to reduce the open circuit voltage of the wide bandgap top cell.

1.2 Central Theme

An attractive solution to these problems is to use a patterned tunnel junction that is grown in Ge. This connecting junction is photolithographically defined into the same pattern as the top contact grid and, when the two are properly aligned, will introduce little additional shadowing of the bottom cell. The reduction in the connecting tunnel-junction area should be compensated by the substantially improved conductivity of the heavily-doped Ge layers in comparison with the higher bandgap AlGaAs tunnel junction in conventional planar structures.

The patterned tunnel-junction structure offers several important advantages related to solving problems presently impeding development of current AlGaAs-GaAs cascade structures utilizing a planar tunnel junction. Because the patterned tunnel junction covers only a small fraction of the bottom-cell area (~ 5 percent), a substantial portion of the top cell will be grown directly on top of the bottom cell without the intermediate n^+ Te-doped AlGaAs tunnel junction layer possessing poor surface morphology. In addition, the patterned structure allows use of a Ge tunnel junction which no longer must be transparent to light incident on the bottom cell. The Ge tunnel junction is expected to yield a substantially reduced tunnel-junction resistance due to its bandgap being lower in energy than the AlGaAs tunnel junction and its larger possible doping concentration. Also, the mismatch of lattice constants and thermal expansion coefficients between Ge

and GaAs (0.8 and 1.7 percent, respectively) are less than those between AlAs and GaAs (0.13 and 10.9 percent, respectively).

For 400-1000 suns, AM1.5 insolation, and a 5 percent cell coverage, the tunnel junction must be capable of conducting current densities between 100 and 250 A/cm^2 with a voltage drop less than 50 mV. A Ge tunnel junction which conducts up to 16,000 A/cm^2 with a voltage drop of 125 mV has been demonstrated. Growth of Ge in the OM-VPE reactor will be accomplished by pyrolytic decomposition of GeH_4 in a manner identical to epitaxial growth of Si. In addition, both n-type dopants (As and Sb) and p-type dopants (Ga), which have been used successfully to fabricate high current density Ge tunnel diodes, are readily available in the OM-VPE reactor as hydrides (AsH_3) and as organometallic compounds [e.g., $(CH_3)_3Ga$ and $(CH_3)_3Sb$].

1.3 Key Technical Issues

The key technical issues in this approach center on growth and fabrication of a low-resistance Ge patterned tunnel junction (PTJ), and successful overgrowth of a high-efficiency $Al_{.38}Ga_{.62}As$ top cell. For a solar concentration of 1000 suns AM1.5 and a tunnel junction active area coverage of 5 percent, the maximum specific resistance of the complete PTJ interface must be less than $2 \times 10^{-4}\ \Omega-cm^2$ to provide a tunnel junction voltage drop less than 50 mV. In

addition, the OM-VPE growth technology must be capable of growing high-quality $Al_xGa_{1-x}As$ over $Al_yGa_{1-y}As$ previously exposed to wet-chemical processes and ambient air.

1.4 Program Goal and Objectives

The eventual goal of this program is to demonstrate a two-junction cascade solar cell (0.5 cm^2 in area) in the AlGaAs-GaAs material system that has an AM2, 400-1000 sun, power conversion efficiency in excess of 30 percent at a cell temperature of $50^\circ C$. This goal will be approached through the accomplishment of several objectives. The objectives for the first year include:

(1) Growth of $Al_xGa_{1-x}As$ on $Al_yGa_{1-y}As$ exposed to air for a minimum of one hour. The purpose of this objective was to demonstrate interrupted growth of $Al_xGa_{1-x}As$ involving substantial exposure of the first $Al_yGa_{1-y}As$ layer prior to reinitiation of growth. This task simulates growth of the top $Al_{.38}Ga_{.62}As$ cell on top of $Al_{.45}Ga_{.55}As-GaAs$ bottom cell following patterning of the Ge tunnel junction.

(2) Growth of Ge by vapor phase epitaxy on GaAs substrate.

(3) Fabrication of p/n patterned Ge tunnel junction grown on n-GaAs and demonstration of current density larger than 80 A/cm^2.

(4) Growth and characterization of top cell on a patterned Ge tunnel junction. This objective includes growth and characterization of

$Al_{.9}Ga_{.1}As-Al_{.38}Ga_{.62}As$ top cell and $Al_{.45}Ga_{.55}As-GaAs$ bottom cell individually on GaAs substrate.

(5) Fabrication and demonstration of an AlGaAs-GaAs cascade solar cell using the patterned Ge tunnel junction.

1.5 Accomplishments

The accomplishments obtained in the first year of this program are summarized in this section according to the objective or task listed above.

(1) <u>Growth of $Al_xGa_{1-x}As$ on $Al_yGa_{1-y}As$ Substrate Exposed to Air:</u>

In three separate experiments, $Al_xGa_{1-x}As$ was grown on $Al_yGa_{1-y}As$ previously exposed to air for a minimum of 1 hour for Al mole fractions of $x = 0.15$, 0.45, and 0.50. Comparison of reinitiated-growth $Al_xGa_{1-x}As$ layer with an $Al_xGa_{1-x}As$ control layer (grown simultaneously on a GaAs substrate), using photoluminescence, indicated equal quality of both layers independent of the substrate material.

(2) <u>Vapor Phase Epitaxial Growth of Ge:</u>

Vapor phase epitaxial deposition of both n^+ and p^+ Ge on GaAs substrates has been established for growth temperatures between 600° and 775^oC. Free carrier concentrations of $n^+ = 3 \times 10^{19}\ cm^{-3}$ and $p^+ = 7 \times 10^{19}\ cm^{-3}$, quite adequate to obtain tunnel junctions, have been obtained for As and Ga doping, respectively. A problem of Ga droplet formation on the wafer surface before or after growth of the Ge epitaxial

layer has been solved by turning the TMGa flow on after the GeH_4 flow is started at growth initiation, and turning the GeH_4 flow off 2.5-3.0 minutes after the TMGa flow is terminated.

(3) Patterned Ge Tunnel Junction Fabrication:

The patterned Ge tunnel junction intercell ohmic contact (IOC) must exhibit a total specific resistance of $2-4 \times 10^{-4}\ \Omega-cm^2$ for an obscuration of 5-10 percent, respectively. The total Ge IOC consists of two Ge-GaAs (or AlGaAs) isotype heterojunctions and a Ge tunnel junction. Substantial effort during this first year was directed to reduction of the isotype Ge-GaAs heterojunction specific resistances. The lowest specific resistances for both p^+-Ge/p^+-GaAs and for n^+-Ge/n^+-GaAs heterojunctions were less than $5 \times 10^{-4}\ cm^2$. The lowest specific resistance obtained for an n^+/p^+ Ge tunnel junction was $2.8 \times 10^{-4}\ \Omega-cm^2$, for the growth temperature of 775°C. Higher values of the tunnel junction specific resistance are related to junction grading caused by Ga diffusion or by a sluggish system response time. These problems can be solved by lowering the growth temperature to 625°C and lengthening flush times. To summarize, these results for the component specific resistances will lead to a combined IOC specific resistance of $1 \times 10^{-3}\ \Omega-cm^2$ for growths performed at 625°C.

Also, selective Ge etching techniques have been obtained with $20H_2O_2:20H_2O:NH_4OH$ at room temperature.

(4) <u>Top Cell Overgrowth on a Patterned Ge Tunnel Junction:</u>

A problem with control of a Mg dopant in the OM-VPE growth of GaAs and AlGaAs limited the development of high-quality AlGaAs top cells during the latter part of this year. Two p-type dopant sources, bis(cyclopentadienyl)magnesium (CP_2Mg) and bis(methylcyclopentadienyl)magnesium (MCPMg), have been tried. The hole carrier concentration has been found to depend on the carrier gas flow rate through the bubbler: at low flow rates, the doping level is poorly controlled and appears significantly compensated, and at high carrier flow rates, the grown material is heavily doped ($p \sim 1-2 \times 10^{19}$ cm^{-3}) usually with a poor surface morphology. This type of behavior has been observed by other workers who attributed the difficulties to source impurities. The impurities are reported to be removed by purification using vacuum sublimation of the organometallic material. Purification capability is currently being developed.

However, successful use of a patterned Ge-tunnel junction to connect an n-type base region of a GaAs cell to a p^+-GaAs substrate has been demonstrated for the first time. Although the cell performance was limited (presumably by the poor surface morphology related to the p-dopant problem) these results are quite encouraging to the eventual use of a Ge PTJ as a cell interconnect technology.

(5) $Al_xGa_{1-x}As$/GaAs Patterned Tunnel Junction Cascade Cell Demonstration

A complete AlGaAs/GaAs cascade cell using a Ge patterned tunnel junction was fabricated and demonstrated, for the first time, voltage addition between the top and bottom cells. The total cell open-circuit voltage was low at 0.94 V, but substantially larger than either voltage for individual bottom or top cells grown simultaneously with the cascade structures.

2.0 DEVICE STRUCTURE

A schematic diagram of a cross section of the patterned tunnel junction cascade solar cell is shown in Figure 2-1. The cross section is taken through one set of aligned patterned-tunnel-junction and top-contact grid stripes. Approximate choices for the alloy composition, impurity concentration, and thickness of each of the layers are shown in Figure 2-2, and a schematic energy-band diagram for the structure is shown in Figure 2-3.

The 1.89 eV bandgap of the base n-type region of the top cell is chosen to provide a current match between the top and bottom cells for AM2 insolation.

The graded-bandgap p-type surface layers for both top and bottom cells serve four separate functions. Two of these functions are unique to graded-bandgap cells, and two are similar to heteroface cells with constant-bandgap surface layers. The two functions unique to GBG cells are to increase the photogenerated current collected from these regions and the photovoltage generated by each cell. Both of these effects result from the presence of a quasi-electric field acting upon the minority carriers. As discussed below, each of these contributions is modest, being 2.5-3 percent each for current and voltage. However, optimization of the device structure may increase the combined improvement of current and voltage up to ~ 7 percent. This is an appreciable gain in efficiency, considering that growth of the graded-bandgap regions is compatible with OM-VPE growth of the required layers and with the need for window layers for each of the cells. The other two functions required of the surface graded-bandgap layers are to provide

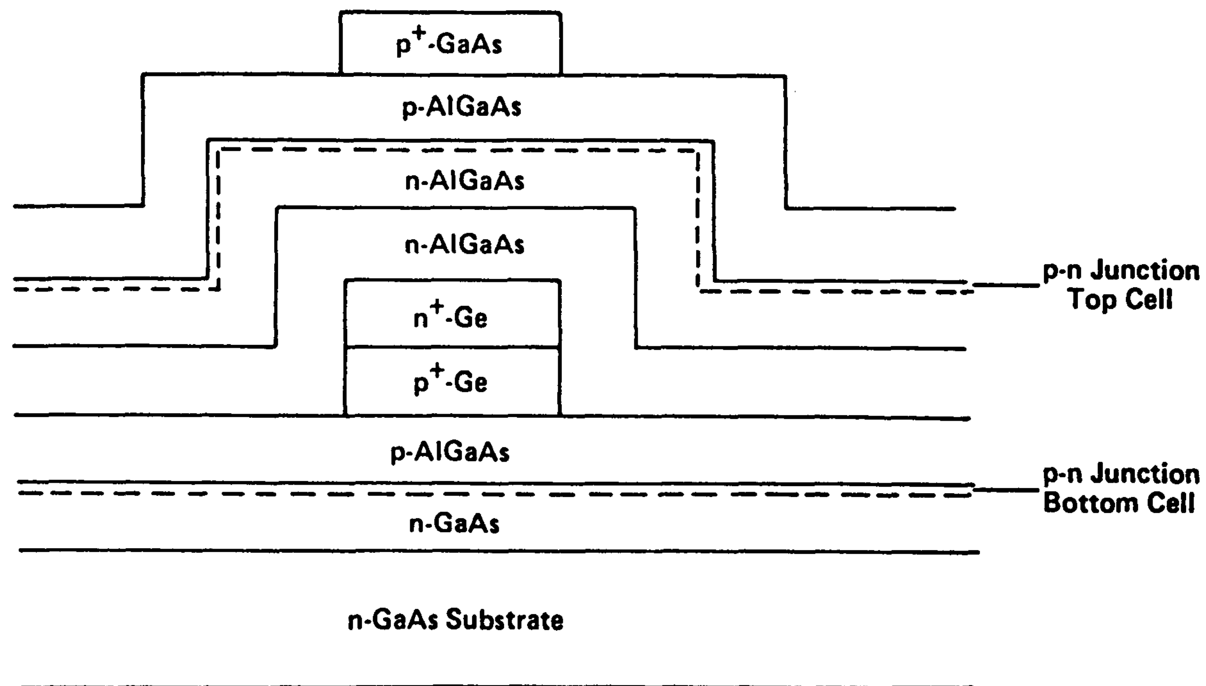


Figure 2-1. Structural diagram of the graded-bandgap AlGaAs-GaAs patterned-tunnel-junction cascade solar cell.

Layer	$n(cm^{-3})$	$p(cm^{-3})$	Thickness (μm)	AlAs (%)
p-GaAs		5×10^{18} (Mg)	1.7	0
p-$Al_xGa_{1-x}As$		1×10^{18} (Mg)	0.5-1	$0.38 < x < 0.45$
n-$Al_xGa_{1-x}As$	1×10^{18} (Si)		3	0.38
n-$Al_xGa_{1-x}As$	1×10^{18} (Si)		0.15	0.92
n^+-Ge	5×10^{19} (As or Sb)		0.15	0
p^+-Ge		5×10^{19} (Ga)	0.15	0
p-$Al_xGa_{1-x}As$		1×10^{18} (Mg)	0.5-1	$0 < x < 0.45$
n-GaAs	1×10^{18} (Si)		4	0
n-GaAs	2×10^{18} (Si)		Substrate	0

Figure 2-2. Detailed doping and thickness data for structure shown in Figure 2-1.

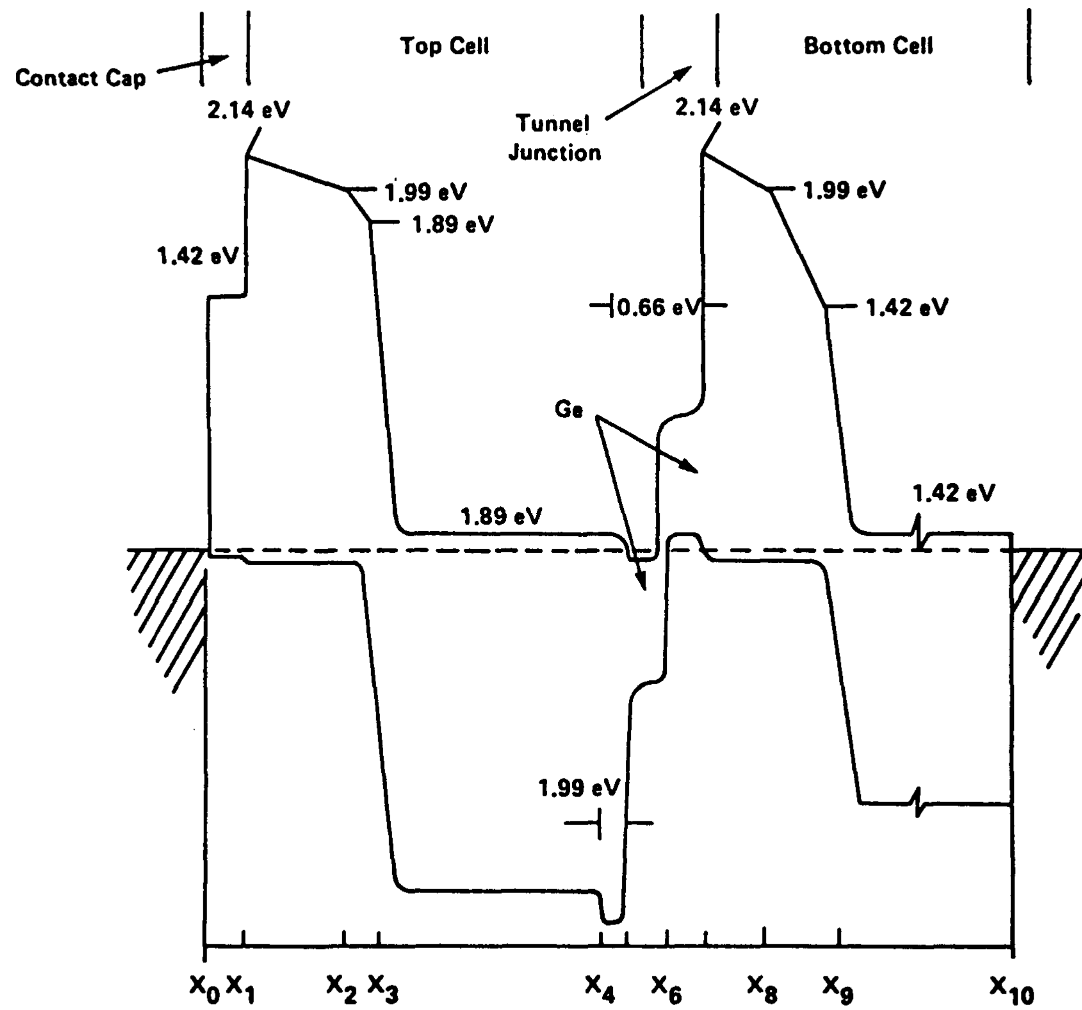


Figure 2-3. Energy band diagram of AlGaAs-GaAs graded bandgap Ge-patterned-tunnel-junction cascade solar cell.

a minority-carrier energy barrier, to prevent back-diffusion of photogenerated electrons, and to provide a low-resistance path for the lateral flow of current to a contact (top cell) or tunnel-junction (bottom cell) stripe. The first two functions require thin graded-surface layers to maximize the quasi-electric field, and relatively low acceptor concentrations $\sim 1-5 \times 10^{17}$ cm^{-3}. However, the last function requires just the opposite, or thick layers and high acceptor concentrations.

The $Al_{.45}Ga_{.55}As$ layer between X_4 and X_5 in Figure 2-3 is required to place an energy barrier for photogenerated holes between the n-type base region of the top cell and the tunnel junction, which will prevent undesirable diffusion of these holes into the p-type emitter layer of the bottom cell. This barrier could also be generated by grading the base region of the top cell between X_3 and X_4. While this would serve to further increase the open-circuit voltage of the top cell and the hole collection efficiency of the base region, it would also increase the optical transmission of the top cell. This increased transmission would then cause additional absorption and current generation in the bottom cell, and thereby destroy the current match between cells. Similar electron diffusion barriers are provided for the surface regions of each cell by the graded bandgap $Al_xGa_{1-x}As$.

A central feature of the structure is the patterned Ge tunnel junction (PTJ) which should provide a very low-resistance interconnect between the top and bottom cells. Also, because it is hidden under the top metalization, the Ge PTJ should offer very little obscuration to light transmitted by the top cell.

3.0 DEVELOPMENT OF Ge-RELATED TECHNOLOGIES

This section contains descriptions of the various technologies related to the growth of Ge and associated with patterned Ge tunnel junctions. These technologies are the following: (1) growth of heavily doped n- and p-type layers and fabrication of tunnel junctions, (2) development of suitable etching techniques to define the patterned structures, and (3) overgrowth of GaAs layers on patterned tunnel junctions.

3.1 Growth and Characterization of Ge Structures

3.1.1 Growth of Ge

The chemical vapor deposition (CVD) of Ge using GeH_4 as a gaseous source has been selected for Ge deposition [2]. Five percent GeH_4 in H_2 is the Ge source. A schematic of the growth system is shown in Figure 3-1. Ga and As were selected as the p- and n-type dopants, respectively, using trimethylgallium (TMGa) and arsine (AsH_3) as the dopant sources. Most growths have been performed at 750° to 775°C because surface morphologies grown in this range are quite good. Figure 3-2 shows a typical surface for an n^+-Ge layer using AsH_3 as the doping source.

Dopant selection is based primarily on the requirements of the tunnel junction: electron and hole carrier concentrations must exceed the density of states in the conduction and valence bands, respectively, and therefore must exceed 1×10^{19} and 6×10^{18} cm^{-3}, respectively. While a number of dopant materials

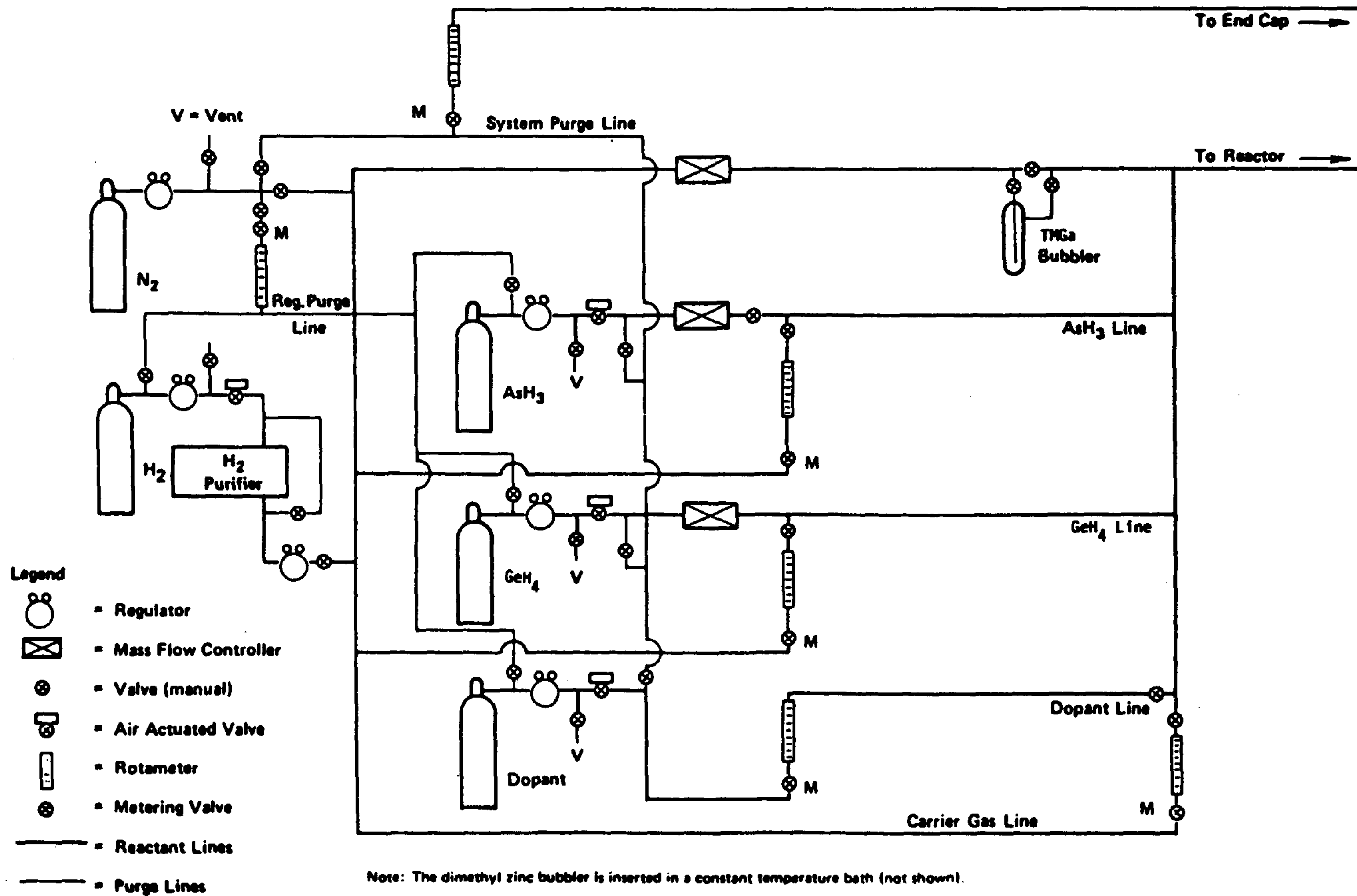


Figure 3-1. Flow schematic for CVD system used to develop Ge layers.

Figure 3-2. Photograph showing surface morphology of As-doped Ge layer. Defect structure used for focussing microscope; defect density very low.

satisfy these requirements, As and Ga are logical choices for the following reasons: (1) the solid solubilities of both elements in Ge are greater then 10^{20} cm^{-3} [2], (2) both have been used in the growth of heavily doped Ge epitaxial layers [2], and (3) both are available during the OM-VPE growth of the GaAs, low-bandgap junction. Using room temperature Hall effect analysis, electron carrier concentrations as large as 3×10^{19} cm^{-3} have been measured for As doping, and hole concentrations have reached 7×10^{19} cm^{-3} in Ga-doped layers. These values are more than adequate to produce degenerate n- and p-type material, respectively, satisfying that requirement of a tunnel junction.

The actual concentrations of the dopants in the layers may be somewhat larger since there tends to be a saturation effect as the solid solubility limit is approached. For the case of As in Ge, the electron density reaches 3×10^{19} cm^{-3} when the As density is approximately twice as large [3]. This type of result has been interpreted as an example of polytropy in heavily-doped semiconductors.

Significant negative features of this doping scheme (Ga and As) are twofold. The first of these involves the formation of Ga droplets on the substrate surface before or after growth of the Ge epilayer. During the initiation of growth, if the TMGa flow begins before the GeH_4 flow, Ga droplets can form on the substrate surface, preventing the uniform nucleation of Ge. When the substrates are subsequently cooled, the Ga-rich droplets expand and form pimple-like protrusions extending from the Ge surface. An example of these protrusions is shown in the

scanning electron micrograph of Figure 3-3. The Ga-rich regions etch more rapidly than the Ge. This allows the underlying GaAs (or AlGaAs) layer to be pitted when the tunnel junction is patterned. This pitting can be seen in Figure 3-4. Figure 3-4 also shows the alignment of rows of Ga-rich regions along approximately (110) directions as well as randomly distributed ones.

Similarly, when the GeH_4 flow is terminated after growth of the p^+ layer but before all the TMGa has flushed from the system, Ga droplets will form on the surface. An example of this effect is shown in Figure 3-5 for a structure grown with the following sequence: (1) growth of n^+-Ge layer (As doping), (2) growth of the p^+-Ge layer using TMGa and GeH_4, and (3) termination of TMGa flow while allowing the GeH_4 flow to continue for 1 minute. In spite of the extended GeH_4 flow, the Ga droplets formed. This indicates a nonoptimized design for the reactor being used for the Ge deposition and indicates the system "response time" exceeds the 1 minute value used for this experiment. In similar experiments we have determined that GeH_4 flows of 2.5 to 3.0 minutes are required to minimize the droplet formation. This problem, which lengthens the necessary growth time and affects valve sequencing, can readily be solved by changing to a high-vapor-pressure gaseous dopant source such as diborane (B_2H_6). Boron, if not incorporated in the crystal lattice will desorb from the substrate surface, behaving like AsH_3.

There is an alternative explanation for the droplet formation which is currently being explored. If the Ga concentration exceeds the solid solubility limit

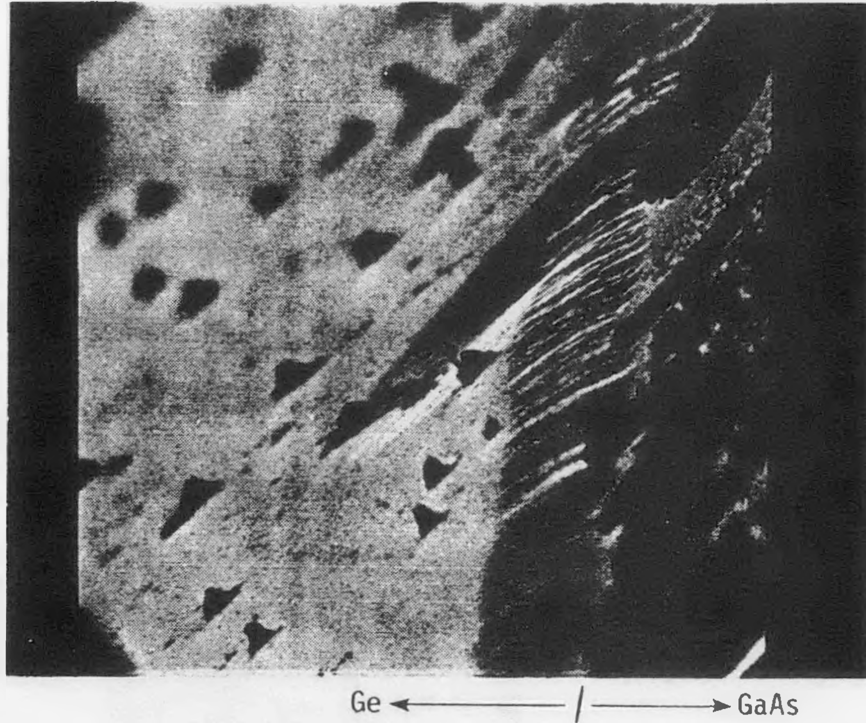
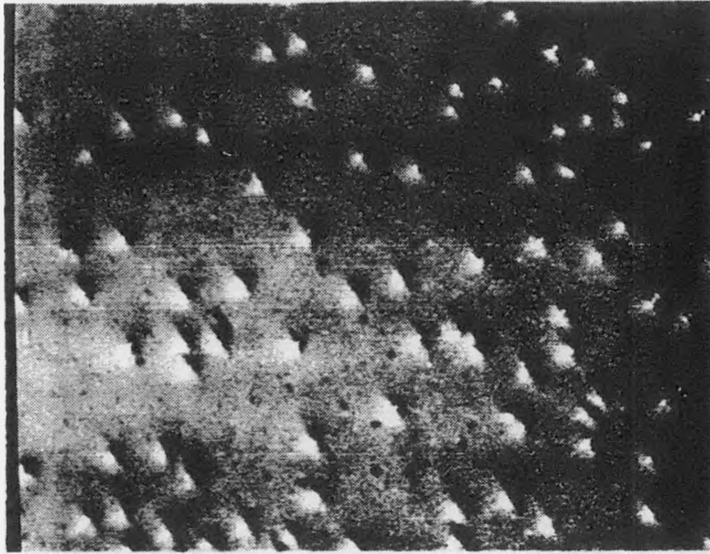
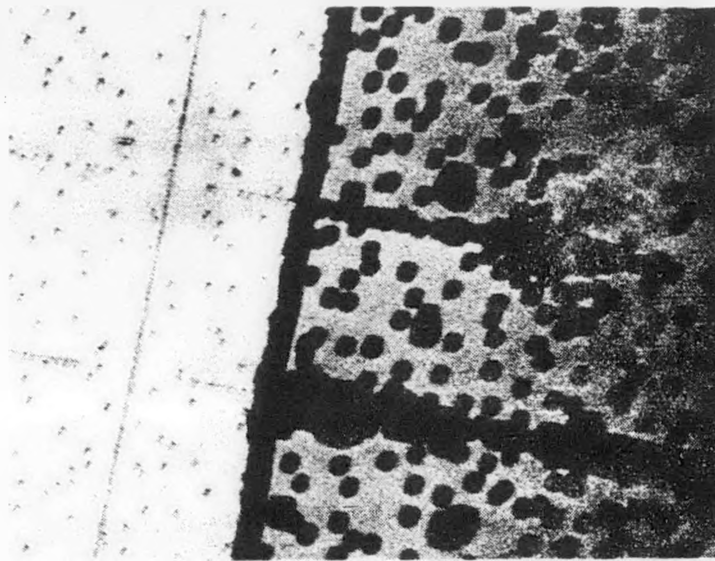


Figure 3-3. SEM photograph showing Ga-rich protrusions in Ge surface and pits etched into GaAs surface.

OM-382



a. Ge surface (1400 X)



Ge GaAs (280 X)

b. Etched surface

Figure 3-4. Surface of Ge tunnel junction: a) before etching and b) after etching of tunnel junction pattern.

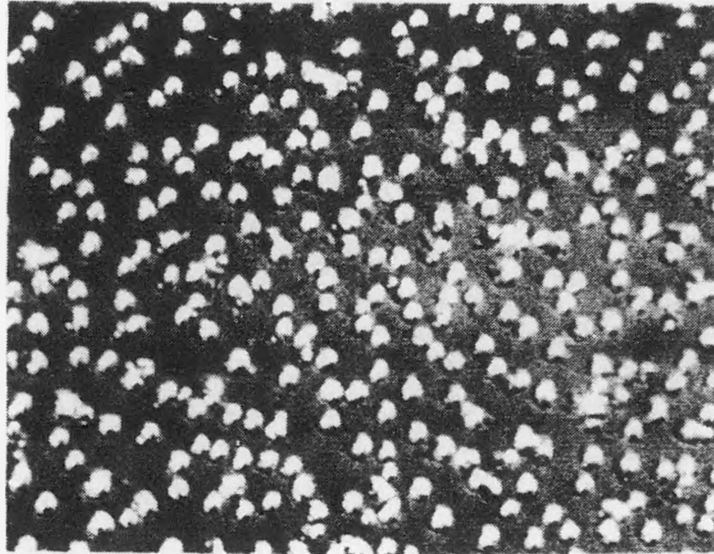


Figure 3-5. Micrograph showing surface of p^+/n^+ Ge tunnel junction (1400×). During growth of the final p^+ layer, the TMG was turned off 1 minute prior to the termination of the growth.

for the pressures being used, droplets would be expected to form. Increasing the partial pressure of GeH_4 in the gas stream should eliminate the problem.

The second disadvantage of Ga-As doping relates dopant diffusion, growth temperature, and the interfacial abruptness required to fabricate tunnel junctions capable of current densities reaching several hundred A cm^{-2} (250 A cm^{-2} required for 1000 suns AM1.5 with 5 percent obscuration). The problem was recognized when grown structures failed to demonstrate resistivities sufficiently low to be ascribed to band-to-band tunneling. Instead, the I-V characteristics and junction resistivities indicate that device currents result from the normal thermal currents seen in all diodes and the "excess" tunnel currents through midgap defect states.

However, degenerately doped p^+/n^+ junction which are abrupt should exhibit band-to-band tunneling currents. To examine this, an effective doping concentration is defined as

$$n^* = \frac{N_A N_D}{N_A + N_D} \tag{1}$$

for which N_A and N_D are hole and electron concentrations, respectively. For the devices grown during this program, n^* equals approximately 2×10^{19} cm^{-3}. In the abrupt step junction approximation, which uses

$$W = (2\epsilon V/qn^*)^{1/2} \quad , \tag{2}$$

where ϵ is the permittivity, q is the electronic charge, V is the built-in potential, and n^* is defined by Eq. (1), the depletion width W equals approximately 75 Å for $V = 0.6$ V and $n^* = 2 \times 10^{19}$ cm^{-3}. Band-to-band tunneling should result, but did not.

These observations, high resistivity and lack of band-to-band tunneling, precipitated a careful examination of the diffusive properties of Ga and As. At the temperature used for the Ge growth, approximately 775°C, the diffusion coefficients for Ga and As, are 4×10^{-14} and 5×10^{-12} cm^2 sec^{-1}, respectively [4]. A diffusion length d can be defined as

$$d = 2\sqrt{Dt} \tag{3}$$

in which D is the diffusion coefficient, and t is time in seconds at 775°C. d equals 40 Å $\sqrt{t}$ and 450 Å $\sqrt{t}$ for Ga and As, respectively. Growth times are generally 60 to 120 sec for the Ga-doped layer. At 775°C, Ga diffuses as much as 450 to 500 Å in two minutes, and As can diffuse as much as 0.5 μm. Fortunately, As diffusion can be tolerated since the Ga doping is greater than twice that of As, and all the As which diffuses into the Ga-doped Ge can be compensated without losing degeneracy in the layer. However, n^* and, therefore, J_p will decrease. The more important problem is the Ga diffusion.

In the model of a diffusion broadened step junction, the depletion layer width is given by [5]:

$$W' = W \left[1 + \left(\frac{N_A}{3n^*} \right) \left(\frac{\pi D t}{W^2} \right) \right]^{1/2} \tag{4}$$

in which all the terms have been defined previously. Using $N_A = 7 \times 10^{19}\ cm^{-3}$, $W = 75$ Å, $n^* = 2.1 \times 10^{19}\ cm^{-3}$, $D = 4 \times 10^{-14}\ cm^{-2}\ sec^{-1}$, and $t = 120$ sec, W′ equals 415 Å.

Tunneling current density (band-to-band) can be expressed from Kane's theory [6] as

$$J = AW'^{-1} \exp(-BW') \tag{5}$$

where A and B are material constants equal to approximately 1.6×10^7 Å and 4.5×10^{-2} Å^{-1}, respectively, for Ge at 300°K and n^* equal to $2.1 \times 10^{19}\ cm^{-3}$. Using a value of W′ equal to 415 Å, equation (5) predicts a tunneling current density of $3 \times 10^{-4}\ A\ cm^{-2}$. Hence, the lack of band-to-band tunneling can be explained by the diffusion broadened barrier width.

The problem can be further exacerbated by the "response time" of the growth system. If the system response to composition or dopant changes is sluggish, dopant gradients can broaden the effective depletion widths producing linearly graded junctions similar to those formed by dopant diffusion. Whichever mechanism is operative, C-V data for the junctions support the absence of abrupt

dopant changes. Plots of C^{-2} versus V do not show the linear behavior associated with step junctions.

The apparent solution for the diffusion problem is to lower the growth temperature, if possible, and still achieve the excellent surface morphologies which have been attained at 775°C; poorer surface morphologies have been reported for layers grown in the 650° to 700°C range [7]. Nonetheless, temperature reductions were attempted, and the results have been quite good. To date, temperatures as low as 600°C have been used to grow layers which have surface morphologies comparable to those of layers grown at 775°C. The key to this development is thought to be the augmented H_2 carrier gas flow rates, increased from 3 to approximately 9 l min^{-1}, which have been used for these growth experiments.

At the present time, we see no reason why growth temperatures in the range of 600° to 650°C cannot be used routinely. At 640°C, for example, the diffusion coefficients of Ga (and also B) and As are about 2×10^{-16} and 1×10^{-13} cm^2 sec^{-1}, respectively, giving diffusion lengths from Equation (3) of $2\sqrt{t}$ and $63\sqrt{t}$ Å where t is the growth time in seconds. The Ge growth rate at the lower temperature is about 0.1 μm per min. Since each layer of the tunnel junction is approximately 0.1−μm thick and requires a 1 min growth, Ga and As diffusion will be limited to 15 and 500 Å, respectively. The As diffusion can be tolerated since the Ga doping level is considerably greater and is relatively immobile.

To summarize this section on Ge growth, high quality crystalline layers have been grown using the thermal decomposition of GeH_4; Ga and As have been used to degenerately dope the Ge p- and n-type, respectively. In the early work the high growth temperatures, around 775°C, coupled with a sluggish system response, produced graded junctions which show very weak band-to-band tunneling characteristics. By increasing carrier-gas flow rates, growth temperatures have been reduced to as low as 600°C without sacrificing surface morphology while reducing impurity diffusion and decreasing the system response time. Devices using these improved growth conditions are currently being developed.

3.1.2 Characterization of Tunnel Junction Resistivity

The patterned Ge interconnect must be capable of carrying from 100 to 250 A cm^{-2} at 1000 suns AM2 for obscurations of 10 and 5 percent, respectively. If the maximum voltage drop which can be tolerated across the tunnel junction is 50 mV, the specific resistance of the total interconnect must be limited to 4×10^{-4} ohm$-cm^2$ for 10 percent obscuration and 2×10^{-4} ohm$-cm^2$ for 5 percent obscuration at 1000 suns. At 400-sun concentration, the necessary specific resistances can be relaxed to 1×10^{-3} and 5×10^{-4} ohm$-cm^2$ for 10 and 5 percent obscurations, respectively.

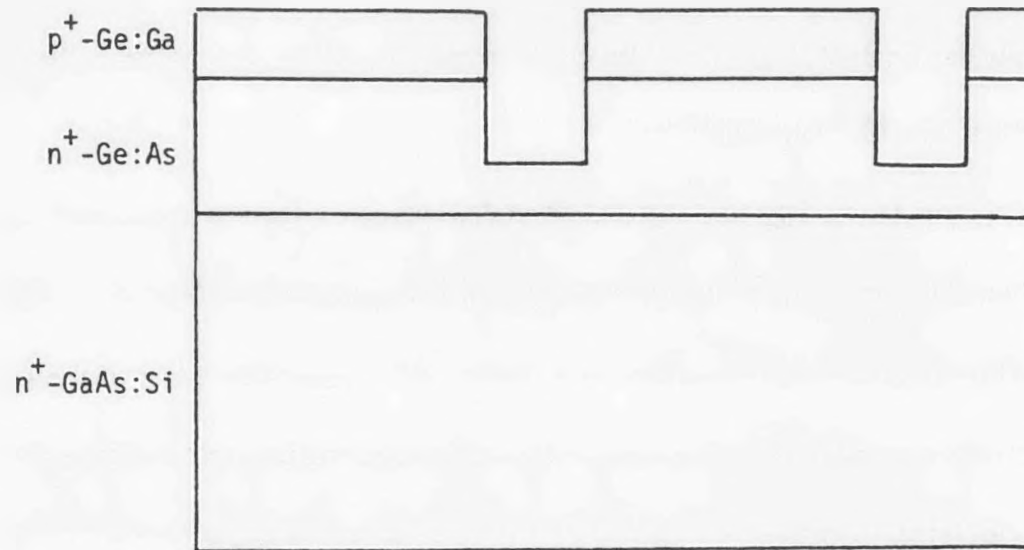
The IOC contains three interfaces which can contribute to structure resistivity: the n^+/p^+ Ge junction has received the most attention. However, there are also two heterointerfaces, $p^+$$-$Ge/$p^+$$-$GaAs (or AlGaAs) and $n^+$$-$Ge/$n^+$$-$GaAs (or AlGaAs), which must be considered. Bulk losses can

generally be neglected at the degenerate doping levels since specific resistances will be 10^{-6} to 10^{-8} ohm cm^2.

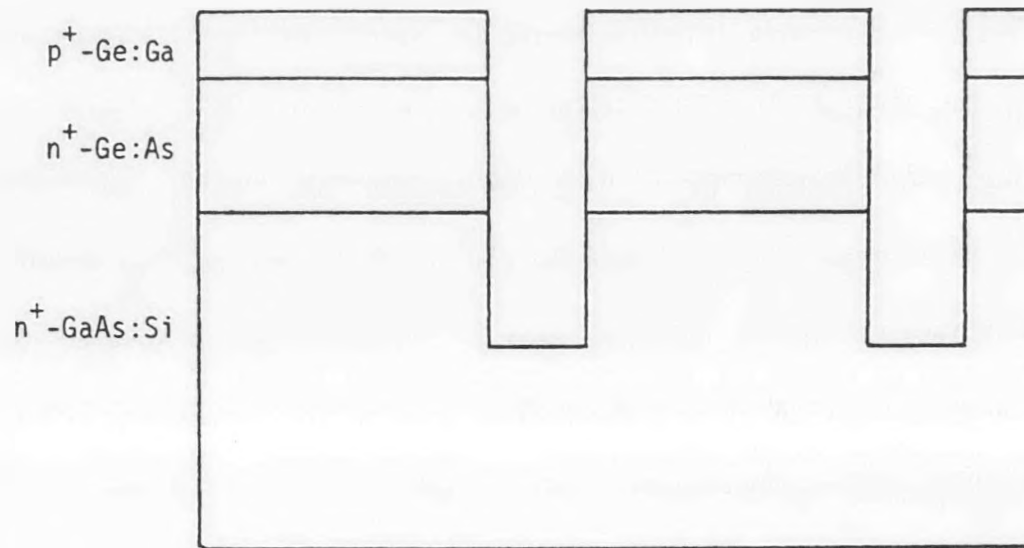
To qualitatively evaluate the resistive contribution from the interfaces, n-on-p and p-on-n tunnel junctions were grown on p- and n-type GaAs, respectively. Arrays of In dots followed by Ag overlayers, 300- and 5000−Å thick, respectively, were depositd on the fronts of the grown structures by e-beam evaporation. Appropriate metalization was depositd on the substrate, and the structures were alloyed at 460°C for about 60 sec. The contacts which resulted are ohmic, but no attempts at optimization were made since the tunnel junctions will not have metallic contacts in the final structures. The resulting structures contain both an n^+-Ge/p^+-Ge homointerface and either an n^+-Ge/n^+-GaAs or a p^+-Ge/p^+-GaAs heterointerface at the epilayer/substrate juncture. Using a wet chemical etch, mesas were then fabricated in which the etching was terminated after penetration of the Ge homojunction but before reaching the substrate, and other mesas were etched completely through the Ge/GaAs interface, penetrating into the substrate. A schematic of the test structure for a p-on-n device is shown in Figure 3-6. The area of the contacts is 1.1×10^{-3} cm^2, and mesa areas are 2.1×10^{-3} cm^2.

The three following measurements were then made to estimate specific resistances:

1) Resistances from two adjacent dots on a nonetched portion of the front surface and on the back surface were measured and multiplied by dot area



a) Partial etching which penetrates only the p^+/n^+ homointerface



b) Etching with penetration of both the p^+/n^+ and n^+/n^+ interfaces

Figure 3-6. Etched structures used to evaluate the interface resistivities for Ge tunnel junctions grown on GaAs substrates.

to approximate the values of specific contact resistances. Note that this also includes probe resistance.

2) The resistance between adjacent partially etched mesas was then measured, and the specific resistance was calculated based on mesa area.

3) The resistance from the front of a fully etched mesa to the back of the substrate was measured and the specific resistance, also based on mesa area, was calculated.

Subtracting the front contact specific resistance from the mesa-to-mesa measurement gives an approximate value for the n^+-Ge/p^+-Ge interface specific resistance, the probe resistance being accounted for by the front contact resistance. Subtracting the front and back contact specific resistances and the n^+-Ge/p^+-Ge specific resistance from the front-to-back measurement of (3) yields a qualitative measure of n^+-Ge/n^+-GaAs heterointerface specific resistance. We consider this measurement technique qualitative because it does not account for the effect of current spreading which the differences in area of the dot contacts and the mesa might produce on the effective area of the mesa. Also, neither current crowding effects nor surface leakage effects are considered. Since most of these parasitic effects will tend to increase the measured resistances, we believe that the results approximate "worst-case" numbers. To substantiate the measurements, single layer n^+-Ge/n^+-GaAs and p^+-Ge/p^+-GaAs structures were prepared, contacted, etched, and evaluated in a similar fashion. The results of these measurements are described next.

Analysis of the n^+-Ge/n^+-GaAs Interface

Because the electron affinity of Ge and GaAs are practically identical, 4.07 and 4.13 eV for GaAs and Ge, respectively, the n^+/n^+ interfaces formed from these materials are expected to show extremely low resistivities for majority carrier currents. The band diagram for such an interface, using Anderson's model of a continuous vacuum level, is shown in Figure 3-7. However, low resistivity has not been the general observation, and more than half of the grown samples show n^+/n^+ resistivities which range between 0.1 and 1 $ohm-cm^2$. Several samples do show resistivities below 10^{-3} $ohm-cm^2$; a minimum value of 5×10^{-4} $ohm-cm^2$ has been achieved. Initially, thermal degradation of GaAs/Ge interface was suspected of producing the higher resistivities. However, examination of the resistivity data indicates a poor correlation with the length of time at which the substrates are at elevated temperatures. This is shown in Figure 3-8. Particularly troublesome are the samples indicated by arrows, OM-381 and OM-399. The resistivities of these two samples are low and high, respectively, by several orders of magnitude.

The nature of the I-V characteristic is as troublesome as the large values of resistivity. Rather than being ohmic, these interfaces predominantly show non-linear behavior, including instances of p^+-on-n^+ band-to-band tunneling characteristics. An I-V characteristic from an n^+-Ge layer/$n^+-GaAs-$substrate interface is shown in Figure 3-9, and both tunneling and rectifying tendencies can be seen. The most likely source of this type of behavior is compensation at the

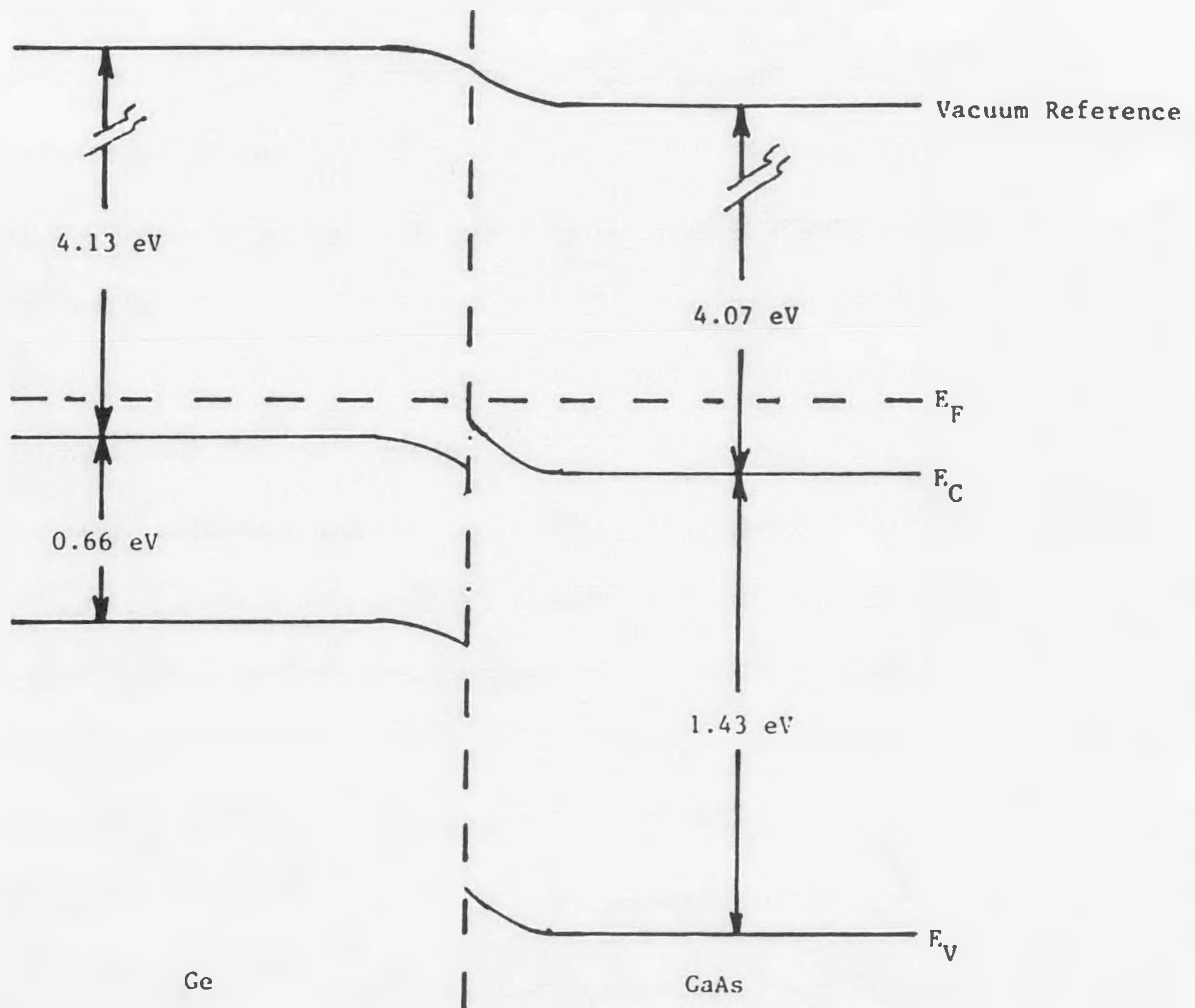
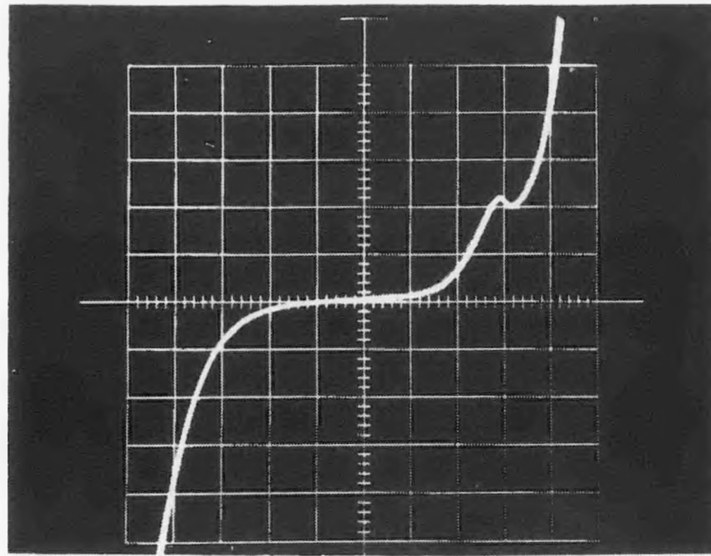


Figure 3-7. Band diagram for Ge-GaAs interface when both materials are degenerately doped. No significant barrier to majority carrier flow.



Vertical scale: 1 mA/div
Horizontal scale: 0.2V/div

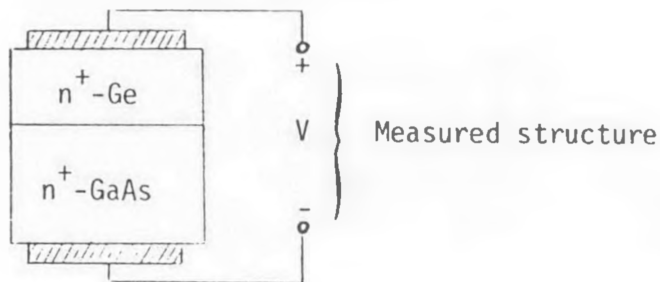


Figure 3-9. I-V characteristic of $n^+ - n^+$ Ge-GaAs interface showing unexpected rectification and tunneling features (growth temperature = 775°C).

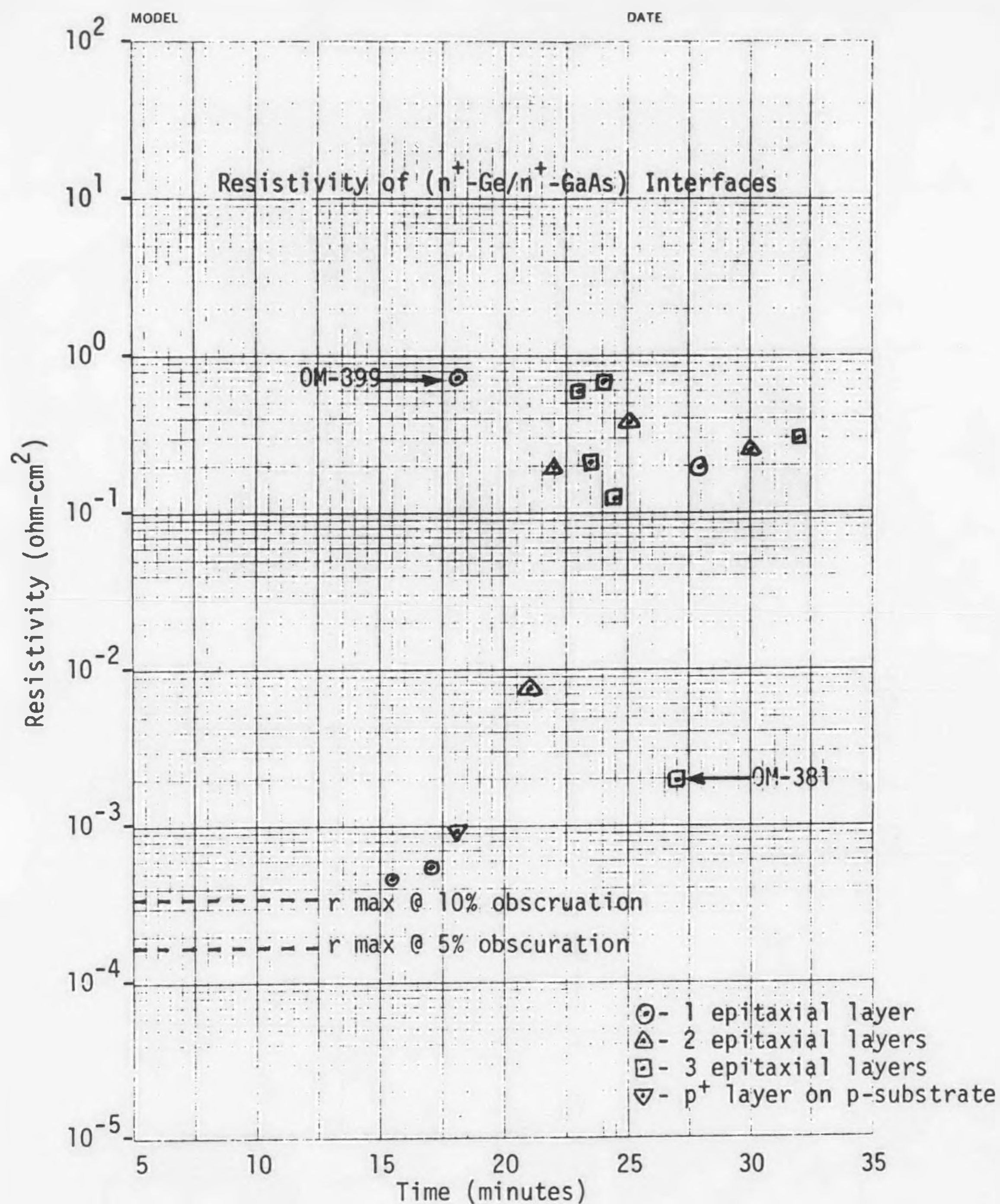


Figure 3-8. Resistivity of $n^+/n^+ -$ Ge/GaAs interfaces versus the time at which substrates see elevated temperatures (growth temperatures $\geq 730^{\circ}C$).

interface which results in either acceptor outdiffusion from the substrate, Ge diffusion into the GaAs (occupying As lattice sites), or contamination of the reactant gases. The compensated behavior is not observed for all samples, eliminating contamination of reactant gases, and Ge occupation of As lattice sites in GaAs is unlikely because of elevated As partial pressures before and during Ge growth. The substrate is the most likely source of the compensating specie. The resistivities of the grown samples, graphed as a function of substrate location in the GaAs ingot, are shown in Figure 3-10. These data indicate that as the substrate material is located further from the seed end of the ingot the resistivity seems to lock into the 0.1- to 1−ohm cm^2 range. The outdiffusion of an acceptor from the substrate has also been suggested by carrier measurements using a Miller feedback profiler for GaAs layers grown on substrates prepared from the same ingot. The appearances of the p^+−on−n^+ tunneling characteristic further suggests a very large acceptor concentration on the GaAs surface, and perhaps, reflects impurity gettering at the GaAs/Ge interface.

To test this hypothesis, an n^+−Ge layer was grown on a 4−μm thick n^+−GaAs epilayer, doped to 2×10^{19} cm^2 with Si. The GaAs was grown on a substrate from the questionable ingot. Partial mesas were etched and evaluated. The result is shown in Figure 3-11 for measurement of the I-V characteristic from contact to contact (curve 1) and from mesa to mesa (curve 2). The characteristic shown in curve 2 is much more linear than that shown in Figure 3-9, and the n^+−n^+ specific resistance is almost two orders of magnitude lower than the 0.1-

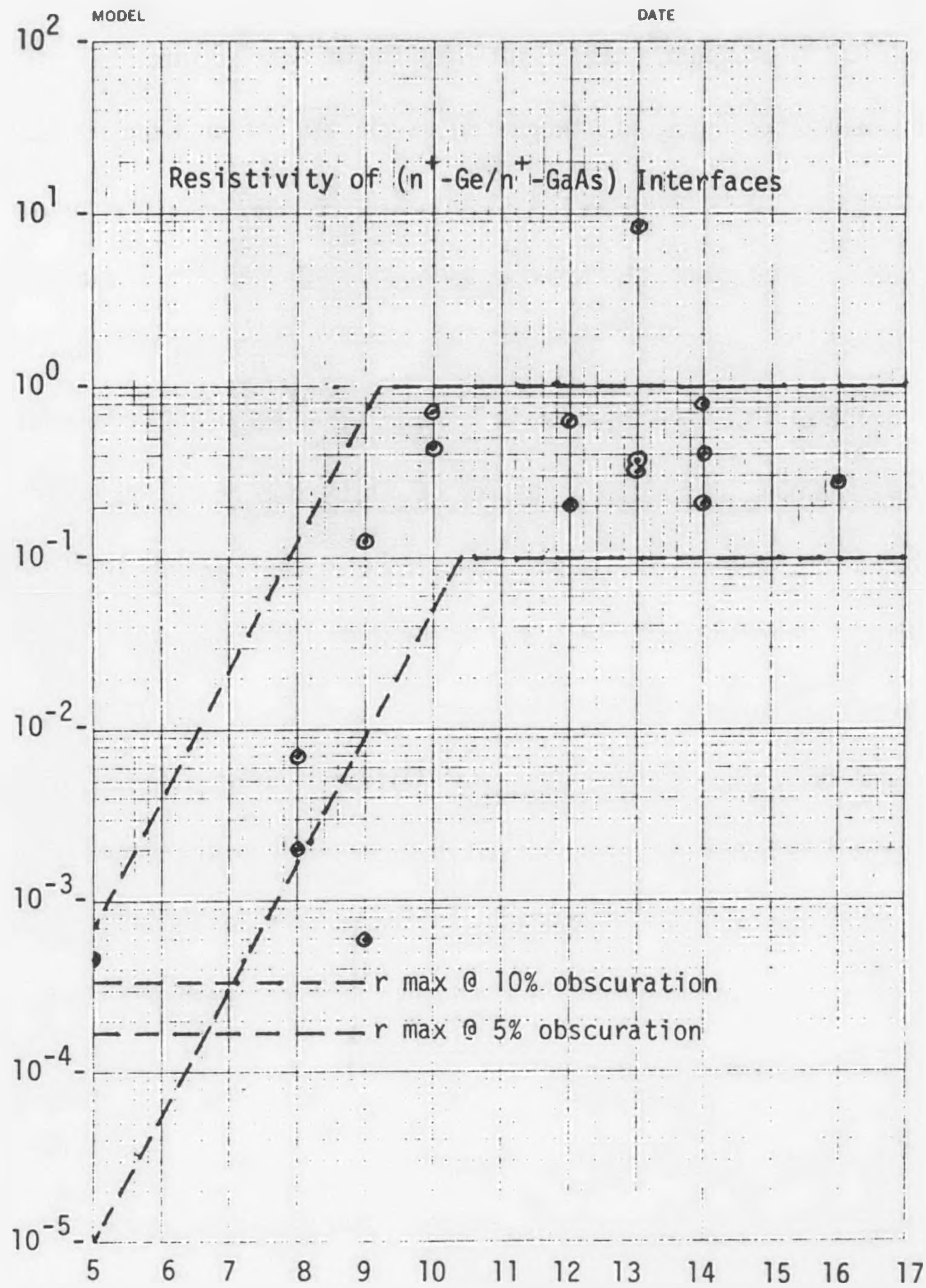
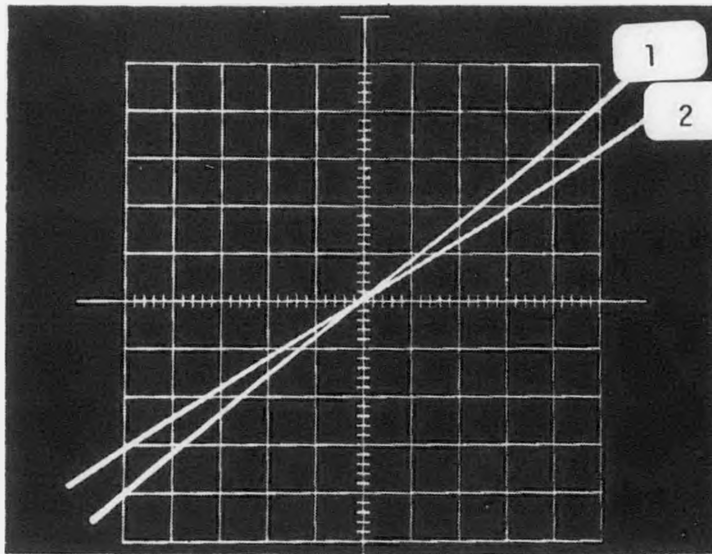
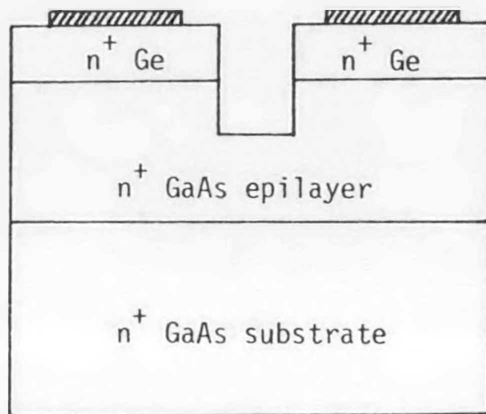


Figure 3-10. Resistivity versus wafer number from Batch 49 of GaAs substrates (numbering proceeds from seed to tail end of ingot). Lowest resistivities measured near seed end of ingot.



Vertical scale: 20 mA/div
Horizontal scale: 0.05 V/div



Structure measured for curve 2

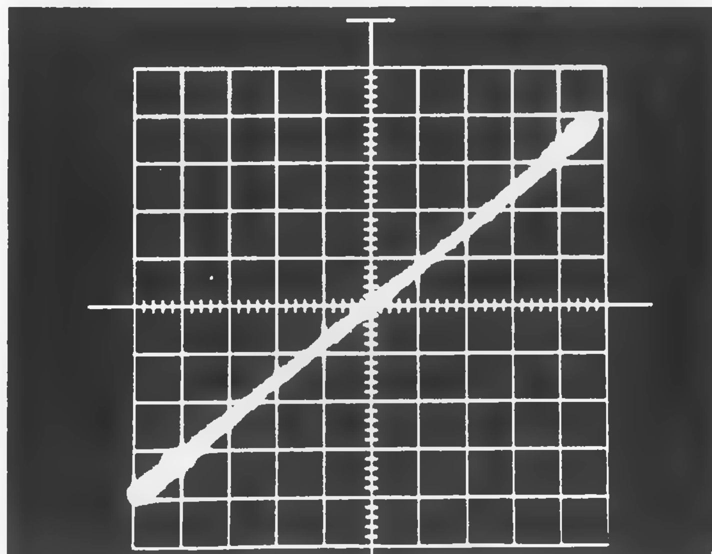
Figure 3-11. Evaluation of n^+-Ge/n^+-GaAs interface using a thick GaAs epilayer doped to 2×10^{19} cm^{-3} with Si. Curve 1 measured between two unetched contacts and curve 2 measured from mesa to mesa after etching.

to 1$-$ohm cm^{2} range. The specific resistance of this interface is about 7×10^{-3} ohm cm^{2}. As mentioned above, other specific resistances for $n^{+}-Ge/n^{+}-GaAs$ interfaces as low as 5×10^{-4} ohm cm^{2} have been measured, and therefore, we have concluded that most of the observed irregularities are related to a problem with this particular batch of substrates and are not a fundamental problem--such as Fermi-level pinning--at the doping levels being employed.

Analysis of the $p^{+}-Ge/p-GaAs$ Interface

Because of a shortage of p-type GaAs substrates few $p^{+}-Ge/p-GaAs$ interfaces were prepared and examined in the early part of the program. The Cd-doped substrate used for this growth have a carrier concentration, 1 to 2×10^{18} cm^{-3}, which is less than the 8×10^{18} cm^{-3} required for degeneracy in p-type GaAs. The measured front-to-back resistivity for this sample is 1×10^{-3} ohm$-$cm^{2} and shows linear behavior as can be seen in Figure 3-12.

In more recent work, Zn-doped GaAs substrates with carrier concentrations of 2.5×10^{19} cm^{-3} were obtained, and $p^{+}-Ge$ layers were grown directly on these substrates. After the application of contacts, the samples were etched to form mesas. A typical I-V curve for contact-to-contact (curve 1) and mesa-to-mesa (curve 2) characteristics is shown in Figure 3-13. Contact resistance dominates the structure, and the specific resistance of the interface is less than 5×10^{-4} ohm$-$cm^{2}.



Vertical scale: 10 mA/div
Horizontal scale: 0.1V/div

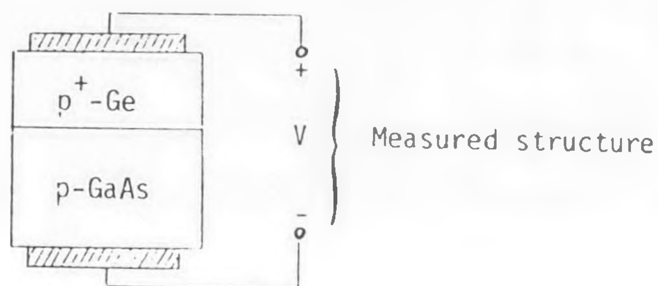
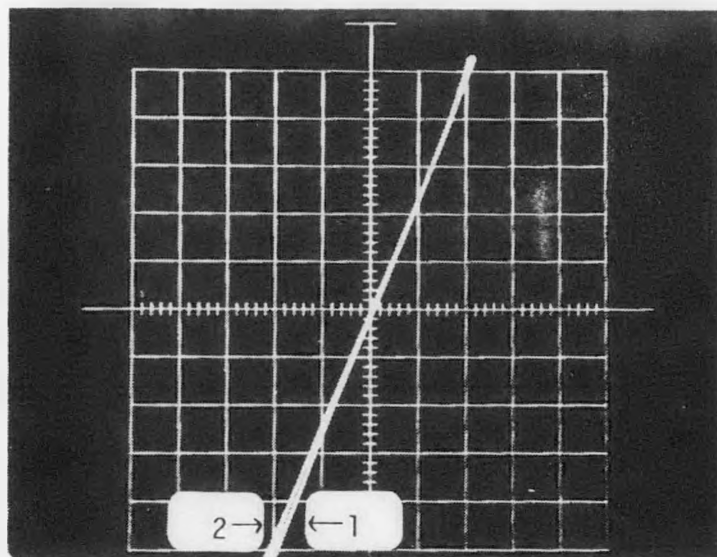


Figure 3-12. I-V curve for a p^+–Ge/p–GaAs interface showing ohmic behavior; $\rho = 1 \times 10^{-3}$ ohm–cm^2 (growth temperature = 775°C).

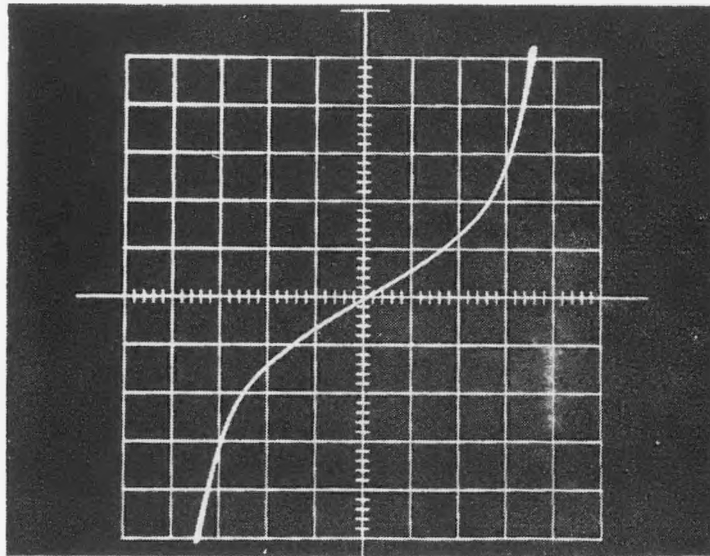


Vertical scale: 20 mA/div
Horizontal scale: 0.05 V/div

Figure 3-13. I-V characteristic for p^+-Ge/p^+-GaAs structure. Curve 1 measured between adjacent contacts on unetched surface; curve 2 measured from etched mesa to etched mesa (growth temperature = 773°C).

Analysis of the $n^+ - Ge/p^+ - Ge$ Interface

Although the interfaces (i.e., the n^+/n^+ and p^+/p^+ interfaces) which connect the tunnel junction with the rest of the cascade structure cannot be ignored and must possess resistivities in the 10^{-5} ohm$-$cm^2 range, the major tunnel junction concerns have focussed upon the ability to produce devices which are capable of carrying the current at 1000-sun concentration with a minimal resistive loss. At 1000 suns, the tunnel junction must also have a specific resistance in the $10^{-5}$$-ohm-$cm^2 range if the target resistivity of the structure, 2×10^{-4} ohm$-$cm^2, is to be attained. This value of resistivity is well within the capability of a Ge tunnel junction; in fact, values in the low $10^{-6}$$-ohm-$cm^2 range have been reported [8]. These are values which result from band-to-band tunneling. However, because of the dopant diffusion (and possible grading related to the slow system response) described in the previous section, band-to-band currents have been practically nonexistent; hence, resistivities are presently higher than required values. A typical I-V curve, shown in Figure 3-14, was measured from mesa to mesa. Since the forward currents of this device are smaller than the reverse currents, the I-V curve shown is the forward characteristic of two, back-to-back diodes. Neither diode shows a band-to-band tunneling characteristic. These forward currents are the combination of normal diode thermal currents and excess tunnel currents. The excess currents depend upon tunneling through defect states located within the bandgap, and typical resistivities are in the range of 10^{-2} to 10^{-3} ohm$-$cm^2 for such currents [9].



Vertical scale: 2 mA/div

Horizontal scale: 0.2 V/div

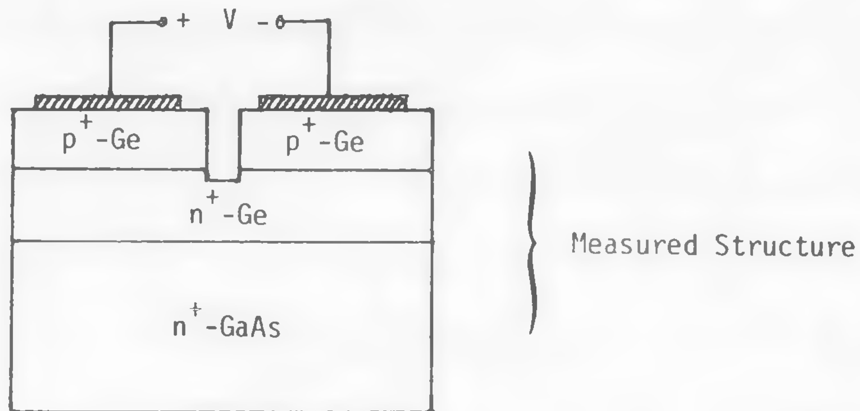


Figure 3-14. I-V curve for back-to-back junctions; lack of band-to-band tunneling characteristic is caused by a diffusion-broadened, p-n interface (growth temperature = 775°C).

The measured resistivities of the n^+/p^+ interfaces have generally been near 1×10^{-2} ohm−cm^2; however, some samples have shown values as low as the mid−10^{-4}−ohm−cm^2 range, with 2.8×10^{-4} ohm−cm^2 being the lowest measured. The larger values are consistent with resistivities expected for structures dominated by excess currents.

The recent development of lower growth temperatures and the use of diborane as the p-type doping source will likely alleviate many of the tunnel junction problems.

To summarize, using the "worst case" values of 5×10^{-4} ohm−cm^2 for the n^+−Ge/n^+−GaAs and p^+−Ge/p^+−GaAs interfaces and the best value of 2.8×10^{-4} ohm−cm^2 for the tunnel interface, a structure resistivity of 1.3×10^{-3} ohm cm^2 results. At a 50 mV loss, this is consistent with currents at approximately 130-sun AM1.5 concentration, and this value is almost certain to improve with the lower Ge growth temperatures.

3.2 Development of Etching Techniques for Ge Patterned Tunnel Junctions

Patterning the Ge tunnel junction places several constraints on wet chemical etching. Since the Ge is grown on a thin GaAs cap layer of the bottom cell, etches which are selective for Ge and GaAs are highly desirable to prevent damage to the bottom cell. The $Al_xGa_{1-x}As$ ($x \cong 0.45$) window layer of the bottom cell also serves as a useful stop-etch layer. Hydrogen peroxide (H_2O_2) based etches are suitable etchants, and three different composition have been examined.

Initially we examined a $19H_2O_2$:NH_4OH solution which is frequently used to etch GaAs selectively on AlGaAs stop-etch layers. This solution was also found to etch Ge with an etch rate of about 0.1 μm per minute for agitated, room-temperature solutions. Some variability in etch rates was observed and is believed to be caused by the variable shelf life of the 30% H_2O_2 solution used to prepare the etchant. Figure 3-15 shows the contact pattern of a field effect transistor etched in $19H_2O_2$:NH_4OH; the etched walls make approximately 30° angles with the (100)-Ge substrate. The pattern was etched for 10 minutes, and 1.03 μm of material was removed.

It was suggested to us that 3% H_2O_2, prepared by dilution of 30% H_2O_2 with DI water, would selectively etch Ge leaving the GaAs intact. We found this to be the case; however, the etch rate is quite slow at room temperature, requiring 1 hour to etch 1 μm of material. The etching characteristics of the heavily doped n- and p-type layers differ: Ge layers doped heavily with Ga etch much more slowly than As-doped layers. This is presumably because the Ga oxides are less soluble than either the Ge or As oxides. If photoresist is applied to As-doped layers, substantial undercutting is observed when etched with the 3% H_2O_2. The undercutting can be reduced somewhat by vigorously bubbling N_2 gas through the etching solution and allowing the bubbles to impinge upon an inverted substrate surface. The best etching results for 3% H_2O_2 have been obtained when the Ga-doped layer is in contact with the photoresist using the bubbling technique. Figure 3-16 shows an SEM micrograph of the cross-section of a finger pattern. Since

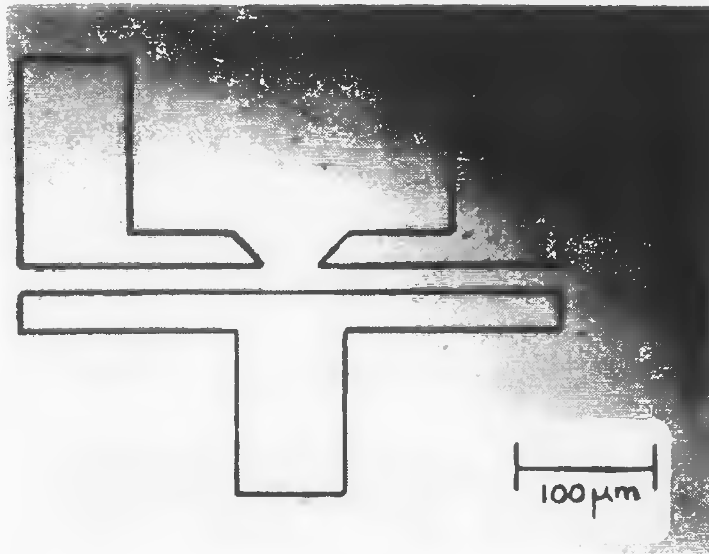


Figure 3-15. Reproduction of a FET contact pattern on a (100) Ge substrate; etched 10 min. in $19H_2O_2:NH_4OH$.

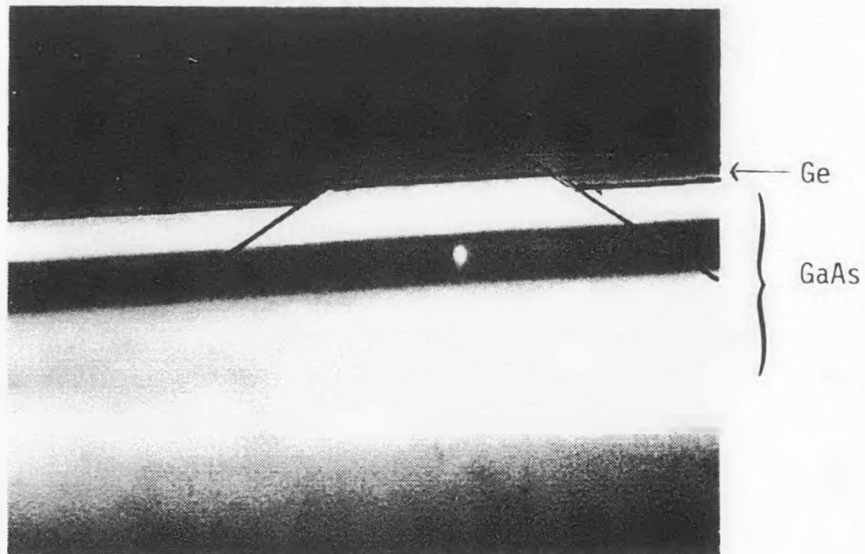


Figure 3-16. Micrograph of patterned 1 $-\mu$m$-$thick Ge finger on GaAs. Angles of etched walls approximately 30°.

the 3% H_2O_2 is selective for Ge, the GaAs cap layer of the bottom cell must then be removed after the Ge. A solution of $20H_2O_2$:$20H_2O$:NH_4OH accomplishes this. The GaAs is rapidly removed, and any oxide which forms on the AlGaAs window layer can be removed in a bubbled solution of NH_4OH:$10H_2O$, leaving a shining surface.

This third solution, $20H_2O_2$:$20H_2O$:NH_4OH, was also examined as a Ge etch with promising results. Stable etch rates of 0.3 μm per minute have been measured for room temperature solutions. The larger etch rate reduces the time to about 2 to 4 minutes for tunnel junction and GaAs cap removal. Therefore, the undercutting problem is reduced. The bubbling technique can also be employed to speed etching even further.

To summarize, Ge etching techniques have been developed. The best results have been obtained using $20H_2O_2$:$20H_2O$:NH_4OH at room temperature on samples with Ga-doped layers in contact with photoresist.

3.3 GaAs Overgrowth of Etched Ge Structures

GaAs layers have been successfully grown over patterned Ge structures. The typical growth sequence is the following:

1) Ge layers are grown on GaAs substrates,

2) the structures are removed from the Ge reactor and processed to define the patterns,

3) the etched structure is given a quick HF dip and returned to the reactor used for III-V growth (separate growth system), and

4) GaAs layers, sometimes single layers and sometimes multi-layered devices, are overgrown using the conditions consistent with good GaAs growth.

Figure 3-17 shows a cross-section of a 5−μm−thick GaAs layer which was grown over a Ge finger which was 31μm wide and 0.4μm thick. The morphology and uniformity of this layer are quite good.

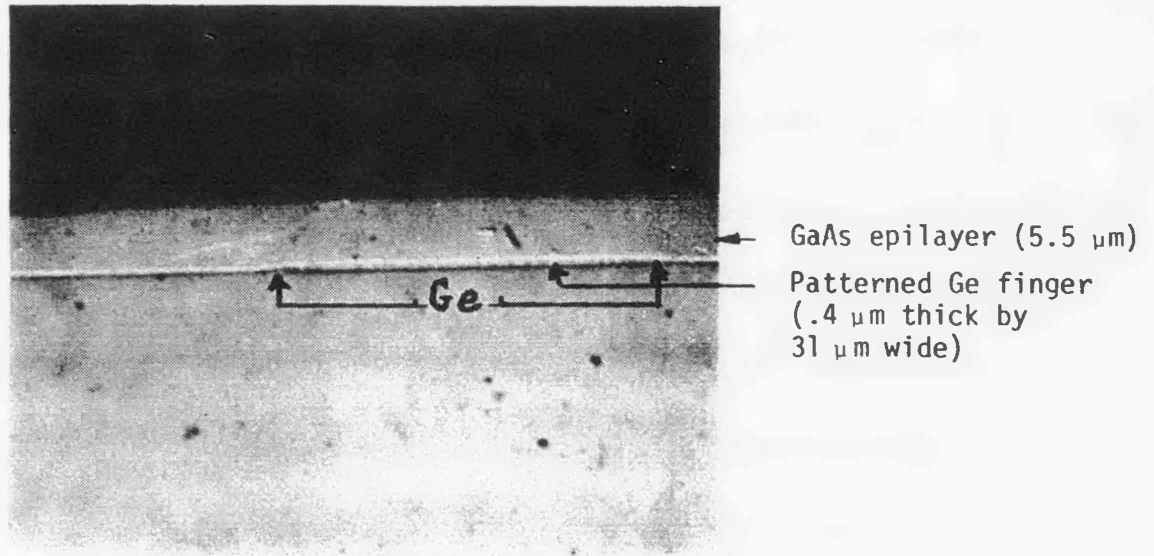
The growth of GaAs junctions on Ge patterned layers is perhaps a more critical test. This has been accomplished. An n^+−on−p^+ Ge tunnel junction was grown on a p^+−GaAs substrate. The tunnel junction was patterned. Because of the accelerated etching rate of Ga-rich protrusions described previously, the underlying GaAs surface was pitted with a pit density of $\sim 10^7\ cm^{-2}$. Nonetheless, this substrate was returned to the OM-VPE system. A GaAs p-n junction consisting of the following layers was grown at 625°C:

1) an n^+−GaAs:Te buffer layer grown for 1 minute,

2) a thick, unintentionally doped, n-type GaAs base region using a 30-minute growth,

3) a thin p-type GaAs:Mg region graded rapidly into a p^+−type AlAs region in a 5-minute growth, and

4) a p^+−GaAs:Mg cap layer (5-minute growth).



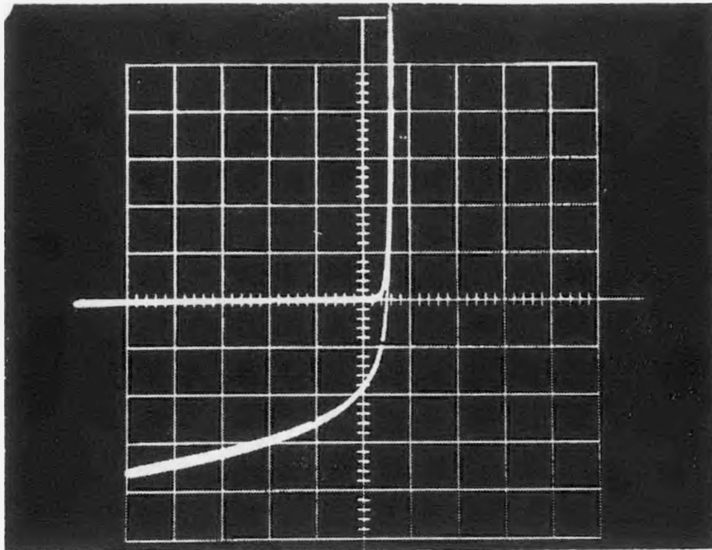
(1400 X)

Figure 3-17. Photograph of cleaved and stained GaAs epilayer (5.5 μm thick) grown over a patterned Ge finger. Areas of the epitaxially grown Ge layer removed via wet chemical etching; the structure then reinserted into the MO-CVD system for growth of epitaxial GaAs layer.

The surface morphology of the device is relatively good considering the nature of the substrate surface. Mesas (0.25 and 0.06 cm^2) were etched using $19H_2O_2:NH_4OH$, and Ag/Mn contacts were depositd and alloyed. The device structure is shown in Figure 3-18.

The GaAs junction grown on the patterned tunnel junction shows photovoltaic action, and current flow is through the tunneling interconnect because the p-type substrate and n^+-GaAs buffer layer produce a potential barrier. The I-V characteristic for a 0.25 cm^2 mesa is given in Figure 3-18 for dark and illuminated conditions (1 sun AM0) and shows that the junction quality is poor; V_{oc} equals 0.55 V, J_{sc} equals 1 mA/cm^2, and the fill factor is poor. However, these results are not surprising considering the densely pitted surface upon which this cell was grown. The ideality factor for this junction is 2.8 as determined from the log I-V curve shown in Figure 3-19 for both large and small area mesas. The currents scale with junction area and therefore indicate bulk characteristics control the device.

The important feature of this work is the clear demonstration of current conduction through a patterned structure which shorts what would have otherwise been a blocking interface.



Vertical scale: 0.1 mA/div
Horizontal scale: 1.0 V/div

Device area: 0.25 cm^2

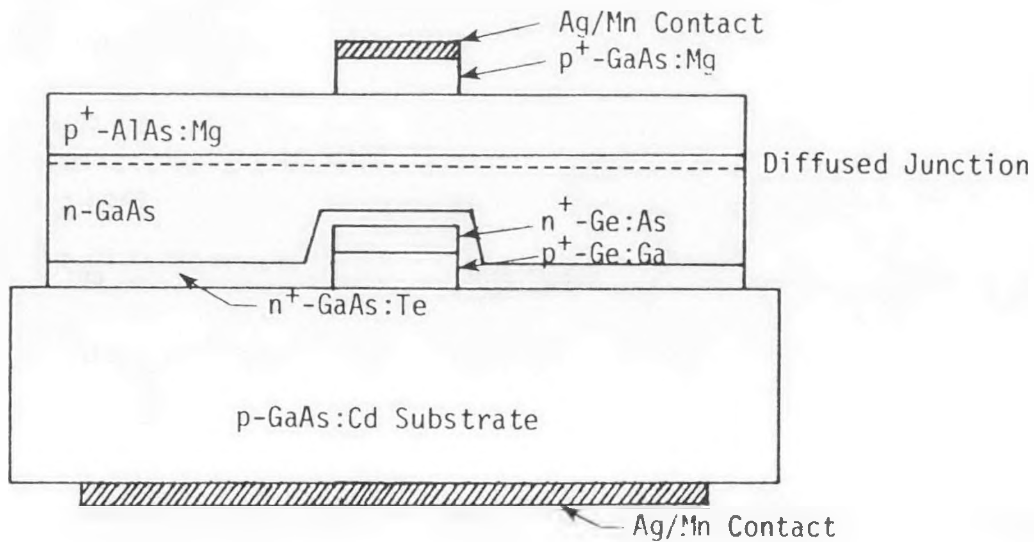


Figure 3-18. Dark and illuminated I-V characteristic for GaAs junction grown on patterned tunnel junction. Epilayer/substrate would be a blocking junction except in region of Ge structure. Demonstrates conduction through tunnel junction.

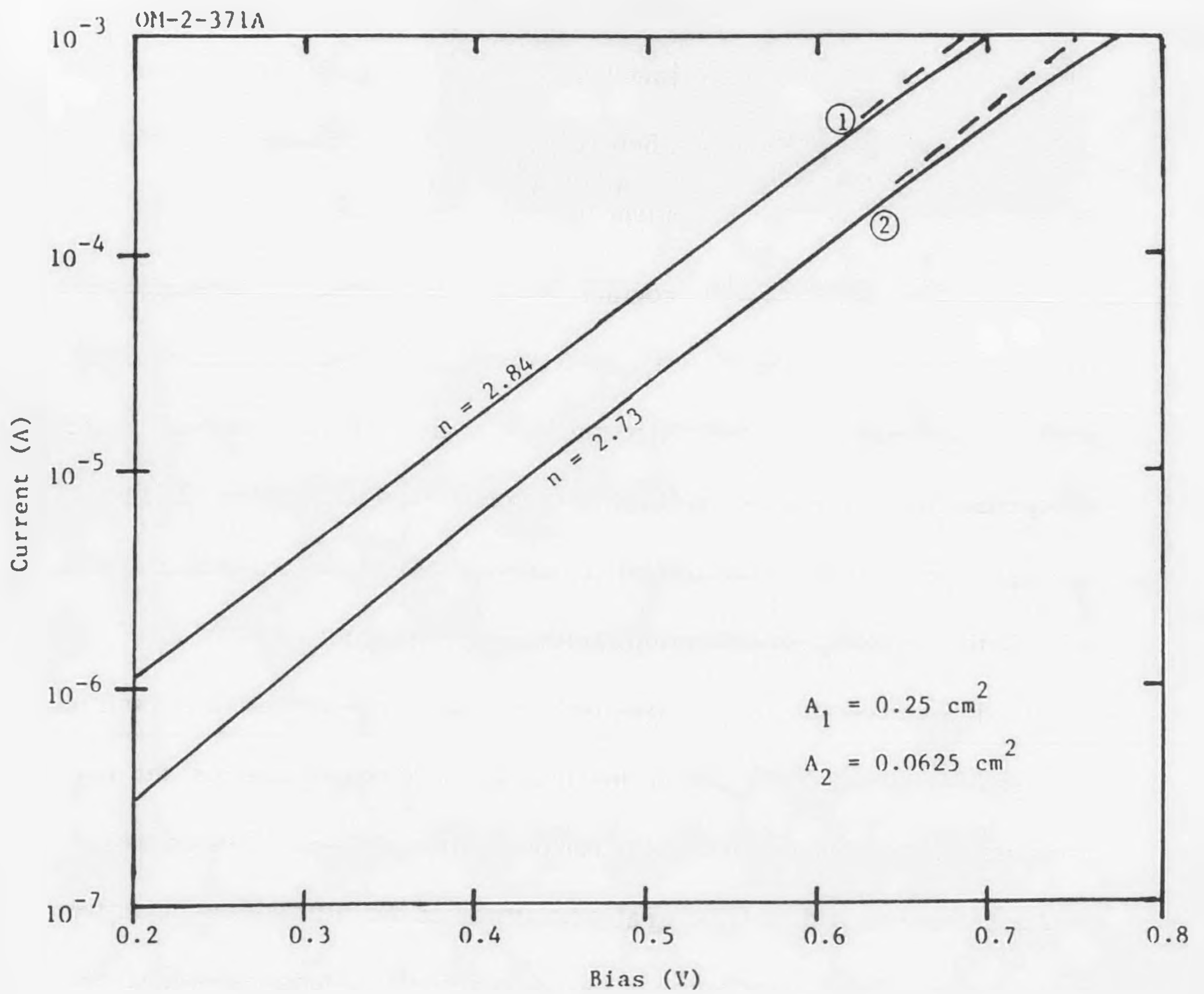


Figure 3-19. Dark log I versus V curves for large- and small-area p-n junctions grown on patterned tunnel junction and p-type GaAs substrates.

4.0 GROWTH AND CHARACTERIZATION OF GaAs AND AlGaAs DEVICES

In this section, we describe the growth of GaAs bottom cells, AlGaAs top cells, and the reinitiation of AlGaAs growth on oxidized AlGaAs surfaces. All photovoltaic junctions were fabricated in an different growth system than that used for Ge growth, and a system flow schematic is shown in Figure 4-1. Mg and Te have been used as the p- and n-type dopants, respectively.

In the final quarter of this program, we have experienced an extremely vexing problem with the Mg dopant: we have not been able to maintain stable dopant concentrations at intermediate gas flows through the bis(cyclopentadienyl)magnesium (Cp_2Mg) bubbler, the source of Mg. The problem has manifested itself as an "all or nothing" effect: with maximum flows through the bubbler, carrier concentrations in GaAs greater than 10^{19} cm^{-3} are measured; however, the morphologies of layers are extremely poor as a result of the high Mg content. When carrier flow through the bubbler is reduced, the morphologies improve but the material is compensated and n-type. This problem is similar to that reported by Fraas et al. who attributed the difficulties to impurities in the organometallics; purification of the organometallic material by vacuum sublimation solved the problem [10]. After purification, the dopant was reported to be well controlled, carrier concentrations correlated with bubbler gas flow rates, and layers showed less compensation. A similar purification capability is currently being established.

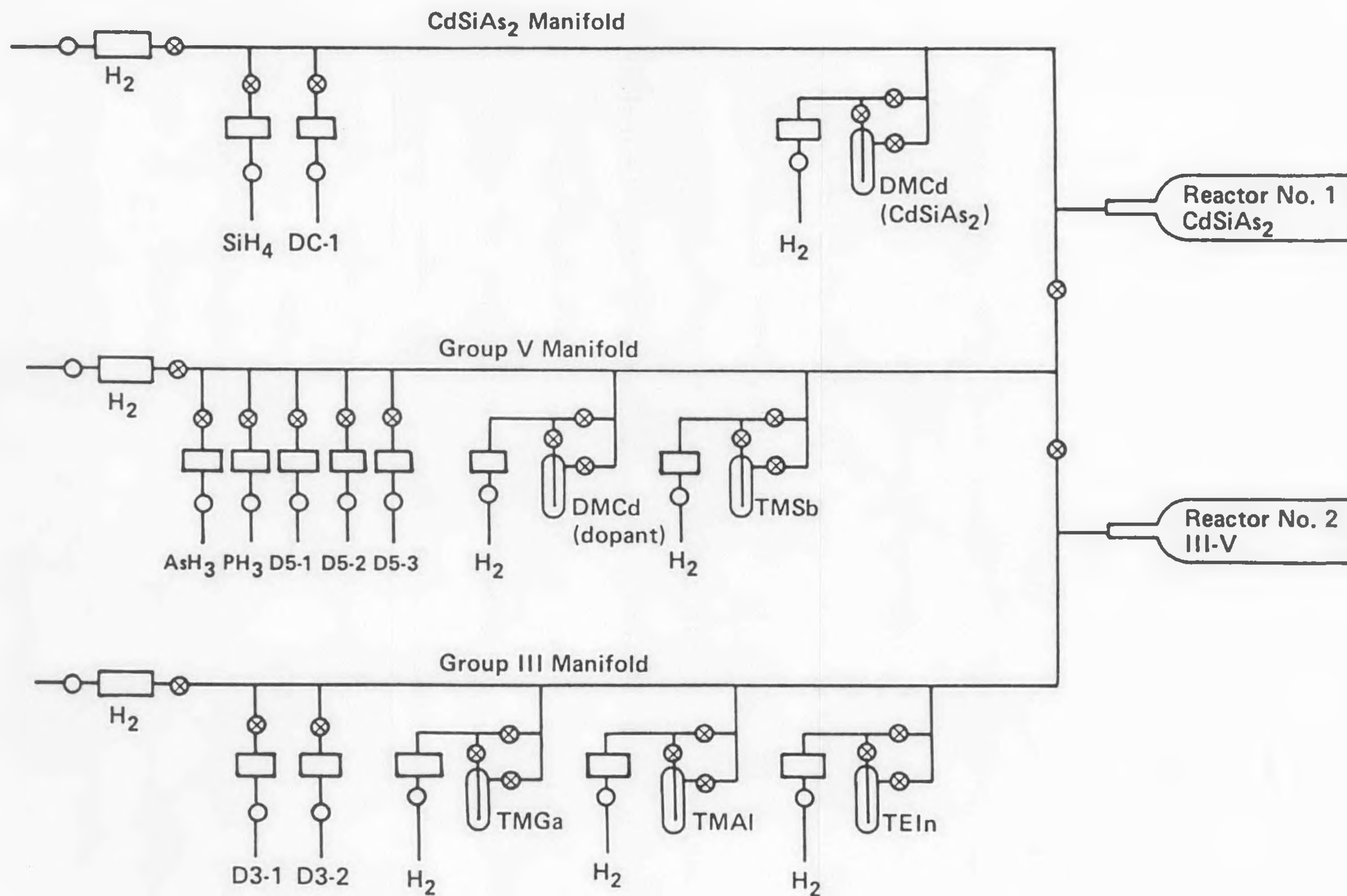


Figure 4-1. Flow schematic of OM-CVD system used for GaAs and AlGaAs growth.

The net effect of the dopant problem has been poorer device performance in the final quarter after some encouraging results earlier in the program. The results are described next.

4.1 GaAs Material and Device Development

4.1.1 Growth of GaAs

The GaAs growths used standard OM-VPE conditions and source materials. Trimethylgallium (TMGa) is the Ga source, and AsH_3 is the As source. Growths are typically performed at 625^0C using As/Ga ratios near 10. The total H_2 carrier gas flow rates are approximately 3 l min^{-1}. The GaAs epilayers have been grown on both n^+- and p^+-GaAs substrates, purchased polished and treated in the following manner:

1) The polished surfaces are scrubbed with a mild soap solution using small foam pads and are then rinsed with copious quantities of DI water.

2) The cleaned substrates are then etched in $8H_2SO_4$:H_2O_2:H_2O for approximately 2 minutes; this step removes any residual damage.

3) The cleaned and etched substrates are rinsed with DI water, blown dry with an N_2, and stored in a dry box under N_2 until use.

At a constant temperature, the GaAs growth rate depends primarily upon the H_2 flow rate through the TMGa bubbler, and growth rates are typically 0.1 μm/min.

The quality of the grown material is determined from Hall effect analysis and photoluminescence (PL). Undoped layers are generally n-type and carrier concentrations are generally in the high 10^{14} to low 10^{15} cm^{-3} range with mobilities of 4000 to 8000 $cm^2 V^{-1} sec^{-1}$ at room temperature. In undoped material, PL analysis often shows a residual acceptor, thought to be Zn, which is a likely contaminant of the TMGa.

Surface morphologies are generally good. Occasionally hillocks appear on the surfaces.

4.1.2 Development of GaAs Devices

The development of GaAs bottom cells has progressed through three structures. The first cell structure contains a small back surface field (BSF), produced by an n^+−GaAs buffer layer, and a graded-bandgap emitter. The second type contains a double heterojunction formed by one AlGaAs layer which develops a large BSF and a second AlGaAs layer which serves as a window layer to a GaAs homojunction. The third structure which we plan for the cascade cell contains both the AlGaAs BSF layer and a graded-bandgap AlGaAs emitter. The development of this final structure has been slowed by the Mg-dopant problem which has rendered surface morphologies rather poor.

The first device structure consists of an n-GaAs base doped with Te ($1-5 \times 10^{17}$ cm^{-3}) grown on an n^+−GaAs substrate (Si doped at 2×10^{18} cm^{-3}); a thin, Mg-doped $Al_xGa_{1-x}As$ layer follows in which x varies from 0.0 to ~0.4 in 0.2 μm. A 0.5−μm−thick AlAs layer is grown after the

graded layer and doped p-type with Mg. A heavily p-doped GaAs layer caps the structure to facilitate contacting. Contacts containing a Mn/Au alloy are then applied using electron-beam evaporation and alloyed at 460°C for 2 minutes. The contacts are thickened by electro-depositing gold. Except for the area beneath the contacts, the GaAs is etched off the surface by a $19H_2O_2:NH_4OH$ solution. The contact pattern, a simple five-finger grid applied photolithographically, has 12.2 percent obscuration for either 0.25 cm × 0.25 cm or 0.5 cm × 0.5 cm mesas. Layer thicknesses, doping levels, and contacts have not been optimized. No AR coatings are used.

The log I-V (dark currents) curves for these mesas exhibit diode factors n ranging between 1.21 and 1.34 for currents dominated by bulk diffusion which obey

$$J = J_o \exp\left[\frac{qV}{nKT}\right] \tag{6}$$

Values for J_o can be determined by extrapolating the above relationship to the V = 0 point, and for the current samples, J_os are between 6.6×10^{-17} and 2×10^{-16} A cm^{-2}. These J_o values are practically identical to those reported by Casey et al. for MBE-grown GaAs junctions with thin, oxygen-doped AlGaAs layers used for surface passivation; the diode factors for these structures are 1.16 [11]. These results certainly suggest that the junction quality is comparable. The open circuit voltages for typical mesas range from 0.97 to 1.00 V at 1 sun (AM0)

and are between 0.98 and 1.03 V at five suns. Contact resistance for these particular samples is high and degrades the fill factors to about 0.75. Short circuit currents, measured without AR coatings, are low; for better cells J_{sc} equals 15 to 18 mA/cm^2. Measured external quantum efficiencies peak at 60 percent at 0.6 μm for the best sample but drops on the long wavelength side of the spectrum. This appears to be due to a thinner than anticipated base layer.

The second GaAs cell structure grown at $725^{o}C$ and illustrated in Figure 4-2 has yielded open circuit voltages in the 1.01 to 1.03 V range, fill factors are near 0.76, and short circuit current densities are as high as 23 mA/cm^2 when measured under simulated 1 sun AM0 conditions without AR coatings. The external quantum efficiency for one of the cells is shown in Figure 4-3. Cell dimensions are 0.5 cm $\times$ 0.5 cm employing the five-finger contact pattern with 12 percent obscuration. The active area efficiency is approximately 13 percent for the best of these cells, projecting to 16 percent with the AR coating.

Notwithstanding the Mg dopant problem, we have attempted to fabricate bottom cells using the third structure type, the one employing the GaAs-BSF layer and a graded bandgap emitter. The results have been mixed. The external quantum efficiency has shown good collection for most of these samples; an example is shown in Figure 4-4. However, the surface morphologies, such as that shown in Figure 4-5, practically preclude the possibility of successful subsequent epitaxy.

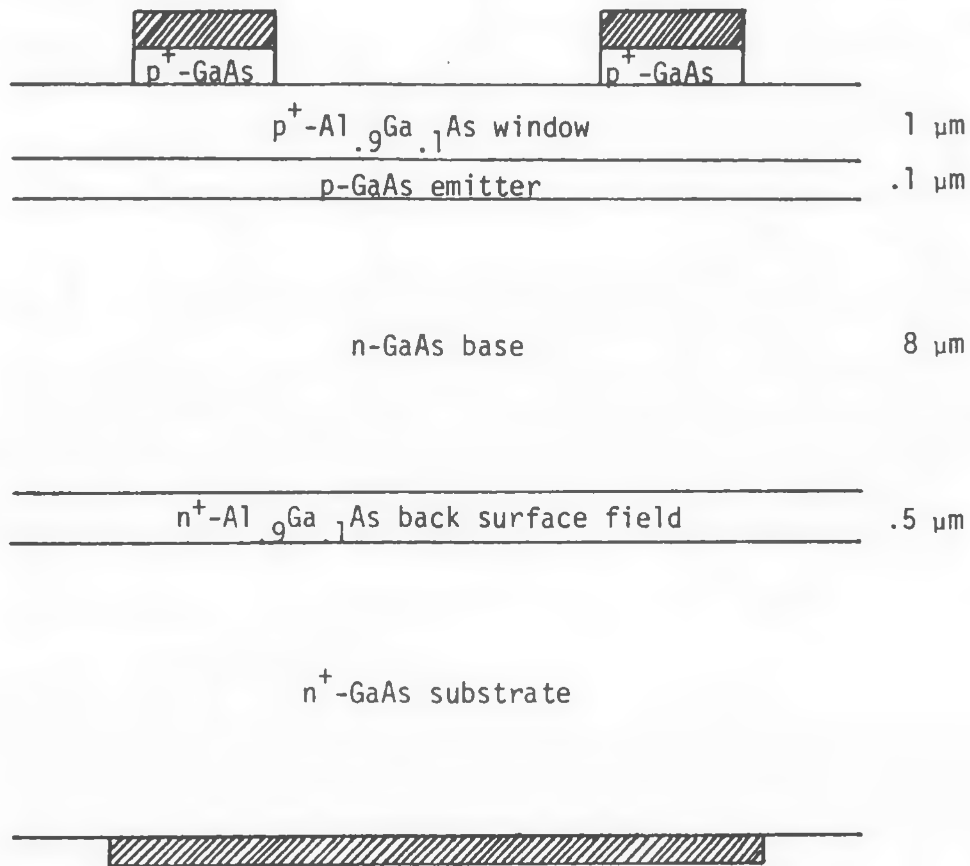


Figure 4-2. Cross section of AlGaAs-GaAs solar cell structure grown at 775°C via MO-CVD. This structure is similar to the bottom cell structure that will be used for the completed cascade structure with the patterned Ge interconnect.

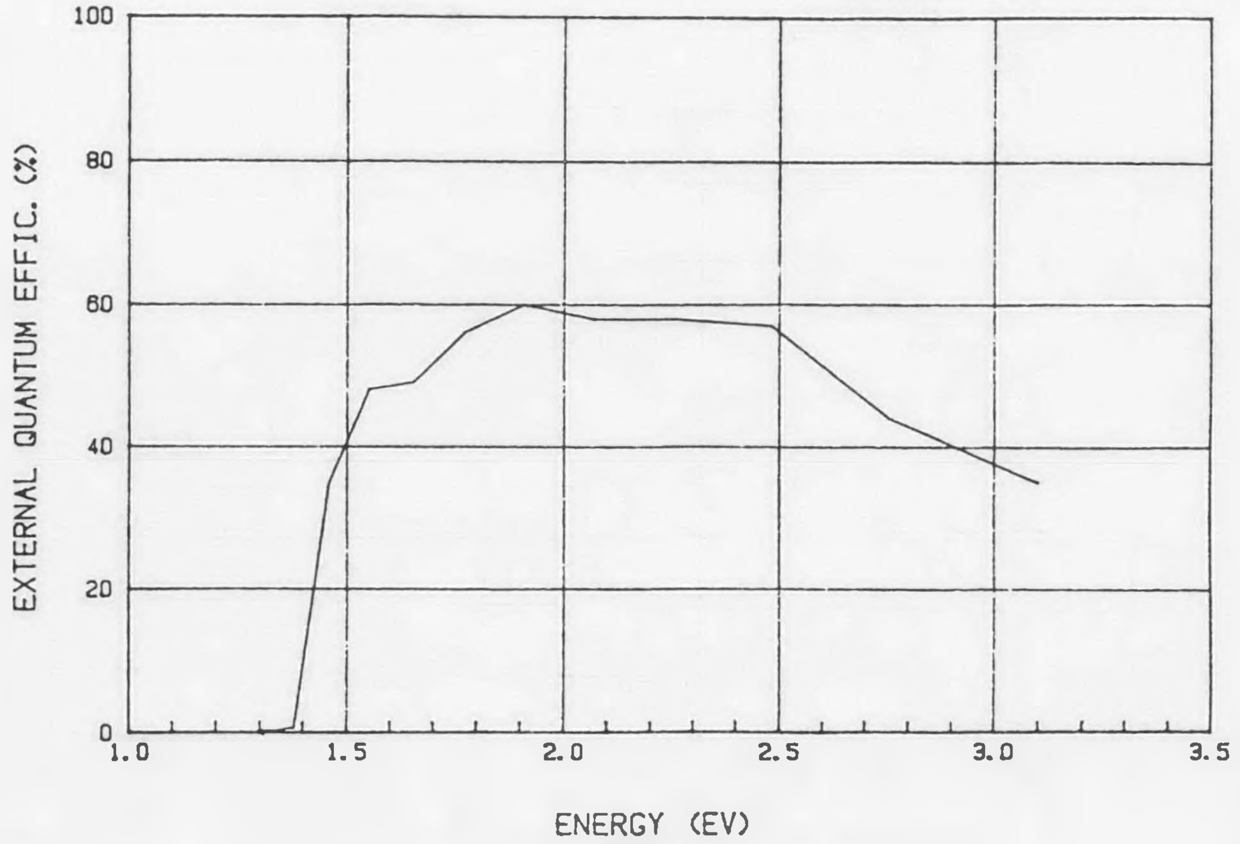


Figure 4-3. External quantum efficiency for nonoptimized, double heterojunction GaAs bottom cell without AR coating.

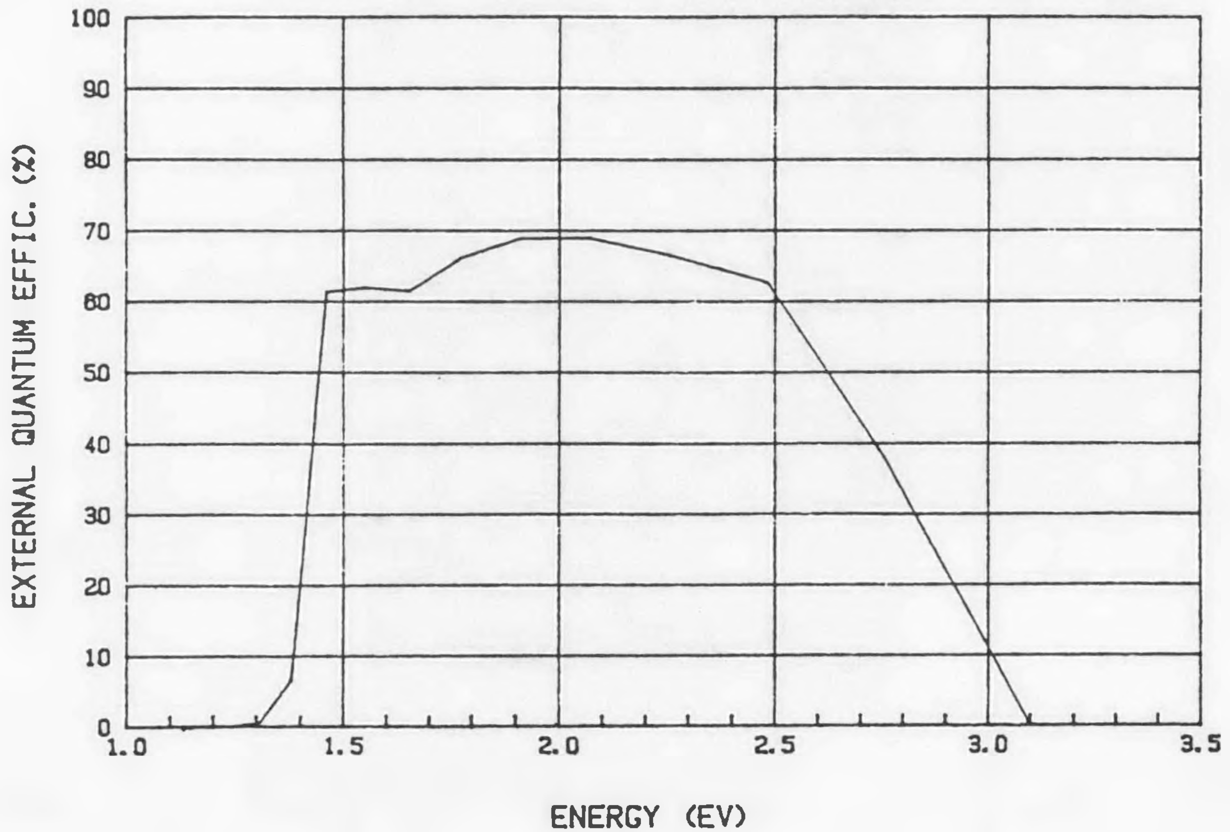


Figure 4-4. External quantum efficiency of GaAs cell without AR coating. Mg doping level in the emitter of this sample is very high resulting in poor surface morphology.

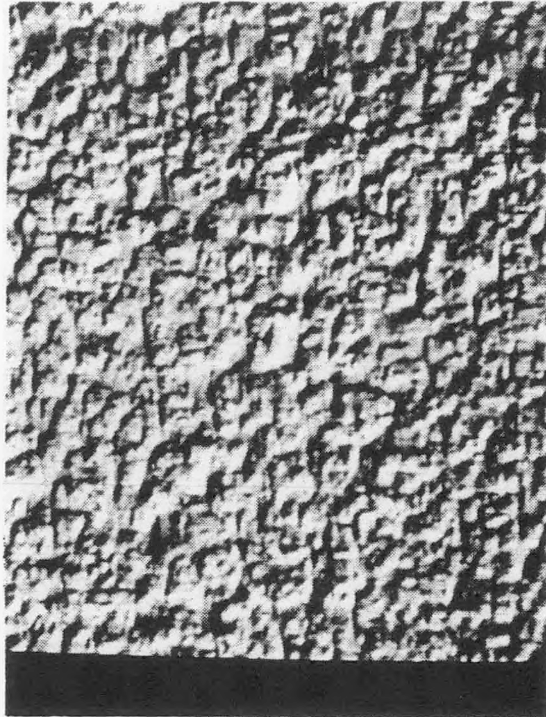


Figure 4-5. Surface morphology of GaAs layer doped very heavily using CP_2Mg as the source.

V_{oc} values are low, ranging from 0.8 to 0.9 V, and fill factors are poor. Figure 4-6 shows the dark and illuminated (1 sun AM0) I-V characteristic for a bottom cell with the heavy p-type doping.

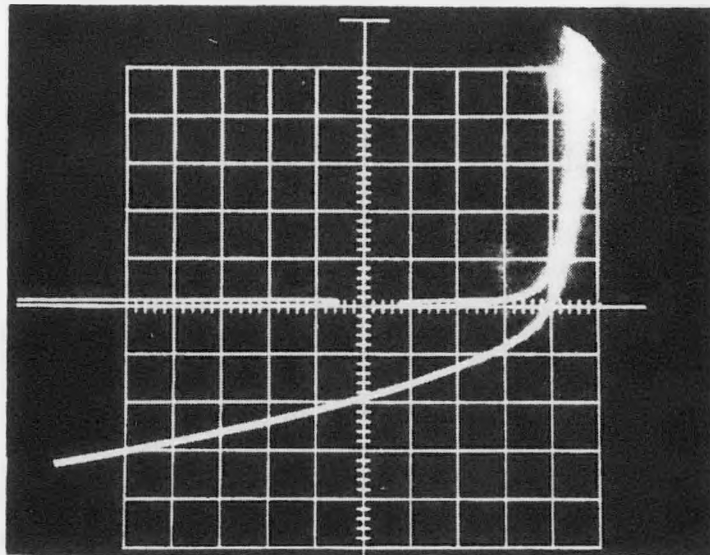
4.2 AlGaAs Material and Device Development

4.2.1 AlGaAs Growth

The AlGaAs growth is practically identical to GaAs growth. Trimethylaluminum (TMAl) is the Al source. Group V/total group III ratios are maintained near 10 as is the case for GaAs growth. Growth temperatures for AlGaAs are generally higher than those used for GaAs and have ranged between 700° and 800°C for most of the growths during this program. The elevated temperatures generally produce material with improved electrical and optical properties. In the next research phase it will be important to develop AlGaAs growth near 625°C, the temperature being planned for the bottom cell and tunnel junction; the lower growth temperatures will retard tunnel junction degradation.

4.2.2 Reinitiation of AlGaAs Growth on an AlGaAs Layer Exposed to the Atmosphere

The first major objective of this program addressed the question of the quality of $Al_xGa_{1-x}As$ (x = 0.45) alloys grown on $Al_xGa_{1-x}As$ (x = 0.45) which has been exposed to the atmosphere and assumed to have oxidized. This situation arises in the processing steps of the cascade solar cell when the Ge tunnel junction layers are patterned. The intent of the first series of experiments is to take a



Horizontal: 0.2 V/div
Vertical: 0.5 mA/div

Figure 4-6. I-V characteristics for a GaAs bottom cell with heavy p-type doping in the emitter.

"worst case" approach by purposefully exposing OM-VPE-grown AlGaAs layers to the atmosphere for one hour. This is far longer than any cascade cell processing would require. After exposure, the samples are reinserted into the reactor, along with a fresh GaAs substrate, and another AlGaAs layer is grown.

The experimental procedure is as follows:

A. Initial Growth

1. Two 100 GaAs substrates (LEC semi-insulating) were degreased, free etched for 2 minutes in 8:1:1 H_2SO_4:H_2O_2:H_2O at room temperature, and were blown dry with dry N_2.
2. The system was purged after loading the substrate.
3. The susceptor was heated from room temperature to the 775°C growth temperature (AsH_3 turned on at 400°C).
4. The susceptor was given a 6-minute soak/stabilization at 775°C.
5. Unintentionally-doped layers were grown for 20 minutes (using TMAl, TMGa, AsH_3).
6. The AsH_3 flow was maintained during cooldown until 400°C was reached.

B. AlGaAs Exposure

1. One sample was removed and stored in plastic sample box for protection from particulate matter settling on surface; a second sample was saved for characterization.

2. After one hour on lab bench at room temperature ($\sim 65^{\circ}F$) and approximately 50% RH, one sample was inserted into reactor with a fresh substrate (the GaAs substrate was prepared for epi-growth as described above).

C. Reinitiated AlGaAs Growth

1. Growth sequence was repeated as described in steps 2 through 6 above.

This procedure resulted in three samples: (1) a two-layer structure in which the second layer represents the reinitiated growth, (2) a single layer grown with the first layer of the two-layer structure, and (3) a single layer grown on a fresh substrate concurrently with the reinitiated growth. The samples were examined using photoluminescence (PL). Alloy compositions were also determined from PL emissions. The surface morphologies of the grown layers were examined using an optical microscope, and stained cross-sections were used to determine layer thickness and uniformity.

4.2.2.1 $Al_{0.15}Ga_{0.85}As$

In the first experimental sequence, an $Al_{0.15}Ga_{0.85}As$ layer was grown on a fresh GaAs substrate (sample no. OM-2-227A) and an $Al_{0.19}Ga_{0.81}As$ layer (sample no. OM-2-227B) which had been exposed as described above. There is no significant difference in the PL intensities of the near-bandedge emission from the two samples at room temperature and 80K. The full-width-at-half-maximum (FWHM) values are 33 and 35.8 meV for OM-2-227A and OM-2-227B,

respectively, for the PL emissions at room temperature.

Examination of the surfaces of the two samples reveals small hillocks on both, as well as on the surface of the layer (sample no. OM-2-226) grown simultaneously with the first layer of the two-layer structure. For the two, single-layer growths, the hillocks are about 1 μm in diameter and appear identical. The two-layer sample OM-2-227B shows both 1 μm and 2 μm hillocks, where the latter appears to be a continuation of the hillocks formed during the growth of the original layer. The hillock density (2×10^6/cm^{-2}) equals the sum of the densities of the two single layers, suggesting that hillock formation is not caused by the reinitiation of growth.

4.2.2.2 $Al_{0.45}Ga_{0.55}As$

The second sequence of samples, OM-2-228, OM-2-229A, and OM-2-229B, prepared in the same manner as the first sequence, shows identical results for $Al_{0.45}Ga_{0.55}As$ layers. OM-2-229A is a single layer grown simultaneously with OM-2-229B, the sample with reinitiated growth. Again the room temperature PL emissions for the two samples are practically the same although, as expected, considerably less intense than observed for the $Al_{0.15}Ga_{0.85}As$ layers of the previous sequence, and the FWHM values for both emissions equal 37 meV. The hillock pattern is also duplicated: OM-2-229A has small, 1−μm diameter hillocks while OM-2-229B has broader, 2−μm hillocks in addition to the smaller variety, and the hillock density (3.3×10^5 cm^{-2}) OM-2-229B is approximately equal to the sum of the densities on OM-2-228 and OM-2-229A.

4.2.2.3 $Al_{0.50}Ga_{0.50}As$

A final sequence of samples with slightly higher aluminum content was prepared. The PL emissions from both OM-2-231A (two-layer sample with reinitiated $Al_{0.49}Ga_{0.57}As$ growth) and OM-2-231B (single layer grown simultaneously with OM-2-231A) were weak but essentially equal. The hillock density at 3×10^5 cm^{-2} is lower than the previous sequences, but the hillock density pattern is the same.

4.2.2.4 Conclusions

Based on the PL results we could discern no significant differences between the layers grown on a fresh GaAs substrate and an AlGaAs layer exposed to atmosphere for one hour. The small hillocks are not attributed to the reinitiation process since they are also present on the single layers and may well be related to other causes such as substrate defects or source impurities, for example. The need for an HCl _in situ_ etch of the original substrate and the exposed layer has not been confirmed; nonetheless, our OM-VPE system has been fitted with this capability should it prove necessary.

4.2.3 AlGaAs Devices

The Mg-dopant problem has severely limited the development of AlGaAs top cells which unfortunately had not begun before the onset of the difficulties. The top cell structure is shown in Figure 4-7. The top cells which have been grown are poor. A typical dark and illuminated (1 sun AM0) I-V characteristic is shown

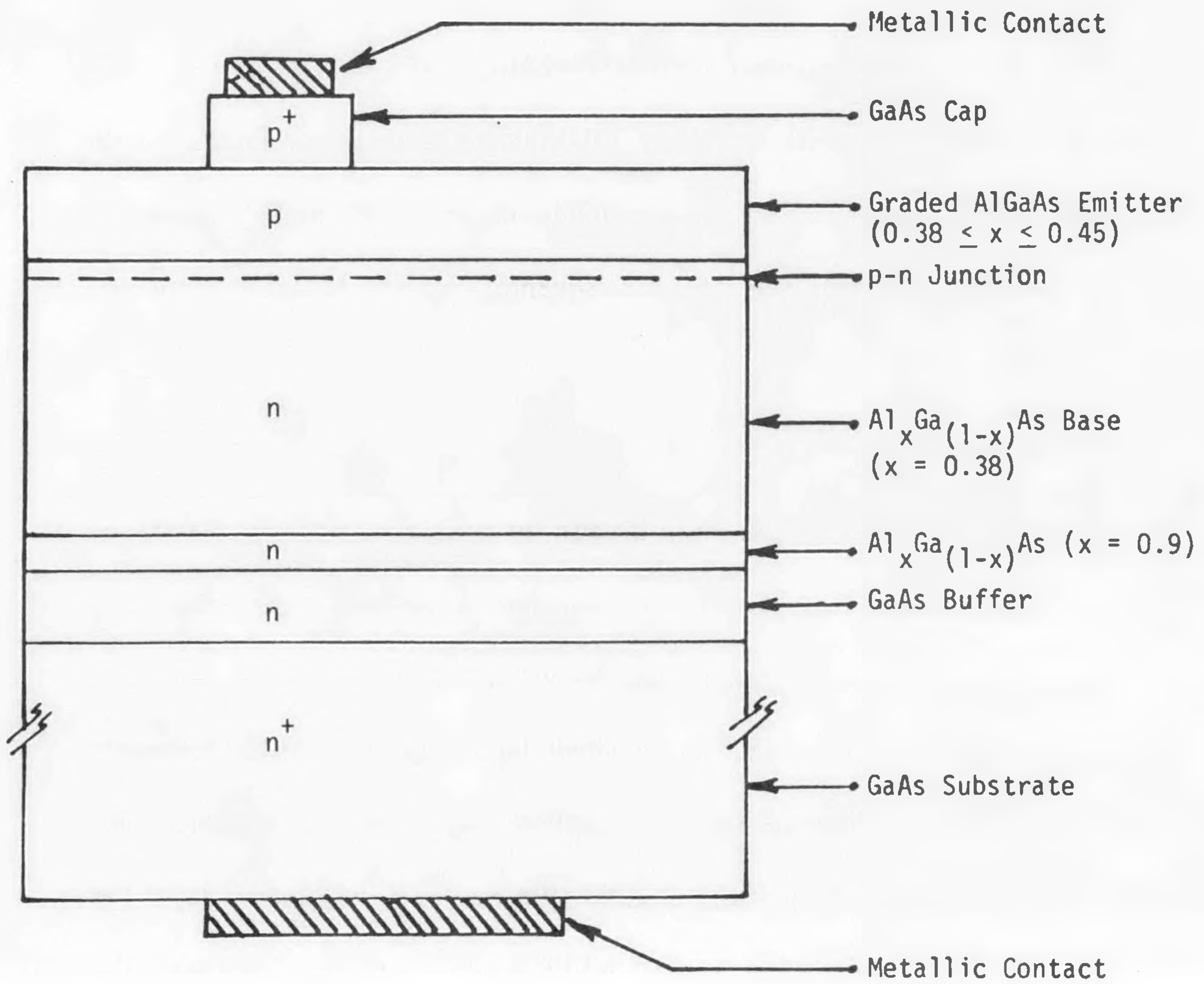
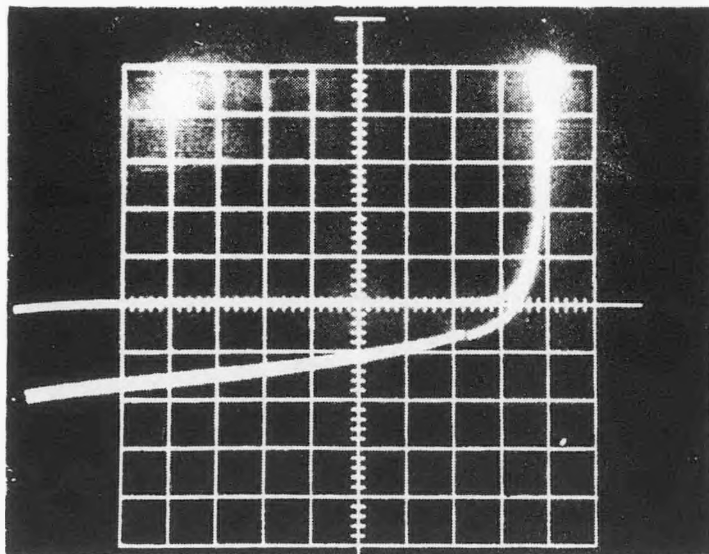


Figure 4-7. Structure of AlGaAs high bandgap junction.

in Figure 4-8 and shows a low V_{oc} and poor fill factor; J_{sc} for this cell is about 1 mA/cm^2.



Horizontal: 0.2 V/div
Vertical: 0.1 mA/div

Figure 4-8. Illuminated and dark characteristic of $Al_{0.35}Ga_{0.65}As$ top cell. Surface morphology very poor due to Mg-doping problems. $V_{oc} = 0.7$ V; $J_{sc} \sim 1$ mA/cm^2.

5.0 CASCADE CELL GROWTH AND CHARACTERIZATION

In this section, we describe the processing steps being developed for cascade cells, including the description of the mask set used to pattern tunnel junctions and to deposit metal contacts. Limited cascade cell performance data are presented.

5.1 Processing Cascade Cells

Processing multilayer cascade solar cells involves several etching and metallization steps. These are described as they occur in the fabrication sequence in the following paragraphs.

5.1.1 Tunnel Junction Etching

The bottom cell and tunnel junction will ideally be grown in a single system without exposing the structure to the atmosphere until the growth is completed. The device is then removed from the OM-VPE system. Photoresist is applied to the surface, the Ge-etch pattern is exposed, and the exposed photoresist is removed by developer. After a brief post-exposure bake to enhance the photoresist adhesion to the Ge surface, the Ge pattern is etched using $20H_2O_2$:$20H_2O$:NH_4OH. Ge etching is described in Section 3.2. The etchant oxidizes the surface of the $Al_{0.45}Ga_{0.55}As$ window layer in the area where the Ge is removed, but the oxides are easily removed by an NH_4OH:$10H_2O$ etch. The result is a shiny surface suitable for subsequent epitaxy. The photoresist covering the Ge is removed with acetone. Care must be exercised to insure the complete

removal of all organic matter from the entire surface to prevent degradation of later growths.

5.1.2 Metalization

The cleaned, patterned surface is then returned to the growth system, and the layers of the top cell are fabricated. After completion of the epitaxy, the sample is again removed from the growth system, and the surface is coated with photoresist. The grid-metallization pattern is exposed. The exposed photoresist is removed. To prepare the sample for e-beam evaporation of the metal, the GaAs, exposed by the photoresist removal, is slightly etched in $NH_4OH:2H_2O_2:40H_2O$ for 30 sec. This etching is quenched in a stop etch consisting of $NH_4OH:15H_20$ to prevent native oxide formation. The wafer is blown dry and immediately loaded into the evaporator or an electroplating fixture.

For making ohmic contact to n-type material, two different metalization schemes have been used. For contacts to n^+-GaAs substrates, 300 Å of Sn followed by 3000 to 5000 Å of Ag is evaporated onto the device. These are large area contacts and produce reproducibly ohmic behavior when sintered at 450°C for 1 to 2 minutes. For front-surface contacts, a Au(400 Å)/Ge(200 Å)/Ni(80 Å)/Au(300 Å) contact is used because lower contact resistances result. These contacts, patterned by liftoff, are alloyed at 490°C for 30 seconds and have produced measured specific contact resistances as low as

3×10^{-5} ohm$-$cm^2. After alloying, these contacts can be thickened by electrodeposition of additional Au.

Making contact to p-type GaAs is more difficult. Low resistance contacts generally require that the material be degenerately doped, preferably with hole concentrations in excess of 10^{19} cm^{-3}. Both front-grid contacts to degenerate p^+-GaAs and large-area backside contacts to substrates have been applied using electroplated Au. Electroplating usually requires 5 to 10 minutes with a current density of 3 mA/cm^2 which provides a contact 1- to 2$-\mu$m thick. The adhesion of the contacts is good, and the thick contacts yield low resistances without alloying. Specific resistances of 2×10^{-5} ohm$-$cm^2 have been measured for contacts when the material is degenerate ($>10^{19}$ cm^{-3}).

5.1.3 Contact Layer Removal

After the ohmic contacts have been applied and alloyed (if necessary), the GaAs contact layer must be removed from the surface except for the area beneath the metalization. To do this, the surface is again coated with photoresist. Using a mask which allows exposure of the entire surface except for the metal contacts, the photoresist is exposed, and the exposed portions are removed with developer. Covering the contacts prevents electrochemical etching which would otherwise severely undercut the grid finger and cause metal liftoff. The GaAs layer is quickly removed with a $20H_2O_2$:$20H_2O$:NH_4OH etch. Depending on the GaAs thickness, the etching usually takes about 45 seconds. Any oxide forming on the AlGaAs stop etch layer must be removed to prevent cracks forming in the

photoresist mask of the following step, the mesa etch; a bubbled etch of $NH_4OH:10H_2O$ removes the oxides. The oxide removal continues until the surface loses all fringe patterns. The remaining photoresist is then removed with solvents.

5.1.4 Mesa Etching

Mesa etching concludes the wet chemical processing required for cascade structures. To form mesas, the device is coated with photoresist, and the mesas are defined with an appropriate mask. After photoresist exposure and treatment with developer, the mesas are etched with $34H_2O:17HBr:Br$ for approximately 2 to 3 minutes. This etchant removes about 10 μm per minute, does not damage the photoresist, and leaves a polished surface. The remaining photoresist is removed with solvents.

5.1.5 Antireflective Coatings

Application of AR coatings concludes the processing of the cascade structure. A two-layer coating is planned. The first layer, Ta_2O_5, is deposited followed by SiO_2 deposition. E-beam will be used for the evaporations, and thicknesses will be optimized.

5.2 Grid Mask Development

Mask sets used to apply the front surface grid network on cascade cells, have been fabricated. The pattern is shown in Figure 5-1. Because of processing planned for later stages of the program, a rectangular grid geometry has been

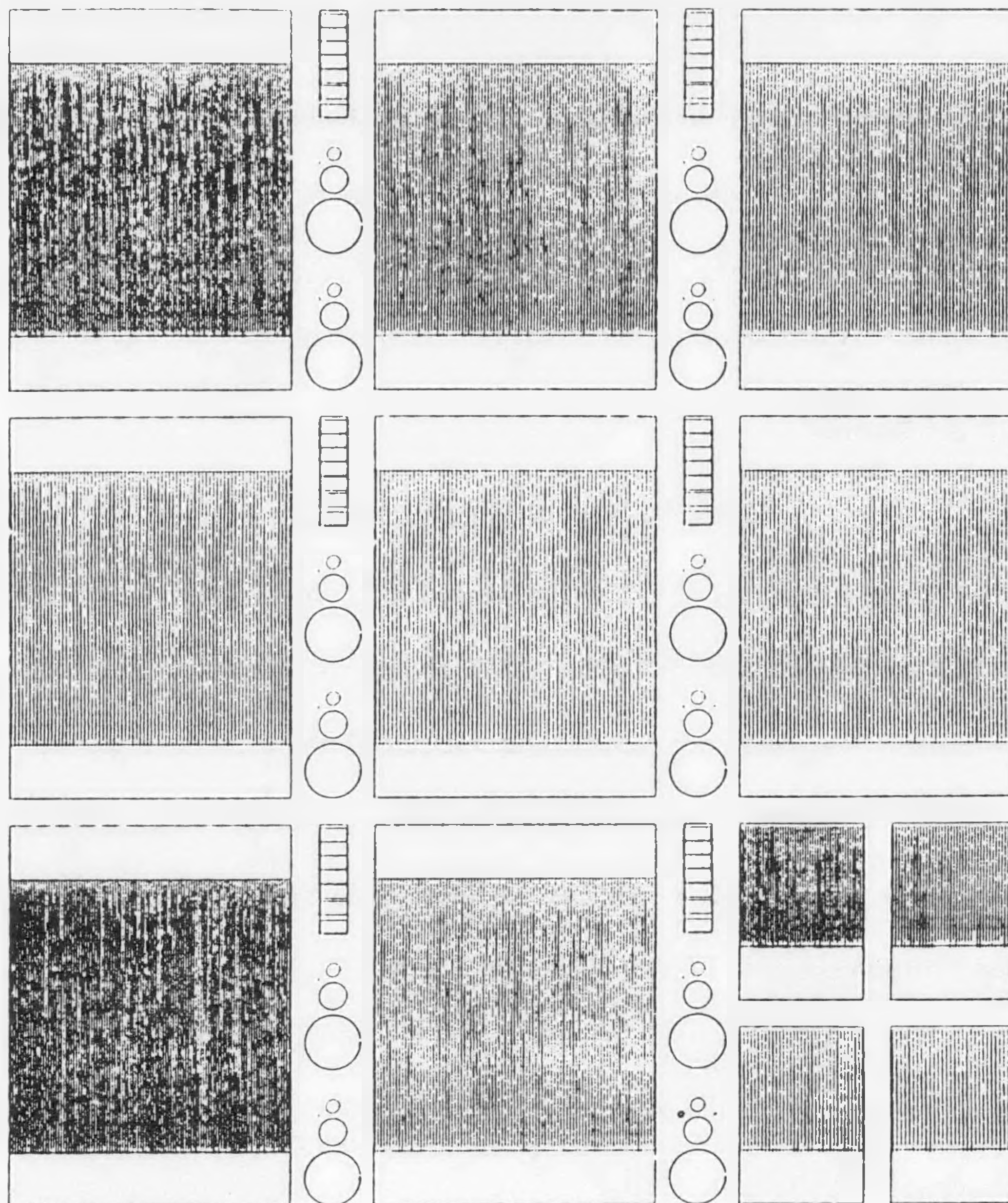


Figure 5-1. Grid mask design for cascade-cell, front-surface metalization. Mask produces 8 cells approximately 0.9 cm^2 and 4 cells approximately 0.2 cm^2. Grid finger spacing varies to accomodate differing surface sheet resistivities. Test structures are included to measure contact resistance and surface leakage effects.

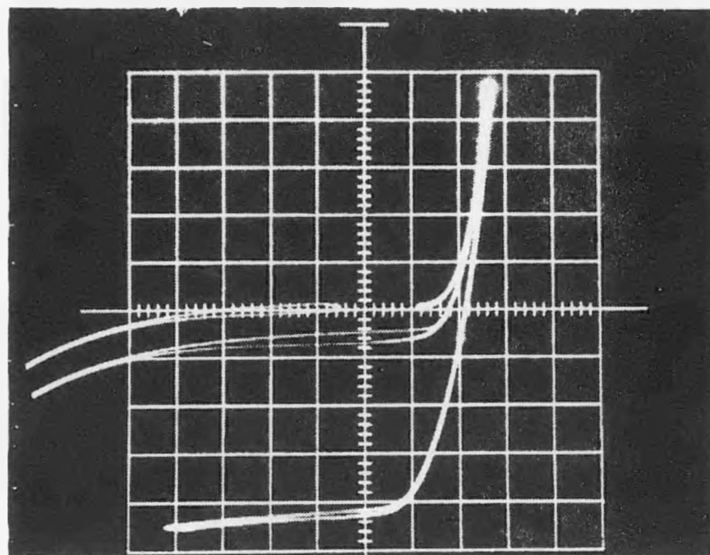
selected. The pattern contains 8 large-area and 4 small-area cells. In the areas between the cells, bar patterns are included to measure contact resistances using the transmission line model. Small mesas with variable area/perimeter ratios are also included to estimate relative contributions of bulk and perimeter leakage currents.

Two sizes of masks have been fabricated using the same general pattern. The first mask set defines active areas of 0.14 and 0.03 cm^2 for the large and small cells, respectively. The second defines active areas of 0.9 and 0.19 cm^2 for the cells.

The grid-line spacing was optimized according to the procedure described by Moore [12]. The spacing between the grid lines varies from 90 to 150 μm in 20−μm increments to accommodate surface sheet resistances ranging from 1000 to about 300 ohms per square which are anticipated to be realistic values for AlGaAs windows. Grid line widths range from 8 to 11 μm for 90- and 150−μm line spacings. Obscuration decreases from 8.8 percent at 90−μm spacing to 7.4 percent at 150−μm spacings.

5.3 Cascade Cell Performance

The dopant control problem limited the cascade cell development as it had for the top cell. Surface morphologies of both bottom and top cells have been poor. These factors limited cascade growth to a single attempted structure with surprisingly encouraging results. The I-V characteristic for this structure is shown in Figure 5-2 for dark, 1-sun (AM0), and approximately 7-sun conditions. V_{oc} is



Horizontal: 0.5 V/div
Vertical: 0.2 mA/div

Figure 5-2. Dark and illuminated I-V characteristics for patterned cascade cell - 1 sun: $J_{sc} = 0.7\ mA/cm^2$, $V_{oc} = 0.94\ V$; 7 suns: $J_{sc} = 4.7\ mA/cm^2$, $V_{oc} = 1.14\ V$.

0.94 and 1.14 V at 1 and 7 suns, respectively. J_{sc} is very low, about 1 mA/cm^2 at 1 sun, and the fill factor is poor. The voltage is the key parameter. We believe that these values, although low, do demonstrate voltage addition based on the following data. First, GaAs and AlGaAs cells were grown on fresh substrates simultaneously with the bottom and top cells, respectively, of the wafer used for the cascade growth. The I-V characteristics for these devices are shown in Figures 4-6 and 4-8. For the separately grown GaAs junction, V_{oc} is near 0.8 V, and for the AlGaAs junction, V_{oc} is about 0.7 V. These values are significantly less than the 0.94 V measured for the cascade cell. Second, the spectral response, shown in Figure 5-3, indicates collection from both junctions although the collection efficiency is very poor, especially for the bottom junction. Unfortunately, junction leakage prevented unambiguous observation of the double breakdown in the reverse I-V curve which is characteristic of the cascade structure.

Based on the observed data we conclude voltage addition has been demonstrated using the patterned Ge interconnect although a more conclusive demonstration (V_{OC} approaching 2 V, for example) is desireable. The cell quality will undoubtedly improve as the dopant problems are resolved and when lower growth temperatures are implemented for the tunnel junction growth.

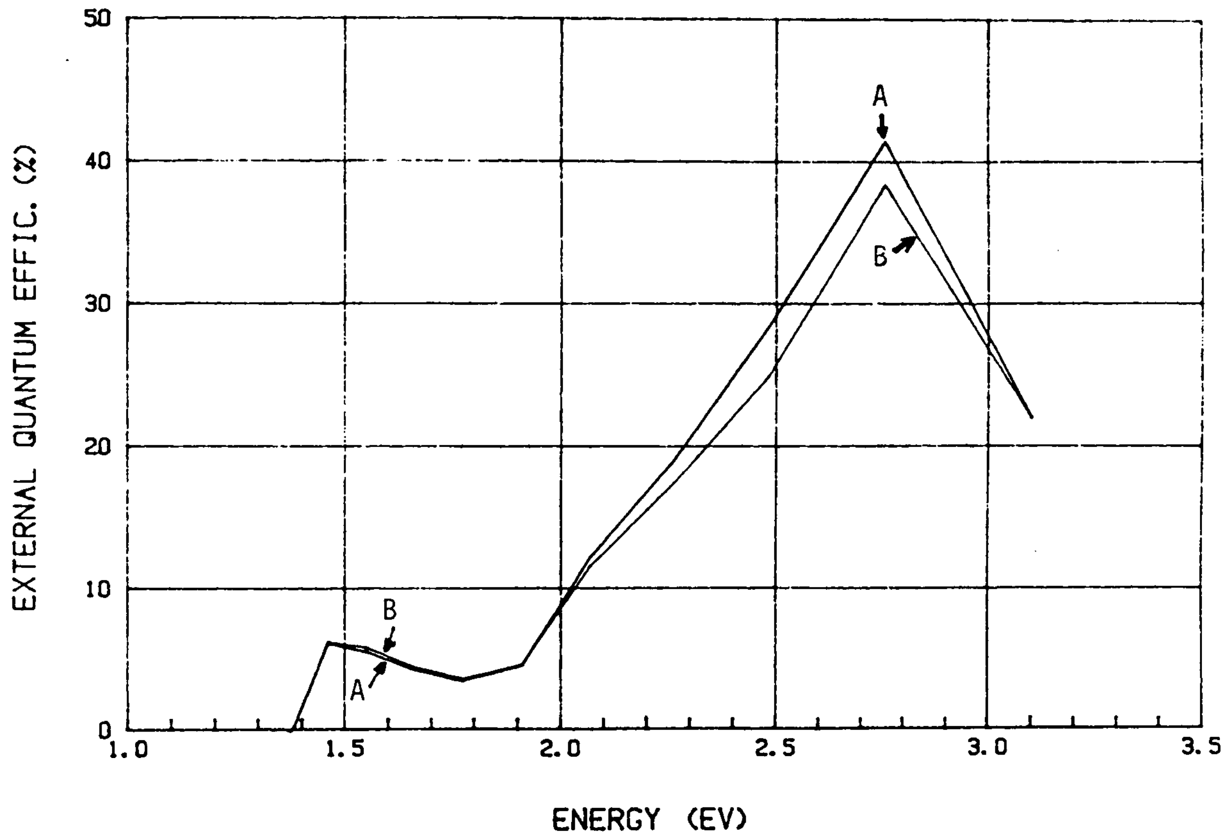


Figure 5-3. Measured external quantum efficiency for cascade cell structure: curve A measured with red bias filter, curve B measured with green bias filters. No AR coating on sample.

6.0 RECOMMENDATIONS FOR FUTURE RESEARCH

The observation of voltage addition under relatively adverse conditions is exciting and suggests a realistic opportunity for the patterned cascade structure to be improved with improved growth and processing technology. The improvements may ultimately lead to the 30 percent efficiency hoped for the cell.

Therefore, the next phase of research will focus on technology issues. Interconnect technology, using low-temperature Ge growth, will be optimized and will aim at total interconnect specific resistances of 2×10^{-4} ohm$-$cm^2 or less.

The dopant control problem using Cp_2Mg or Methyl CPMg will be corrected with further material purification, and the quality of both GaAs and AlGaAs junctions will be ascertained. Structures will be optimized. Particular attention will be paid to the development of low temperature AlGaAs growth. Growth of the AlGaAs at 625°C would be ideal since that is the temperature planned for GaAs and Ge growth, and tunnel junction degradation would be minimized.

Finally, metalizations and AR coatings need to be examined. Contacts with reproducible specific resistances of 5×10^{-5} ohm cm^2 or lower need to be standard for the cascade cell. The thicknesses of AR-coating layers need to be optimized.

If all of the above technology improvements are fruitful, performance of the first patterned cascade cell will improve dramatically, and the program objectives will probably be attained.

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