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Comparison of Metallization Systems for Thin Film Hybrid Microcircuits

By R. A. Hines and M. K. Raut

Published August 1980

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Five metallization systems were evaluated for fabricating thin film hybrid microcircuits. The titanium/palladium/electroplated gold system proved superior in terms of thermocompression bond-ability, corrosion resistance, and solderability.

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SUMMARY

Five metallization systems for thin film hybrid microcircuits (HMCs) were evaluated for their thermocompression bondability, corrosion resistance, and solderability. The chromium/palladium/gold (Cr/Pd/Au) system and the titanium/palladium/gold (Ti/Pd/Au) system with either electroplated or evaporated gold were compared to the currently used evaporated chromium/gold (Cr/Au) system. The evaporated gold systems used a gold etchant to etch unwanted gold in order to form the conductors. The electroplated gold system uses pattern plating to form the conductors. This work was motivated by the need to develop a backup or alternate thin film conductor metallization system to the Cr/evaporated Au system which has encountered seasonal decreases in manufacturing yields caused by metallization adhesion rejects at lead frame bond acceptance testing.

Fully processed thin film networks (TFNs) were used to evaluate each metallization system. Lead frames were thermocompression bonded to the monitors and peel tested. Peel strengths and failure modes were measured on over 7000 leads to evaluate the bondability and adhesion of each system and of several substrates tested on each system. The Ti/Pd/electroplated Au metallization system produced the most desirable lead frame bond results.

Each system's susceptibility to corrosion was determined by exposing both stabilized and unstabilized monitors to solutions used in fabrication and then measuring the change in interface resistance. Corrosion was significantly reduced on systems with the palladium barrier layer.

Solder-filled via resistance and solder bond strengths were measured on electroplated and evaporated gold monitors before and after temperature cycling. Electroplating deposits more gold on the via walls and produces lower initial via resistance. The solder-filled electroplated gold vias do not degrade significantly with temperature cycling. Soldered components pulled from both electroplated and evaporated gold failed at similar values.

In each evaluation, the Ti/Pd/electroplated Au system proved equal or superior to the other systems. A plating and etch line is being established to provide Bendix Kansas City with a Ti/Pd/electroplated Au capability for the production of thin film HMCs.

DISCUSSION

SCOPE AND PURPOSE

Several potential replacements for the currently used evaporated chromium/gold (Cr/Au) thin film metallization system were evaluated. Previous investigations at Bendix Kansas City and at Sandia and work reported by others in the hybrid industry influenced the selection of the systems to be studied.

Chromium/palladium/gold (Cr/Pd/Au) and titanium/palladium/gold (Ti/Pd/Au) metallization systems with either evaporated or electroplated gold were compared to the current Cr/Au system. Recurring seasonal decreases in manufacturing yields caused by metallization adhesion rejects at lead frame bond acceptance testing motivated this activity. Cost savings could result from improved yields or process simplification.

This work was part of a Bendix-Sandia team effort to find an improved metallization system for fabricating thin film networks (TFNs) at Bendix. Lead frame bondability and solderability tests proved the most informative for comparing the systems. Many other tests were conducted to develop the fabrication processes for each metallization system, but only the basic steps in the fabrication process for each system are reported.

PRIOR WORK

The initial Cr/Au development work by Sandia and Bendix showed that as a result of chromium diffusion during resistor stabilization, a prebond chromium etch was needed to remove Cr_2O_3 from the surface.[1,2] The Cr/Au process has been very successful at producing high reliability hybrids for weapon systems. No field failures caused by the thin film system have been detected during the extensive production history.

Seasonal decreases in the Cr/Au network yields have proved to be a significant problem. The yield decrease is a result of metallization adhesion problems detected during lead frame bond acceptance testing. The failures can result from the prebond chromium etch attacking the chromium "glue" layer through the porous evaporated gold, or by iodine attack during processing.[3] Yields are lowest in spring and summer when humidity is high.

Electroplated gold has been studied as a possible replacement for evaporated gold. J. W. Dini at Sandia National Laboratories Livermore (SNLL) used electrochemical measurements to quantify the reduced porosity that can be obtained with electroplated gold.[4] Bendix investigated the possibility of substituting electroplated gold for the outer 5.5 μm of a 6-μm-gold layer.[5] Although the electroplated gold may help in reducing corrosion, the Cr/electroplated Au system had infrequent but low strength ceramic-metallization failures.

The use of an intermediate palladium layer for corrosion and diffusion protection was studied by Hampy.[3] Hampy found that 0.05 μm of palladium did not sufficiently reduce the diffusion of chromium to the surface, but 0.2 μm did reduce the amount of chromium at the surface below a concentration that would interfere with thermocompression bonding. Because 0.2 μm of palladium was needed, Hampy recommended that additional testing include a Ti/Pd/Au system that also uses 0.2 μm of palladium. Ti/Pd/Au was recommended because palladium was reported to be an effective barrier for titanium diffusion[6] and because the Ti/Pd/Au system is widely used by others, including Bell Labs,[7] Western Electric,[8] and Collins Radio.[9]

ACTIVITY

Description of Conductor Metallization Systems

Three basic metallization systems were studied: Cr/Au, Cr/Pd/Au, and Ti/Pd/Au. The Cr/Au system, with evaporated chromium and gold, is the current Bendix production standard. A Cr/Au system using electroplated gold over a thin evaporated gold layer had previously been evaluated.[3,4] This study compares Cr/Pd/Au and Ti/Pd/Au (with either evaporated gold or pattern electroplated gold) to the Cr/evaporated Au system.

The conductor metallization is deposited on a 99.5 percent Al_2O_3 substrate which may include a sputtered Ta_2N coating on one side. The optional Ta_2N layer is used to form thin film resistors. Some circuits also require back side metallization and vias through the ceramic to provide a conductive path between the back side metallization and the conductors on the patterned front side. Twelve combinations of ceramic-Ta_2N-via variables were evaluated with each of the five metallization systems. The deposition steps for each system are shown in Figure 1. Although not included in this study, the Cr/Au system using electroplated gold also is shown in Figure 1.

All the evaporation was done in a single system. The energy for evaporation was supplied by an electron beam for all the evaporation, with the exception of chromium in the Cr/Au system. The production evaporation system uses a resistively heated boat for chromium evaporation. Both electron beam and resistively heated chromium were used to form the Cr/Au circuits for these tests. Chromium evaporation was done at a rate of 0.1 nm/s to a total

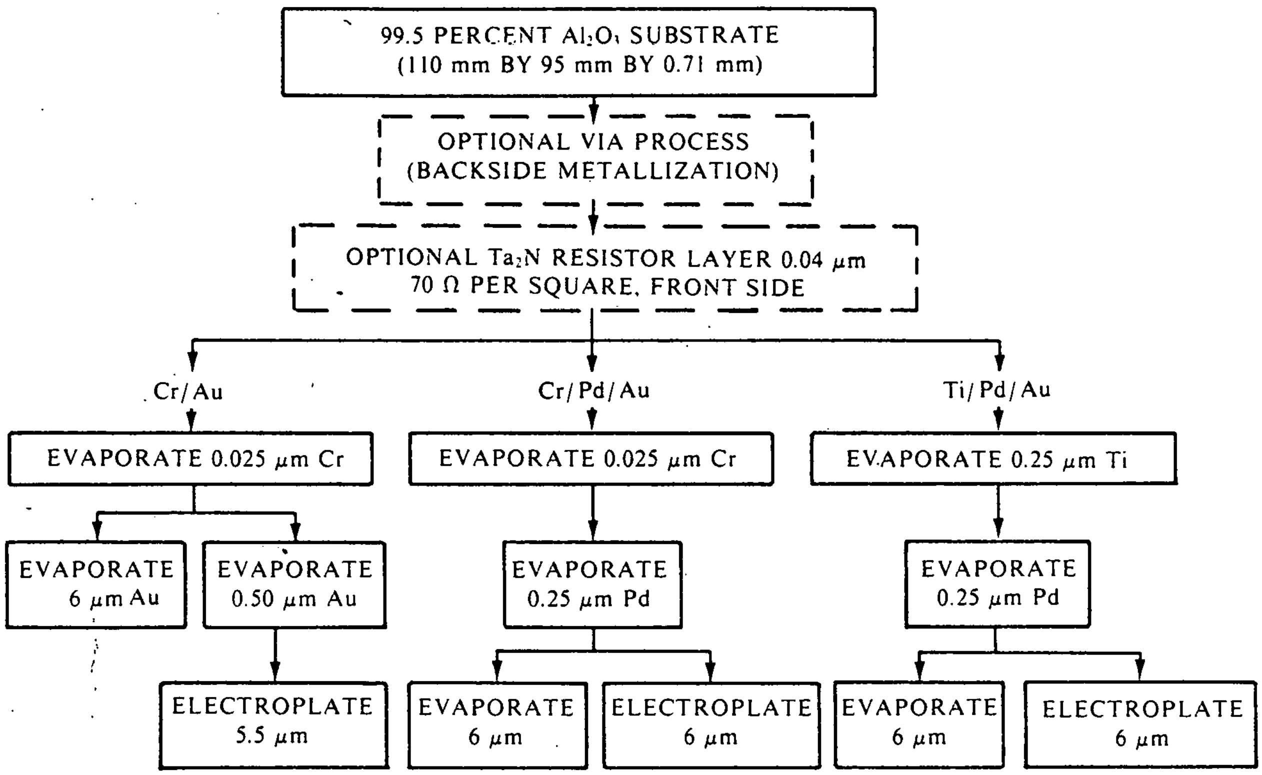


Figure 1. Description of Metallization Systems

thickness of 25 nm. Palladium and titanium were deposited at a rate of 1 nm/s; 0.25 μm of palladium and 0.2 μm of titanium were used. Gold was deposited in the evaporation system at a rate of 6 nm/s to a thickness of 6 μm. Gold was pattern plated on palladium using a gold cyanide-phosphonic acid solution to deposit a pure, soft gold at a rate of approximately 1.8 nm/s.

<u>Substrates and Metallization Combinations Tested</u>

Previous evaluations of new metallization systems and production experience indicated that lead frame bond results could vary as a function of ceramic or Ta_2N processing variables. Three types of ceramic processing and four types of Ta_2N were tested with each of five metallization systems. The three types of ceramic (all from a common vendor lot) include:

> 800°C--standard blank or nonvia ceramic processing which includes an 800°C firing operation.
>
> Via (1400°C)--standard via processing which includes coating, drilling, peening, cleaning, and a 1400°C refire operation.

1400°C--standard nonvia processing plus a 1400°C refire.

Production substrates (95 by 114 mm) containing vias are processed through several more operations than are nonvia substrates. The via substrates are coated, drilled, glass bead peened, and refired at 1400°C; an additional cleaning operation is included.

The four Ta_2N variables were Ta_2N from each of three sputtering systems and one without Ta_2N. The substrates without Ta_2N had the metallization deposited directly on the bare ceramic. These substrates are similar to the back side of production via substrates which have metallization directly on the ceramic. Two nearly identical batch sputtering systems (B I and B II), which coat six substrates per pumpdown, were used. These two systems and a larger, continuous processing machine which coats substrates at a rate of one every 40 seconds were used to sputter Ta_2N for this evaluation. All 12 combinations of ceramic-Ta_2N variables were evaluated for each of the five metallization systems. Three Cr/evaporated Au, two Cr/Pd/evaporated Au, one Cr/Pd/electroplated Au, one Ti/Pd/evaporated Au, and one Ti/Pd/electroplated Au metallization runs were made.

Circuit Fabrication

Fabrication of thin film resistor-conductor networks from the Cr/Pd/Au and the Ti/Pd/Au systems required development of several process steps that differed from the production Cr/Au process. The processing steps for each metallization system are shown in Figure 2. The initial processing steps through Ta_2N sputtering are independent of the conductor metallization system used. Processing steps from resistor photolithography through lead frame bonding are the same for all systems, with two exceptions. A prebond chromium etch using ceric ammonium nitrate (CAN) solution was used only on the Cr/Au circuits. The stripping of titanium from above the resistors can be done either directly before or after resistor photolithography. The titanium was stripped from the top of the resistors after resistor photolithography on the Ti/Pd/evaporated Au system. The titanium was removed prior to resistor photolithography on the Ti/Pd/electroplated Au system. The timing of the titanium etch had no measurable effect on the final product.

The three systems that used evaporated gold required a gold etch step to form the conductors. The conductors on the electroplated system were pattern gold plated. The pattern-plated systems have the advantage of not exposing the circuits to the iodine-containing gold etch. Pattern plating reduces gold salvage costs by eliminating the deposition of gold on the bell jar walls and on the nonconductor areas of the substrate.

PROCESS STEPS \ METALLIZATION SYSTEM	Cr/Au EVAPORATED	Cr/Pd/Au EVAPORATED	Cr/Pd/Au ELECTROPLATED	Ti/Pd/Au EVAPORATED	Ti/Pd/Au ELECTROPLATED
PHOTOLITH (DRY FILM)	X	X		X	
PHOTOLITH, PATTERN PLATE AND STRIP RESIST			X		X
Au ETCH (1.2/1 KI/I_2) AND Cr ETCH WITH CAN	X				
Au AND Pd ETCH (4/1.5 KI/I_2)		X		X	
Cr ETCH WITH CAN		X			
STRIP DRY FILM RESIST	X	X		X	
STRIP Pd (ANODIC OR $FeCl_3$)			X		X
ANODIC STRIP Cr			X		
STRIP Ti (1 PERCENT HF)					X
PHOTOPROCESS RESISTORS	X	X	X	X	X
STRIP Ti (1 PERCENT HF)				X	
LASER SCRIBE AND NUMBER	X	X	X	X	X
STABILIZE	X	X	X	X	X
PREBOND CAN ETCH	X				
CLEAN, BOND AND PULL TEST LEAD FRAMES	X	X	X	X	X

Figure 2. Process Steps

A new etch solution was developed at Sandia to etch gold and palladium in a single step. The production gold etchant used on the Cr/Au circuits is a 1.2 normal KI/1.0 normal I_2 solution. This solution did attack palladium but at a slow rate, resulting in excessive gold etch when tested as a combined gold/palladium etch.

Sandia found that increasing the concentrations to four normal KI/1.5 normal I_2 increased the palladium etch rate relative to the gold etch rate. The concentrated solution was used on the two systems containing palladium and evaporated gold with satisfactory results. Palladium was removed from the pattern-plated systems by an immersion etch in an $FeCl_3$ solution or by anodic stripping in an ethylene glycol solution containing 0.5 molar LiCl and 0.2 molar $Mg(ClO_4)_2$.

Both methods for stripping palladium in the presence of gold were satisfactory, but the $FeCl_3$ solution was faster and did not require any special equipment. The $FeCl_3$ solution will be used in the future for palladium etching.

Chromium was anodically stripped from the Cr/Pd/Au system using a 0.1 kg/L K_2CO_3 solution. Anodic stripping was used to avoid exposing the circuits to CAN etch.

Titanium was stripped from the Ti/Pd/Au system using a 1 percent HF solution. The 1 percent HF strips the titanium in about 20 seconds with no measurable damage to the Ta_2N resistors.

Mod III Monitor

The circuit pattern used exclusively for this study is shown in Figure 3. The Mod III monitor normally is used at the four corners of a production ceramic substrate (95 by 110 mm) for quality control testing. For this study, the Mod III monitor pattern was repeated 49 times on the substrate. The bond sites (19 along each 25-mm side), vias, and the control and series shorted resistor are the primary features of this monitor.

Two types of bond pads on the monitor were used. One of the 25-mm sides of the monitor contains four checkerboard bond pads and 15 standard bond sites. The standard pads are at least 1-mm square. The checkerboard pads are made up of alternately metallized and unmetallized 0.13-mm-square areas. The checkerboard pads provide half the metallized area to support lead frame bonding and were designed to force a failure at some point other than the lead to help identify the weak point in the metallization.

Lead Frame Bond Parameters and Pull Testing

Bare (unplated) copper lead frames were thermocompression bonded to the Mod III monitors and individual leads were bent 90° and pulled to failure. The load at failure and the failure mode are recorded. The lead frame contains 19 individual leads that have a rectangular cross section of 0.18 by 0.38 mm. Bare copper leads are used for adhesion acceptance testing of thin films in production and were used to collect all the lead frame bond data reported here. Gold-plated leads are used for electrical connection to production circuits and were used for some elevated temperature testing of circuits produced in this study. Although the gold-plated leads pulled were only 5 percent of the total, the trends matched those of the bare copper leads.

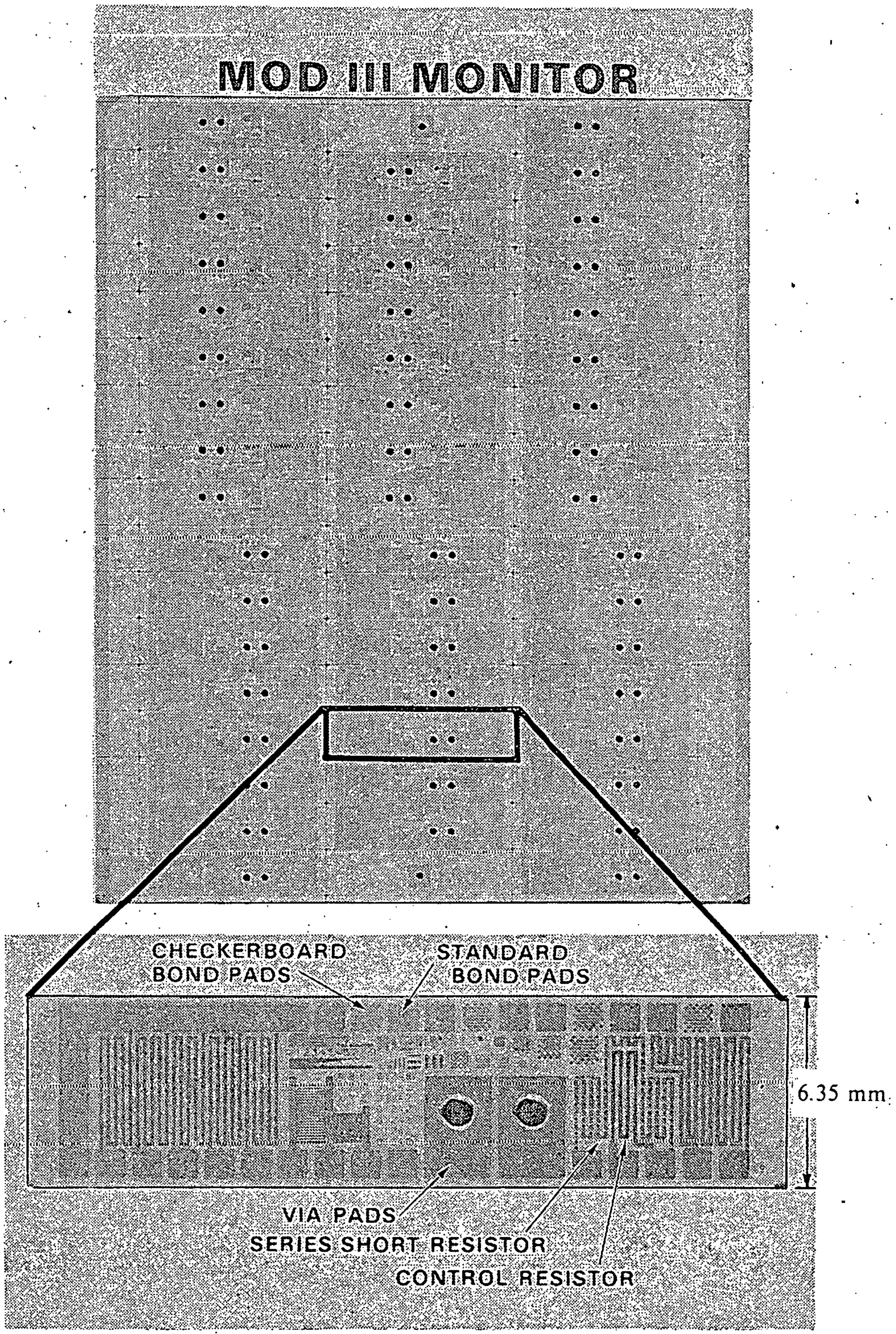


Figure 3. Mod III Monitor

The production copper lead frame bond schedule was used for all bare copper lead frame bonding. No attempt was made to optimize the bond schedule for each metallization system. Nineteen leads were bonded at a time, using a tool with a rail 0.36-mm wide at 620°C for 30 seconds with a load of 76.9 N.

The data were collected on the front side of fully processed monitors. Unpatterned mirrors and the back sides of some monitors were lead frame bonded and tested to determine if the failure modes and strength measured on the processed front sides were caused by processing or were a function of the basic metallization system. No processing problems were found, and the trends on the unprocessed mirrors and on the back side test were the same as those reported.

Over 7,000 leads were pull tested. Every other lead on the checkerboard side of each monitor tested was pulled; leads were pulled from eight standard pads and from two checkerboard pads. Five monitors from a substrate (95 by 114 mm) representing each of the 12 ceramic-Ta_2N variables were tested from each of the eight conductor metallization runs. An evaluation of gold-plated leads, back side metallization, mirrors, and elevated temperature aging increased the number of leads tested to over 7,000.

A series of interactive computer programs were written to reduce lead frame bond data. Strength and failure modes are interactively entered into a data base along with identification substrate, monitor, and lead numbers. Other programs sort the data base by any combination of substrates, monitors, or leads. The selected set of data is reduced to average, maximum, minimum, sigma, and percent of each failure mode. Other programs use the data base to display the data in graphic form.

Four basic failure modes were encountered on leads pulled from the substrates. The failure modes are shown schematically in Figure 4. Of the four failure modes, the most desirable is a Type B failure-a heel break-which is a lead failure and indicates a sound thermocompression bond and a sound metallization system. A Type C failure-a bond delamination-indicates a thermocompression bonding problem.

The other two failure modes are more direct indicators of the relative quality of the metallization system. A metallization failure (M failure), is pull out of the metallization which typically exposes some non-gold underlying metal. Type E failures are delaminations at the ceramic substrate. Historically, the E failure rate has been less than 2 percent on production Cr/Au edge monitors. Initial evaluations of electroplated gold on Cr/Au systems showed a 20 to 50 percent E failure rate.[5]

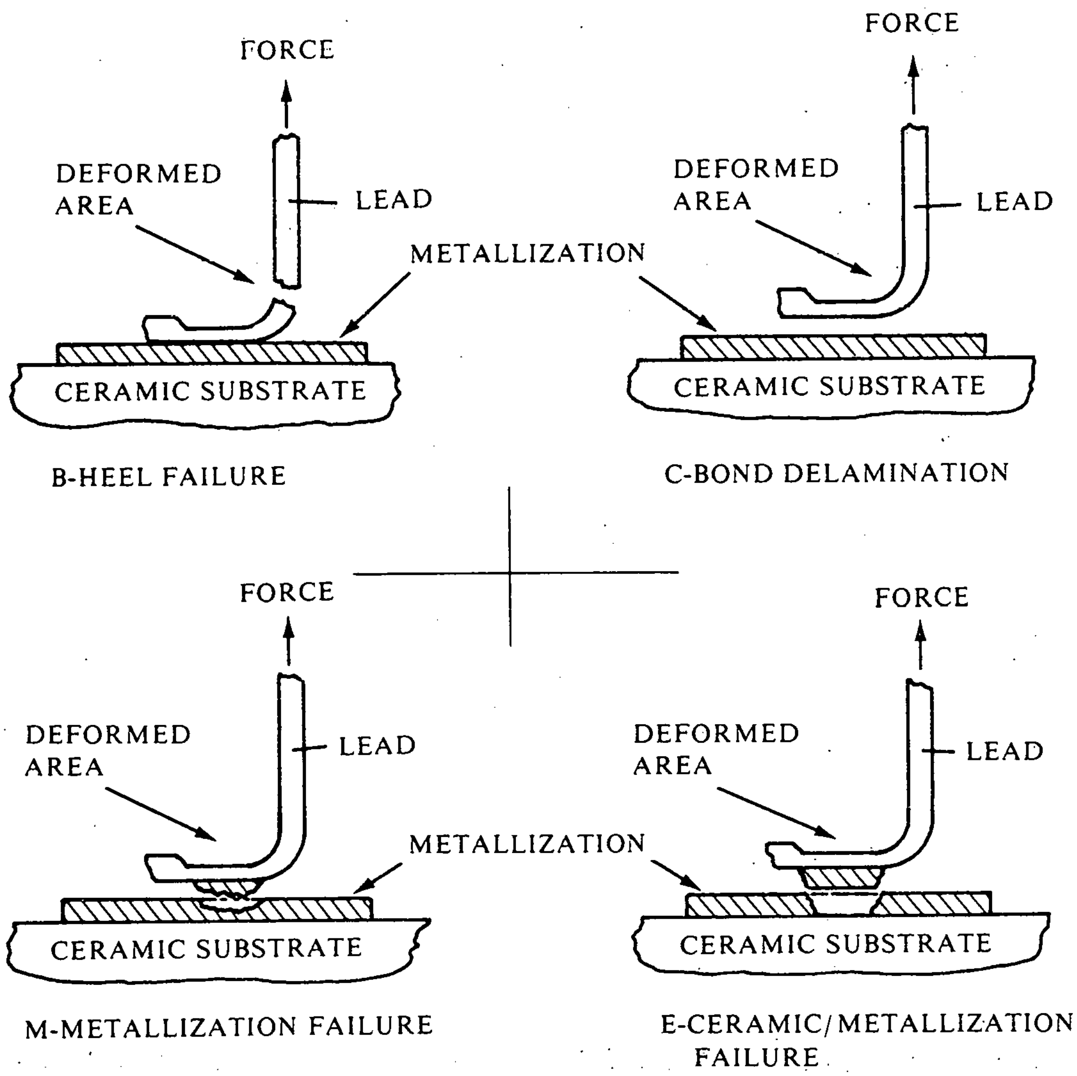


Figure 4. Lead Frame Bond Failure Classification

This study is the first to use checkerboard bond sites to help evaluate metallization systems. Because the checkerboard bond sites almost always produce non-B failures, they reveal the "weak link" in the metallization system instead of establishing that metallization is "stronger" than the lead. The stress distribution during lead frame pull testing from checkerboard pads is different from that on standard bond pads; therefore, more use will be necessary before the significance of failure modes on checkerboard pads can be determined.

Lead Frame Bond Results

Table 1 and Figures 5 through 9 display the strength and failure modes measured during lead frame pull testing. The data have

Table 1. Bond Results as a Function of Ceramic-Ta_2N Type (Standard Pads, Bare Copper Lead Frame)

	Ta_2N			No Ta_2N
	CP	B1	B2	
Ceramic (800°C)				
Leads	319	319	320	320
Average Strength (N)	12.4	14.2	13.5	6.2
Maximum (N)	18.7	19.6	19.1	18.7
Minimum (N)	0.0	5.3	0.0	0.0
Sigma (N)	4.4	1.9	2.9	7.2
Failure Mode (Percent)				
B	86.8	96.2	82.5	42.5
C	0.6	0.3	0.9	0.0
M	0.3	1.6	12.5	0.0
E	12.2	1.9	4.1	57.5
Via (1400°C)				
Leads	319	312	312	280
Average Strength (N)	13.3	14.0	13.3	5.3
Maximum (N)	14.1	14.6	19.6	18.2
Minimum (N)	0.0	0.0	0.0	0.0
Sigma (N)	3.0	2.4	3.2	6.7
Failure Mode (Percent)				
B	83.1	97.8	78.5	33.9
C	0.0	0.0	0.0	0.0
M	11.9	0.3	12.8	0.0
E	5.0	1.9	8.7	66.1

Table 1 Continued. Bond Results as a Function of Ceramic-Ta_2N Type (Standard Pads, Bare Copper Lead Frame)

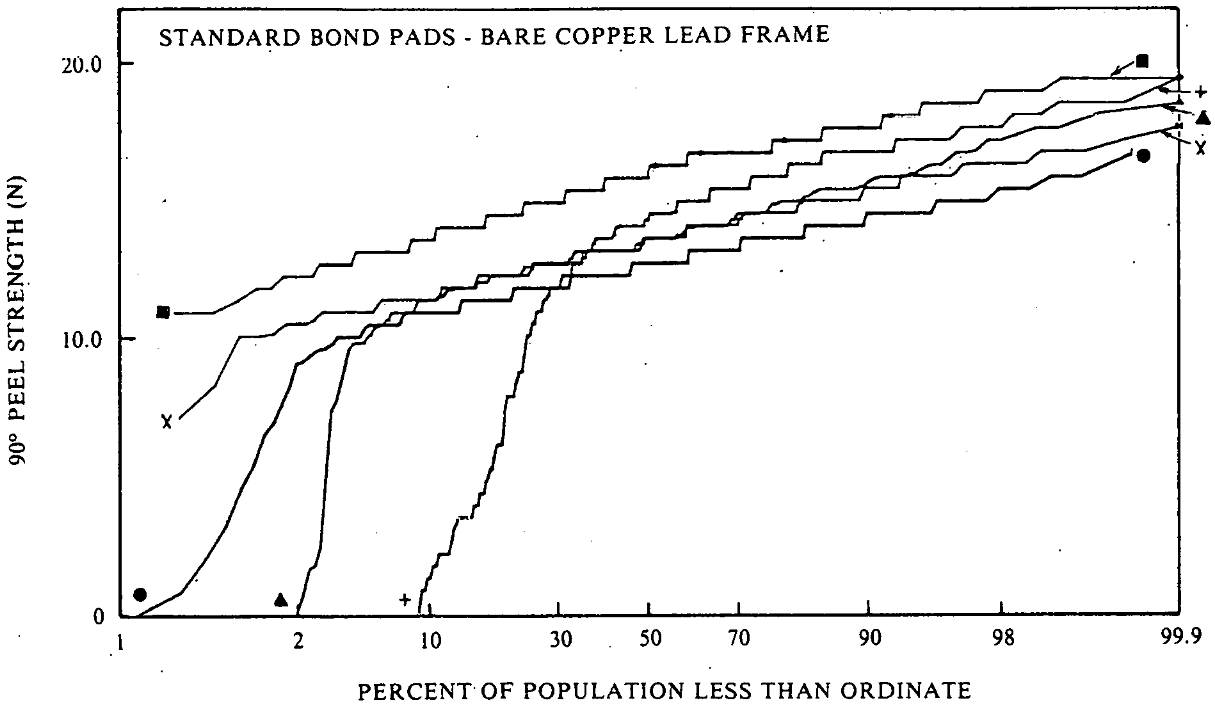
	Ta_2N			No
	CP	B1	B2	Ta_2N
Ceramic (1400°C)				
Leads	312	320	312	320
Average Strength (N)	12.9	13.7	13.4	6.5
Maximum (N)	19.6	18.7	19.1	18.7
Minimum (N)	0.0	4.4	0.0	0.0
Sigma (N)	3.0	1.9	2.6	6.9
Failure Mode (Percent)				
B	91.7	85.6	88.1	37.5
C	0.6	0.6	0.6	0.0
M	0.3	13.8	7.4	0.0
E	7.4	0.0	3.9	62.5

been organized to show trends as a function of ceramic-Ta_2N type, metallization system, and time-temperature aging for each system.

Table 1 shows lead frame bond data for each of the 12 ceramic-Ta_2N types. The data are reduced from the data from all five metallization systems. Some of the correlations between ceramic-Ta_2N type and bond results apply to only certain metallization systems. In other words, some of the metallization systems were relatively insensitive to ceramic-Ta_2N types.

From Table 1 one can see that the E failure rate is much higher and the average strengths are lower on the substrate without Ta_2N. The continuous processing machine resulted in a higher E failure rate than the two batch sputtering machines. Also, when the E failure rate is significant, some zero strength values are measured. No significant differences can be attributed to ceramic processing.

Figures 5, 6, and 7 display lead frame bond data for different sets of data in a similar format. The strength distribution for

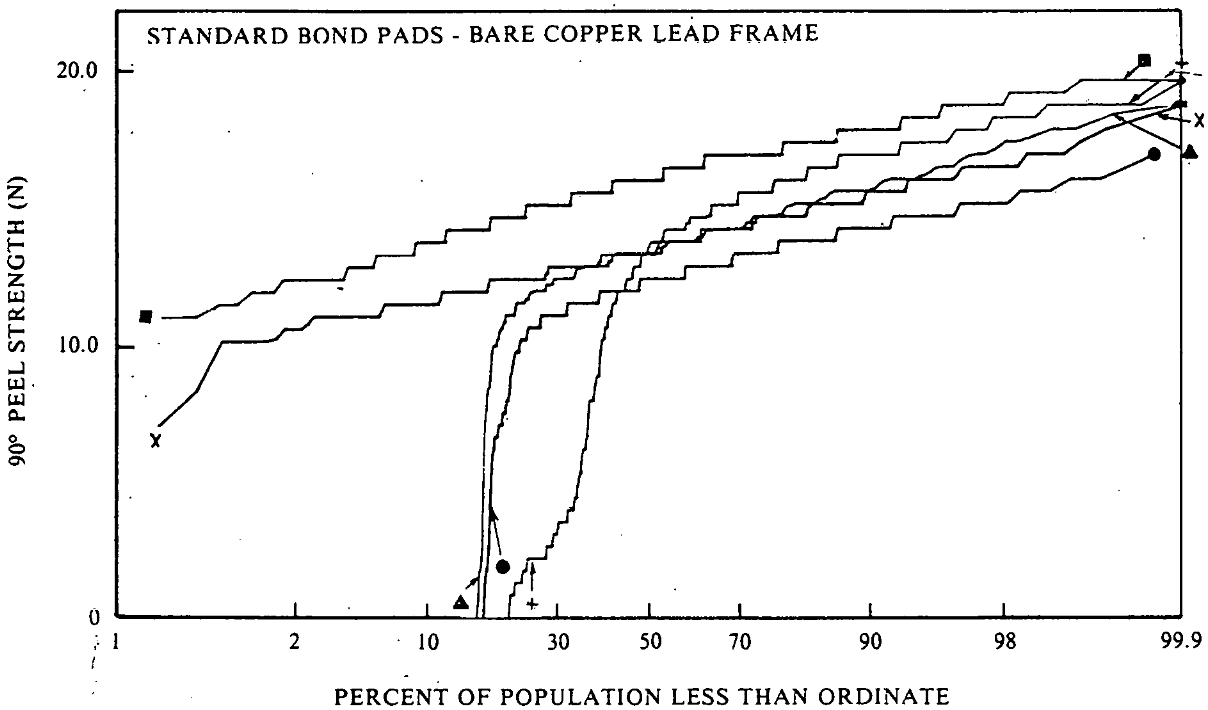


NUMBER	AVERAGE	SIGMA	PERCENT OF B	PERCENT OF C	PERCENT OF M	PERCENT OF E	SYSTEM
1398	10.4	1.7	81.3	0.46	16.70	1.58	● Cr/Au (EVAPORATED)
1232	11.1	2.8	94.9	0.40	0.00	4.74	▲ Cr/Pd/Au (EVAPORATED)
463	10.0	5.6	70.9	0.00	3.79	25.40	+ Cr/Pd/Au (ELECTROPLATED)
472	13.6	1.5	98.6	0.67	0.00	0.85	x Ti/Pd/Au (EVAPORATED)
480	16.0	1.6	98.4	0.28	0.00	0.28	■ Ti/Pd/Au (ELECTROPLATED)

Figure 5. Bond Results for 12 Substrates, Standard Pads

each metallization system is plotted. The peel strength is measured on the ordinate and a probability scale is used on the abscissa. The peel strength is plotted against the percent of population having lower strength. If the strength values are a normal distribution, the plot will be a straight line with a slope inversely proportional to sigma. Each figure also includes a table showing the number of leads in the population, the average strength at failure, the standard deviation, and the failure modes by percent for each system.

Figure 5 shows the bond data for each of the five metallization systems with data from all 12 ceramic-Ta_2N combinations included. These data are from standard bond pads. The Ti/Pd/electroplated Au system produced the best results, with an average strength of

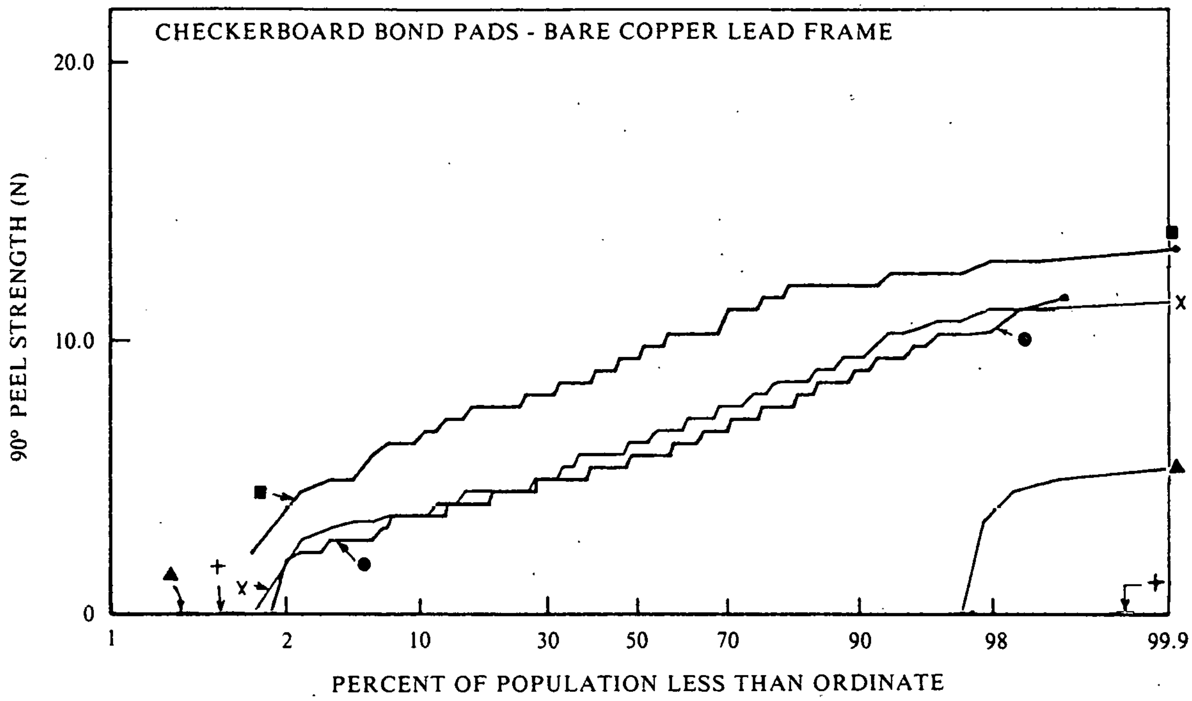


NUMBER	AVERAGE	SIGMA	PERCENT OF B	PERCENT OF C	PERCENT OF M	PERCENT OF E	SYSTEM
1398	10.4	5.0	65.8	0.36	12.90	21.00	● Cr/Au (EVAPORATED)
1232	11.1	5.4	80.6	0.32	0.00	19.10	▲ Cr/Pd/Au (EVAPORATED)
463	10.0	6.9	55.7	0.00	2.81	41.50	+ Cr/Pd/Au (ELECTROPLATED)
472	13.6	1.5	98.9	0.42	0.00	0.64	X Ti/Pd/Au (EVAPORATED)
480	16.0	1.6	99.6	0.21	0.00	0.21	■ Ti/Pd/Au (ELECTROPLATED)

Figure 6. Bond Results for Nine Ta_2N Substrates, Standard Pads

15.7 N and a B failure rate of 99.6 percent. Data from the two Ti/Pd/Au systems closely follow a straight line with no zero-strength failures. The other three systems have from 15 to 20 percent zero-strength failures.

Figure 6 displays a subset of the data given in Figure 5, including only the data from the nine ceramic-Ta_2N combinations containing Ta_2N. Most of the zero strength failures on the Cr/evaporated Au and the Cr/Pd/evaporated Au system occurred on substrates that contained no Ta_2N. The Cr/Pd/electroplated Au system still has a high percent of E failures and zero strength E failures that were not isolated to a particular set of ceramic-Ta_2N combinations. Data from both Ti/Pd/Au systems are nearly identical to the data displayed in Figure 5. The Ti/Pd/Au



NUMBER	AVERAGE	SIGMA	PERCENT OF B	PERCENT OF C	PERCENT OF M	PERCENT OF E	SYSTEM
270	6.0	2.1	0.37	81.10	17.00	1.48	● Cr/Au (EVAPORATED)
248	0.1	0.8	0.00	0.00	0.00	100.00	▲ Cr/Pd/Au (EVAPORATED)
86	0.0	0.0	0.00	0.00	98.80	1.16	+ Cr/Pd/Au (ELECTROPLATED)
88	6.5	2.3	0.00	30.00	34.10	36.40	x Ti/Pd/Au (EVAPORATED)
80	9.5	2.2	17.80	8.89	2.22	71.10	■ Ti/Pd/Au (ELECTROPLATED)

Figure 7. Bond Results for Nine Ta_2N Substrates, Checkerboard Pads

systems work equally well on bare ceramic or on Ta_2N. In general, the Ti/Pd/Au bond results showed no correlation to ceramic-Ta_2N variables.

Figure 7 displays the checkerboard bond data from the monitors used for Figure 6. Again, data from the substrates without Ta_2N have been omitted. The checkerboard data tend to exaggerate the differences between the systems. The two Cr/Pd/Au systems show nearly 100 percent zero strength failures. The Ti/Pd/electroplated Au system yielded the best results, with an average strength of 9.5 N and a B failure rate of 17.8 percent. Subsequent tests on other Ti/Pd/electroplated Au monitors have produced approximately 80 percent B failures on checkerboard bond pads.

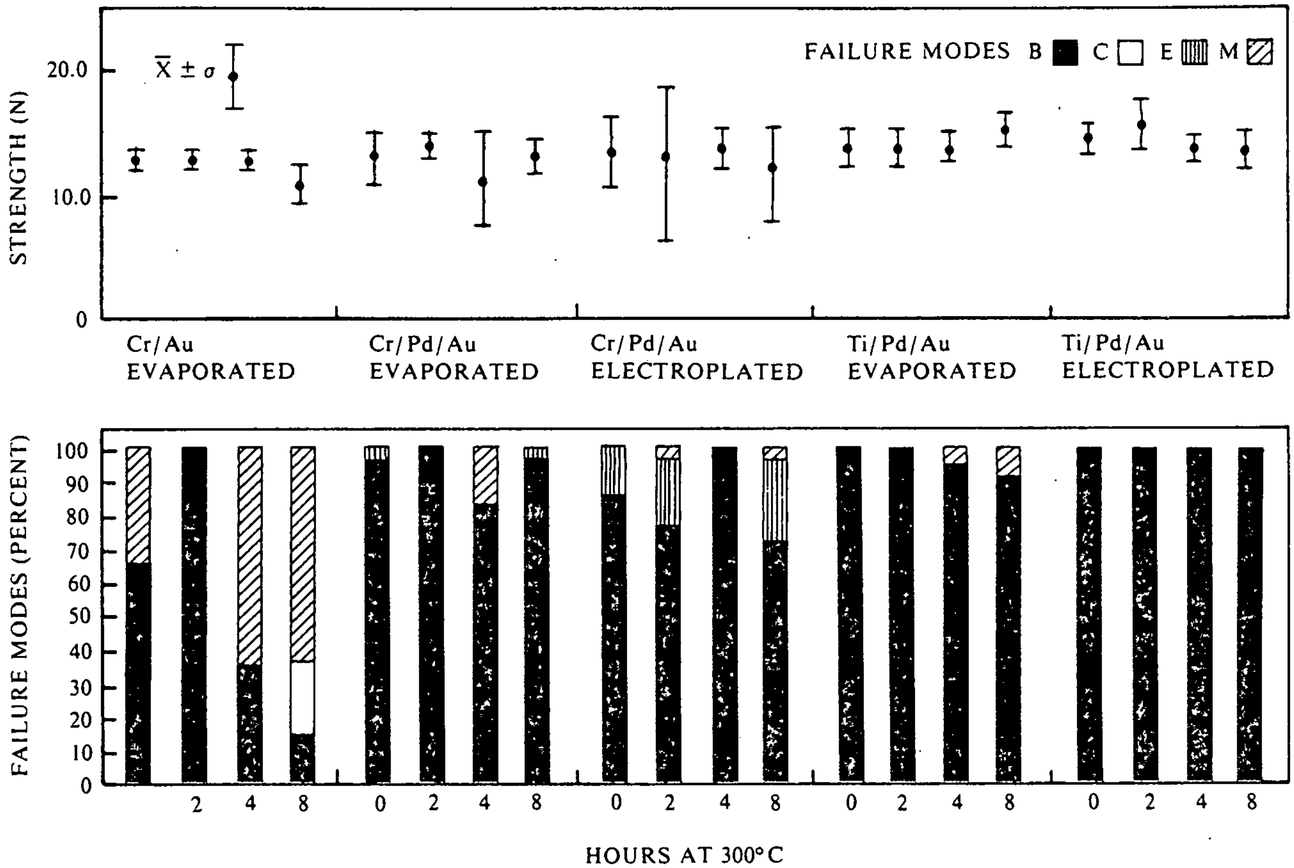


Figure 8. Bond Results for 300°C Aging, Standard Pads

The standard Bendix process for fabricating TFNs containing Ta_2N resistors includes a 2-hour bake in air at 300°C to oxidize the Ta_2N and stabilize the resistor values. The data mentioned so far were collected on stabilized monitors.

In the Cr/Au system, the stabilization results in the diffusion of chromium to the surface, which necessitates a prebond chromium etch step to restore bondability. Monitors from each system were aged at 300°C to determine how sensitive the systems were to elevated temperature aging. Baking at 300°C was conducted for 0, 2, 4, and 8 hours. The data are displayed in Figures 8 and 9.

Figure 8 displays the lead frame bond data for standard bond pads. The strength data showed no clear trend as a function of time at 300°C. Most of the systems, particularly the Cr/Au system, showed a decrease in the number of B failures as the time at 300°C is increased. The Ti/Pd/electroplated Au system was the only one to produce 100 percent B failures at all times.

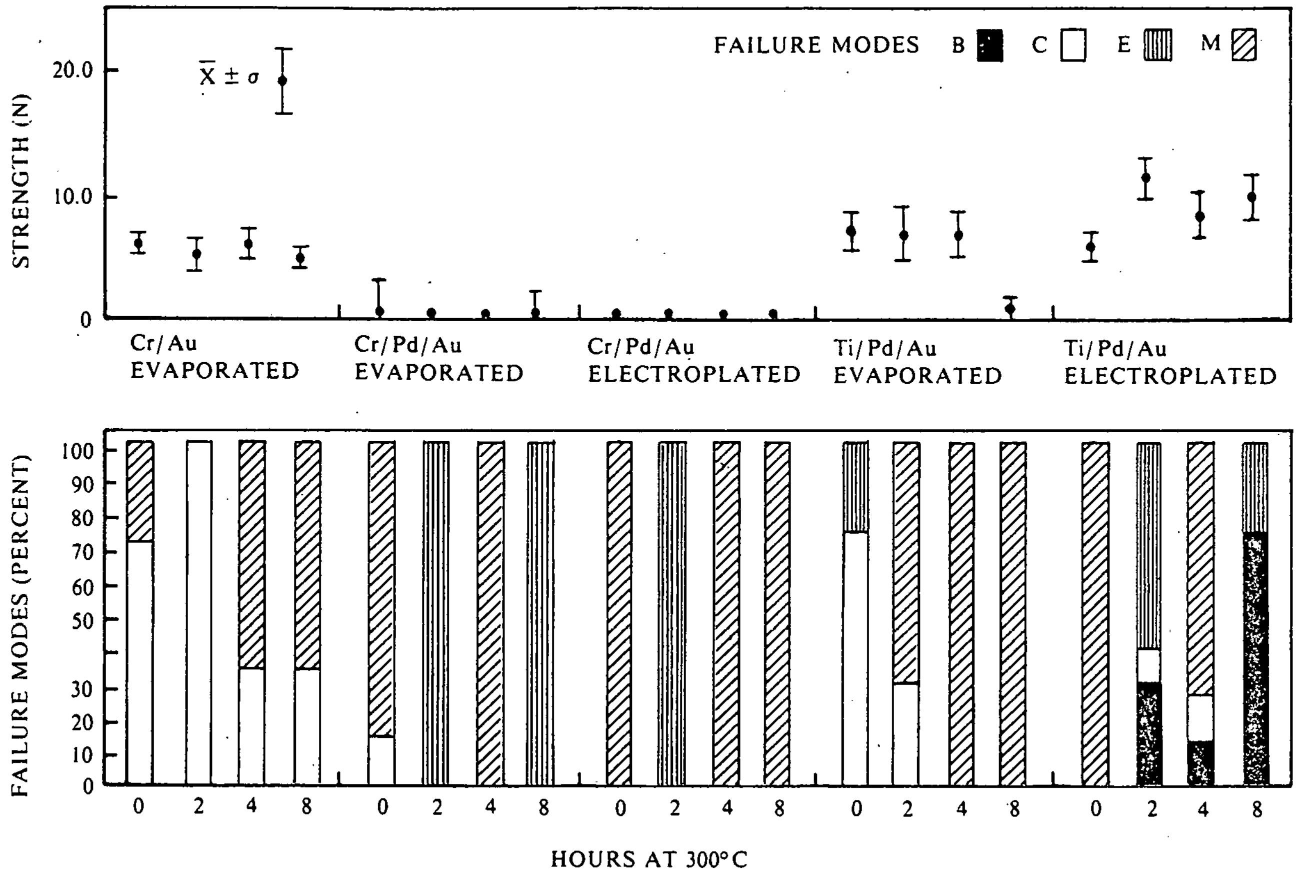


Figure 9. Bond Results for 300°C Aging, Checkerboard Pads

Figure 9 displays checkerboard data from the same monitors. Again, the checkerboards tend to exaggerate the differences between the systems. The only B failures measured were on the Ti/Pd/electroplated Au system.

Corrosion Susceptibility

This study included both vapor and immersion exposure to the corrosives. For the vapor exposure, the networks were kept in petri dishes with lids, which were enclosed in ground glass joint weighing bottles containing the corrosives. Care was taken to ensure the monitors did not contact the solutions. For the immersion exposure, the networks were immersed in a corrosive, rinsed in deionized water for 1 minute, and blown dry with dry nitrogen. The Ta_2N/conductor interface resistance of the network was measured before and after exposure. The detailed procedures for each exposure are shown in Figures 10 and 11.

The pattern used for measuring the interface resistance between the conductive and resistive (Ta_2N) layers is shown in Figure 12.

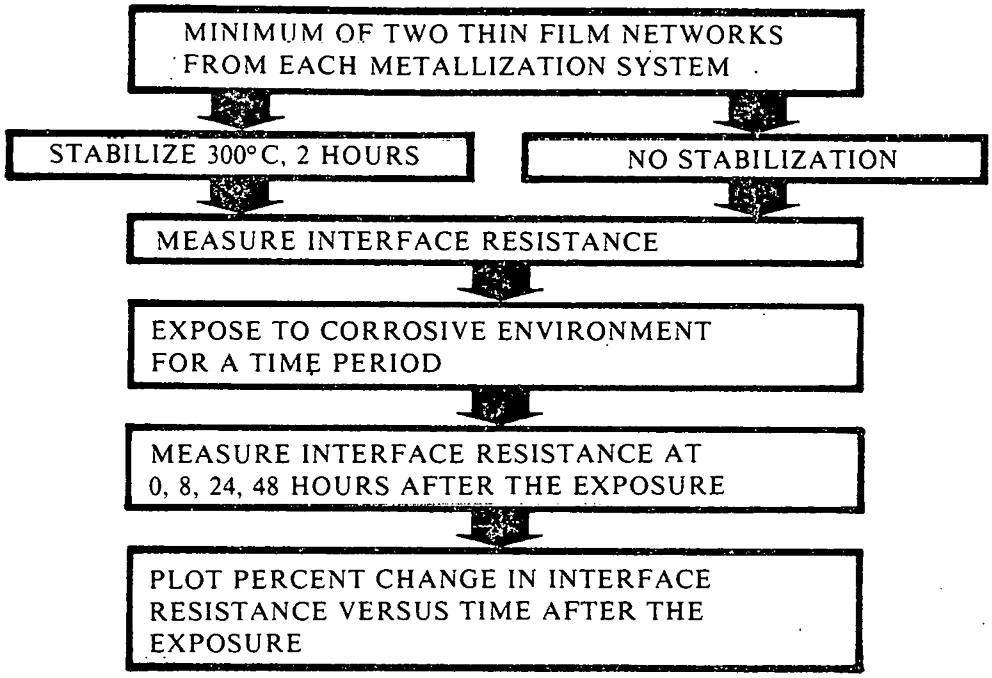


Figure 10. Vapor Exposure Test

The pattern includes two resistors of equal design value: (1) a control resistor in a typical meandering configuration and (2) a series of small resistors totaling the same value as the control resistor. Both resistor patterns contain 98 squares of resistor material. The control has two interfaces, and the series shorted has 196 interfaces. Both resistors are 0.12-mm wide, large enough for good photolithography processing but sufficiently narrow so that interface resistance (an inverse function of width) can be significant. For a good typical film, interface resistance would be about 28 Ω for the control and 2800 Ω for the series shorted, or 0.28 and 28 percent, respectively, of the total value of the resistors.

The corrosives used during the vapor exposure study were gold etchant--KI/I_2 solution, chromium etchant--CAN-nitric acid solution, tantalum etchant--hydrofluoric-nitric acid solution, and titanium/palladium etchant--ferric chloride-hydrochloric and hydrofluoric acid solution. For the immersion studies, the corrosives used were palladium etchant, chromium etchant, and water. Chemical composition of each etchant is shown in Table 2.

The change in interface resistance after the exposure was plotted against time. Typical plots are shown in Figures 13 and 14. Table 3 shows the change in interface resistance for various metallization systems. The study showed that Cr/evaporated Au

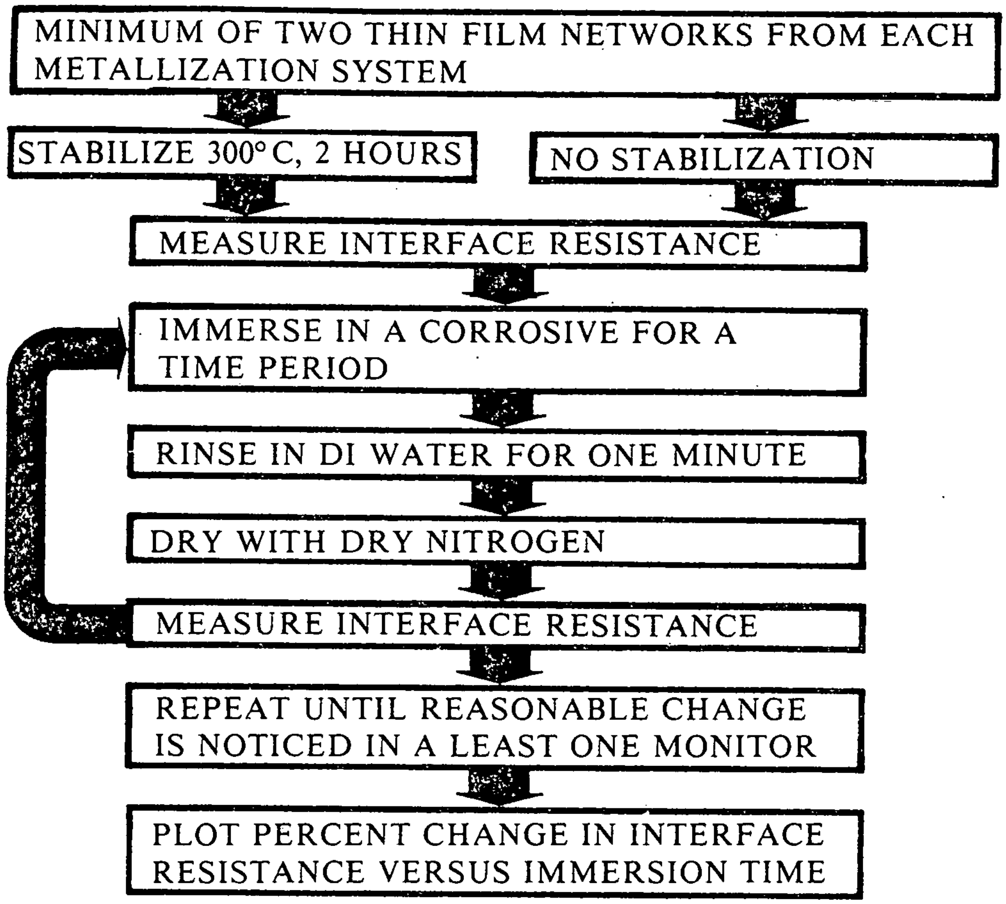


Figure 11. Immersion Exposure Test

was much more susceptible to the corrosives than were the tri-metal systems. The highest corrosion occurred when the Cr/Au system was exposed to the gold etch vapors.

Solderability

A thin film metallization system used in manufacturing HMCs must be solderable and withstand specific environmental tests after assembly. Lead-50 indium solder is used at Bendix to solder capacitors and other components to Cr/evaporated Au thin films.

The solderability of Pb-50In solder was compared between Cr/Au and Cr/Pd/pattern-plated gold. Seven 95- by 114-mm substrates with vias (five with electroplated gold and two with evaporated gold) were used for the study. Vias are metallized holes which act as intraconnections between the front side of the conductor-resistor network and the back side of the ground phase. Soldered TFNs were subjected to three different time and temperature

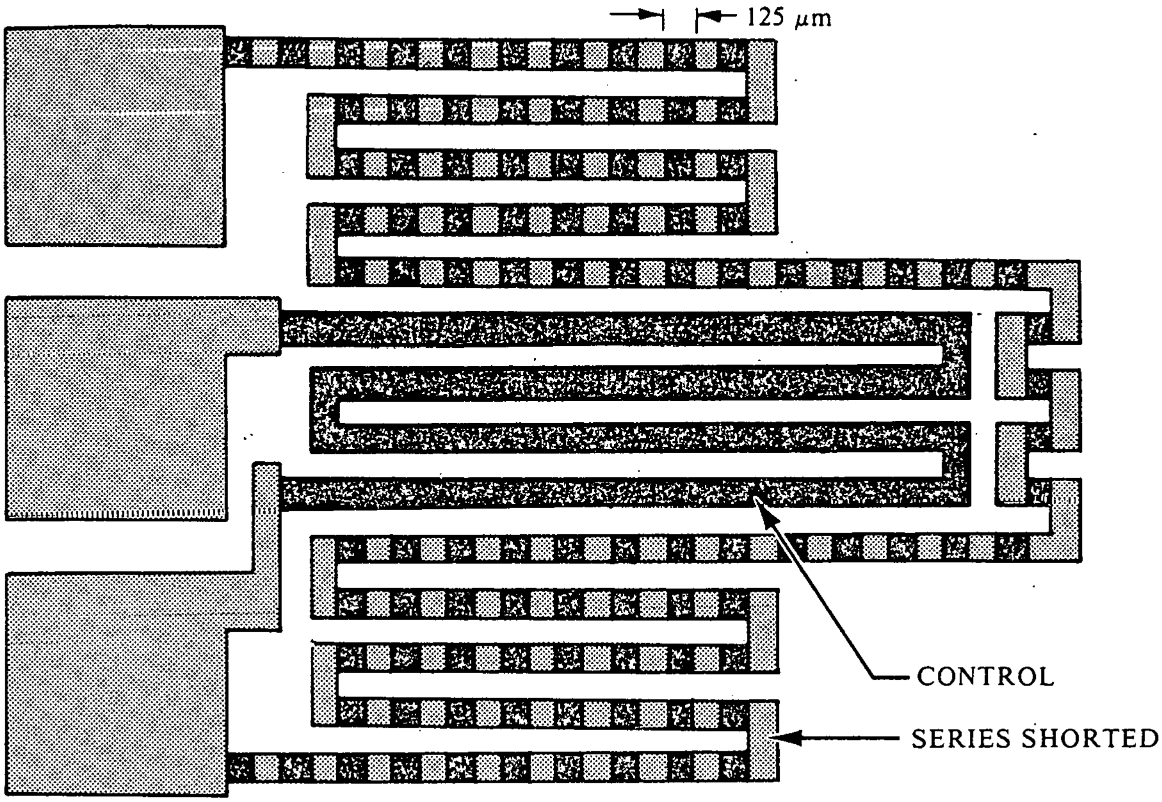


Figure 12. Interface Resistance Pattern Used to Evaluate Corrosion Susceptibility

schedules. Visual examination, via resistance, and capacitor shear strength were means of evaluating the solder joints (Figure 15).

Solder Test I (Figure 16) included extensive vacuum baking and temperature cycling. The results are shown in Table 4 and in Figures 17 through 21. Solder Test II simulated the conditions to which a soldered product is exposed during production, along with extended periods of temperature exposure. The procedure for this test is shown in Figure 22, and the results are shown in Table 5 and Figure 23. Solder Test III was an extended baking cycle. The samples were baked four times at 125°C for 16 hours (Figure 24). The results are shown in Table 6 and Figure 25.

Via resistance change between pre- and post-soldering and during temperature cycling was greater with evaporated gold metallized vias than with electroplated gold metallized vias. All three tests showed that under normal conditions the shear strength of capacitors soldered on electroplated gold was equivalent to that

Table 2. Composition of Corrosive Solutions

Corrosive Etchant	Composition
Au	1.5 NI_2 + 4.0 N KI
Cr	0.164 kg $(NH_4)_2$ Ce $(NO_3)_6$ + 0.135 L HNO_3 Per L Solution
Ta	3.4 Parts HF:1 Part HNO_3:10 Parts CH_3CO_2H
Pd	0.5 M LiCl + 0.2M $Mg(ClO_4)_2$ in Ethylene Glycol
Ti/Pd	0.10 kg $FeCl_3$ + 0.5 L HCl 0.05 L HF + 0.50 L H_2O

of evaporated gold. After the substrates had been exposed to excessive temperature cycles, however, the soldered capacitors on evaporated gold had low shear strength failures at metallization-solder interfaces.

ACCOMPLISHMENTS

Five metallization systems were evaluated for the fabrication of thin film HMCs. Based on lead frame bond data, corrosion susceptibility, and solderability, the best of the five metallization systems is Ti/Pd/electroplated Au, followed by Ti/Pd/evaporated Au, Cr/evaporated Au, Cr/Pd/evaporated Au, and Cr/Pd/electroplated Au.

The Ti/Pd/electroplated Au system produced the best overall lead frame bond results with the highest average strength and nearly 100 percent heel failures. The checkerboard lead frame bond data on the Ti/Pd/electroplated Au system indicated a considerable margin of safety. Leads bonded to checkerboard pads (only half the metallization area to support the bond) failed at strengths sufficient to pass the Cr/Au specification for standard bond pads.

The thermocompression lead frame bond results on the Ti/Pd/Au systems showed no dependence on ceramic or Ta_2N variables. The other systems produced poor results when deposited on bare ceramic. Of the three sputtering machines tested, the continuous processing machine produced a higher percentage of E failures. When E failures were encountered, some zero strength E failures were measured. No correlation was found between bond results and the three types of ceramic processing.

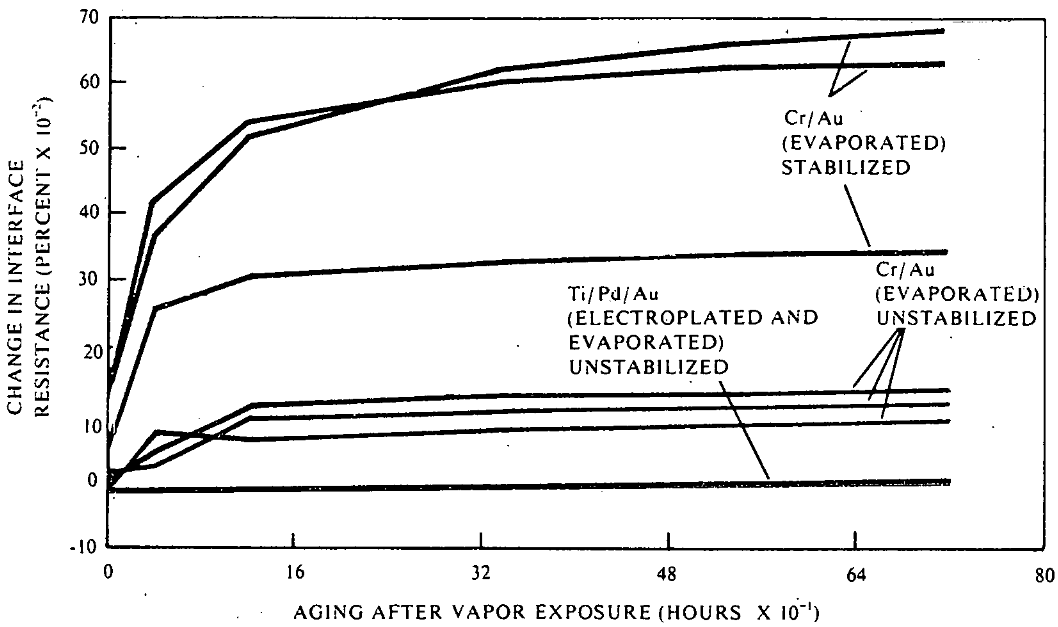


Figure 13. Gold Etch Vapor Exposure

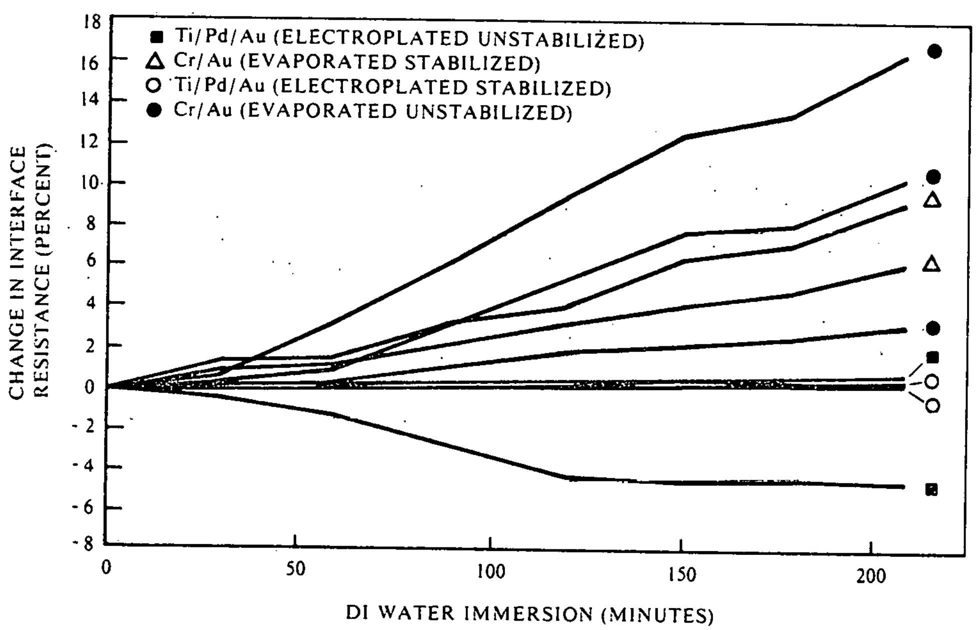


Figure 14. Water Immersion

Table 3. Percent Change in Interface Resistance

Solution (Time)	Evaporated Systems: Cr/Au 1*	Cr/Au 2**	Cr/Pd/Au 1*	Cr/Pd/Au 2**	Ti/Pd/Au 1*	Ti/Pd/Au 2**	Electroplated Ti/Pd/Au 1*	Electroplated Ti/Pd/Au 2**
Vapor Exposure: 20 minutes* and 2 hours**								
Au Etch (529 Hours)	34.40	293.70	0.03	0.07	0.07	-1.95	0.00	-0.35
Cr Etch (529 Hours)	17.57	8.90	0.22	0.08	1.90	-2.30	0.09	0.20
Ta Etch (529 Hours)	16.59	5.75	0.63	0.01	0.0	13.40	0.33	-3.10
Vapor Exposure: 2 Hours								
Ti-Pd Etch (718 Hours)	337.80	162.60					-0.03	0.09
Ta Etch (718 Hours)	74.80	28.90					-0.01	0.30
Au Etch (718 Hours)	5479.00	1155.00					-0.04	0.06
Immersion								
H_2O (210 M)	7.40	9.70					0.0	-1.73
Cr Etch (142 M)	23.60	44.30					0.0	0.89
Anodic (20 M)	55.20	442.60					0.0	0.15

*Stabilized
**Unstabilized

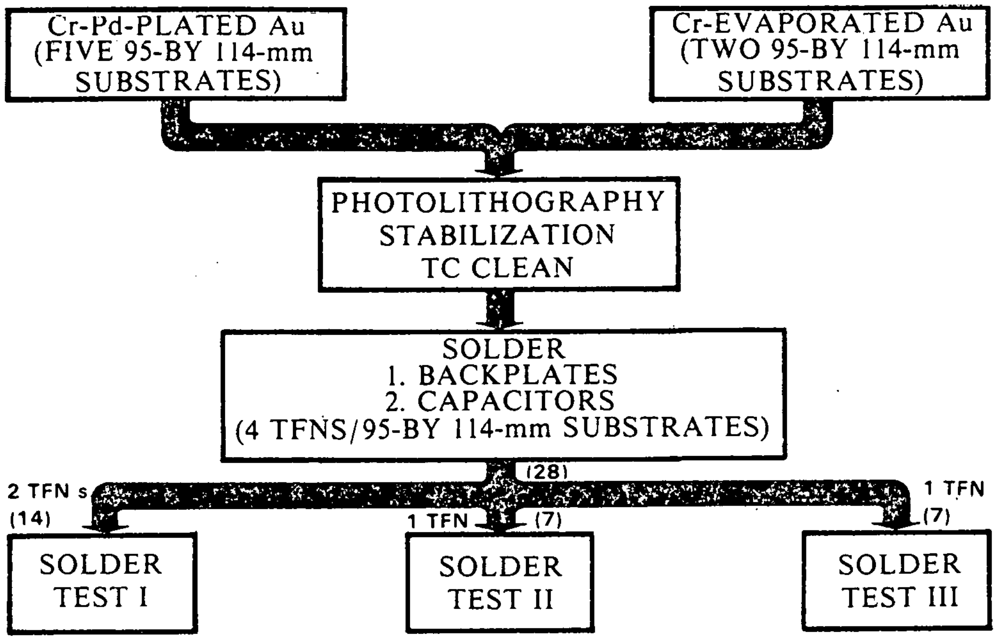


Figure 15. Solder Evaluation

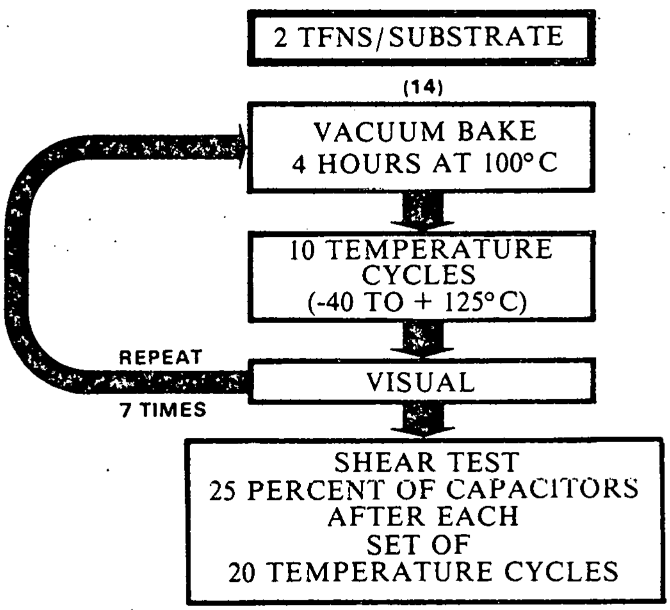


Figure 16. Solder Test I

Table 4. Solder Evaluation, Solder Test I Sequence

	Capacitor Shear Strength (N)				
	Temperature Cycles				
	20	40	60	70	80
Cr/Pd/Au (Plated)					
	11.57	8.90	16.01	12.90	16.01
	11.57	10.23	12.01	15.57	19.13
	10.23	13.34	10.68	11.57	13.34
	12.90	12.46	10.68	9.79	16.01
	13.34	16.01	8.90	12.46	10.23
	8.01	11.12	12.90	13.79	18.24
	12.01	10.23	14.23	19.57	11.12
	12.01	15.57	16.90	13.34	15.12
	12.46	11.57	13.79	14.68	12.01
	15.12	14.23	21.35	19.57	14.68
Cr/Au (Evaporated)					
	12.90	10.23	13.79	12.90	19.57
	12.01	12.46	9.79	16.01	21.35
	8.45	12.46	12.46	9.34*	16.01*
	11.12	12.46	12.90	20.91	13.34*

*Failures at solder/metallization interface (all other failures occurred in solder fillet)

The checkerboard bond pads exaggerate differences between the metal systems, and after some additional experience, a checkerboard bond test may be useful for quality control. The 2-hour, 300°C resistor stabilization did not degrade the bond results on any of the systems tested, and extending stabilization times to 8 hours had little effect. The smaller data base collected using gold-plated lead frames shows no deviation from these conclusions.

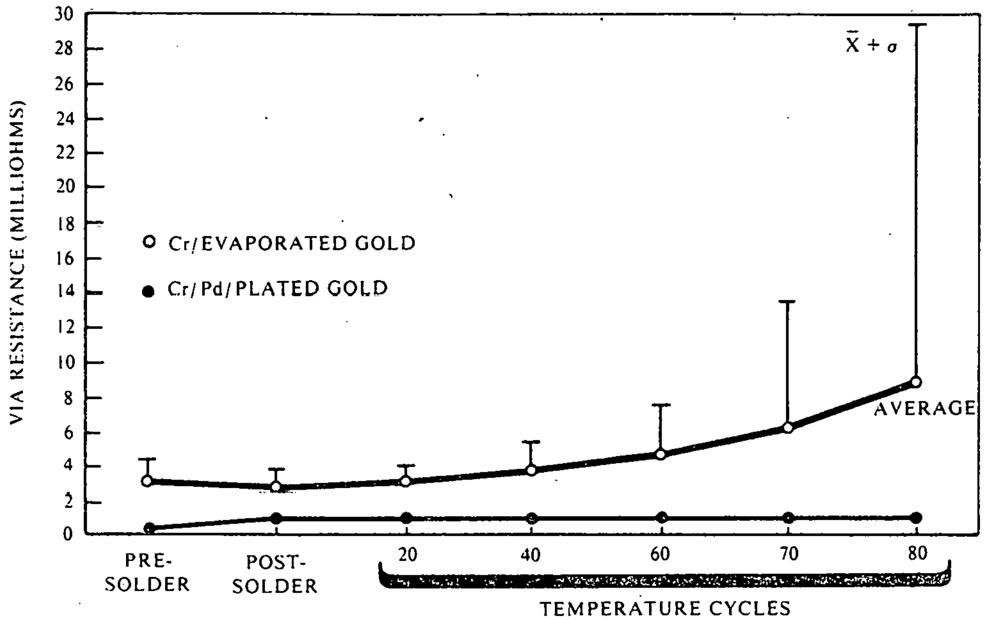


Figure 17. Soldered Via Resistance, Solder Test I

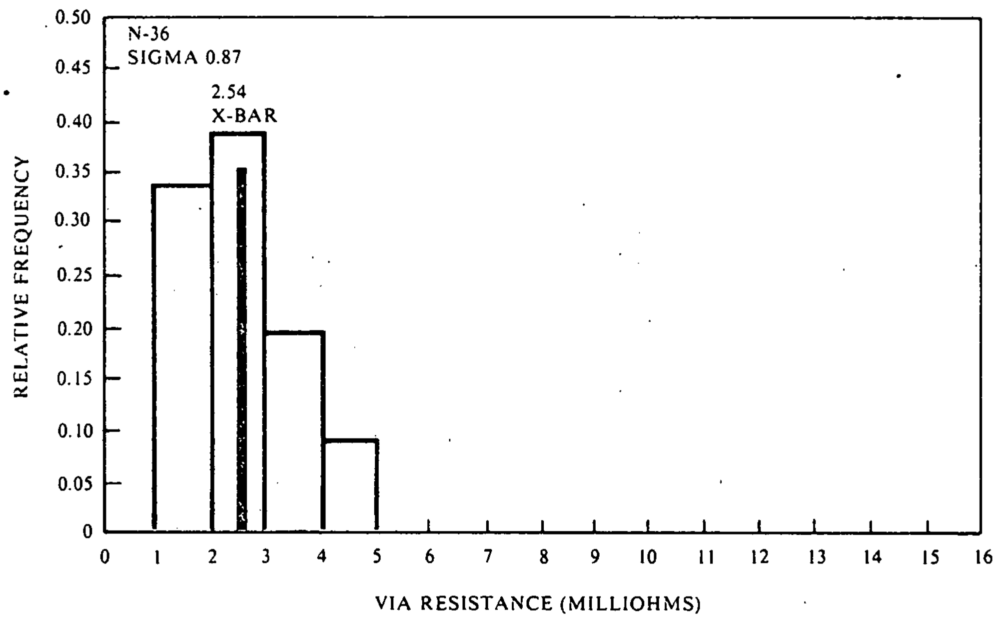


Figure 18. Evaporated Cr/Au, Post-Solder

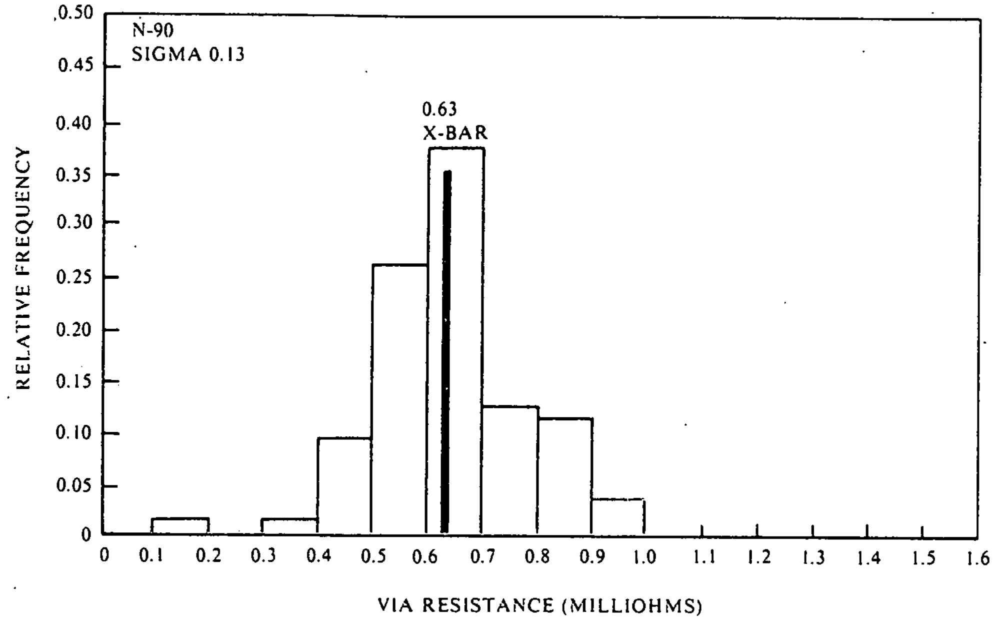


Figure 19. Cr/Pd/Plated Gold, Post-Solder

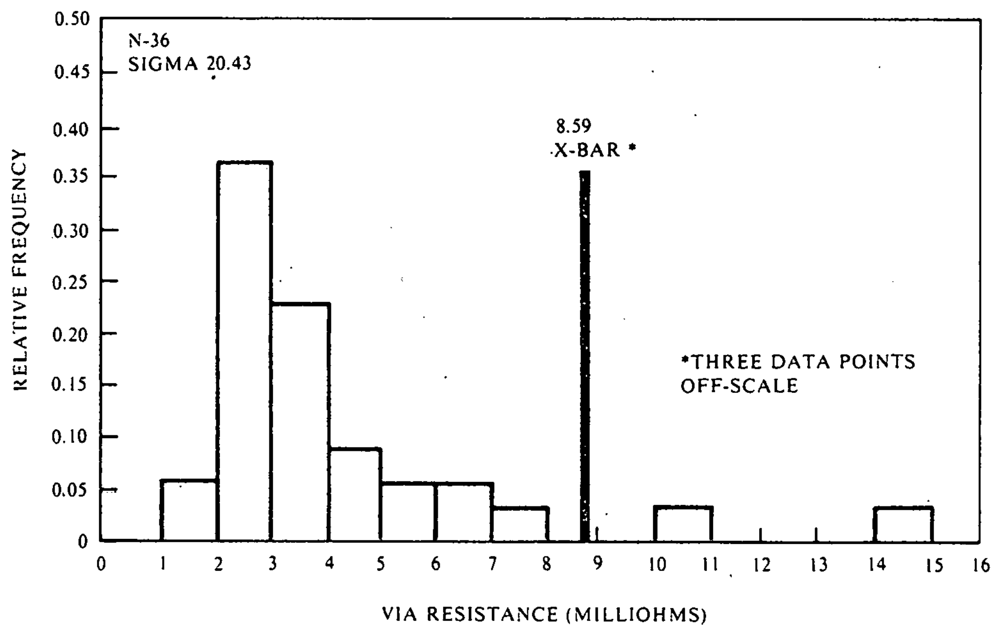


Figure 20. Evaporated Cr/Au, After Temperature Cycles

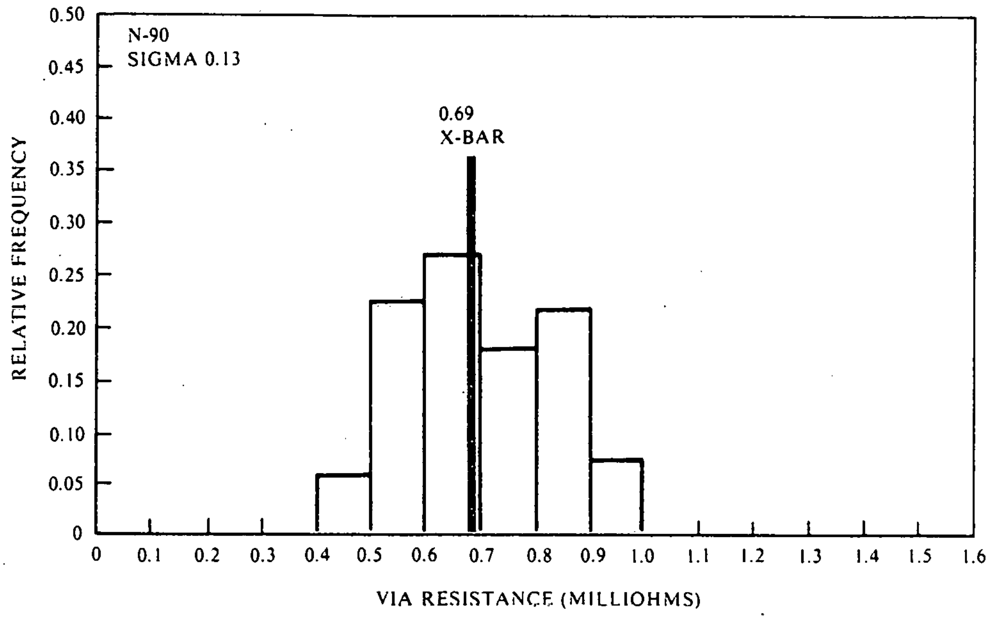


Figure 21. Cr/Pd/Plated Gold, After Temperature Cycles

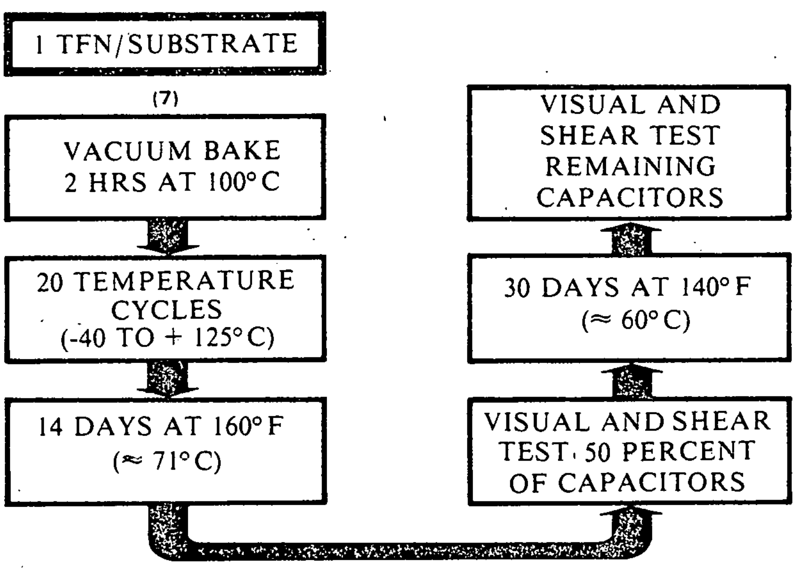


Figure 22. Solder Test II

Table 5. Solder Evaluation, Solder Test II Sequence

	Capacitor Shear Stength (N)	
	Vacuum Bake (2 Hours at 100°C) 20 Temperature Cycles	
Cr/Pd/Au (Plated)	14 Days at 71°C	30 Days at 60°C
	8.90, 9.79	12.46, 13.34
	10.68, 13.34	13.34, 12.01, 16.61
	8.01, 12.90	20.46, 12.01, 17.35
	12.46, 13.34	13.34, 14.23, 16.46
	9.79, 10.68	12.46, 8.90, 12.46
Cr/Au (Evaporated)		
	11.12, 10.23	14.23, 10.23*, 11.12*
	8.90, 10.68	10.68, 7.12*, 8.45*

*Failures at substrate metallization interface (all other failures occurred in solder fillet)

According to corrosion data, the intermediate palladium layer greatly increased corrosion protection regarding the Cr/evaporated Au system. Typically, the interface resistance change for the Cr/Au system was 100 to 1,000 times larger than for the other systems containing palladium.

The highest corrosion rate was observed when the Cr/Au system was exposed to gold etch vapors. Stabilized Cr/Au films are more susceptible to corrosion than unstabilized films.

Solderability tests showed little difference between electroplated gold and evaporated gold with respect to component or back plate soldering. The tests did show a significant advantage with electroplated vias. As expected, electroplated vias had "as-deposited" via resistance values of about 10 percent of the evaporated gold-coated vias. Since electroplating is not a "line-of-sight" process, more gold is deposited on the via walls. The increased gold thickness on the electroplated via walls results in a low (less than $1 \times 10^{-3}\ \Omega$), stable resistance

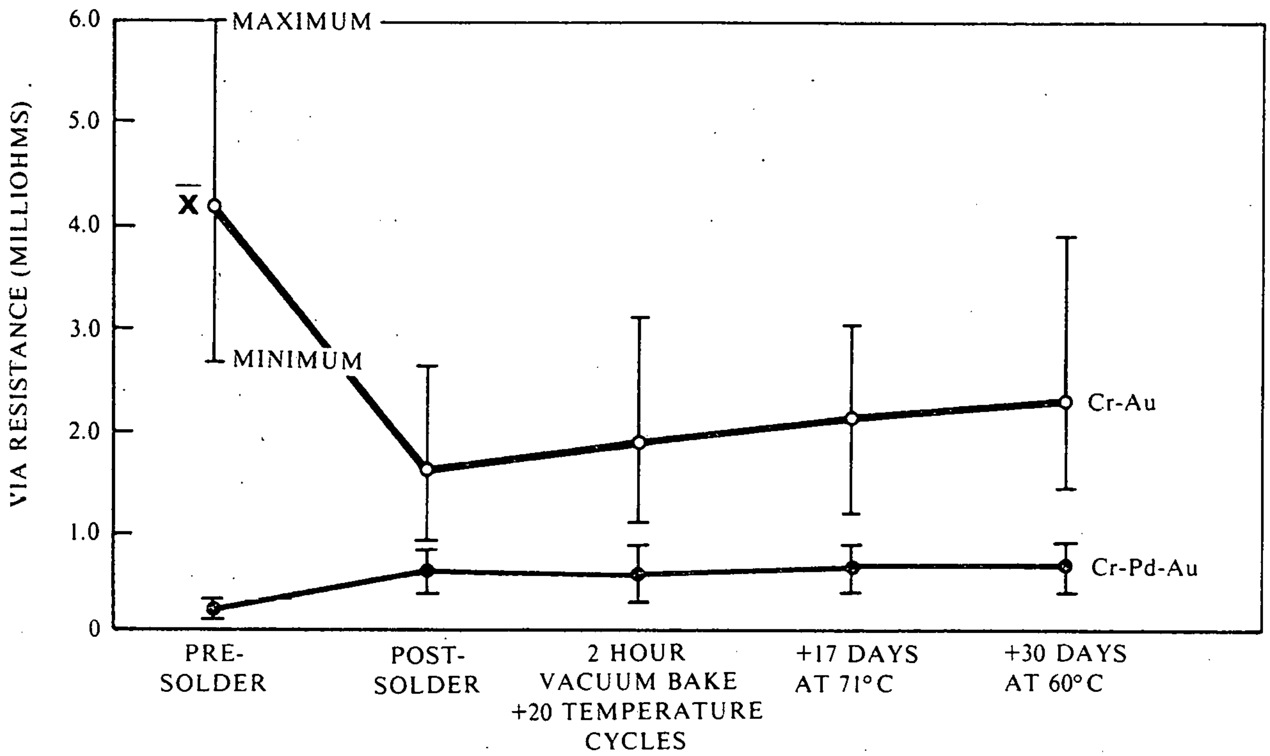


Figure 23. Soldered Via Resistance, Solder Test II

value after post soldering and during temperature cycling. With similar temperature cycles (higher than the normal production product's), some of the evaporated gold-coated vias increased in resistance to 1 x 10^{-2} to 1 x 10^{-1} Ω.

FUTURE WORK

Process development is continuing to refine the Ti/Pd/electroplated Au process. The initial operating parameters were selected from available literature and from experience with Bendix evaporation and plating systems. Future work will attempt to optimize these parameters and determine how broad the operating range may be. Specifically, the evaporation rate and thickness for titanium and palladium and the prebake and deposition temperatures will be studied. The addition of Pb^{++} to the electroplating bath to reduce cathodic polarization will be studied and may allow higher plating rates and reduce resist under plating.

The Ti/Pd/electroplated Au process is currently being used to fabricate TFNs for a Sandia reimbursable order for joint test assembly (JTA) hybrids. The plating and etching operations are

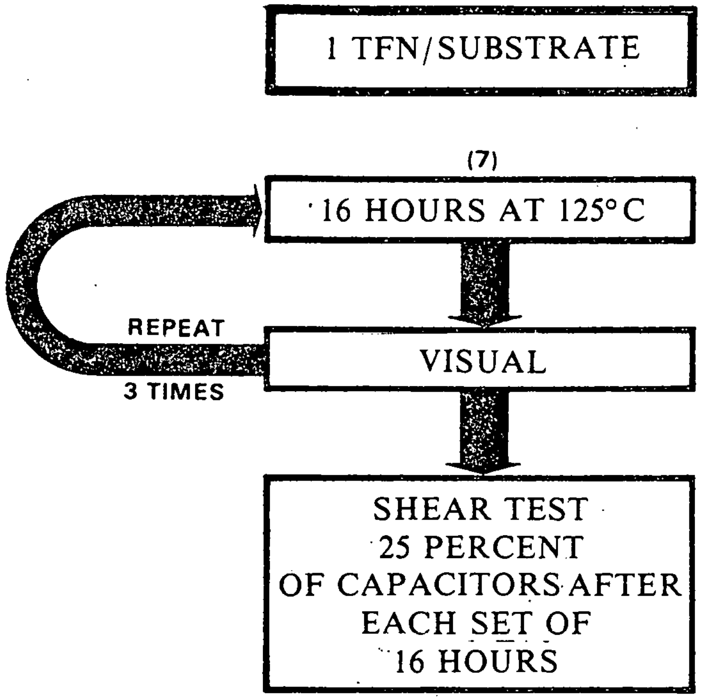


Figure 24. Solder Test III

now being done in an engineering lab. A facility is being prepared and work instructions are being written so that the thin film fabrication process may be completed within the production department. Ti/Pd/electroplated Au will be considered for future production programs and as a backup or possible replacement for the Cr/Au metallization on two current production programs.

Table 6. Solder Evaluation, Solder Test III Sequence

	Capacitor Shear Strength (N)				
	Hours				
Cr/Pd/Au (Plated)	16	32	48	64	
	12.90	11.57	12.01	11.57	
	17.79	17.35	12.90	17.79,	13.34
	9.79	11.12	16.46	16.46,	21.80
	12.01	16.46	15.12	17.35,	12.46
	13.34	14.23	22.24	20.46,	17.79
Cr/Au (Evaporated)					
	8.90	12.01	17.79	9.79*	15.57
	9.79	13.34	15.57	10.23*	9.79*

*Failures at substrate metallization interface (all other failures occurred in solder fillet)

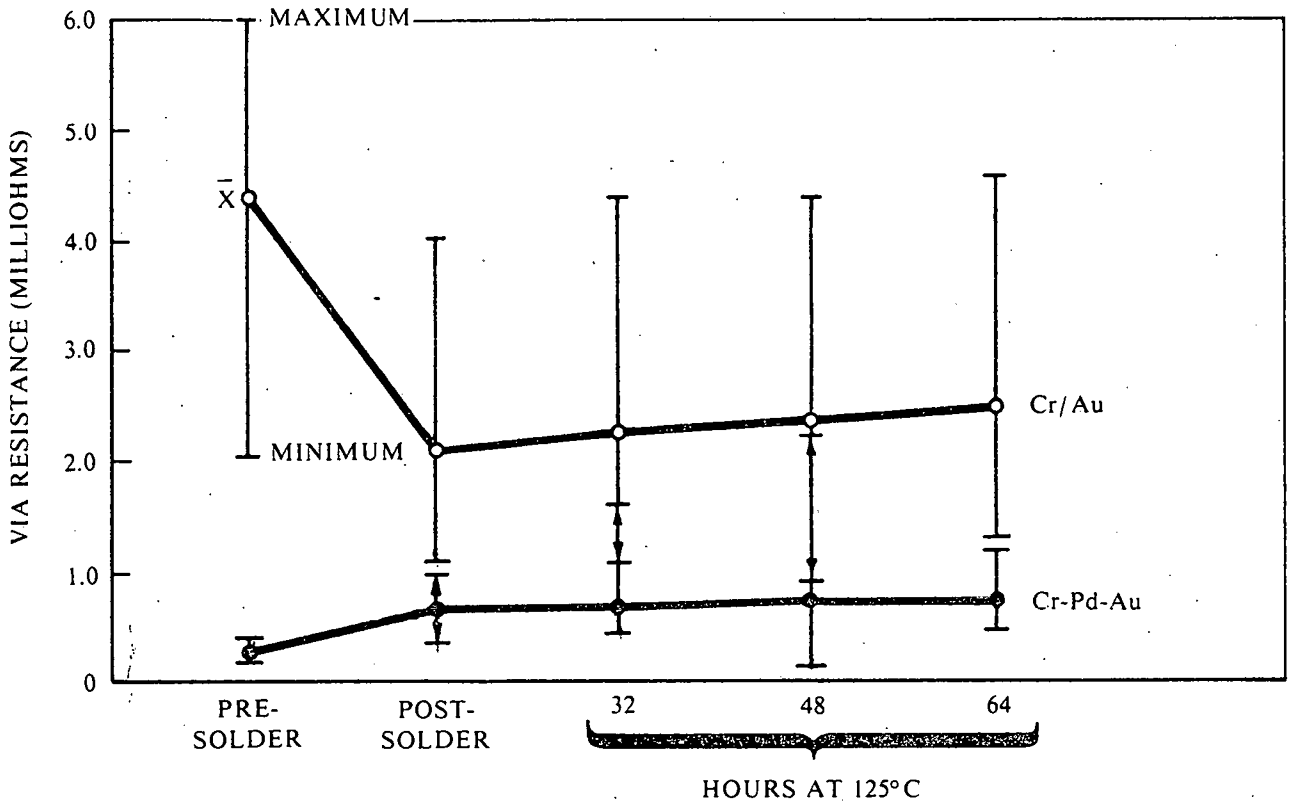


Figure 25. Soldered Via Resistance, Solder Test III

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BDX-613-2489

COMPARISON OF METALLIZATION SYSTEMS FOR THIN FILM HYBRID MICROCIRCUITS, R. A. Hines and M. K. Raut, Topical, August 1980

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