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ENCAPSULATED SURFACE-BARRIER PARTICLE DETECTORS  
Some Methods and Techniques

by

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# ENCAPSULATED SURFACE-BARRIER PARTICLE DETECTORS

## Some Methods and Techniques

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### I. INTRODUCTION

This report will describe in detail techniques that have been developed for the manufacture of encapsulated surface-barrier particle detectors. There is a belief among some workers in the field that it is not possible to control the conditions of manufacture well enough to assure consistent results. We have developed a method with which even inexperienced workers have been able to produce good devices with almost 100% yield. The devices manufactured to date have found use as counters and spectrometers for fission fragments, alpha particles, and low-energy electrons from radioactive nuclei. Devices, 50 mm<sup>2</sup> in area, have a resolution for 6.1-Mev alpha particles of 26 kev at room temperature and 18 kev at 78°K. Resolution for 1.1-Mev electrons has been measured as 7.5 kev at 78°K for devices 28 mm<sup>2</sup> in area. The silicon used has been n-type, grown with a 111 orientation, and purchased in the form of ingots about 2 cm in diameter; the resistivity has ranged from 100 to 3000 ohm-cm.

### II. HISTORICAL CONSIDERATIONS AND SIMPLE THEORY

The ordinary, gas-filled ionization chamber<sup>(1)</sup> has been used for many years in various branches of nuclear physics as a detector of ionizing nuclear particles. Essentially, it consists of a parallel-plate capacitor, the space between the plates being filled with a gas; a high voltage is applied across the capacitor to produce a high field between the plates. The particles enter the chamber and lose their energy by collision with the gas molecules, and leave in their wake a trail of ionized gas atoms and free electrons. The electrons are swept up by the applied electric field; the charge is collected on the plates and the voltage thus produced is amplified for analysis. For a brief period some interest was shown in the crystal, or solid-state bulk conductivity, counter.<sup>(2)</sup> This device consisted of a piece of single crystal insulator, such as diamond, across which a voltage was applied: the energy lost by the ionizing particles as they were stopped in the material excited electrons into the conduction band, and they were subsequently swept up by the applied field; the voltage pulse produced was amplified for analysis. The usefulness of this device was limited by the polarization of the insulator.

Beginning with the work of Mayer,(3) much has been done to develop the semiconductor junction detector. The bulk of the work that has been done is reported in the proceedings of two symposia that brought together most of the workers in the field.(4) The junction detector is simply a reverse biased semiconductor diode.(5) When ionizing particles traverse the charge-depleted region of the diode, holes and electrons are produced and these carriers are swept up by the applied field. The device is linear with the energy of the ionizing particles when the lifetime of the carriers against recombination or trapping is long with respect to the collection time of the carriers. There are at present two kinds of broad area p-n junctions used as diodes for the detection of charged particles: the diffused junction, and the surface-barrier junction.

The diffused junction is produced by thermal diffusion of a donor impurity into single-crystal p-type silicon, or of an acceptor impurity into single-crystal n-type silicon to produce a shallow p-n junction, perhaps a micron or so below the surface of the silicon. When a reverse bias is applied across such a junction, carriers are withdrawn from the region of a junction, and a charge-depleted region is produced just beneath the surface. If the depth of the junction is shallow enough the charged particles will enter the depletion region with little energy loss in the dead volume, or "window," at the surface. The diffused junction has one serious drawback: the heat treatment which is necessary to accomplish the thermal diffusion tends to degrade, or shorten, the lifetime of the carriers against recombination, trapping, or both. Long carrier lifetime is desirable, as pointed out above, because, in order that the output of the device be linear with the energy of the particles detected, it is essential that the carriers be collected before they recombine or are trapped. We have confined most of our efforts to the development of the surface-barrier junction because of its inherent simplicity.

The surface-barrier junction is the easiest to produce because nature does most of the work. Surface states on germanium were postulated by Bardeen(6) to explain the fact that the contact potential and the rectification characteristics of metal-semiconductor diodes did not appear to depend upon the metal that was used for the contact. The surface states are represented as a well containing electrons that are withdrawn from the interior of the semiconductor; the surface levels trap electrons until the height of the Fermi level in the surface is equal to that of the Fermi level in the interior. There results a thin region, just below the surface, which has been depleted of its ordinary share of electrons; the space charge due to uncompensated donors gives rise to an electric field which distorts the energy levels and leads to the formation of an asymmetrical potential barrier. The bending of the energy levels in effect lowers the Fermi level at the surface, such that a p-type surface results. P-type silicon will thus have formed a more strongly p-type surface, whereas in the case of n-type material, there will exist an inversion layer with a

p-n junction just below the surface (see Figure 1). The Bardeen theory does not specify the exact nature of these surface states, but there is a possibility that they arise from the formation on the surface of a stable, or quasi-stable, oxide layer. The surface-barrier detector is made of n-type silicon; the metal contact to the p-type surface is made with gold which is evaporated over the surface.

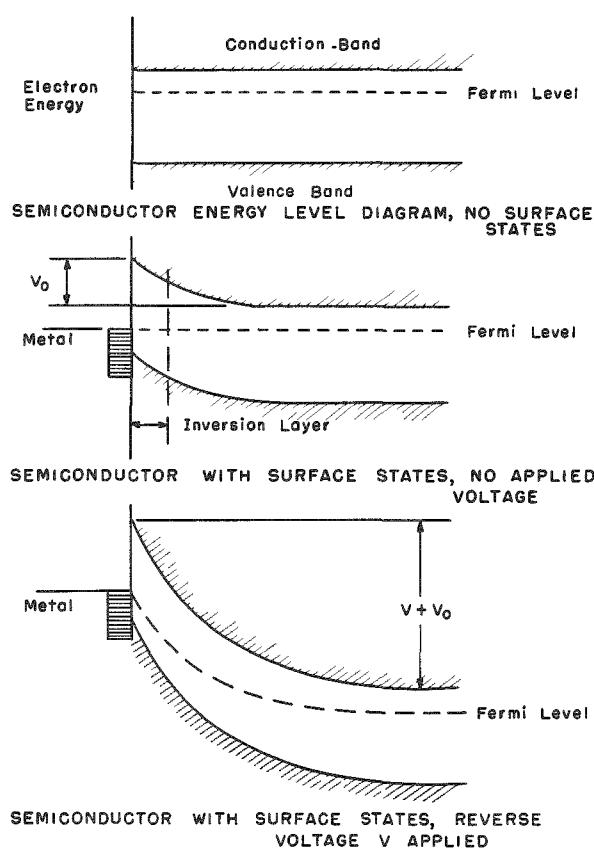


Figure 1

Energy Levels of Semiconductor Surface Barrier Rectifier

When an external reverse bias is applied, the depth of the space-charge region will be given by

$$D = \sqrt{\frac{\kappa(V_0 + V)}{2\pi e N_d}} \quad (\text{cm})$$

The shape of the potential barrier and the depth of the charge depleted region can be obtained from the solution of Poisson's equation for the case of uniform conductivity in the semiconductor.(7) Poisson's equation for the one-dimensional case is

$$\frac{d^2V}{dx} = -\frac{4\pi\sigma}{\kappa} \quad ,$$

where  $\sigma$  is the charge density, which, at room temperature is given by  $eN_d$ ,  $N_d$  the donor impurity concentration,  $e$  the electronic charge (in esu), and  $\kappa = 12$  for silicon. The solution is

$$V = \frac{2\pi e N_d (D^2 - x^2)}{\kappa} \quad (\text{in esu}) \quad .$$

If the potential  $V$  drops from  $V_0$  on the surface ( $x = 0$ ) to zero inside the semiconductor, the depth of the space-charge, or charge-depleted, region will be given by

$$D = \sqrt{\frac{\kappa V_0}{2\pi e N_d}} \quad (\text{cm}) \quad .$$

The associated capacity of the junction will be

$$C = A \frac{\kappa}{4\pi D} = A \sqrt{\frac{eN_d \kappa}{8\pi(V_0 + V)}} ,$$

where A is the area of the junction in  $\text{cm}^2$ .

A broad space-charge region is desirable because the associated capacity will decrease as the charge-depleted region is increased: a low capacity results in a larger signal and an improved signal-to-noise ratio. From the above relations, we see that the dependence on resistivity and bias voltage is

$$D \propto \sqrt{V\rho} \quad ; \quad C \propto \frac{1}{\sqrt{V\rho}} ,$$

where the resistivity is related to the impurity concentration by

$$\rho = \frac{1}{\mu e N_d} ,$$

in which  $\mu$  is the mobility of the carrier.

### III. PRELIMINARY TREATMENT AND ENCAPSULATION

#### A. Preparation of the Silicon Wafers

The ingot is mounted in black wax and cut into slices with a precision diamond cutoff saw. Devices smaller than 2 cm in diameter are made by cutting small wafers out of these slices with an ultrasonic boring machine by means of a hollow tool. Rectangular pieces can be cut with the diamond saw and irregular shapes can be formed with the ultrasonic boring machine. The wafer is lapped on both sides on a glass plate in a slurry of optical finishing powder<sup>(8)</sup> in water to remove the gross damage done by the saw, rinsed in running tap water, cleaned in an ultrasonic cleaner in a strong detergent solution to remove the crushed bits of silicon and finishing powder adhering to the surface, and again rinsed in tap water. The wafer is nickel plated in an electroless nickel plating solution<sup>(9)</sup>: about 15 min in the boiling solution is long enough to permit the deposition of a suitable layer of nickel.

#### B. Assembly and Encapsulation

The ohmic contact is made to the wafer by soldering a #22 tinned copper wire to one side of the wafer with ordinary rosin-core solder; the flux is cleaned off with trichloroethylene. The solder connection is painted with Q-Dope (polystyrene dissolved in toluene),<sup>(10)</sup> and when the paint is

dry the nickel is stripped off by immersion in CP-4(11) for a few seconds, after which it is rinsed in running tap water. After being dried in air, the back of the device is again painted with Q-Dope to protect the edge of the nickel plating under the solder joint, and the silicon is etched in CP-4 at room temperature for about 10 sec to polish the edges of the wafer, after which it is rinsed in running tap water and then in running distilled water. The assembly is now ready for encapsulation.

The wafer is mounted on a piece of tape with adhesive on both faces which has been laid down on a thin piece of Lucite, or any other flexible material. A short piece of polystyrene tubing is mounted concentrically about the wafer, and a gold contact wire is inserted beside the wafer (see Figure 2). An epoxy resin is poured into the tubing, care being taken to remove any bubbles before the resin sets. The resin we have been using is R-313,(12) mixed in the proportions 2 drops hardener B to one gram of resin.

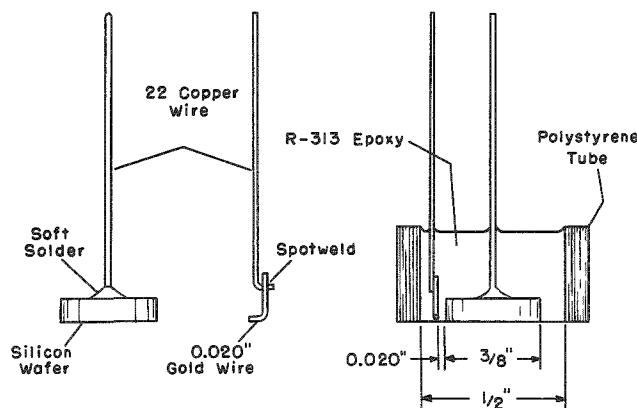


Figure 2  
Assembly and Details of Device Construction

#### IV. PREPARATION OF THE SURFACE

##### A. Lapping

The surface is lapped on a glass plate in a slurry of grinding powder and water, starting with any convenient grade of grinding powder and working down by stages to #95 optical finishing powder.(8) An essential step in the lapping process is the cleaning of the surface between each grade of grinding powder and after the final lapping with the #95 finishing powder. The surface is rinsed in running tap water and then cleaned in an ultrasonic cleaner in a strong detergent solution to remove the crushed bits of silicon and finishing powder adhering to the surface. The ultrasonic agitation serves to shake the bits of material loose and the detergent solution holds

it in suspension, and thus prevents recombination with the surface. The ultrasonic cleaning is followed by a rinse in running tap water and then in running distilled water. This is a most important step in the preparation of the surface, as it is essential that the surface be free of loose matter during the etching: small particles clinging to the surface will react more rapidly with the etch than will the body of the silicon wafer, and the result will be a variation of the etch rate over the surface owing to the presence of "hot spots" caused by the rapid reaction at the sites of these small particles. This variation in etch rate will result in the formation of pits or protuberances on the surface. The technique described enables one to chemically polish a silicon surface, 3 cm<sup>2</sup> in area, completely free of these unsightly blemishes.

#### B. Etching

The etching and all the subsequent handling of the device are carried out in a dust-free atmosphere. A Lucite glove box has been outfitted with a large, highly efficient filter and a stack which is vented into a hood. The surface is etched with CP-4,(12) a preferential etch that we have used with great success. The etch is mixed in a large polyethylene bottle, 1.1 liters being mixed up at a time. The etch is stored in the polyethylene bottle and aging seems to have no adverse effect. It is important that all the bottles and graduates used in mixing and measuring be clean, of course. The etch is used in a polyethylene beaker, and is cooled to 0°C in an ice bath. The etch is stirred with a magnetic stirring device, and no more than four wafers of 50 mm<sup>2</sup> area are etched in one 100 ml batch of etch; if larger pieces are to be polished then the number of pieces per pot of etch will be reduced accordingly. The silicon surface is immersed in the cold etch for 3½ min, and must not be lifted out of the etch before the time is up. The piece is removed immediately into a stream of running distilled water, and rinsed until it passes the water film break test. The test is easily performed and will indicate the presence of hydrophobic contaminants. The device is removed from the stream of distilled water and the excess water is shaken off; it is held with its surface vertical: if the surface is free of hydrophobic contaminants the water film that remains on the surface will dry slowly and interference fringes will be seen at the edge of the film; if the surface is not free of hydrophobic contaminants the film will break and the water will run off the surface. This is a good test for cleanliness, but our experience has been that there is no correlation between passing the water film break test and performance as a good detector. No attempt is made to remove organics or ions from the distilled water. The device is permitted to dry and is stored in the dust free atmosphere for twenty four hours, or more, to permit the growth of an oxide layer, after which edge protection is applied.

## V. EDGE PROTECTION

A close examination of the device after etching reveals that the edge of the silicon surface is very irregular at the silicon epoxy interface (see Figure 3). Owing to this irregularity the surface barrier junction at the edge is very nonuniform. When an electric field is applied across the junction breakdown will occur around the edge. The high electric field can be moved away from the irregular edge of the junction by the application, after etching, of an insulation of some sort around the edge of the silicon wafer. When such edge protection is applied, the devices are able to take very high voltages and the reverse leakage current will be very small.

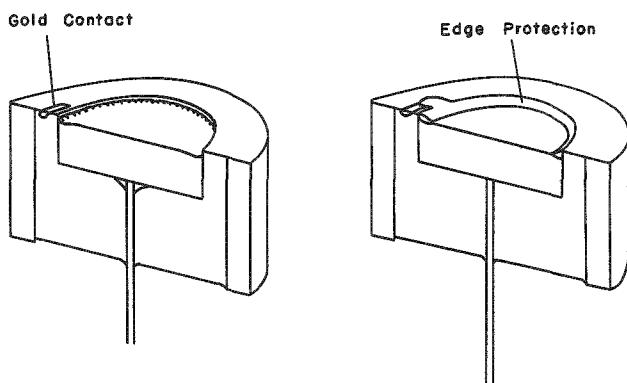


Figure 3

Application of Edge Protection

We have found 3 different materials to be effective for edge protection:

1. Ciba Amine Free Epoxy: 502 Araldite with #204 Hardening Agent.<sup>(13)</sup>

This is the material reported by Blankenship, Borkowski, and Fox.<sup>(14)</sup> They used it with a small amount of iodine in solution, but we have found that it works just as well without the iodine. It is a good protective material, but it has a very short pot life: it hardens so quickly that it is not possible to apply it with a hypodermic syringe.

2. Shell Epoxy Paint Ax 211 (Resin #1002 in a solvent).<sup>(15)</sup>

This material is mixed according to the manufacturer's specifications and is permitted to stand until it gets too thick to run when applied to the semiconductor surface. It can be applied with a fine brush or with a hypodermic syringe.

3. Grodan #1 HIVAC<sup>(16)</sup>

This is the material we have used for almost all of our work. Four drops of hardener are mixed with 1 gram of resin. It is allowed to

stand until it begins to get so thick that it will not run when applied to the semiconductor surface. It can be applied with either a fine brush or a hypodermic syringe. We have used a  $\frac{1}{2}$  -ml syringe with a #30 needle.

## VI. GOLD EVAPORATION

The device is stored overnight in the dust-free atmosphere while the edge protection hardens. It is then removed to a vacuum evaporator and a layer of gold, about 200 Å (approximately  $40 \mu\text{g}/\text{cm}^2$ ) thick, is evaporated onto the surface to establish contact between the gold lead and the p-type surface, at a pressure of about  $5 \times 10^{-6}$  mm Hg. The device is mounted about 6-8 in. from the source filament; this assures that if many devices are coated at one time that the thickness of gold will be about the same on all of them. It has been our experience that on some occasions the evaporated layer does not make contact with the gold lead, or that the contact becomes noisy when voltage is applied. The front surface of the epoxy and the surface of the gold wire do not join smoothly because they are rough, even when lapped with a fine grade of finishing powder. The 200-Å-thick layer of gold is not heavy enough to form a bridge from the epoxy surface to the gold wire. This can be remedied in advance when the edge protection is being applied: simply run a little string of epoxy from the edge over to just touch the gold wire such that, when gold is evaporated over the surface, there will be a smooth, continuous layer of gold from the silicon surface to the gold wire (see Figure 3). This establishes a continuity that will permit cooling the device to liquid nitrogen temperature ( $78^\circ\text{K}$ ) without causing the contact to open or to become noisy because of differential contraction.

## VII. TYPICAL PERFORMANCE DATA

Results with devices prepared in this manner are shown in Figures 4, 5, and 6. As is evident from the figures, measurements were made at room temperature ( $300^\circ\text{K}$ ) and at liquid nitrogen temperature ( $78^\circ\text{K}$ ). No curve of current vs reverse bias is presented for  $78^\circ\text{K}$  because the current in all cases was less than  $10^{-10}$  amp up to a bias of 350 v. In general, devices made with material in the resistivity range from 100 to 850 ohm-cm have all given the same results. Figure 5 shows the resolution obtained for the 6.1-Mev alpha particles from curium-242 (the two lines are separated by 44 kev) for 3 sizes of device. The 3000-ohm-cm material that we have has not been useful for low-energy alpha-particle spectroscopy because the best resolution for 6.1-Mev alphas has been about 70 kev for a device  $28 \text{ mm}^2$  in area. It has, however, proven to be useful for electron spectroscopy, and Figure 6 shows the resolution that has been measured at  $78^\circ\text{K}$  for the 625-kev conversion line from barium-137 and the conversion lines from bismuth-207. The best room-temperature figures are: 17 kev for the 625-kev line at 175 v, and 25 kev for the 1.1-Mev line at a bias of 400 volts. Figure 7 shows the vacuum chamber which has been used for cooling the devices.

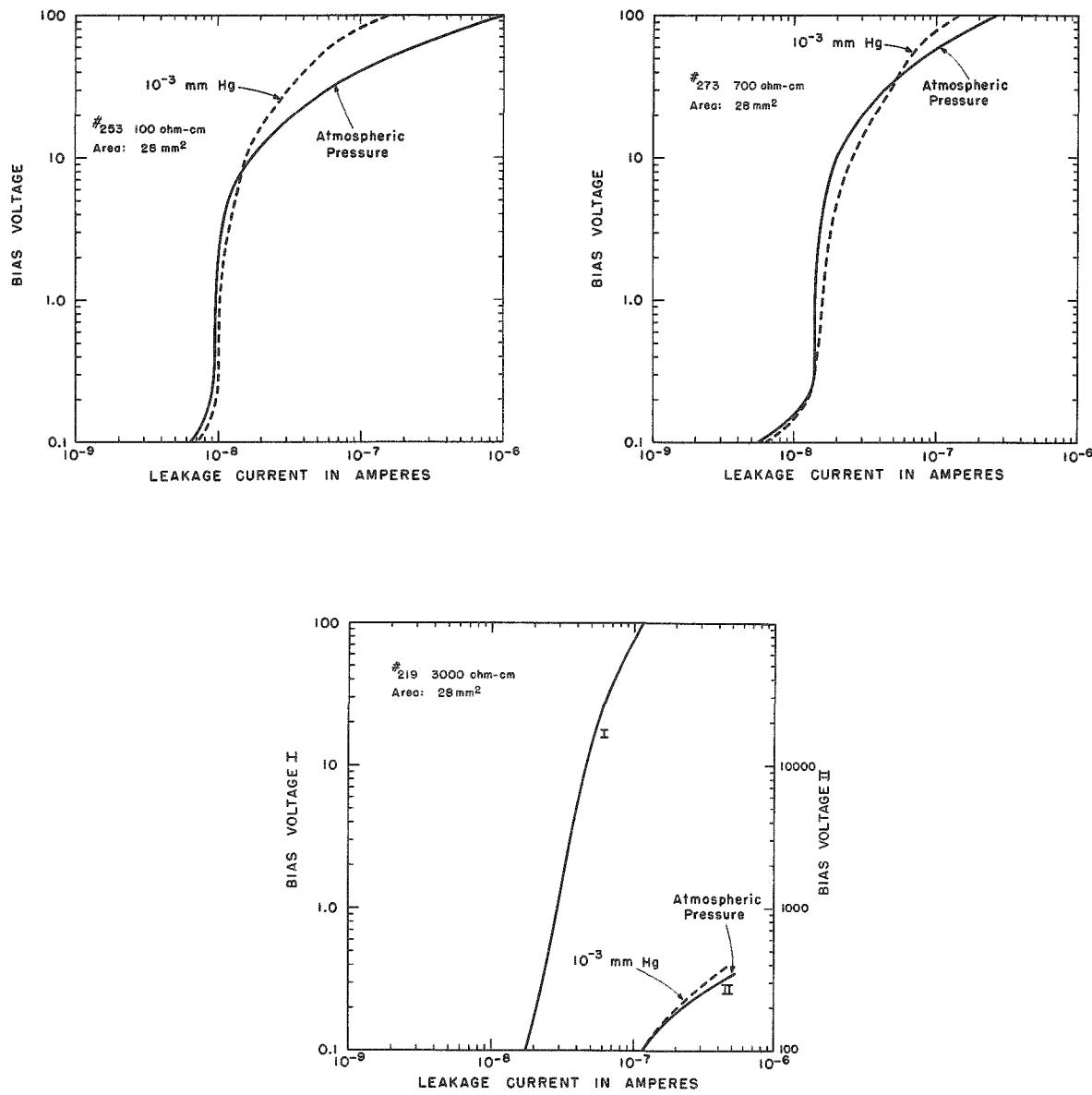


Figure 4

Reverse Characteristics of Typical Devices  
at Atmospheric Pressure and at  $10^{-3}$  mm Hg

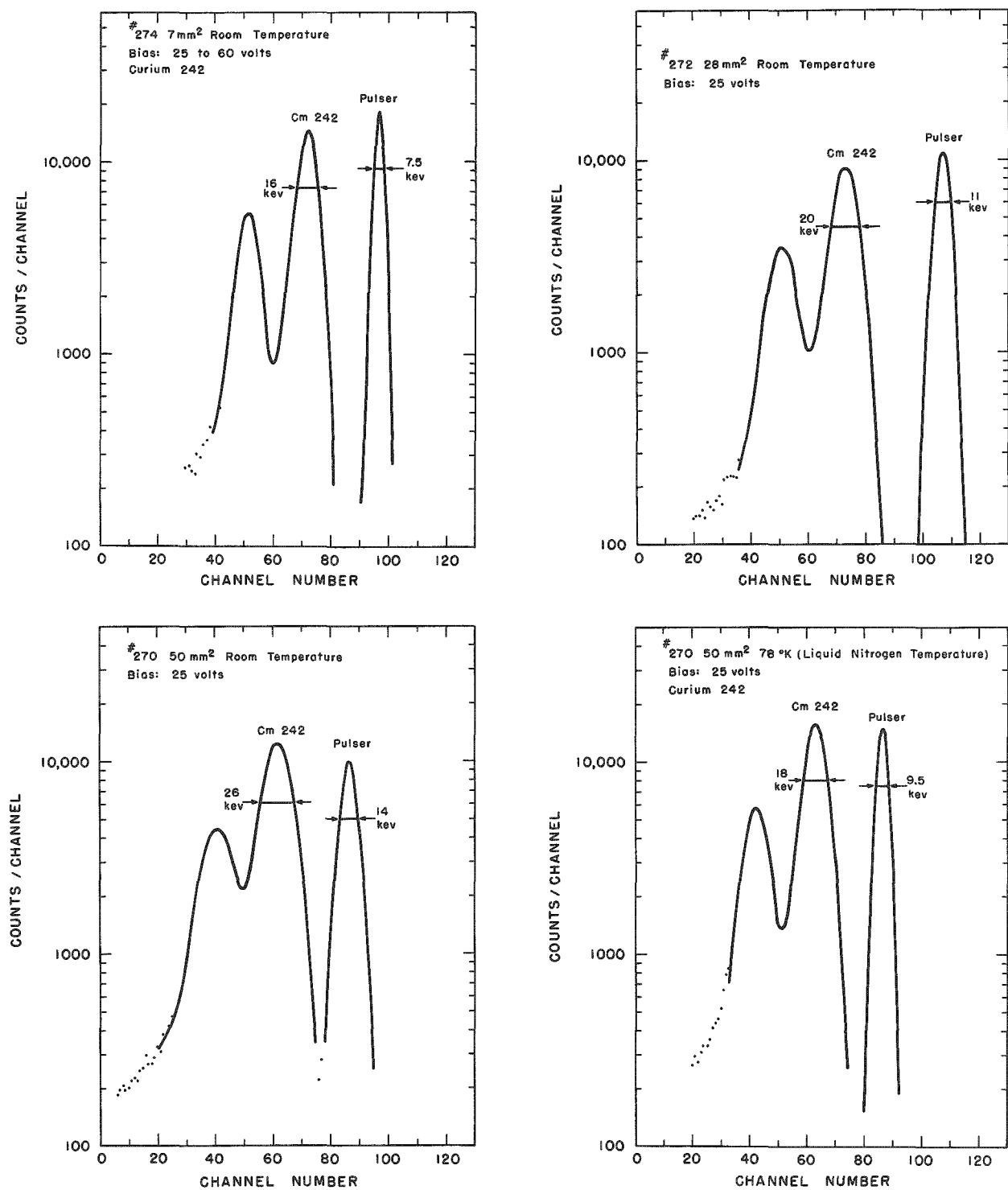


Figure 5

Resolution of Typical Devices for the 6.1 Mev  
Alpha Particles from Curium-242

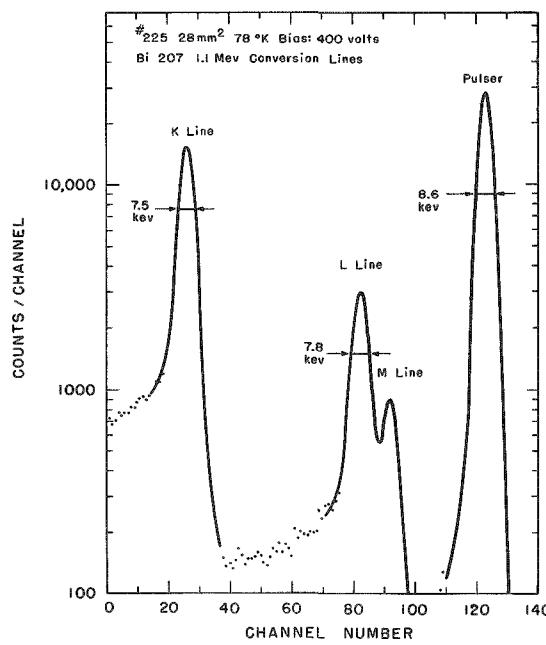
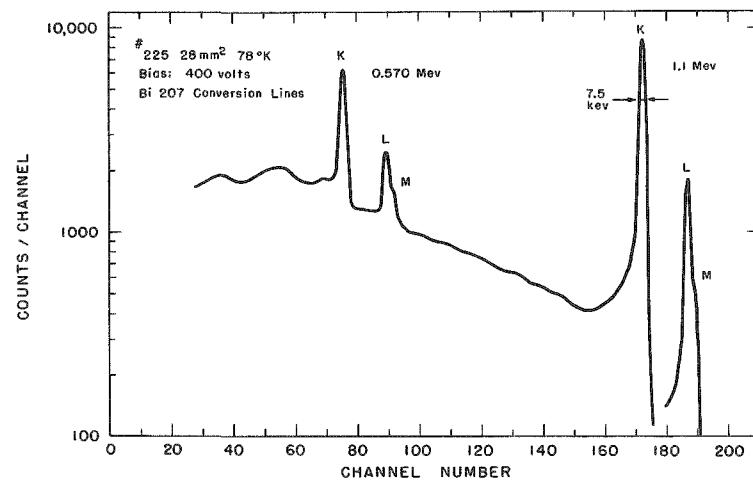
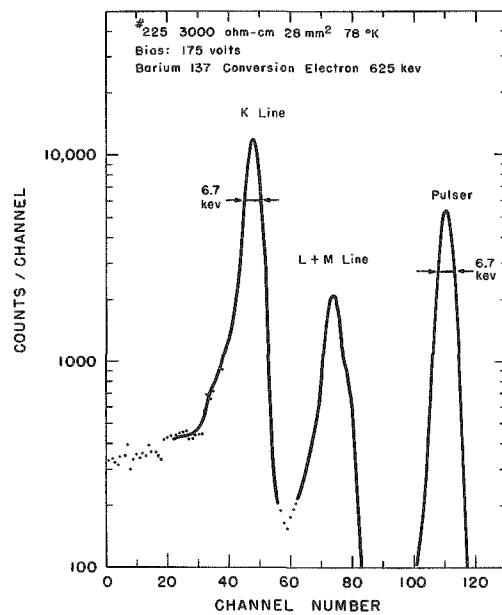
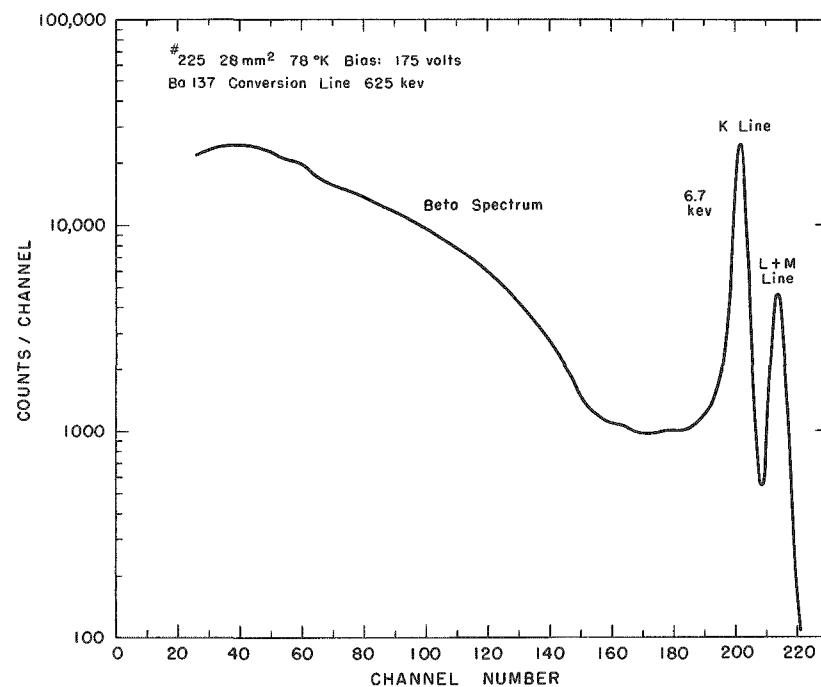


Figure 6

Resolution of 3000 ohm-cm Devices for Conversion Electrons from Ba<sup>137</sup> and Te<sup>125</sup>

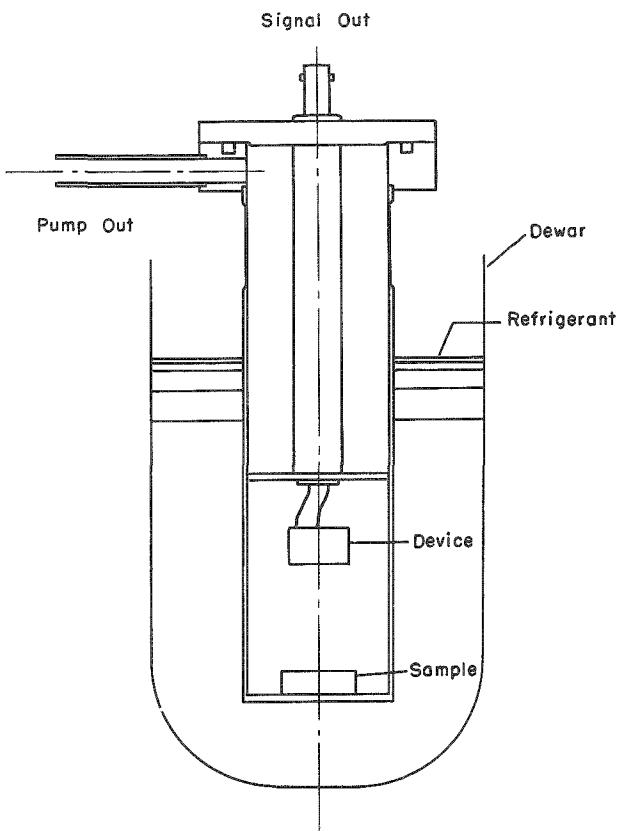


Figure 7  
Vacuum Chamber for Cooling Devices

### VIII. CONCLUSION

The technique described above has been used successfully at this laboratory for the fabrication of detectors that have found use as gross counters and as spectrometers; it has been found that with a little practice workers with no previous experience have been able to manufacture devices that compare with those discussed in the present report. We feel that with a modest investment in time and money any laboratory can easily set up to manufacture devices for their own use.

### IX. ACKNOWLEDGEMENTS

Mention must be made of the contributions made by Donald Sparlin, who began the present program, John Dame, and Alan Sandborg, all three of whom were employed as cooperative or part-time employees while attending Northwestern University. Special mention must be made of the time spent by Dale Henderson, of the Chemistry Division, in improving the behavior of the Instrument Development Laboratory charge-sensitive amplifier that was used in making the measurements.

## X. APPENDIX

A. Chemical Polish: CP-4

From: Transistor Technology, Edited by Bridges, Scaff, and Shive,  
Bell Labs Series, D. Van Nostrand (1958), Vol. I, p. 354.

Hydrofluoric Acid HF (48%)	300 cc
Nitric Acid $\text{HNO}_3$ (71%)	500 cc
Glacial Acetic Acid $\text{CH}_3\text{COOH}$	300 cc
Bromine (omitted in our etch)	5 cc

Mix and store in polyethylene container.

B. Electroless Nickel Plating Solution

From: Transistor Technology, Edited by F. J. Biondi, Bell Labs Series,  
D. Van Nostrand (1958), Vol. III, p. 173.

Nickel Chloride	30 gm/l
Sodium Hypophosphate	10 gm/l
Ammonium Citrate	65 gm/l
Ammonium Chloride	50 gm/l
Filter	

To use: Add ammonium hydroxide ( $\text{NH}_4\text{OH}$ ) to pH 8-10 and heat to boiling; at pH 8-10 the solution should be a bright blue color.

## REFERENCES

1. B. B. Rossi and H. H. Staub, Ionization Chambers and Counters, National Nuclear Energy Series V-2, McGraw Hill, New York (1949).
2. R. Hofstader, Crystal Counters, Proc. Inst. Radio Engrs., 38, 726 (1950).
3. J. W. Mayer, Performance of Ge and Si Surface Barrier Diodes as Alpha Particle Spectrometers, J. Appl. Phys., 30, 1937, (1959).
4. Semiconductor Nuclear Particle Detectors, edited by J. W. T. Dabbs and F. J. Walter, NAS-NRC 871, Nuclear Science Series Report #32, (1960). Proceedings of the Meeting on Solid State Radiation Detectors, IRE Trans. on Nuclear Science, Vol. NS-8, No. 1, (1961).
5. W. Shockley, The Theory of p-n Junctions in Semiconductors and p-n Junctions Transistors, Bell System Tech. J., 28, 335, (1949).
6. J. Bardeen, Surface States and Rectification at a Metal Semiconductor Contact, Phys. Rev., 71, 717 (1947).
7. W. C. Dunlap, An Introduction to Semiconductors, John Wiley and Sons, New York (1957), Chap. 7.
8. The Carborundum Company, Electro Materials Division, Niagara Falls, New York.
9. Transistor Technology, Edited by F. J. Biondi, Bell Labs Series, D. Van Nostrand (1958), Vol. III, p. 173.
10. General Cement Manufacturing Co., Rockford, Illinois.
11. Transistor Technology, Edited by Bridgers, Scaff, and Shive, Bell Labs Series, D. Van Nostrand (1958), Vol. I, p. 354.
12. Carl H. Biggs Co., 1547-14th Street, Santa Monica, California.
13. Ciba Products Corporation, Fairlawn, New Jersey.
14. J. L. Blankenship, C. J. Borkowski, and R. J. Fox, Silicon Surface Barrier Nuclear Particle Detectors, from a Conference on Nuclear Electronics (References Number NE/136).
15. Shell Chemical Corporation, 380 Madison Avenue, New York 17, New York.
16. Grodan Manufacturing and Sales, Inc., 5815 West Jefferson Avenue, Detroit 9, Michigan.