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Ion-Implanted GaAs JFETs with f_t > 45 GHz for Low-Power Electronics

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Abstract - GaAs Junction Field Effect Transistors (JFETs) are reported with gate lengths down to 0.3 μm. The structure is fully self-aligned and employs all ion implantation doping. p^+-gate regions are formed with either Zn or Cd implants along with a P co-implantation to reduce diffusion. The source and drain implants are engineered with Si or SiF implants to minimize short channel effects. 0.3 μm gate length JFETs are demonstrated with a sub-threshold slope of 110 mV/decade along with an intrinsic unity current gain cut-off frequency as high as 52 GHz.

I. INTRODUCTION

GaAs Junction Field Effect Transistors (JFETs) have attracted renewed attention for low-power, low-voltage electronics [1-3]. JFETs have a significant advantage over MESFETs for low-power operation due to the higher gate barrier of the p/n junction gate which results in less gate leakage. Although some JFET structures suffer a degradation in high-frequency performance due to the added gate-to-source capacitance (C_{GS}) of the junction gate and the gate length broadening associated with formation of the p^+-gate region, we have previously demonstrated a self-aligned GaAs JFET technology that minimizes C_{GS} and closely aligns the p^+-gate with the gate contact [3]. In our earlier work, JFETs with a 0.7 μm gate length were reported with an f_t of 26 GHz and f_{max} of 42 GHz [4]. These devices have been employed as the n-channel FET in a complementary heterostructure field effect transistor (CHFET) technology with the demonstration of 319 ps loaded gate delays at 8.9 fJ [5]. Furthermore, these JFETs are being applied to low-power microwave circuits. A hybrid amplifier has been reported that operates at 1 mW of DC power with a gain of 10 dB and a noise figure of less than 2.5 dB at a frequency of 2.15 GHz using 0.7 μm gate lengths JFETs[6].

In this work we present results for all ion implanted GaAs JFETs with gate lengths down to 0.3 μm. Details of the process sequence, particularly those aspects required to reduce short channel effects, are reviewed. Finally, DC and rf device results are presented.

II. JFET PROCESSING

Fig. 1 shows a schematic of the all ion-implanted GaAs JFET with seven different implanted regions. To reduce short channel effects in an all ion implanted device, the doping profiles must be significantly modified as compared to a longer gate transistor. In particular, the depth of the source and drain (n^+) implant must be reduced and the lateral profile must be off-set from the gate contact. Since a Varian 400-10 ion implanter with a minimum operating energy of ~40 keV was used, we employed 40 keV SiF implants next to the gate contact (n" implants) to realize an effective Si ion energy of 25 keV which gives a projected range of 26 nm with a lateral straggle of 20 nm. Next, 100 nm SiO_2 sidewall spacers were

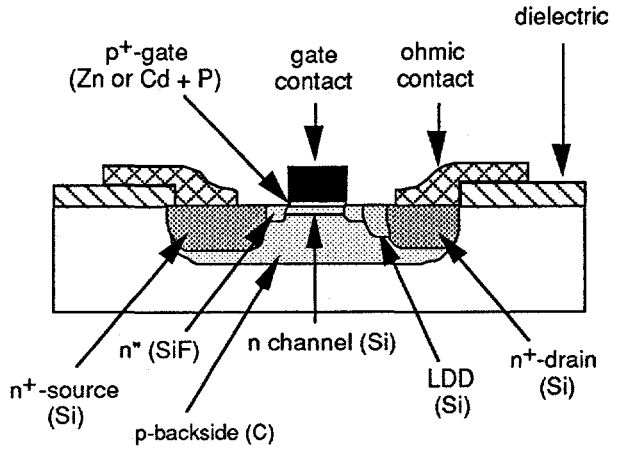

Fig. 1. Schematic of self-aligned GaAs JFET showing the multiple implant areas.

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defined by a deposition and etchback process and a lightly-doped drain (LDD or n') region was implanted with 50 keV ^{29}Si ions self-aligned to the sidewalls. Finally the n^+ source and drain implant is done with a photolithographically defined LDD region. This lateral doping profile is critical to minimizing output conductance and achieving good channel pinch-off characteristics. In addition to the n-type doping profile, the p^+-gate region has been made extremely shallow by using the heavy acceptor species Zn or Cd implanted at 45 keV to achieve very shallow p^+-regions as shown in Fig 2 for Cd. Fig 2 also shows the utility of P co-implantation for reducing indiffusion of Cd. This is understood by the P increasing the probability for Cd to occupy the Ga-sublattice and thereby reduce interstitial diffusion [7]. Backside confinement is achieved with carbon implantation (90 keV, $4x10^{12}$ cm^{-2}) which has been shown to give enhanced high-frequency performance compared to Mg (or Be) implants particularly at higher doses [8]. The gate contact is sputter deposited tungsten defined by electron beam lithography and patterned in a subtractive RIE-based etch [9]. Realization of a near vertical gate profile is critical since the gate contact feature acts as a self-aligning mask for n-type implants in the source and drain regions. All implants are activated in a single rapid thermal anneal at 800 to 850 °C for 15 s. Finally, ohmic contacts (Ge/Au/Ni/Au) are defined by liftoff and alloyed at 400 °C for 15 s.

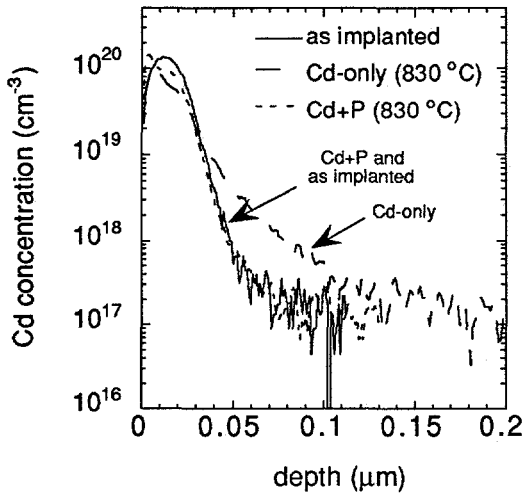

Fig. 2. SIMS profile of implanted Cd (45 keV, $3x10^{14}$ cm^{-2}) alone or along with P($^{62}P_2$: 40 keV, $3x10^{14}$ cm^{-2}) as implanted or annealed at 830 ° for 15 s.

III. DEVICE RESULTS

Fig 3 shows DC performance of a 0.3 μm x 20 μm GaAs JFET with a Cd-implanted gate region that demonstrates a transconductance of 230 mS/mm and a saturation current of 160 mA/mm for V_{GS} = 1 V and V_{DS} = 1.5 V. Although this device has a threshold voltage of ~-0.2 V, this can be shifted to enhancement mode operation by adjusting the channel implant dose. The output conductance (g_{DS}) between V_{DS} = 1.5 to 2.5 V is 17 mS/mm and the sub-threshold slope, as seen in Fig. 4, is 110 mV/decade. Both of these values are comparable to previous longer gate length implanted JFETs [4] and are the result of the optimized doping profiles in this device. The gate diode has a forward turn-on voltage at 1 mA/mm of gate current of 1.0 V, allowing the JFET to operate at low power with minimal gate leakage on a 1 V power supply.

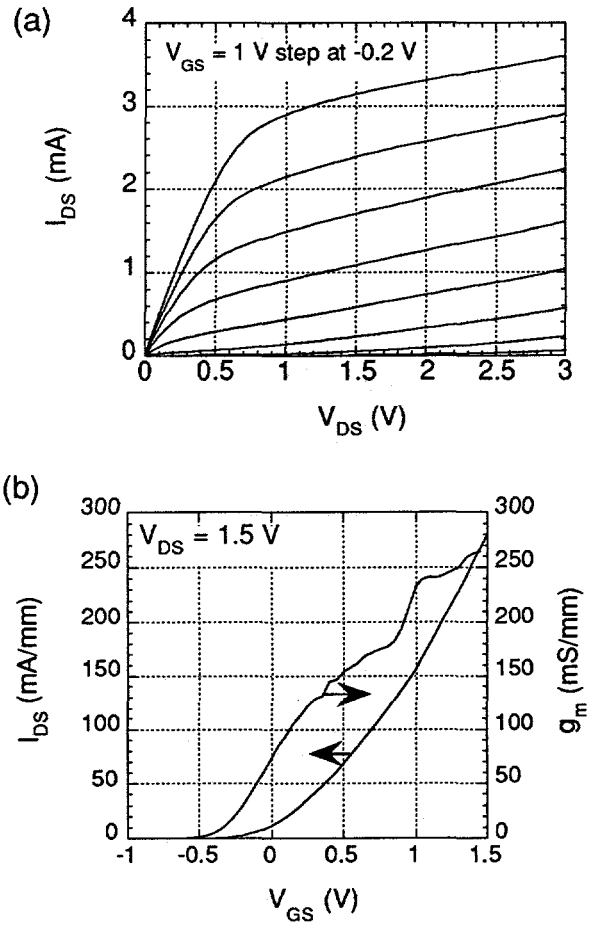

Fig. 3. DC performance of a 0.3 x 40 μm^2 Cd-gate GaAs JFET.

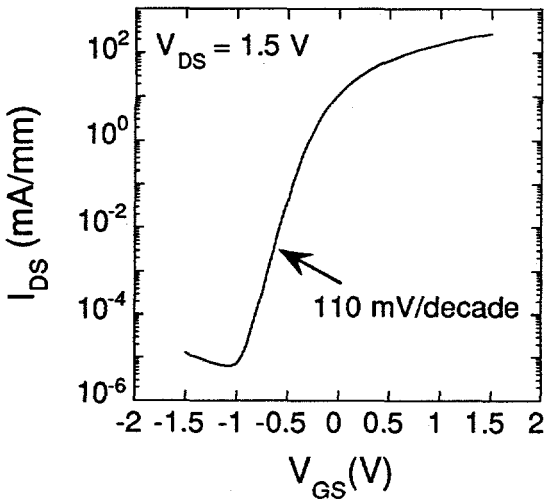

Fig 4. log I_{DS} versus V_{GS} at V_{DS} = 1.5 V showing a sub-threshold slope of 110 mV/decade.

Fig 5 shows the dependence of intrinsic f_t (corrected for pad capacitance) versus gate length at several values of V_{DS} for Cd-gate JFETs which follows a $1/L_g$ dependence down to 0.4 μm before showing some roll-off at the shortest gate length. At increasing drain biases intrinsic f_t decreases due to the increase in the effective gate length with the increase in the gate/drain depletion region.

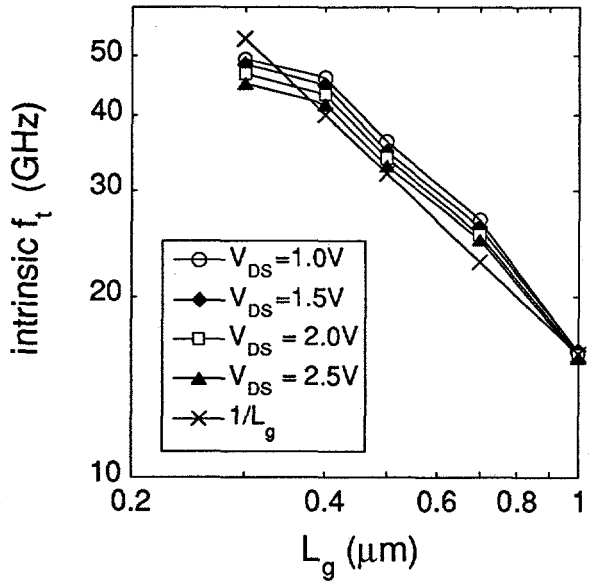

Fig. 5. f_t vs. gate length for various drain biases for 40 μm wide GaAs JFETs at V_{GS} = 1.0 V.

Fig. 6 shows the intrinsic f_t and I_{DS} versus gate bias at V_{DS} = 1 V for a 0.3 x 40 μm² Zn-gate JFET. This shows the enhancement mode operation of the device as well as the excellent frequency performance for 1 V operation. An intrinsic unity current gain cut-off frequency of 52 was measured for this device. The roll off at higher gate biases was due to increased gate conduction. The maximum oscillation frequency (f_{max}) on this device was 48 GHz. f_{max} was limited by a high ohmic contact resistance on this device (0.27 Ω-mm, < 0.1 Ω-mm is typically achieved) and the high resistance of the small geometry tungsten gate contact. A gold overlayer will be required to reduce this gate resistance in future devices.

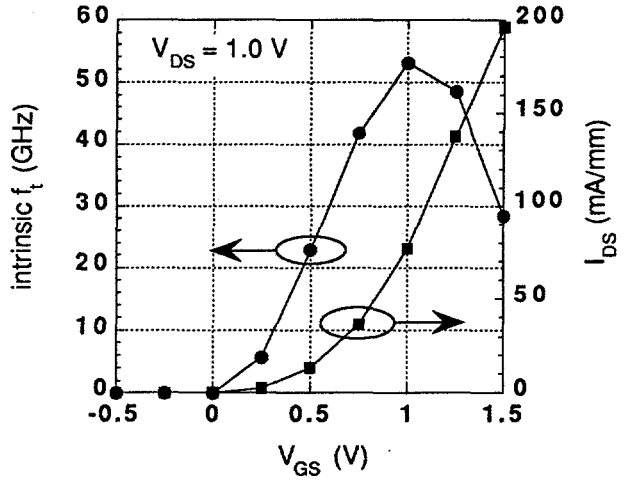

Fig. 6. Intrinsic f_t and I_{DS} versus V_{GS} at V_{DS} = 1.0 V for a 0.3 x 40 μm² Zn-gate GaAs JFET.

IV. CONCLUSION

In conclusion, we have demonstrated 0.3 μm gate length all ion implanted GaAs JFETs with V_{GS}(on) = 1 V with DC and rf performance comparable to a similar gate length GaAs MESFET with V_{GS}(on) ~ 0.6 V. Since this JFET is based solely on ion implantation it should be readily manufacturable. In addition, this device should be very attractive for low-power, low-voltage, high-frequency operation.

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