

FORMATION OF A BURIED SOFT LAYER IN SiC FOR 'COMPLIANT SUBSTRATE' BY ION IMPLANTATION

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Radiation damage and its removal have been studied in ion implanted 6H-SiC by Rutherford backscattering/Channeling (RBS). We have implanted Ga and Ti at 800°C using doses of 1×10^{16} to 2×10^{17} cm⁻². The implanted samples have been subsequently annealed at 1050°C, and then at 1400°C for 30 sec to study the removal of damage produced during implantation. The energies of implanted species have been chosen to obtain 20 - 40 nm projected ranges to form a buried metallic or graphitic layer. No significant damage removal has been observed after 1050°C anneal, however 1400°C annealing of 40 and 120 keV Ga implanted samples (fluence 2×10^{16} cm⁻²) resulted in significantly less damage as can be observed from RBS/Channeling data. In the case of Ti implanted samples annealing led to an appreciable increase in the channelled backscattering yield, which might be due to the formation of some new phase (e.g. TiSi or TiSi₂) and may be related to distortions of the existing lattice.

INTRODUCTION

High-quality thin films epitaxially grown on a mismatched substrate have found applications in many areas of electronics, optics and optoelectronics [1-2]. However, the films used are thinner than their critical thickness, since the quality of the film and hence the performance and reliability of devices start deteriorating beyond the critical thickness. To circumvent this limitation compliant substrate has been proposed [3]. The main idea of this approach is to use very thin flexible substrates, which would comply to the overgrowth. If the film grown on top of this substrate is thicker than the substrate, then the film starts to play the role of the substrate, and the defects will be predominantly formed in the substrate thus leaving the film of a very good quality. Although the original idea of a thin free standing membrane [3] is appealing, the shortcomings of this approach (e.g. small areas, difficulties in handling, warping) led us to the idea of a compliant substrate consisting of a thin compliant membrane bonded by a soft viscous layer to a thick rigid substrate.

In this paper we present initial results of the creation of a soft buried metallic or graphitic layer in SiC by ion implantation. The implant species should be selected by their ability to form amorphous (e.g. Si, C implantation), low melting metallic (e.g. Ga, In implantation) layers, or be able to produce a silicide layer (e.g. Ti implantation) which would be able to accumulate stress generated in compliant membrane during the thin film deposition. Since the crucial part of this approach is to find appropriate implantation and annealing parameters which would also allow to achieve a nearly defect-free thin compliant layer, much of the discussion will be devoted to this.

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EXPERIMENT

The samples were prepared by implanting 40, 100, 120 keV Ga⁺ and 35 and 50 keV Ti⁺ ions into n-type 6H-SiC (0001) made by Cree Research, Inc. The SiC wafer was cut into 6 mm × 6 mm pieces, and cleaned with acetone and methanol using an ultrasonic agitator. Implantations were performed at 800°C in a medium current Extrion implanter at Oak Ridge National Laboratory. The samples were tilted 7° to minimize channeling during the implantation. The elevated temperature was chosen to effectively remove the damage *in situ*. Implant fluences ranged between 1×10^{16} and 2×10^{17} cm⁻². Implantation energies were calculated to obtain projected ranges of 20 - 40 nm using the TRIM'95 program. The implanted as well as the virgin reference samples were analyzed by means of RBS/Channeling using 1.6 MeV He⁺ ions at a backscattering angle of 165°. Subsequent analysis of the measured backscattering spectra was performed using the RUMP program. Rapid Thermal Annealing (RTA) was performed at two different temperatures, 1050°C in nitrogen, and 1400°C in argon atmosphere for 30 sec. Some of the samples were also annealed at 1600°C in a conventional furnace in nitrogen for 10 min. The samples were then studied by RBS/Channeling to evaluate the amount of residual damage. Transmission Electron Microscopy (TEM) was carried out for 35 keV Ti implanted and for 120 keV Ga implanted SiC samples after 1600°C annealing using a Topcon EM0002B electron microscope.

RESULTS AND DISCUSSION

Fig. 1 shows RBS spectra for the 120 keV Ga implanted SiC sample (dose 2×10^{16} cm⁻²). The Ga concentration was determined from the Ga peak of the non-aligned spectrum, using RUMP and was found to be in good agreement with the implant fluence. Fur-

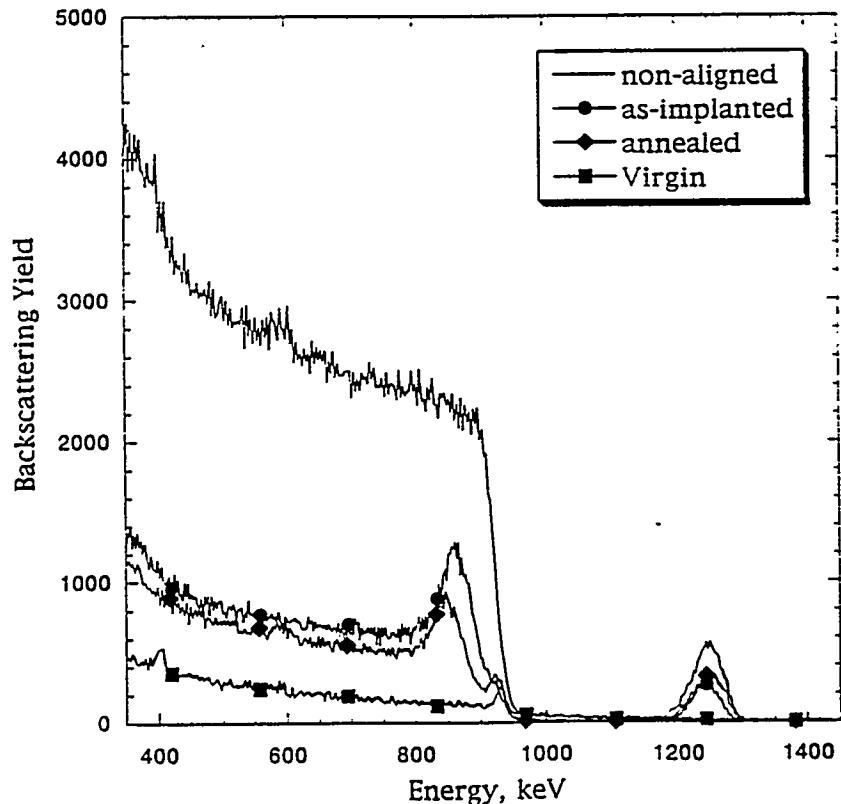


Fig. 1. RBS/Channeling spectra for 120 keV Ga implanted into SiC (dose 2×10^{16} cm⁻²) at 800°C.

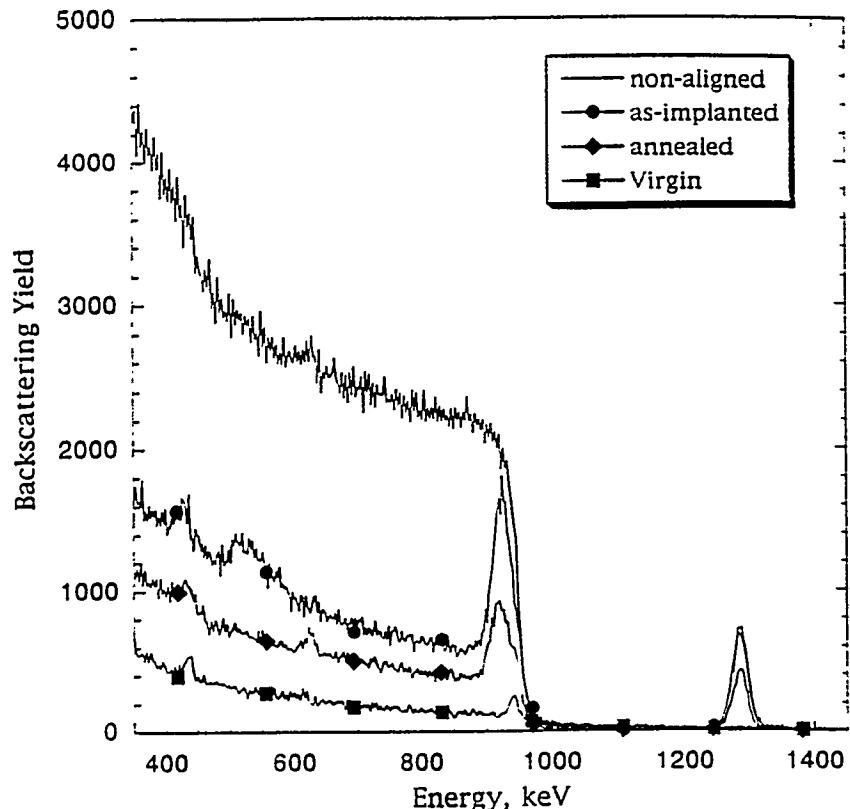


Fig. 2. RBS/Channeling spectra for 40 keV Ga implanted into SiC ($2 \times 10^{16} \text{ cm}^{-2}$) at 800°C .

thermore, the Ga peak is about 2 times smaller for the channelled spectrum which means that about half of the Ga atoms are on substitutional sites ($\sim 1 \times 10^{16} \text{ cm}^{-2}$). Burdel et al [4] reported an appreciable Ga loss during 1900°C anneals, while temperatures of $1400 - 1600^\circ\text{C}$ were shown to be sufficient for successful recrystallization of SiC [5] which determined our choice of annealing temperature. Since the Ga peak remains unchanged after annealing, it may be concluded that no loss of Ga occurs during the anneal. On the other hand, the near-surface damage peak shrunk, both in width and height after 1400°C annealing, as compared to the as-implanted sample. The number of displaced Si atoms can be estimated from the peak and has been found to be $\sim 1 \times 10^{17} \text{ cm}^{-2}$ after the anneal. However, the near-surface layer appears to be of quite good quality, since the surface peak has about the same height as the one of the virgin sample.

The case of the SiC sample implanted with 40 keV Ga ($2 \times 10^{16} \text{ cm}^{-2}$) shown in Fig. 2 is quite different. Since the implantation energy is considerably lower, the damage is produced in a layer very close to the surface and in fact the damage peak overlaps the surface peak. The Ga concentration is substantially lower in this case, being only $0.8 \times 10^{16} \text{ cm}^{-2}$ for non-aligned and as-implanted spectra. This loss of Ga may be explained by sputtering during implantation.

The SiC sample implanted with 35 keV Ti exhibited quite interesting behavior, namely, annealing even at 1050°C appears to lead to the formation of some defects in the top layer, and drastically increases the backscattering yield in the channeling mode (Fig. 3). In fact, practically no channeling could be achieved in these samples after the anneal. In order to be sure that this was a real result we repeated this experiment by implanting 50 keV Ti into SiC at the same temperature but with a lower fluence ($1 \times 10^{16} \text{ cm}^{-2}$). No significant deviation from the above-mentioned result was found. Because this behavior was monitored

exclusively in Ti implanted SiC samples. It would be reasonable to assume that this might be caused by the formation of islands of TiSi or TiSi₂ phases. It is known that TiSi starts forming at a temperature as low as 600°C and TiSi₂ at a temperature close to 800°C [6]; however no noticeable structural changes can be seen in the RBS spectra even though the temperature of implantation was 800°C. Another interesting peculiarity is that the estimate for Ti concentration gives roughly $0.9 \times 10^{16} \text{ cm}^{-2}$ in the as-implanted sample (the fluence was $2 \times 10^{16} \text{ cm}^{-2}$), with the majority of Ti atoms (~80%) being on interstitial sites. It seems that Ti is either spread over a larger region than the RBS peak indicates, or again, as in the case of the sample implanted with 40 keV Ga (see above), some Ti is lost due to sputtering during the implantation. There was no significant loss of Ti observed in the sample implanted with 50 keV Ti. In any case this matter requires further investigation.

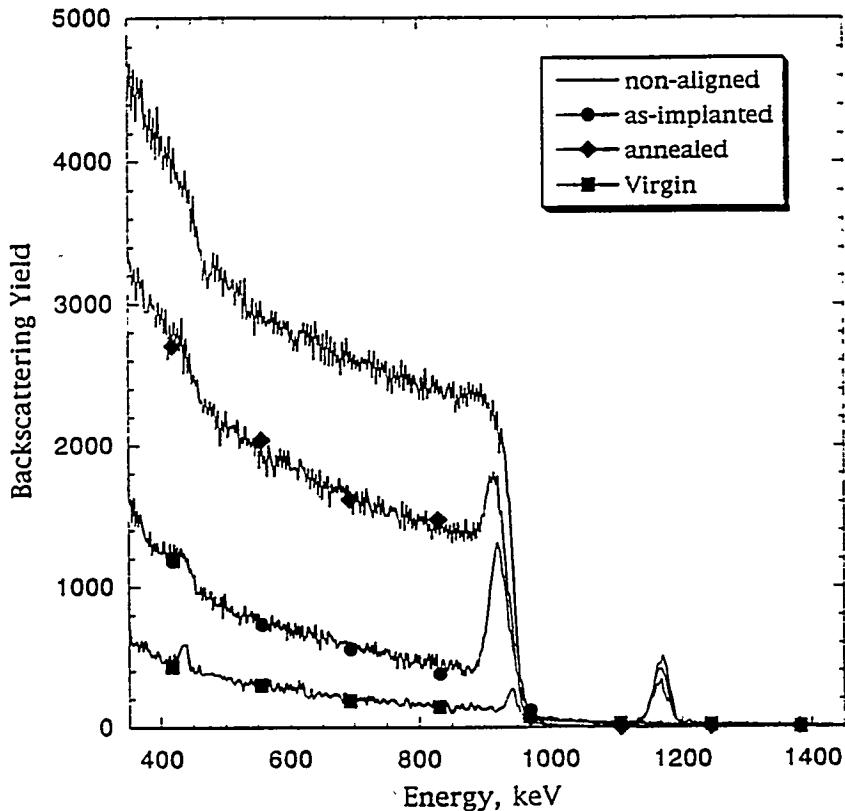


Fig. 3. RBS/Channeling spectra for 35 keV Ti implanted into SiC (dose $2 \times 10^{16} \text{ cm}^{-2}$) at 800°C.

In an attempt to examine the quality and thickness of both the near - surface and the implanted layers, TEM was performed on 2 samples. The samples were first covered with SiC powder to avoid the loss of Si from the surface, and then annealed in nitrogen at 1600°C for 10 min, cleaned and prepared for TEM.

Fig. 4a is a TEM image of the SiC sample implanted with 35 keV Ti at 800°C (dose $2 \times 10^{16} \text{ cm}^{-2}$). The implanted layer is not clearly seen and contains much damage and, probably, a mixture of phases. The top layer is only a few Å thick, and seems to be of relatively good quality. However, underneath some agglomeration of point defects is observed.

The sample shown in Fig. 4b was implanted with 120 keV Ga at 800°C (dose $2 \times 10^{16} \text{ cm}^{-2}$). In this case the implanted region is located much deeper due to the higher implantation energy, and looks fairly continuous. The top layer is ~5-6 nm thick and seems to be of comparably good quality, with few detectable defects.



a



b

Fig. 4. TEM of the samples implanted at 800°C (dose $2 \times 10^{16} \text{ cm}^{-2}$) with 35 keV Ti (a) and 120 keV Ga (b) and annealed at 1600°C in nitrogen for 10 min.

The TEM and RBS results indicate that it is possible to form a rather well-defined buried layer by ion implantation. The quality of the top layer turns out to be of reasonably good quality which is one of the essential parts of our approach. However, one of the ideas underlying our model is the formation of a continuous metallic layer, which requires the use of much higher fluences. In fact, we have implanted several SiC samples with $2 \times 10^{17} \text{ cm}^{-2}$, 100 keV Ga^+ ions at 800°C. No channeling could be performed on these samples, even after 1400°C annealing. It is likely that a higher annealing temperature may bring about partial removal of the damage generated by this high fluence. However, possible solution might involve the use of higher energy ions, which would penetrate deeper and create less damage in the near surface region.

CONCLUSIONS

The implantation of 35 keV Ti into SiC at 800°C (dose $2 \times 10^{16} \text{ cm}^{-2}$) leads to the formation of a damaged layer. Annealing appears to bring about the formation of islands of an amorphous TiSi_2 phase. The damaged layer starts closer to the surface than predicted by TRIM calculations which leads to a very thin top layer.

Sputtering at low energies (below 50 keV) seems to be a common problem for high fluences, as evidenced by the loss of Ga and Ti observed for 40 keV Ga and 35 keV Ti implantations, respectively.

120 keV implantation of Ga into SiC at 800°C (dose $2 \times 10^{16} \text{ cm}^{-2}$) produces continuous implanted layer, and a reasonably good quality and rather thick (5 - 6 nm) top layer. The amount of damage appears to diminish by ~20% after annealing at 1400°C.

To effectively anneal the damage produced during the implantation, one should use temperatures higher than 1400°C, as no damage removal has been observed after annealing at 1050°C. No significant annealing of damage has been observed even after 1400°C in the SiC samples implanted with $2 \times 10^{17} \text{ cm}^{-2}$ of 100 keV Ga.

Further investigations will study the effects of higher energy/higher fluence implantation on the quality of the top and implanted layers, and attempts will be made to grow GaN single crystal films on top of the created 'compliant substrate'.

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REFERENCES

1. J.B. Kuang, Y.K. Chen, D. Sivco, A.Y. Cho, and L. Eastman, *Appl. Phys. Lett.* **57**, p. 1784 (1990).
2. C.E. Zah, R. Bhat, K.W. Cheung, N.C. Andreadakis, C.J. Fauire, S.G. Menocal, E. Yablonovitch, D.M. Hwang, M. Koza, T.J. Gmitter, and T.P. Lee, *Appl. Phys. Lett.* **57**, p. 1608 (1990).
3. C.L. Chua, W.Y. Hsu, C.H. Lin, G. Christenson, and Y.H. Lo, *Appl. Phys. Lett.* **64**, p. 3640 (1994).
4. K.K. Burdel', A.V. Suvorov, and N.G. Chechenin, *Sov. Phys. Solid State*, **32**, p. 975 (1990).
5. H. Bohn, J.M. Williams, C.J. McHargue, and G.M. Begun, *J. Mater. Res.* **2**, p. 107 (1987).
6. S.P. Murarka, Silicides for VLSI Applications, Academic Press, Inc., New York, 1983, pp. 100-102.