Fabrication of Large Area Gratings with Sub-micron Pitch using Mold Micromachining

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Abstract

In this work, we have applied mold micromachining and standard photolithographic techniques to the fabrication of parts integrated with 0.4 micron pitch diffraction gratings. In principle, the approach should be scaleable to considerably finer pitches. We have achieved this by relying on the thickness of deposited or grown films, instead of photolithography, to determine the grating pitch. The gratings can be made to extend over large areas and the entire process is compatible with batch processing. Literally thousands of parts can be batch fabricated from a single lot of six inch wafers. In the first stage of the process we fabricate a planarized silicon dioxide pad over which the silicon nitride wave guide runs. The grating is formed by first patterning and etching single crystalline silicon to form a series of trenches with well defined pitch. The silicon bounding the trenches is then thinned by thermal oxidation followed by stripping of the silicon dioxide. The trenches are filled by a combination of polysilicon depositions and thermal oxidations. Chemical mechanical polishing (CMP) is used to polish back these structures resulting in a series of alternating 2000Å wide lines of silicon and silicon dioxide. The thickness of the lines is determined by the oxidation time and the polysilicon deposition thickness. The silicon lines are selectively recessed by anisotropic reactive ion etching, thus forming the mold for the grating. The mold is filled with low stress silicon nitride deposited by chemical vapor deposition. A wave guide is then patterned into the silicon nitride and the mold is locally removed by a combination of deep silicon trench etching and wet KOH etching. This results in a suspended diffraction grating/membrane over the KOH generated pit.

Keywords: Micromachining, Mold, Batch fabrication, Diffraction Grating.

Introduction

Micromachining is increasingly employed for the fabrication of a wide variety of structures, examples range from accelerometers to ink jet print heads to micromotors to atomic force microscope tips to sensors. The attraction of silicon based micromachining technologies is that they offer the advantages of batch fabrication and leveraging of the extensive technology base supporting the silicon integrated circuit industry. Micromachining processes can be classified into three main types, bulk micromachining, surface micromachining, and mold micromachining. Bulk micromachining is the oldest class of process and involves the fabrication of parts through the large scale removal of the bulk substrate, typically by wet etching, though more recently by reactive ion etching using fluorine based high density plasmas. Bulk micromachining has been used to fabricate such things as ink jet nozzles and accelerometers. Surface micromachining involves the deposition and patterning of thin film structural and sacrificial layers. This class of micromachining has been used to fabricate devices such as micromotors. The structural layers are typically ~2 μm thick polysilicon. The final class of micromachining is mold micromachining. In this process, a mold is created which is then filled with a structural material. The mold is then removed. Recent advances in silicon trench etching have enabled the integration of bulk, mold and surface micromachining [1]. In this work, we have used mold micromachining to generate gratings which have features far finer than those obtainable using standard photolithography. Our demonstration vehicle incorporated a low stress silicon nitride wave guide and a grating with a nominal pitch of 0.4

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μm, it is schematically represented in Fig.1. All of the processes described here are based on those supported by the integrated circuit and micromachining industries and all are batch compatible.
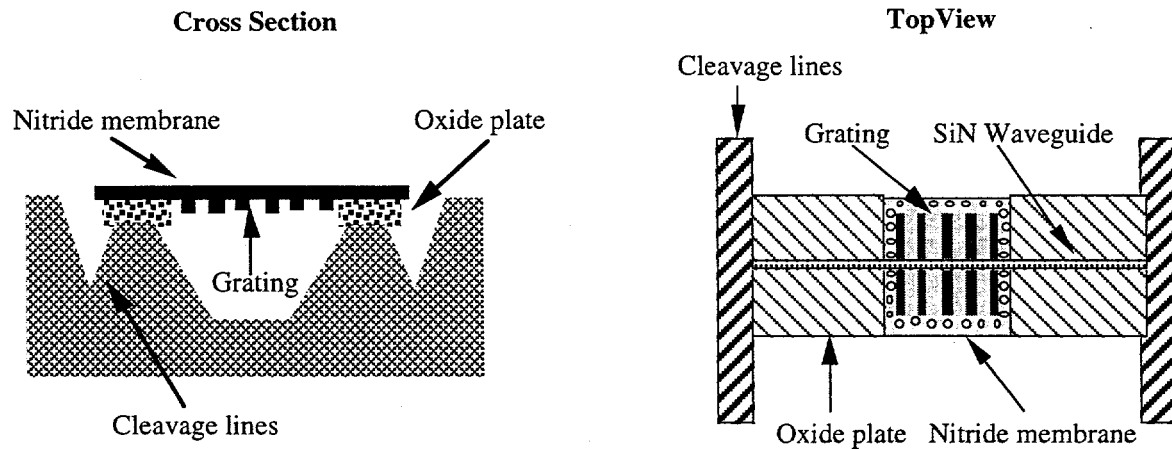
Cross Section   **TopView**

Fig. 1

Schematic showing the main components of the test vehicle used in this work.

Fabrication Approach

Standard monitor grade 6 inch {100} silicon wafers were used throughout this work. In the first stage of the process a recessed planar, relatively low refractive index, silicon dioxide pad is fabricated for the wave guide to run along. This is done by cutting a trench through a silicon nitride oxidation mask and into the silicon substrate. The trench is then filled with a combination of thermally grown and chemical vapor deposited (CVD) silicon dioxide. The wafers are then planarized using CMP, Fig. 2. A cross section showing the oxide pad is given in Fig. 3. Next, the mold for the grating is fabricated, Fig. 4. This is done by patterning and etching a series of lines and spaces with a 1.2 micron pitch. The lines are thinned down to 3750Å by first oxidizing the wafer and then striping the oxide from the trenches using HF. This is followed by the growth of 2000Å of silicon dioxide by thermal oxidation and the deposition of 2440Å of undoped, fine grained polysilicon. The polysilicon is oxidized until the two growing oxide films met and lateral oxidation stops. An example of a cross section through a mold at this step of the process is given in Fig. 5. CMP is then used to expose the edges of the vertically oriented, alternating sheets of oxide and silicon. The grating mold is completed by preferentially recessing the silicon 500Å with respect to the silicon dioxide using a high selectivity reactive ion etch. This mold is filled with 4000Å of low stress CVD silicon nitride with a refractive index of 2.1. Following this, the waveguide is patterned into the top of the silicon nitride. The next steps involve the removal of the mold. This is done by first patterning and etching through the silicon nitride and trenching into the underlying silicon. The depth of the holes etched into the silicon is determined by the hole pitch and the orientation of the {111} planes. A wet KOH etch then removes the silicon, polysilicon and silicon dioxide used to form the mold. This is shown schematically in Fig. 6. The KOH etch is also used to form "crackoffs" to facilitate the separation of the individual die. These are deep trenches etched into the silicon along which a crack can propagate. A series of different views of the finished parts are given in Figs. 7-9.

1) Deposit SiN, photo and etch, SiN and trench well 1.4 µm into Si

2) Grow 2 microns of thermal oxide
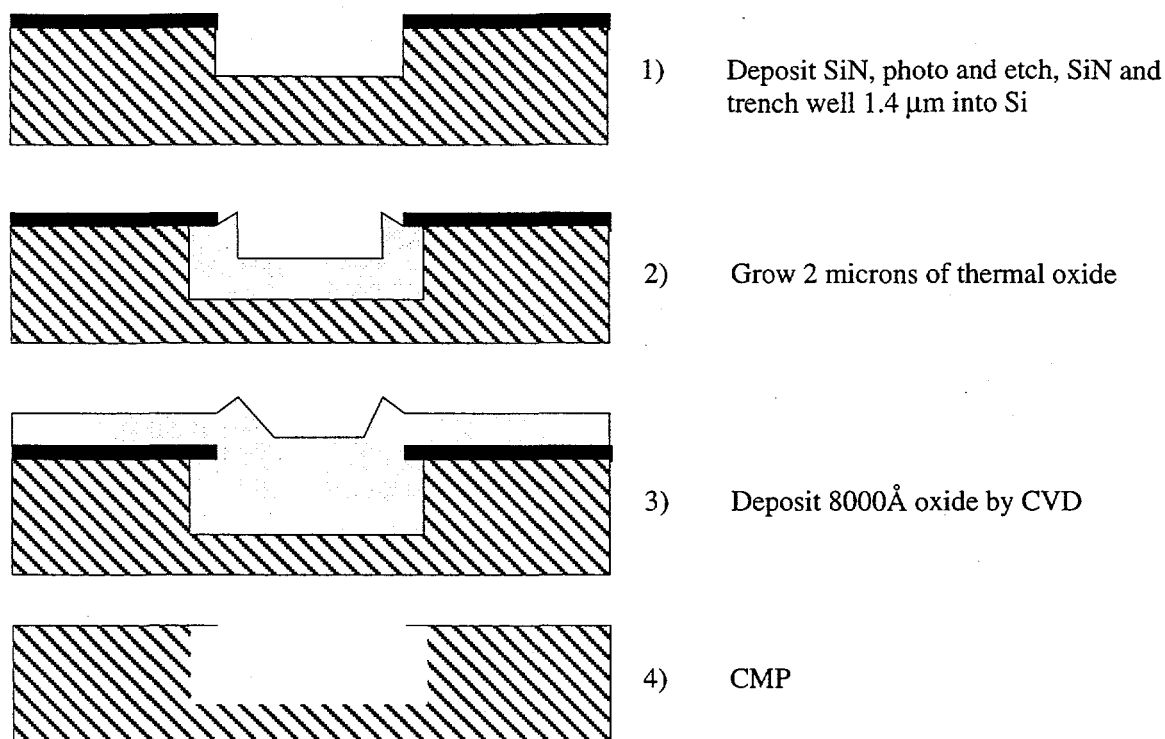
3) Deposit 8000Å oxide by CVD

4) CMP

Fig. 2.

Schematic of the process used to form the oxide pad on which the silicon nitride wave guide will run.
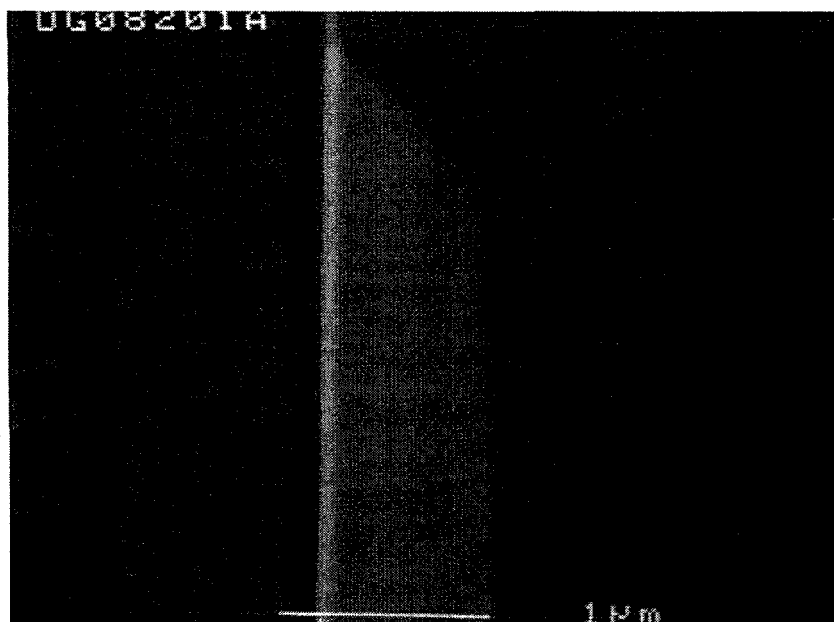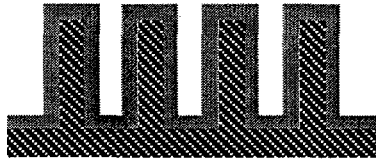

Fig. 3.

Micrograph of the cross section through a vertically orientated oxide pad.
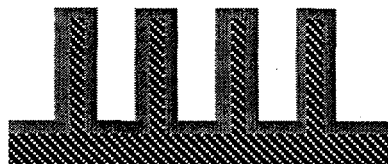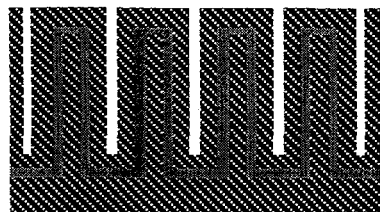
1) Etch 0.6 µ wide, 2µ deep trenchs on 1.2 µ centers.
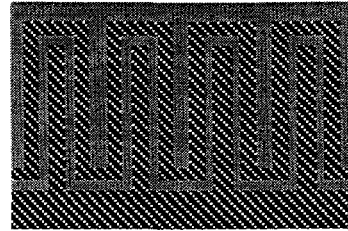
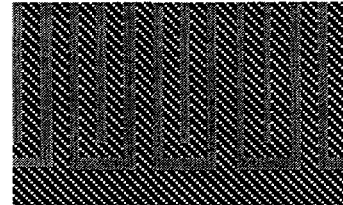2) Grow 2550A thermal oxide to thin the Si.

3) Strip thermal oxide in HF.

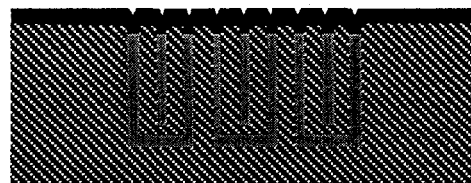4) Grow 2000Å thermal oxide, leaves 2000Å Si core
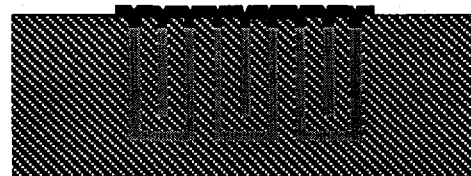
5) Deposit 2440Å poly Si

6) Oxidize until trenches close

7) CMP till planar and the edges are exposed.

8) Recess silicon (or silicon dioxide) using reactive ion etching.

9) Deposit 4000Å SIN, refractive index 2.01.

10) Photo pattern and RIE etch SIN with a 2000Å timed etch to from wave guide.

Fig. 4

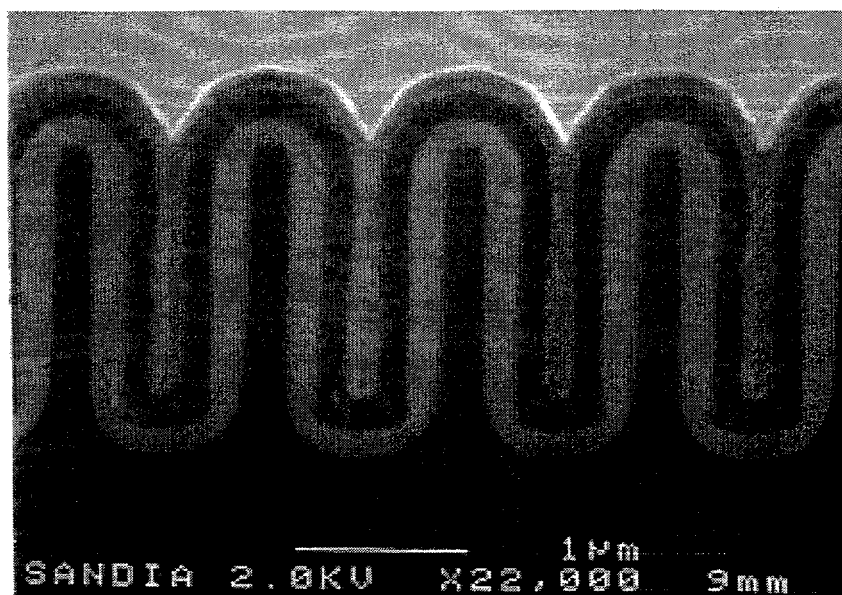Schematic showing the steps involved in mold and waveguide formation.

Fig. 5

Electron micrograph of the cross section through a mold structure prior to CMP.

Top View

Trace of the boundaries of overlaping KOH pits.

Cross section View

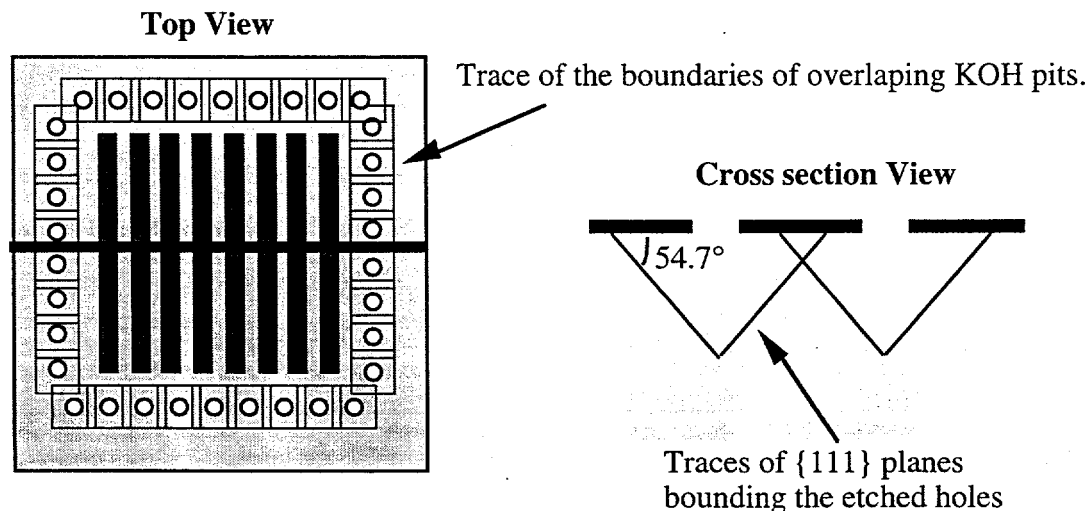54.7°

Traces of {111} planes
bounding the etched holes

Fig. 6.

Formation of the membrane. A series of holes are etched through the silicon nitride and into the underlying silicon substrate. The holes are deep enough that during the subsequent KOH etch the {111} planes bounding the holes will intersect. This creates a series of "outside corners" which are readily attacked by the KOH, leading to removal of the mold under the silicon nitride layer.
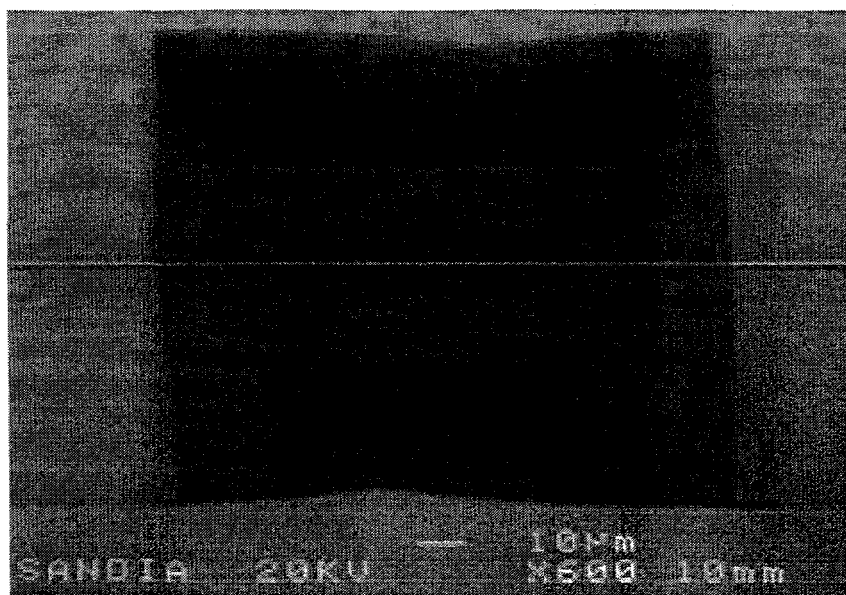
Fig. 7

Scanning electron micrograph of an oblique view of a finished part. The waveguide can be seen running along the upper middle of the photo. The membrane is visible as the dark central rectangle. The lighter, slightly smaller, central rectangle is the grating. The KOH etch access holes are readily visible. The oxide pad has been undercut by ~4μm.
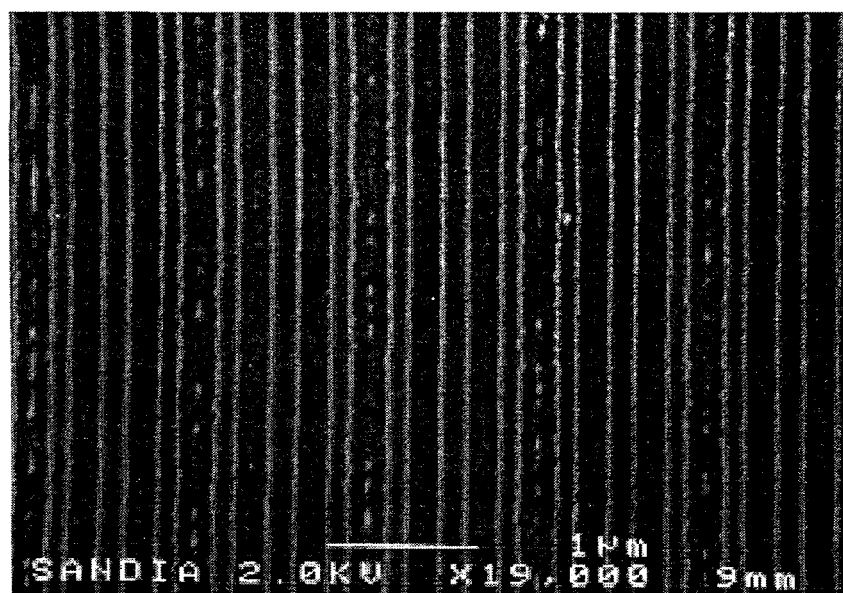

Fig. 8

Scanning electron micrograph of the underside of the silicon nitride grating. The slightly darker portions of the grating were generated by the silicon dioxide portion of the mold. The white "dots" running along the center of some of the wide "oxide" lines are the result of voids along the seam formed during the final oxidation as a result of the slight variations in the oxidation rate of different polysilicon grains.
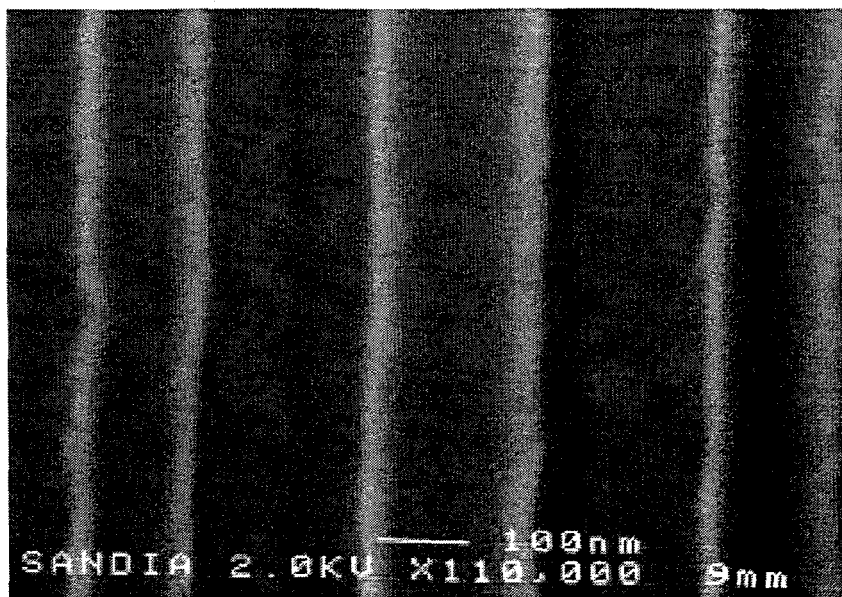
Fig. 9

High magnification scanning electron micrograph of the bottom view of the silicon nitride grating. The slightly darker portions of the grating were generated by the silicon dioxide portion of the mold. The increased roughness of the silicon dioxide-polysilicon interface observed along the far left interface is the result of the slight variations in the oxidation rate of polysilicon grains of differing crystallographic orientation. The error in the line width is the result of either an error in pitch, or errors involved in the measurement system. The errors inherent in the actual polysilicon deposition and oxidation steps are considerably less.

Results and Discussion

All of the steps described above were batch processed so that even though the process is relatively complex, the actual cost per part can be low since a very large number of parts are fabricated simultaneously. Though the minimum feature size generated is below that achievable using standard photolithography, mold micromachining eliminates the need for sequential, low throughput processes such as electron beam patterning. However, it should be noted that if the trend of rapid reductions in integrated circuit critical dimensions continues, then 2000Å minimum feature photopatterning will be readily available within the next 5 years [2]. The mold technique described above has the potential to extend down to considerably smaller dimensions. The major problem with the mold approach is that the fidelity of the completed part is a function of the stability of the processes used to thin, deposit, and grow, the various silicon dioxide and silicon layers. In our case, these problems appear to be the result of either an error in the line pitch, or more likely, an error in the SEM measurement which was used to determine the various dimensions throughout the process. Though this error is relatively easy to correct, there will always be a ~1% (1 sigma) process variation in the polysilicon thickness and somewhat lesser non-uniformity in the oxide thickness. Another problem exists in the determination of the initial silicon line dimension. The oxidation process used to thin the line is very repeatable, however, the amount of line thinning required is determined by a relatively inaccurate SEM measurement.

Due to differing rates of oxidation of the various crystallographic planes of silicon, the poly silicon/oxide interface is relatively rougher than that of the single crystalline silicon/oxide

interface, Figs. 8-9. This roughness also creates a slight, discontinuous seam along the interface between the two oxide layers grown on the polysilicon, Fig. 8.

As was explained above, we have used a series of holes etched in from the top to define the position of the membrane. The depth of the holes was determined by the hole spacing and the orientation of the slowly etching {111} planes. It may also be possible to form the membrane by etching from the back of the wafer. However, this is a much less controllable process since it is dependent upon the wafer thickness and is more sensitive to mask missorientation.

Conclusion

In this work, we have tried to demonstrate how a wide range of micromachining processes, especially mold micromachining, can be applied to the fabrication of optical components. The strength of this approach is that it employs batch processes and tools which are supported by the semiconductor industry infrastructure. We have also demonstrated how mold micromachining can be used to generate large area gratings using standard, batch processed photolithography.

Acknowledgments

References

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2.   *The National Technology Roadmap For Semiconductors*, Semiconductor Industry Association, 1994.

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