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LA-5073-MS

INFORMAL REPORT

MASTER

Using Multiwire Proportional Chamber Decoders

los alamos
scientific laboratory
of the University of California
LOS ALAMOS, NEW MEXICO 87544

UNITED STATES
ATOMIC ENERGY COMMISSION
CONTRACT W-7405-ENG. 36

In the interest of prompt distribution, this LAMS report was not edited by the Technical Information staff.

Printed in the United States of America. Available from
National Technical Information Service
U. S. Department of Commerce
5285 Port Royal Road
Springfield, Virginia 22151
Price: Printed Copy $3.00; Microfiche $0.95

LA-5073-MS
Informal Report
UC-28
ISSUED: November 1972

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by

E. R. Martin
D. F. Jones

ABSTRACT

MP-Division has now designed and constructed the decoder units for processing the signals from up to 8K active wires in a multiwire proportional chamber system, reducing these wire hits to binary information, and storing these data in an output buffer for computer consumption. This note describes in detail the operation of these units from the user point of view and discusses briefly how one might interface these units to various minicomputer systems.

USING MULTIWIRE PROPORTIONAL CHAMBER DECODERS

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I. INTRODUCTION

The purpose of this report is to describe the function and operation of the digital decoder units constructed for the equipment pool by Group MP-3. The primary function of these units is to decode and store for computer consumption the amplified signals from multiwire proportional chambers (MWPC), but they will decode into binary data any signal presented at the appropriate inputs.

The first main part of this report will attempt to make the potential user sufficiently conversant with the decoder that he can use it as a black box in his experimental set-up, aware of its idiosyncrasies, capabilities and limitations, albeit without such detailed engineering technicalities as one would require for its construction.

The second section of the report will dwell on somewhat greater technical detail in order to permit an average technician to do basic troubleshooting and routine maintenance. For exact mechanical and electrical drawing detail of each element of the decoder system, the interested reader is referred to the Group MP-1 technical files where such information is available.

A final section will treat the general problem of interfacing the decoders to computer central processors and the specific methods we have used to interface up to 40 of these decoders to both the Data General Supernova and DEC PDP-11 computers.

II. HOW DOES ONE USE THE DECODER UNITS?

A. General Philosophy

The decoder unit is designed to fill the gap between the amplified output at each active wire in a multiwire proportional chamber (MWPC) and the data acquisition device - usually an on-line minicomputer. In accomplishing this function, special care has been taken to preserve every advantage that the MWPC offers in particle detection systems; viz., good time resolution (~20 nsec), high background rates (up to 10^6 hits per wire per second), self-triggering capability, and high system event rates - the latter limited ideally solely by the data storage medium. In addition, we do not limit the number of wires struck per wire plane per event, except by the size of the output storage buffer. This permits decoding events where there are large particle multiplicities.

Fig. 1 indicates a simplified drawing of how the decoder accomplishes these goals. Each decoder handles up to 200 signal inputs, utilizing 8-bit output data, a format particularly suited to byte-oriented data acquisition computers. As shown, the OR-ed output of all inputs is made available promptly at a GATE OUT terminal, where it is available for use in a coincidence requirement, if desired. This permits the chambers to be used as self-triggering detectors.

The individual signals are now subjected to a 500 ±5 nsec delay, which allows for decision-making coincidence time, while at the same time preserving the intrinsic ~20 nsec time resolution of the MWPC. When a GATE IN signal is received at the decoder after the proper time delay, the data then present at the shift register inputs are memorized, the unit is disabled for further data until the present event has been processed, and conversion to binary format is immediately begun. This latter is accomplished in the following manner: The same clock signal which shifts the data along the input shift register one stage per clock pulse is also used to drive a binary scaler whose count is stored in the output buffer for each set bit shifted out of the input shift register.

The output storage buffer consists of an 8-bit push-down data stack which is written only so deeply as there were data present on the inputs, up to a maximum of 8 wire hits. The 8-wire limit per 200 inputs is not a fundamental limitation of the method, but represents a reasonable choice for a fairly complex event. Should the user desire to record more than 8 wire hits per plane of 200 wires - and it is doubtful that more complex particle trajectories could be reconstructed from the data without a very large number of chambers - he can simply use more decoders and connect fewer active wires to each unit. Unused inputs can be left floating without causing spurious data.

Clearly, the conversion time for decoding up to 8 hits on 200 inputs is dependent on the rate of internal clocking in the unit. Since TTL integrated circuits are used throughout, clocking rates are limited to below about 20 MHz. In our units, the total conversion time is set at approximately 12 microseconds per event.

At completion of internal conversion, the unit gives a READ READY signal, and is now prepared to have its data read. This is accomplished by giving a READ signal. The data in the buffer stack is now "pulled", i.e., the last datum in is the first read. A SHIFT pulse is given when it is desired to read the next struck wire in the event, which is then read by another READ pulse. In this way, the device reading the buffer need read only so deeply as real data is stored; as soon as a zero is encountered on the data lines, the last struck wire has been read.

In practice, two decoder units are generally read together simultaneously to form 16-bit data words for maximum rate transfer. More will be said on this point in the section dealing with computer interfacing.

At the conclusion of the data read operation, the acquisition device must give a RESET pulse, which clears the decoder unit and activates it for the next event.

B. Physical Parameters

Figs. 2a, 2b, 2c, 2d and 2e show the physical construction of a 200-wire decoder unit. It is built to be mounted in a standard 19" rack, occupies 5-1/2" of rack space, and requires a depth of 25". It can be most conveniently mounted on side rail supports in order to facilitate cable connection and maintenance.

It is wholly self-contained so far as power and cooling are concerned. It requires 110 V.A.C., 60 cycle and uses about 120 watts of power.

All of the input and output, as well as control line connections are made to the unit at the rear of the chassis, except for the GATE OUT and GATE IN signals, which are brought to coaxial connectors on the front panel.

C. Front Panel Switches and Indicators

The front panel is illustrated in Fig. 2e, and most of the labels for switches and indicators are self-explanatory. When the unit has received a GATE IN signal, the busy light is lit, and remains on until the unit receives a RESET pulse. At the speeds with which data are handled in normal operation, no indicators will ever be seen, except that the intensity of the BUSY light is a crude indicator of percentage deadtime. The indicators are mostly used for set-up and testing, when the decoders are being operated manually. The OVER 8 indicator will be lit whenever the present event being processed has received more than eight inputs for a single event. In this case, a signal is also made available to the computer interface, so that the unit can be simply reset without reading its data if the user so desires. The OVER 8 indicator merely signals the loss of some data in the output buffer (only the eight highest-numbered inputs can be stored), but does not interfere in any way with the conversion or data reading process. The user is thus only made aware of data loss - he is not prevented from reading what data is there.

The binary data lights indicate the data at the top of the push-down data buffer. Thus, as each SHIFT pulse is given in order to read the next datum, the lights will follow the changing data - always indicating the data word which is currently being read. The binary weights for the various data indicators are labeled on the unit front panel as shown.

The RESET and SHIFT pushbutton switches have exactly the same function as their control signal counterparts. They permit an event to be manually read out for test and set-up purposes. In practice, an event is handled manually in the following manner: As soon as a GATE IN signal is received, the busy light goes on, the OVER 8 indicator light is lit if applicable, and the last struck wire is shown in the data indicator lights. If now the SHIFT pushbutton is pressed, the data lights will change to show the next datum, and so on until the data lights will indicate a zero, which means the final datum has been shown and no more data is present for that particular event. A manual RESET must now be given to ready the unit for the next event.

D. Input Connections and Pulse Requirements

Fig. 2b shows the connectors on the back panel of the unit. Jacks A-J are 50-pin connectors, which permit the connection of 200 twisted pair inputs. Table 1 lists the pin-by-pin connection of inputs to the unit; e.g. an input at connector C, pins 47 and 48, will yield the number 127 after conversion by the decoder. The decoder is designed to accept positive input signals which go from ground potential to +3.5 volts, but since these inputs are all differentially driven, negative signals will be acceptable by simply reversing the + and - wires on the signal lines as shown in Table. 1. Each input is transformer-coupled inside the decoder so that both leads of the input twisted pair must be connected. This eliminates crosstalk altogether, and enormously reduces noise pick-up.

Because of internal transformer coupling, the input signals must have risetimes of better than 50 nsec, and durations no greater than a few microseconds. The inputs will respond to signals as short as twenty nanoseconds.

E. Data and Control Signal Lines

Jacks L and K on the rear panel are the data output connectors, and Jack M provides control line connections to the decoder. The pin connections to these connectors are given in Table 2.

The data outputs are jumpered to both output connectors to permit data busing on the output lines. Thus connectors L and K are identical. This permits busing data lines in several different ways selected by the user. All eight data lines from many decoder units can be bused together very simply as shown in Fig. 3a. A somewhat more useful data scheme for 16-bit computers is shown in Fig. 3b, where decoder units are linked on the data bus in groups of two to permit 16-bit data word transfers. Data is outputted via tri-state logic differential line drivers gated by the READ signal.

Each decoder must be provided separate RESET, READ and SHIFT signals. We found very early in the development that a general RESET line gave rise to severe crosstalk problems, and that occasionally it is useful to be able to reset the units individually. A separate OVER 8 signal is provided by each unit. Likewise, each unit is capable of providing its own separate READ READY signal.

TABLE I

	A	B	C	D	E	F	H	J		A	B	C	D	E	F	H	J
1	200+	175+	150+	125+	100+	75+	50+	25+	26	188-	163-	138-	113-	88-	63-	38-	13-
2	200-	175-	150-	125-	100-	75-	50-	25-	27	187+	162+	137+	112+	87+	62+	37+	12+
3	199+	174+	149+	124+	99+	74+	49+	24+	28	187-	162-	137-	112-	87-	62-	37-	12-
4	199-	174-	149-	124-	99-	74-	49-	24-	29	186+	161+	136+	111+	86+	61+	36+	11+
5	198+	173+	148+	123+	98+	73+	48+	23+	30	186-	161-	136-	111-	86-	61-	36-	11-
6	198-	173-	148-	123-	98-	73-	48-	23-	31	185+	160+	135+	110+	85+	60+	35+	10+
7	197+	172+	147+	122+	97+	72+	47+	22+	32	185-	160-	135-	110-	85-	60-	35-	10-
8	197-	172-	147-	122-	97-	72-	47-	22-	33	184+	159+	134+	109+	84+	59+	34+	9+
9	196+	171+	146+	121+	96+	71+	46+	21+	34	184-	159-	134-	109-	84-	59-	34-	9-
10	196-	171-	146-	121-	96-	71-	46-	21-	35	183+	158+	133+	108+	83+	58+	33+	8+
11	195+	170+	145+	120+	95+	70+	45+	20+	36	183-	158-	133-	108-	83-	58-	33-	8-
12	195-	170-	145-	120-	95-	70-	45-	20-	37	182+	157+	132+	107+	82+	57+	32+	7+
13	194+	169+	144+	119+	94+	69+	44+	19+	38	182-	157-	132-	107-	82-	57-	32-	7-
14	194-	169-	144-	119-	94-	69-	44-	19-	39	181+	156+	131+	106+	81+	56+	31+	6+
15	193+	168+	143+	118+	93+	68+	43+	18+	40	181-	156-	131-	106-	81-	56-	31-	6-
16	193-	168-	143-	118-	93-	68-	43-	18-	41	180+	155+	130+	105+	80+	55+	30+	5+
17	192+	167+	142+	117+	92+	67+	42+	17+	42	180-	155-	130-	105-	80-	55-	30-	5-
18	192-	167-	142-	117-	92-	67-	42-	17-	43	179+	154+	129+	104+	79+	54+	29+	4+
19	191+	166+	141+	116+	91+	66+	41+	16+	44	179-	154-	129-	104-	79-	54-	29-	4-
20	191-	166-	141-	116-	91-	66-	41-	16-	45	178+	153+	128+	103+	78+	53+	28+	3+
21	190+	165+	140+	115+	90+	65+	40+	15+	46	178-	153-	128-	103-	78-	53-	28-	3-
22	190-	165-	140-	115-	90-	65-	40-	15-	47	177+	152+	127+	102+	77+	52+	27+	2+
23	189+	164+	139+	114+	89+	64+	39+	14+	48	177-	152-	127-	102-	77-	52-	27-	2-
24	189-	164-	139-	114-	89-	64-	39-	14-	49	176+	151+	126+	101+	76+	51+	26+	1+
25	188+	163+	138+	113+	88+	63+	38+	13+	50	176-	151-	126-	101-	76-	51-	26-	1-

TABLE II

	K L	M
1	Out 1+	Read +
2	Out 1-	Read -
3	Out 2+	Shift +
4	Out 2-	Shift -
5	Out 4+	Reset +
6	Out 4-	Reset -
7	Out 8+	Over 8+
8	Out 8-	Over 8-
9	Out 16+	Read Ready +
10	Out 16-	Read Ready -
11	Out 32+	N.C.
12	Out 32-	N.C.
13	Out 64+	N.C.
14	Out 64-	Ground
15	Out 128+	Ground
16	Out 128-	Ground
17	Jumper	Ground
18	Jumper	Ground
19	Jumper	Ground
20	Jumper	Ground
21	Jumper	Ground
22	Jumper	Ground
23	Jumper	Ground
24	Jumper	Ground
25	Jumper	Ground
26	Jumper	
27	Jumper	
28	Jumper	
29	Jumper	
30	Jumper	
31	Jumper	
32	Jumper	
33	Jumper	
34	Jumper	
35	Jumper	
36	Jumper	
37	Jumper	

All control lines driving the decoder units are expected to be driven by a differential line driver, since they are received differentially. The READ READY and OVER 8 indicator lines from the unit employ line drivers and should be differentially received. The final section of this report will describe the general Supernova PDP-11 interface unit, which provides proper signal and control line drivers and receivers for up to 40 decoder units.

WARNING: ATTEMPTS TO SHORTCUT THE DIFFERENTIAL DATA AND CONTROL LINE DRIVERS AND RECEIVERS AND REPLACE THEM BY SUBSTITUTE SINGLE-ENDED LINE DRIVING ELEMENTS ARE FRAUGHT WITH GREAT DANGER OF NOISE AND CROSSTALK. SHOULD UNITS BEING THUS IMPROPERLY CONNECTED START TO MALFUNCTION, IT IS ALMOST CERTAIN THAT THE TROUBLES CAN BE TRACED TO DATA AND/OR CONTROL LINE NOISE.

F. Timing Requirements

The signals present at the data inputs give a 200-OR signal out at the GATE OUT terminal on the front of the decoder panel. This output will drive a 50-ohm cable. In order to memorize a given event, a TTL positive-going 50-ohm signal must appear at the GATE IN front panel connector exactly 450 ±25 nsec after the prompt OR output signal appears. The memorization gate window is determined internally by TTL gate delays at 30 nsec; hence, the width of the INPUT GATE signal can be anything over 20 nsec up to about 10 microseconds without affecting the time window on the memorization time. Any signal which was present during the 30 nsec memorization time at the inputs to the input shift register or 480 nsec earlier at the decoder inputs will be memorized by the shift register and decoded as valid data.

The unit conversion time for 200 wire inputs is 12 ±1 μsec, after which time a READ READY pulse signal will be given by the decoder. It is important to note that this signal is a 350 nsec pulse - not a level which is held - so the computer interface must be sensitive to this signal at all times when the decoder is "live."

The data may now be read out at the convenience of the data acquisition device, but no further events can be processed until the decoder receives a RESET signal. The timing of the READ signal is not critical, but data should not be read during a SHIFT signal, as the data lines will be changing during this time. The READ gates are differential drivers which require at least a 200 nsec signal. The SHIFT pulse can occur anytime subject to the above cautionary remark, but ought to be at least 200 nsec long for reliable operation.

The OVER 8 indicator will be a level which can be read at anytime on the appropriate line, commencing after the event decoding, and remaining until the unit receives a RESET pulse.

The RESET signal can be given at any time, and overrides all other operations. Thus, it can be used to reset the decoder and render it active for further events regardless of whether the data it contains has been read or not. This permits, for example, rejecting events which have an OVER 8 indication without waiting for the data to be read.

III. MAINTENANCE AND TROUBLESHOOTING

A. Individual Boards, Functions, and Physical Locations

Fig. 4 shows a top view of the individual printed circuit boards located properly in the decoder chassis. The arrows there also indicate the path of data shifted during the conversion cycle. This is particularly useful in locating a faulty circuit board when one input line fails to give a decoded datum.

As is readily apparent, most of the boards in the decoder are input delay boards, which handle six inputs apiece. This is where the signal reception, partial OR-ing, and coincidence delays are accomplished. The next most numerous board comprises the input shift register - a parallel load, serial out shift register, 200 elements long. The final OR-ing of input signals is done on the three input OR boards, and the input control board, which furnishes the GATE OUT signal. Only five boards remain now - these are all distinct. The input control card is responsible for accepting the GATE IN signal and generating the appropriate internal signals to memorize the input signals in the shift register and start the conversion cycle. The output control board accepts the read and shift signals and controls the loading and unloading of data from the output storage buffer. The eight-word output storage buffer itself consists of two appropriately designated cards, which also contain the drivers for the front panel indicators. Finally, the clock and counter board provides the 17 MHz clock signal and the counter to stop the conversion after 200 pulses. It also supplies the binary-coded numbers to the output buffer.

It is possible to repair almost any unit failure by simply observing the symptoms on the manual readout mode, and carefully studying the PC board functions and signal flow indicated on Fig. 4. Individual PC boards which fail are simply replaced by spare boards, the unit is put immediately back into operation, and the boards themselves are repaired at the technician's leisure.

B. Troubleshooting Hints

The most common decoder problems with symptoms and probable causes are listed in Table III for the benefit of technicians who may encounter these troubles.

TABLE III

SYMPTOM	PROBABLE CAUSE
1. The decoder will not accept a legitimate hit. The busy light never comes on.	1. A GATE IN signal is not present at the proper time, or the input control card (B-1) is bad.
2. The decoder does not give a GATE OUT signal when an input signal is present.	2.a. An associated input OR card is bad. Inputs 1-68 are on card B-15, 69-130 on card A-1, and 131-200 are on card A-15. b. The input control card (B-1) is bad. c. The associated input delay card is bad. See Fig. 4 for card location.
3. Regardless of input signal, the output buffers hold numbers 194-201 as data.	3. An input shift register card has ceased to function properly. These can be replaced sequentially until the problem is found, or the shifted signal can be traced by a scope until the break is found.
4. A legitimate event is received, the busy light comes on, but no numbers are stored in the output buffers.	4.a. The clock and counter board (B-5) is not functioning properly. b. The output control card (B-2) is bad. c. The computer READ, RESET OR SHIFT lines are being held true at the wrong time. d. The input termination and delay card is bad.

TABLE III (continued)

SYMPTOM	PROBABLE CAUSE
5. One or more of the output lines cannot be set.	5.a. The associated output buffer driver card is not functioning properly. The first four least significant bits are on card B-4 and four most significant bits on card B-3. b. The clock and counter board (B-5) is bad.
6. The unit does not give a READ READY pulse at the end of the decoding cycle.	6. The clock and counter board (B-5) is bad.
7. The unit does not give an OVER 8 indication when there are more than 8 legitimate hits in a given event.	7.a. The output control card (B-2) is bad. b. The output buffer driver B (B-3) is bad.
8. The computer READ or SHIFT lines cannot be driven by a good differential signal input.	8. The output control card (B-2) is bad.
9. The computer RESET line does not function properly.	9. The input control card (B-1) is bad.
10. High event rates cause the unit to hang up or give erroneous data.	10. The input control card (B-1) is bad.

IV. INTERFACING DECODER UNITS TO THE COMPUTER

A. General Considerations

If an arbitrary number of decoder units are to be interfaced to a given computer, it will generally be necessary to provide a simple but separate interface module to provide the necessary line buffering and unit addressing for a multiple-unit system. Furthermore, the user will usually not desire to use the READ READY signal from every decoder unit in the system. Assuming that all decoders of the system were given GATE IN signals at the same time, the conversion times are sufficiently close that a READ READY from any one of them will provide the necessary flag to the computer that data is waiting to be read.

It is important to note that each decoder unit of the system will require separate RESET, READ and SHIFT pulses, and will give individual OVER 8 and READ READY signals. It must be reiterated here that all lines to and from the individual decoder units must be differentially driven and received, and since most minicomputer systems - in the interest of a cheaper machine - use single-ended bus drivers, the general computer interface will have to provide the proper drivers and receivers for the decoders. Since it must also use single-ended data and control lines from the computer, it ought to be physically close to it.

The data lines from the decoders can be bussed together as referred to earlier. This is accomplished in spite of differential line drivers by employing tri-state logic integrated circuits, which are gated off when not being read.

B. MP-3 Supernova and PDP-11 Interface Unit

We have constructed and tested a single MWPC interface unit which mates up to forty decoder units. (8000 active wires) with either the Data General Supernova or DEC PDP-11/20 computers. The block diagram of this unit is shown in Fig. 5a and 5b. In order to make the PDP-11 compatible with this unit, a DEC DR11-A system module was used to provide the control signals which drive the interface unit. As can be readily seen, most of this interface box consists of line drivers and receivers (and, of course, connectors for cables), as might be expected for servicing forty decoders.

Fig. 6 makes clear exactly how the DEC DR11-A system was used to complete the connection to the PDP-11/20.

We have included here for completeness simple sample programs for each of the above minicomputers to service 40 decoders and store all of the data present in a core data buffer. Note that data in each of these cases is separated by interstitial zero words rather than by assigning decoders separate addresses. There is, of course, no hardware prohibition against a more elegant addressing scheme, since the general interface addresses each decoder separately anyway, but the present method, while perhaps lacking the polish of general elegance, does have the twin virtues of speed and simplicity.

C. Sample Supernova Program to Read 40 Decoders

The following simple routine (Table IV) assumes the proper interrupt service routine is addressed through location #1, that polling has determined the decoders to require servicing, and the appropriate jump to MWPCSERV is then made. It further assumes that somewhere in the event processing, INITIALIZE is executed before the next event is taken.

The reason, of course, that only 20 (24_8) units are read is that the decoders are tied together on the data lines in groups of two, so that reading forty decoders requires only twenty separate addresses. Also, this provides 16-bit data word transfers to the computer.

Data is transferred into the PDP-11 at the rate of 17 microseconds per 16-bit word.

For the Supernova, data is transferred from a given unit at the rate of one 16-bit data word every 6.1 microseconds. A data channel transfer would considerably speed up the operation, but at the expense of much less program flexibility and greater interface complexity.

D. Sample PDP-11/20 Program to Read 40 Decoders

The following simple routine (Table V) assumes that an interrupt is made at the appropriate BR level, and that the interrupt vector points to PCSER. It further assumes that at some point prior to actual event transfer, START has been executed to initialize the various registers within the interface.

TABLE IV

INITIALIZE:	LDA 0, BUFFAD	Load the starting address of storage buffer into
	STA 0, 20	memory cell #20
	LDA 0, DECODERS	Set up counter UNITCT with number of decoders to
	STA 0, UNITCT	be serviced
	LDA 0, WTD	Set up INST to read first decoder
	STA 0, INST	
MWPCSERV:	SKPBZ 64	Test for "over 8" and reset units if found
	JMP OVR8	
INST:	DIAP 0, 40	Read decoder data buffer
	STA 0, @20	Store data in core buffer
	MOV 0, 0, SZR	Is this all the data in this buffer?
	JMP .-3	No, go back for more
	ISZ INST	Yes, go to next unit
	DSZ UNITCT	Was this the last unit?
	JMP INST	No, continue reading data
	STA 0, @20	Yes, put another zero to separate events
OVR8:	NIOC 64	Reset all units
	JMP @0	Return from interrupt
WTD:	DIAP 0, 40	

TABLE V

```
START:    RESET               All registers and units are cleared to start
          MOV #BUFST, R3      We will use R3 to point to core buffer storage
          CLR ERCNT           Let us count the number of "over 8" events
          CLR UNITAD          Set up the register to read the first decoder
          MOV #100, MWPCGO    Enable the decoder interrupt
                .
                .
                .
PCSER:    TST MWPCGO          Test this event for "over 8" indication
          BPL READ            No "over 8" found
          INC ERCNT           Found an "over 8", increment error counter
READ:     MOV PARTPT, R2      Pick up data from decoder
          MOV R2, (R3)+       Store data in core buffer
          TST R2              Is this the final data for this unit?
          BNE  READ           No, go back for more
          INC UNITAD          Get set up to read next unit
          CMP #23, UNITAD     Have we read all units?
          BNE  READ           No, go back for more
          MOV #24, UNITAD     Yes, give a general reset
          RTI                 Return from interrupt
```

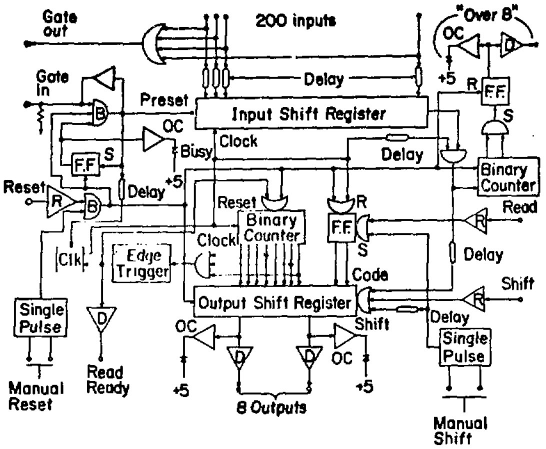


Fig. 1. Decoder block diagram

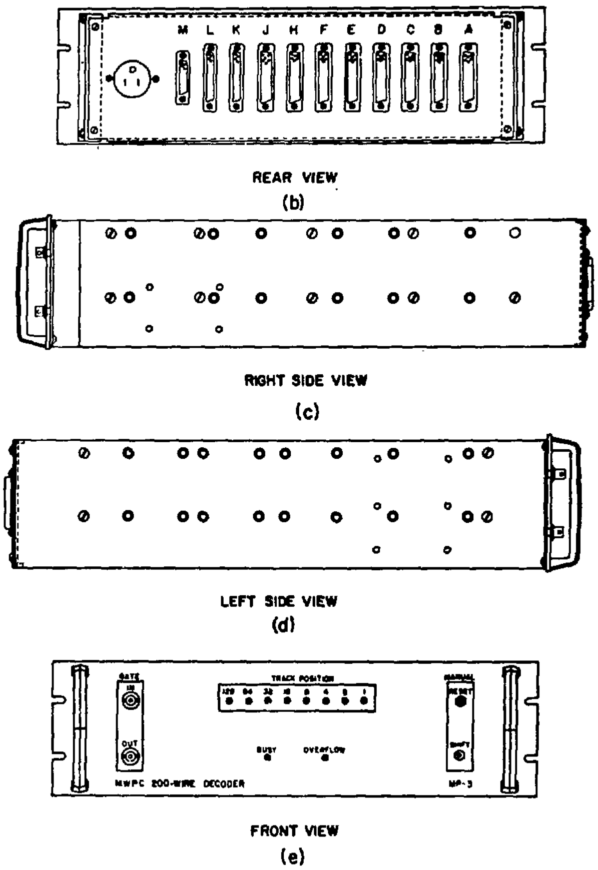
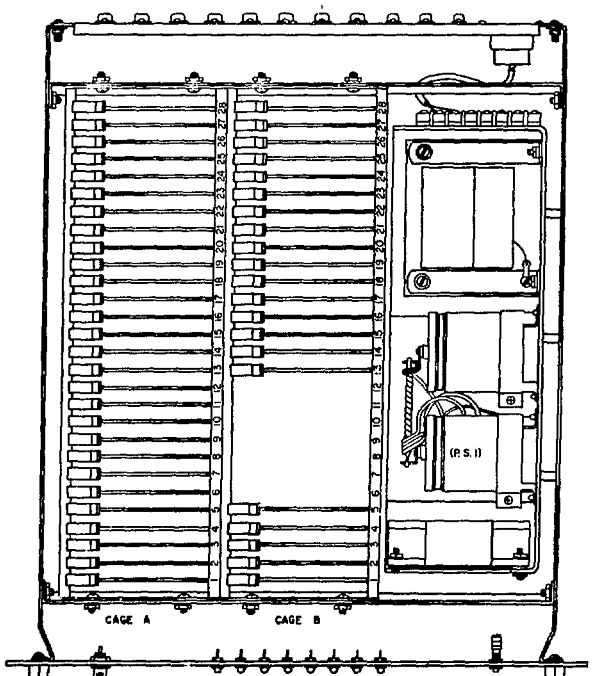


Fig. 2(b)(c)(d)(e). Decoder physical layout



(a)

Fig. 2(a). Decoder physical layout

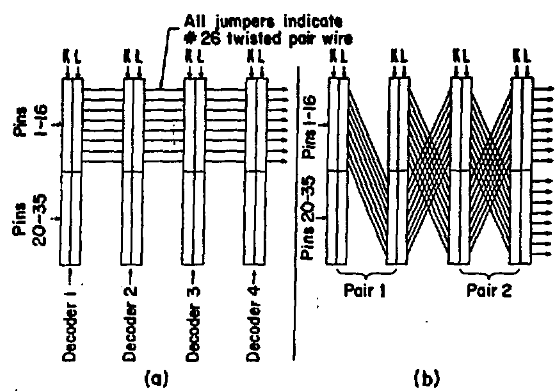


Fig. 3(a)(b). Decoder output data line bussing diagram

TOP VIEW

Shift Direction	Cage "A"	Related Output Nos.	Shift Direction	Cage "B"	Related Output Nos.
28	Delay [1]	195-200	28	Delay	63-68
27	Delay	189-194	27	Delay	57-62
26	Delay	183-188	26	Delay	51-56
25	Delay	177-182	25	Delay	45-50
24	Delay	171-176	24	Shift in	41-72
23	Shift in [2]	169-200	23	Delay	39-44
22	Delay	165-170	22	Delay	33-38
21	Delay	159-164	21	Delay	27-32
20	Delay	153-158	20	Delay	21-26
19	Delay	147-152	19	Delay	15-20
18	Delay	141-146	18	Delay	9-14
17	Shift in	137-168	17	Shift in	9-40
16	Delay	135-140	16	Delay	3-8
15	Or [3]		15	Or	
14	Delay	129-134	14	Delay	1-2
13	Delay	123-128	13	Shift in	1-8
12	Delay	117-122	12		
11	Delay	111-116	11		
10	Delay	105-110	10		
9	Shift in	105-136	9		
8	Delay	99-104	8		
7	Delay	93-98	7		
6	Delay	87-92	6		
5	Delay	81-86	5	Clock and counter	
4	Delay	75-80	4	Output buffer driver Section"A"	
3	Shift in	73-104	3	Output buffer driver Section"B"	
2	Delay	69-74	2	Output control	
1	Or		1	Inptu control	

① "Delay" = Input termination and delay cards
② "Shift in" = Input shift register cards
③ "Or" = Input or cards

FRONT

Fig. 4. Decoder board location chart

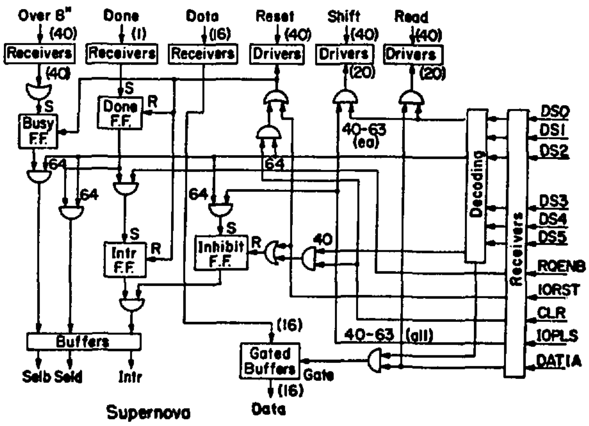


Fig. 5(a). Supernova interface block diagram

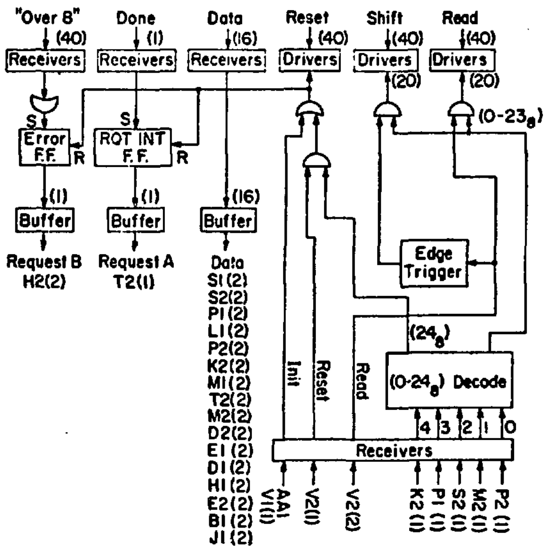


Fig. 5(b). PDP-11 interface block diagram

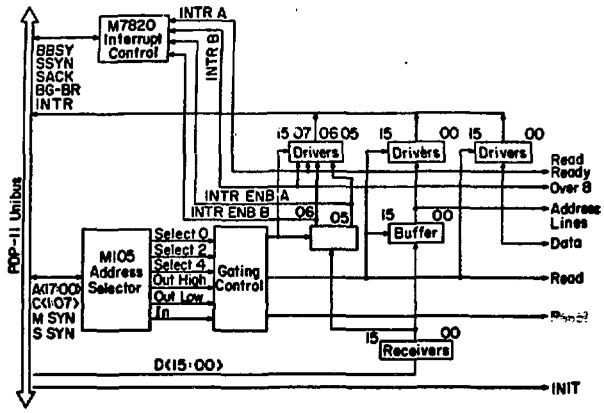


Fig. 6. DR 11-A device register interface (block diagram)