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Effects of Focused Ion Beam Irradiation on MOS Transistors

Ann N. Campbell, Kenneth A. Peterson, Daniel M. Fleetwood,
and Jerry M. Soden
Sandia National Laboratories
Albuquerque, NM 87185-1081

505-844-7452; FAX 505-844-2991; e-mail ancampbe@sandia.gov

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ABSTRACT

The effects of irradiation from a focused ion beam (FIB) system on MOS transistors are reported systematically for the first time. Three MOS transistor technologies, with 0.5, 1, and 3 μm minimum feature sizes and with gate oxide thicknesses ranging from 11 to 50 nm, were analyzed. Significant shifts in transistor parameters (such as threshold voltage, transconductance, and mobility) were observed following irradiation with a 30 keV Ga^+ focused ion beam with ion doses varying by over 5 orders of magnitude. The apparent damage mechanism (which involved the creation of interface traps, oxide trapped charge, or both) and extent of damage were different for each of the three technologies investigated.

INTRODUCTION

Focused ion beam systems are now used routinely to perform circuit modifications during the design debugging phase of integrated circuit (IC) production. Circuit modifications are also used frequently during IC failure analysis to verify proposed failure scenarios. While it is well known that FIB imaging and circuit modification processes can cause electrostatic discharge (ESD) damage in ICs [1] and that the FIB modification process can degrade IC performance, FIB-induced changes of transistor or IC parameters are described in only a few papers [2]. No systematic studies of these phenomena have been published to date. We have observed that extreme care must be exercised when performing circuit modifications on certain types of ICs, particularly when the modifications are in close proximity to active (transistor) regions. In general, we find that the success rate of FIB modifications is increased by reducing the ion dose for imaging and navigation purposes to an absolute minimum and by using charge neutralization whenever possible. Even with these precautions, post-modification electrical testing invariably indicates that the ICs are altered to some extent by FIB exposure.

The objectives of this study were to analyze how the focused ion beam interacts with ICs to cause degradation and to learn how to minimize or prevent that degradation so that FIB circuit modification processes can be optimized. To achieve these objectives we have studied the effect of FIB exposure on transistor parameters as a function of ion dose, dose rate, charge neutralization, and subsequent thermal annealing. The implications for actual ICs are described in the discussion section.

EXPERIMENTAL APPROACH

Both *n*- and *p*-channel transistors of several geometries were exposed to FIB irradiation with ion doses ranging from ~10^{-6} nC/μm^2 to ~1 nC/μm^2. Parametric testing was performed prior to and after ion beam exposure. Exposures from ~10^{-6} nC/μm^2 to ~10^{-2} nC/μm^2 are representative of the ion dose due to image acquisition during navigation to an area of interest. In practice, higher imaging doses result from using higher beam currents, achieved by using larger beam-limiting apertures. Ion doses above 10^{-2} nC/μm^2 cause significant milling of the sample. For reference, the general rule of thumb is a dose of 4 nC/μm^2 removes typical IC materials to a depth of about 1 μm.

Experiments were conducted with a Micrion 9000 FIB system which has a 25 nm nominal resolution column and uses 30 keV Ga^+ ions. Irradiation of the MOS transistors was performed with the electron floodgun active ("ion mode") and disabled ("electron mode"). The floodgun directs a low energy (~ 80 eV) spray of electrons at the sample surface, helping offset the charging effects of the Ga^+ ions. The electron floodbeam current is at least an order of magnitude higher than the ion beam current (for example, the floodbeam current is ~ 35 nA for an ion beam current of 1.7 nA). The FIB system's navigation capability was used to move directly to the transistor of interest without delivering an imaging dose to other areas on the IC. The ion dose was delivered to the surface above the entire test transistor and extended to the surrounding area as well. A square or rectangular region ranging from 50 x 50 μm to 100 x 100 μm in size was used for the irradiation exposures. Figure 1 is an optical photomicrograph of a transistor following FIB irradiation, showing a 70 x 70 μm FIB-exposed area (indicated by the arrow). Figure 2 is a schematic cross section showing the interaction between the ion beam and the sample. When the ion beam strikes the sample, Ga is implanted to a shallow depth (~ 30 nm), and secondary particles (electrons, ions, and neutral atoms) are produced.

The desired dose per unit area was achieved either by using the FIB system's milling function (for doses of 10^{-4} nC/μm^2 or greater) or by "grabbing" one or more single frame images of the area of interest. The milling parameters (pixel spacing and pixel

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dwell time) were adjusted to match those used in grabbing single frame images. The ion dose delivered in a single frame image, D_0, is calculated from the expression $D_0 = [(I_b)(t_d)/X_pY_p)]$, where I_b is the beam current in nA; t_d is the time the ion beam dwells at each pixel, expressed in seconds; and X_p and Y_p are the pixel spacings in the x- and y-directions. For example, a single frame image acquired with t_d = 16 μs and I_b = 1.7 nA (400 μm aperture) delivers an ion dose of about 2 x 10^{-4} nC/μm^2 for a 256 x 256 pixel image. I_b in the irradiation experiments ranged from 10 pA to 4.8 nA, t_d was 1 or 16 μs, and X_p and Y_p were ~ 0.4 μm.

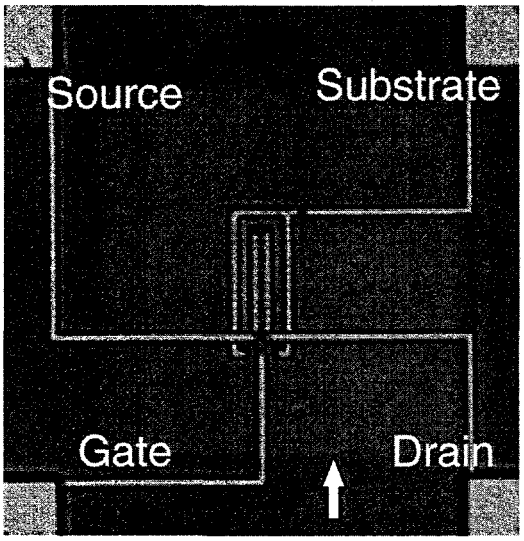

Fig. 1 Optical photomicrograph showing the FIB-irradiated region (indicated by the arrow) around a 20 x 0.6 μm *n*-channel transistor. The bond pads are visible at the corners of the image.

FIB exposures were performed on transistors implemented in three different MOS technologies. These experiments are summarized in Table I. Transistors in test structures on intact wafers and packaged in 24 pin ceramic DIPs (dual in-line packages) were used. For loading the wafers into the FIB system, a metal sample holder that accommodates up to an 8 inch wafer was used. Electrical contact between the wafer substrate and sample holder (which was grounded to the system power ground) was made by using conductive tape, but the other contacts (source, gate, drain) were electrically open (floating). In general, three transistors were exposed for each test condition on the wafers. A special sample stage that permits electrical biasing in our FIB system [3] was used for the experiments with packaged transistors. Standard FIB sample holders were used for some of the packaged transistor experiments, in which case the pins were grounded to the metal sample holder. Because of limitations on the number of samples and test time, fewer packaged transistors than wafers were exposed per given test condition.

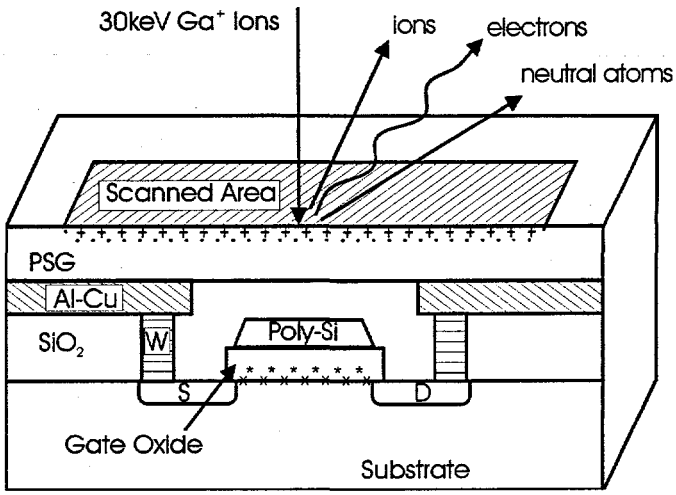

Fig. 2 Schematic cross-section showing interaction of the ion beam with a test transistor. The "+" indicates buildup of a positive surface potential and implantation of Ga. In the gate region, "*" indicates the location of oxide-trap charge and "x" indicates the location of interface traps.

Table I - Summary of Transistor Experiments

IC Technology	Sample Type	Description of Transistor Structure	Experiments
0.5 μm CMOS, 3 metal, 1 polysilicon, CMP planarized, W-stud vias, LOCOS isolation, 13 nm GOX.	wafer, 24 pin DIP	0.3 μm polysilicon gate, 1.5 μm ILD (PETEOS), 1 μm PSG passivation. Fixed geometry: 20 x 0.6 μm *n*-, 20 x 0.75 μm *p*-channel. Variable geometry: 12 x 12 μm to 2.3 x 0.6 μm.	Constant and variable dose rate. Fixed and variable transistor geometry, thermal annealing, biased transistors. Doses 10^{-6} to 1 nC/μm^2. FIB exposed area 50 x 50 - 100 x 100 μm.
1 μm BiNMOS, 3 metal, 1 polysilicon, LOCOS isolation, LDD, 20 nm GOX.	wafer	0.4 μm polysilicon gate, 1.2 μm ILD (2K SOG, 5K TEOS, 5K PSG), 1.7 μm passivation (0.9 μm PSG + 0.8 μm nitride). Fixed geometry: 30 x 1 μm. Variable geometry: 1 x 1 - 30 x 1 μm.	Constant dose rate. Doses from 10^{-4} to 0.2 nC/μm^2. Fixed and variable transistor geometry. FIB-exposed area 60 x 60 μm.
3 μm CMOS, 1 metal, 1 polysilicon, 50 nm GOX.	wafer, 24 pin DIP	0.6 μm polysilicon gate, 0.7 μm ILD (TEOS), 1 μm PSG passivation. Transistor geometry: 16 x 2, 3, and 4 μm.	Constant dose rate. Doses from 10^{-4} to 0.3 nC/μm^2. Three transistor geometries. Biased transistors. FIB exposed area 40 x 40 μm.

The wafer level measurements of transistor I_d - V_{gs} curves and parameters were made with an HP4062 Data Acquisition System in conjunction with either an Electroglas 2001X or a KLA 1007 probe station. Package tests were performed with an HP 4145 Semiconductor Parameter Analyzer. Standard transistor parameters V_t (threshold voltage, linear), μ, (mobility), and G_m (transconductance) were determined from the I_d - V_{gs} curves, where I_d is the drain current and V_{gs} is the gate-to-source voltage.

Test capacitors (3 μm technology, 32 and 50 nm gate oxide thickness) were FIB-irradiated to gain additional insight into potential damage mechanism(s). The capacitors were packaged in 24 pin ceramic DIP packages. High-frequency (1 MHz) capacitance - voltage (C-V) analysis was performed via the method of Winokur *et al* [4].

RESULTS

Initial experiments were performed on the 0.5 μm CMOS transistors to determine the general effects of FIB irradiation on transistor parameters and behavior. In order to assess whether the results of FIB irradiation observed for the 0.5 μm CMOS technology were generally applicable, transistors from two other MOS technologies, 1 μm and 3 μm, were investigated for comparison. The experiments are outlined in Table I.

0.5 μm Technology

Initial Experiments. The initial experiments were conducted using intact wafers. Minimum gate length *n*- (0.6 μm) and *p*-channel (0.75 μm) test transistors (with 20 μm gate width) were exposed to FIB irradiation over a wide range of ion doses (from ~10^{-6} to ~1 nC/μm^2). Typical I_d - V_{gs} curves for *n*- and p-channel transistors before FIB-irradiation and after a FIB dose of 0.1 nC/μm^2 are shown in Figs. 3 and 4, respectively. These figures show that the post-FIB I_d - V_{gs} curves exhibit significant subthreshold stretchout. Correspondingly, all of the transistor parameters (including threshold voltage, transconductance, mobility, off-state leakage current, and on-state current) showed measurable changes as a result of FIB exposure.

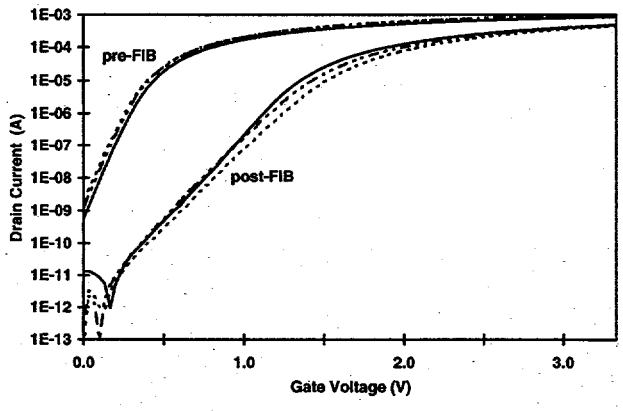

Fig. 3 I_d vs. V_{gs} curves showing the effect of an ion dose of 0.1 nC/μm^2 for 20 x 0.6 μm *n*-channel transistors in the 0.5 μm technology.

Figure 5 shows that V_t increases in magnitude as a function of total ion dose for both *n*- and *p*-channel transistors. The increase in V_t is approximately linear with the ion dose plotted on a logarithmic scale. This increase is large when charge neutralization is not used and ranged in magnitude from a few tenths of a volt for typical imaging doses to as much as 1.1 V for *p*-channel and 1.8 V for *n*-channel transistors for typical milling doses. The fact that V_t increases in magnitude for both *n*- and *p*-channel transistors means that both move further into enhancement mode with increasing ion dose. It is interesting to note that, despite the use of relatively large ion doses, none of the 0.5 μm technology transistors experienced gate oxide failure as a result of FIB exposure. The dose rate was held constant in this experiment (1.8 x 10^{-2} nC/μm^2-min).

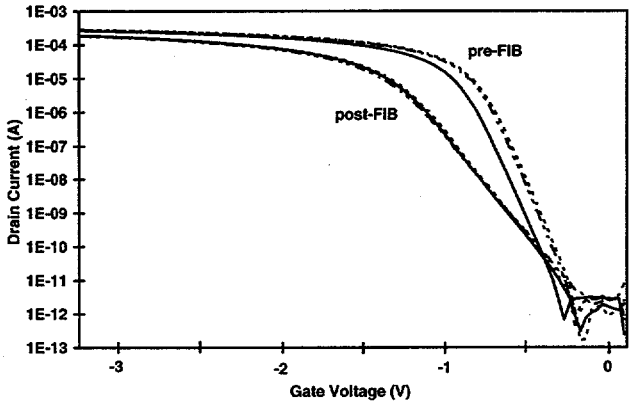

Fig. 4 Pre- and post-FIB I_d vs. V_{gs} curves for 20 x 0.75 μm *p*-channel transistors in the 0.5 μm technology showing the effect of a 0.1 nC/μm^2 ion dose. The absolute value of current is plotted.

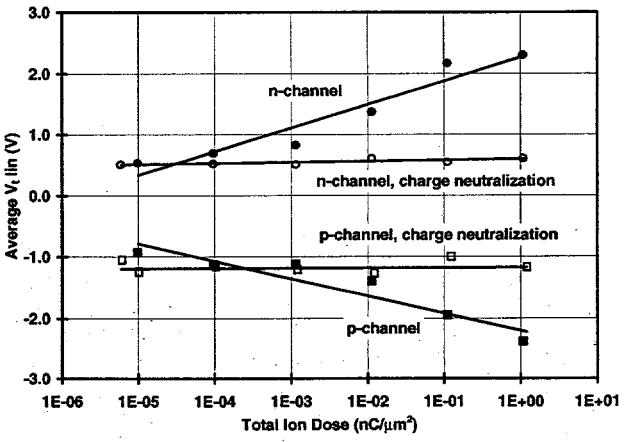

Fig. 5 V_t vs. ion dose, showing effects of FIB irradiation with and without charge neutralization for 20 x 0.6 μm *n*-channel and 20 x 0.75 μm *p*-channel transistors. Pre-irradiation values are ~ 0.6 V for the n-channel and ~ -0.9 V for the p-channel transistors. A constant dose rate was used for this experiment.

In a second experiment, the dose was varied by changing the beam current (i.e., varying the beam limiting aperture) while acquiring the same number of single frame images of the area around each transistor. The dose rate varied from 1 x 10^{-4} nC/μm^2-min for I_b = 10 pA to 4.8 x 10^{-2} nC/μm^2-min for I_b = 4.8 nA. The results of this experiment are given in Fig 6. Comparison of Fig. 6

with Fig. 5 shows good agreement between the two. Thus, it appears that the degradation of transistor parameters for the 0.5 μm technology is independent of ion dose rate over the range of dose rates used here.

Figure 7 shows the change in K', expressed as a ratio of K' (post-FIB) to K'_0 (pre-FIB) for both n- and p-channel transistors with increasing ion dose. The K' parameter in the linear region is the slope of I_d vs. V_{gs}. The carrier mobility (μ) is directly proportional to K'. Thus, the decrease in K' with increasing ion dose indicates a corresponding decrease in μ. Figure 7 shows that K' decreases with ion dose, that the shift in K' is larger for the n-channel transistors, and that use of the electron floodgun minimizes the parameter shifts, in good agreement with the V_t results shown in Figs. 5 and 6.

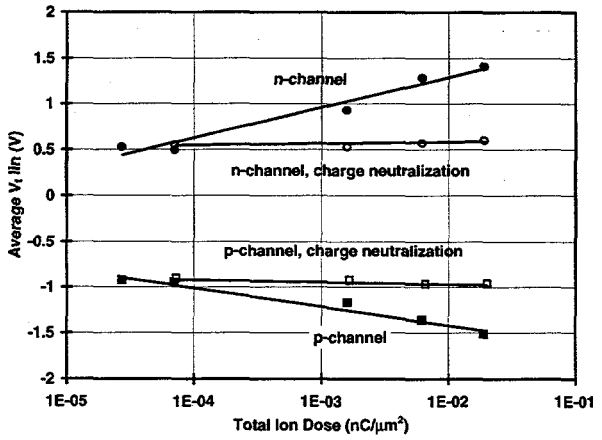

Fig. 6 V_t vs. ion dose, showing effects of FIB irradiation with and without charge neutralization. Pre-irradiation values are ~ 0.6 V for the n-channel 20 x 0.6 μm and ~ -0.9 V for the p-channel 20 x 0.75 μm transistors. A variable dose rate was used for this experiment.

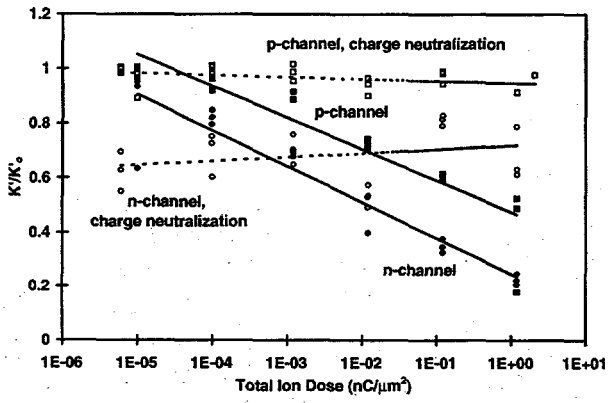

Fig. 7 K' as a function of ion dose for both 20 x 0.6 μm n- channel and 20 x 0.75 μm p-channel transistors, with and without charge neutralization. A constant dose rate was used for this experiment.

Figures 5, 6, and 7 demonstrate that the use of an electron floodgun for charge neutralization significantly reduces (but does not entirely eliminate) V_t and K' degradation. Similarly, the use of the floodgun also minimized changes in the other measured parameters. Most of the remaining experiments were performed without charge neutralization to maximize the FIB effects. When charge neutralization is used, it is noted in the description of the results.

Transistor geometry effects. Next, experiments were performed to determine the effect of transistor geometry on the parameter shifts due to FIB irradiation. Both n- and p-channel transistors were used in this experiment. Transistors with gate areas ranging from 1.38 to 144 μm² were irradiated with an ion dose of 0.1 nC/μm². The pre- and post-FIB irradiation data for V_t and K' were plotted as a function of gate length (L), gate width (W), transistor area, gate perimeter ($2W + 2L$), and W/L aspect ratio. The best fit was found when the V_t data were plotted as a function of gate area, as illustrated in Fig. 8. However, the parameter shifts also scaled reasonably well with the perimeter length and W/L. In general, the parameter shifts varied considerably with transistor geometry, and larger effects were observed for the smaller transistor dimensions.

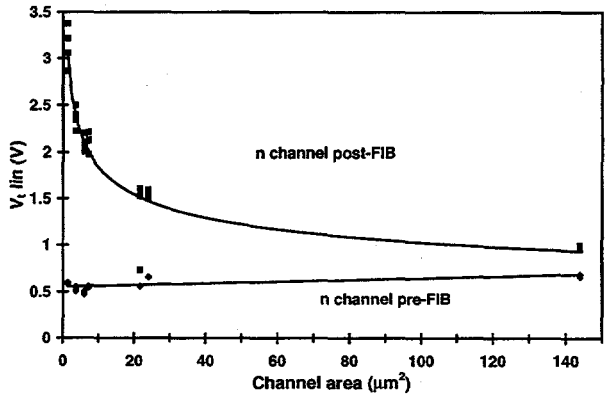

Fig. 8 Variation of V_t with transistor channel area for the 20 x 0.6 μm n-channel transistors in the 0.5 μm technology.

Annealing Recovery Experiments. Thermal annealing experiments were performed to determine whether the FIB-induced parameter shifts were bake-recoverable. In an initial experiment, some room temperature recovery of the measured parameters was noted when the transistors were retested several weeks after irradiation (~25% reduction). Full recovery (within measurement error) of the transistor parameters was observed after a 150 °C, 10 hour bake in a room air ambient. Figure 9 illustrates a more systematic investigation of the thermal recovery effects for the 20 x 0.6 μm n-channel transistors which were irradiated with a 0.1 nC/μm² dose without charge neutralization. The room temperature mobility before and after irradiation and following a 15 hour (overnight) anneal at 100 and 125 °C is shown. Partial recovery (~ 40%) was observed following the 100 °C anneal. Full recovery was found following the 125 °C bake. The V_t also showed recovery that paralleled the mobility data in Fig. 9 .

Packaged Transistor Experiments. Experiments on the 0.5 μm packaged transistors indicated that it was difficult to deliver enough ion dose to the transistors to induce I_d - V_{gs} shifts without causing gate oxide shorts. If the experiments were conducted with the package pins grounded or biased, essentially no shift in the I_d - V_{gs} curve was observed. However, if the pins were allowed to float electrically, gate oxide shorts occurred at relatively low doses (2.5 x 10^{-3} nC/μm²). This is in contrast to the irradiation experiments on wafers, where doses as high as 1 nC/μm² did not lead to gate oxide shorts.

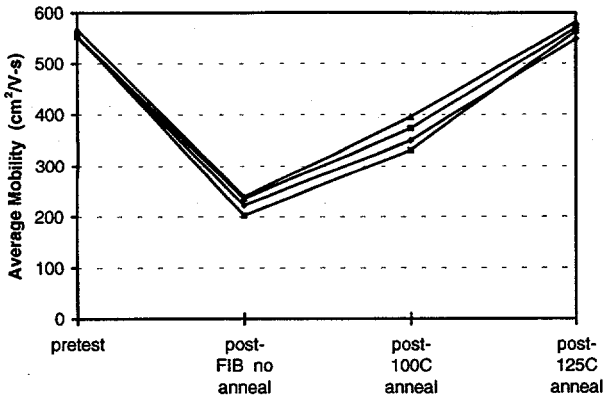

Fig. 9 Mobility (μ) for the 20 x 0.6 μm n-channel 0.5 μm technology transistor as a function of annealing temperature. Essentially complete recovery was noted following a 125 °C anneal. The other transistor parameters exhibited similar recovery.

1 μm Technology

FIB effects were studied for both *n*- and *p*-channel transistors on wafers for the 1 μm technology. Transistor geometries ranged from 30 x 1 μm to 1 x 1 μm, and the ion doses varied from 1 x 10^{-4} to 0.2 nC/μm^2. The results of FIB irradiation on these transistors were different than for the 0.5 μm technology. Figures 10 and 11 show typical pre- and post-FIB (0.1 nC/μm^2 dose) I_d - V_{gs} curves for 30 x 1 μm *n*- and *p*- channel transistors. Inspection of these figures shows that only very minor shifts in the I_d - V_{gs} curves result from FIB irradiation and that the effects are larger for the *p*-channel transistors. The *p*-channel V_t shift was -0.08 V, compared with -0.02 V for the *n*-channel transistors.

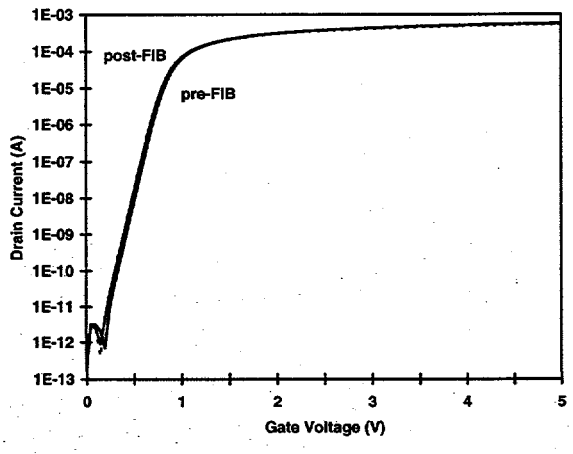

Fig. 10 Pre- and post-FIB I_d vs. V_{gs} curves for 30 x 1 μm *n*-channel transistors in the 1 μm technology. The ion dose was 0.1 nC/μm^2.

Larger effects were observed (ΔV_t = -0.37 V) for a smaller gate area transistor (30 x 0.75 μm) with a larger ion dose (0.2 nC/μm^2), as shown in Fig. 12. The post-FIB curves shift to lower voltages for both *n*- and *p*-channel transistors (i.e., the *n*-channels move toward depletion mode while the *p*-channels move further into enhancement mode). I_d - V_{gs} curves for 30 x 1 μm *n*- and *p*- channel transistors irradiated with charge neutralization showed no appreciable post-FIB shifts. Unlike the 0.5 μm technology, the 1 μm technology transistors are quite ESD sensitive. Gate oxide shorts were observed at ion doses as low as 0.01 nC/μm^2. At a dose of 0.2 nC/μm^2, gate oxide shorts occurred for all of the *p*-channel test transistors smaller than 30 x 0.75 μm and for some of the 30 x 0.75 and 30 x 1.0 μm transistors as well. Fewer gate oxide shorts were observed for the *n*-channel transistors, consistent with the observation that FIB effects are less pronounced in the *n*-channel transistors.

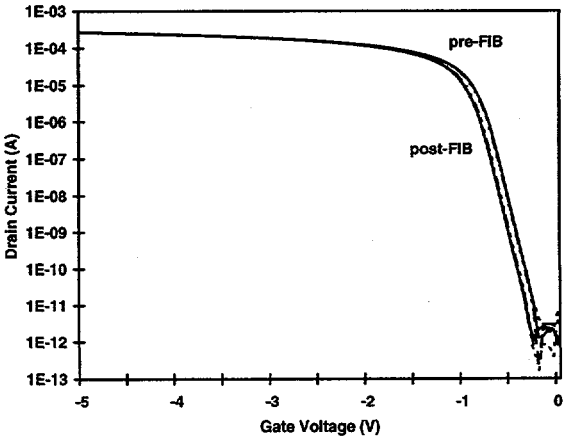

Fig. 11 Pre- and post-FIB I_d vs. V_{gs} curves for 30 x 1 μm *p*-channel transistors in the 1 μm technology. The ion dose was 0.1 nC/μm^2. The absolute value of current is plotted.

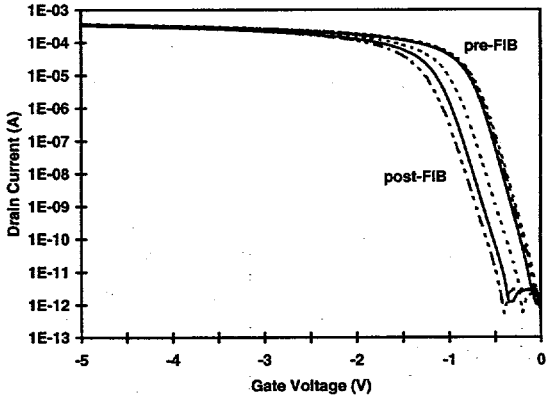

Fig. 12 Pre- and post-FIB I_d vs. V_{gs} curves for 30 x 0.75 μm *p*-channel transistors in the 1 μm technology. The ion dose was 0.2 nC/μm^2. The absolute value of current is plotted.

3 μm Technology

The effects of FIB irradiation on an older (3 μm, single-metal, single-polysilicon) technology were also investigated. 16 x 3 μm *n*-channel test transistors on wafers were exposed to ion doses of 1 x 10^{-4} to 0.3 nC/μm^2. Very little change in the I_d - V_{gs} curves was noted until the largest dose was reached. Figure 13 shows pre- and post-FIB (dose = 0.3 nC/μm^2) I_d - V_{gs} curves for *n*-channel transistors on wafers. These curves exhibit both a slight shift to

lower voltages and subthreshold stretchout. The subthreshold stretchout effect is predominant, and the V_t shift is ~ 0.15 V.

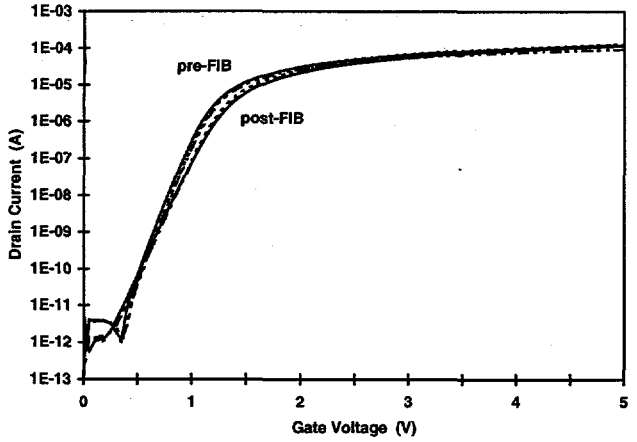

Fig. 13 Pre- and post-FIB I_d vs. V_{gs} curves for 16 x 3 µm *n*-channel transistor in the 3 µm technology. The ion dose was 0.1 nC/µm^2.

Very different results were obtained for 16 x 2, 3, and 4 µm *n*-channel transistors packaged in 24 pin DIPs. Figure 14 shows typical I_d - V_{gs} curves for 16 x 2 and 16 x 3 µm *n*-channel transistors pre- and post-FIB exposure (dose = 0.01 nC/µm^2). The post-FIB curves are shifted to lower voltages, with ΔV_t = -0.7 V for the 16 x 2 and -0.6 V for the 16 x 3 µm transistor. While the wafer experiments resulted in a few gate oxide shorts at the highest dose, the packaged transistors were far more ESD sensitive. Ion doses as low as 2.5 x 10^{-2} nC/µm^2 produced gate oxide shorts. Somewhat inconsistent results were obtained for the packaged transistors. Parameter shifts were not always observed after the application of the standard ion dose for these experiments (0.01 nC/µm^2). The parameter shifts were more likely to occur when the package pins were electrically floating, rather than biased or grounded.

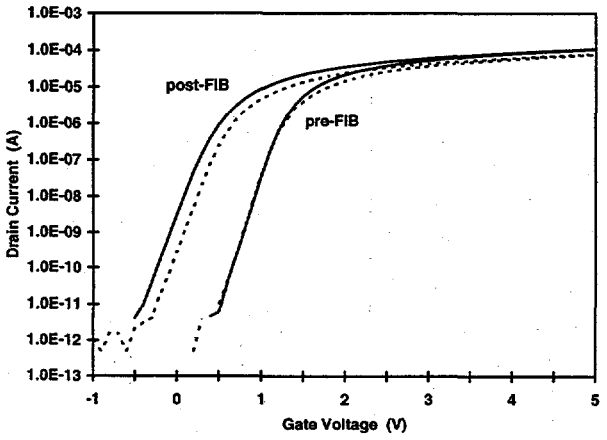

Fig. 14 Pre- and post-FIB I_d vs. V_{gs} curves for 16 x 2 µm and 16 x 3 µm *n*-channel transistors in the 3 µm technology. The ion dose was 0.01 nC/µm^2.

Charging Effects

Charging of the region receiving FIB exposure was observed directly in experiments that involved grabbing a number of single frame images to deliver the ion dose. Each image is displayed on the video monitor as it is collected, so the effect of single and subsequent images can be assessed "real time". It was observed that, for a fixed number of single frame images (10), increasing I_b from 10 pA to 4.8 nA led to greatly increased charging effects. Figure 15 is an electron mode image (i.e., no charge neutralization) of a 0.5 µm technology, 20 x 0.6 µm *n*-channel transistor at the wafer level (substrate grounded, other pins floating) with I_b = 4.8 nA. At this I_b, acquisition of each image delivered a dose of 2 x 10^{-3} nC/µm^2. Figure 15 displays voltage contrast effects; darker areas of the image represent a relatively higher surface potential than those which are brighter. Capacitive coupling between underlying conductors and the surface can modulate the surface potential (which would otherwise be uniform) and permit subsurface potentials to be imaged [5]. The contrast difference between the relatively brighter and darker regions is strong, and the darker regions outline the metal interconnects to the transistor, suggesting that the conductor lines rise to a relatively high voltage during FIB exposure. Figure 15 was the fourth scan of this particular transistor. The particle visible in the image was electrostatically attracted to one of the highly charged regions above an interconnect line and was not present in the first three scans of this transistor. Electrostatic attraction of particles was observed for several other transistors at I_b = 4.8 nA but not at lower beam currents. Figure 16 shows a similar charge contrast image acquired at I_b = 1.6 nA. There is less contrast difference between the relatively brighter and darker areas in this image, indicating less severe charging. Finally, Fig. 17 is an electron mode image of a packaged 20 x 0.6 µm transistor with the pins grounded, acquired with I_b = 4.8 nA. The charging effects are considerably less in Fig. 17 than in the previous two images. For Figs. 15 - 17, t_d = 16 µs, and the image size was 512 x 512 pixels.

Measurements of the gate voltage were made *in situ* using the electrical biasing capability of the FIB system to observe charging effects of the ion beam under a variety of conditions for packaged 0.5 and 3 µm technology transistors. The source, drain, and substrate were grounded and the gate was unbiased for these experiments. If charge neutralization was not used, V_g was observed to rise steadily to a positive voltage ranging from 0.5 to 9.6 V depending on the transistor technology for I_b = 1.7 nA. Larger V_g values were observed for the 3 µm technology than for the 0.5 µm technology. By using a variable gate geometry test structure in the 0.5 µm technology, it was observed that the charge-up rate is greater for transistors with smaller gate areas, consistent with the finding of larger parameter shifts for smaller transistor geometries. It was also observed that the accumulated charge would dissipate within a few minutes at a rate of approximately 0.5 to 2 V/min after irradiation ceased. When electron flood charge neutralization was activated, V_g tended to a negative voltage, ranging from -0.3 V for the 0.5 µm technology to -7 V for the 3 µm technology. While these experiments did show that a positive V_g is developed during FIB irradiation, the results were limited by the fact that electrical connection to the transistor terminals had a grounding effect and did not permit the voltages on the gate to be as large as if it was floating. This is consistent with the observation that parameter shifts occurred for packaged transistors only when the pins were electrically floating.

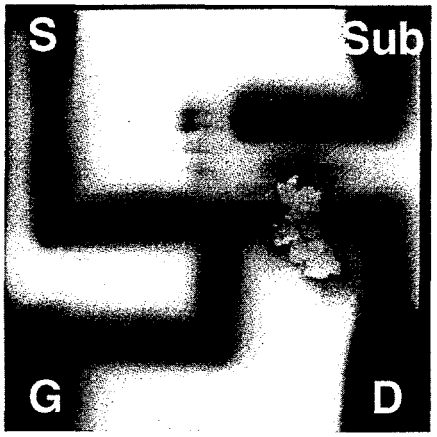

Fig. 15 Electron mode FIB image of 20 x 0.6 μm transistor showing voltage contrast effects that reveal charging during FIB irradiation with 4.8 nA beam current. Note particle electrostatically attracted to surface above a conductor line.

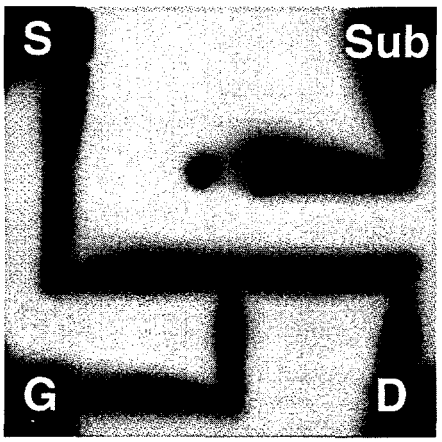

Fig. 16 Electron mode FIB image of 20 x 0.6 μm transistor showing less severe charging during FIB irradiation with a 1.6 nA beam current.

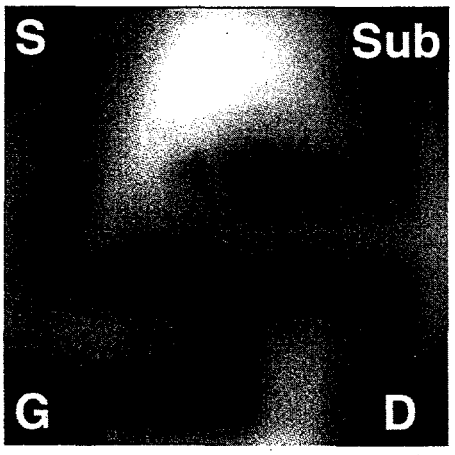

Fig. 17 Electron mode FIB image of 20 x 0.6 μm transistor with pins grounded, with 4.8 nA beam current. This figure shows much less severe charging during FIB irradiation than the image in Fig. 16.

Capacitor Experiments

In addition to the transistor tests, irradiation experiments were performed on both *p*- and *n*-substrate test capacitors in the 3 μm technology. The capacitors were 340 x 340 μm with Al over polysilicon gates. Experiments were performed both with and without electron flood charge neutralization with the pins electrically floating, with the pins grounded, and with the capacitor biased with the polysilicon contact at +5 V for the *p*-substrate and -5 V for *n*-substrate. Ion doses of 0.01 - 0.04 nC/μm^2 were used for these experiments, and the FIB-exposed area was 310 x 310 μm. The net oxide-trap charge density, ΔN_{ot}, was estimated from midgap voltage shifts in the C-V curves [4]. In all cases, midgap shifts were negative, indicating an excess of trapped positive charge (i.e., holes). Interface-trap densities were negligible in all capacitor tests performed here. The results of these tests are summarized in Table II.

Table II
Summary of C-V Measurements

Ion Dose	Biasing	Charge Neutrali-zation	ΔN_{ot} (10^{11} cm^{-2})
***p*-substrate**			
50 nm GOX			
0.01 nC/μm^2	pins floating	no	1.02
0.01 nC/μm^2	pins floating	yes	0.38
0.04 nC/μm^2	pins floating	no	2.59
0.04 nC/μm^2	pins grounded	no	0.82
0.04 nC/μm^2	+5 V	yes	2.20
0.04 nC/μm^2	+5 V	no	2.03
32 nm GOX			
0.04 nC/μm^2	pins grounded	no	0.22
0.04 nC/μm^2	+5 V	no	0.19
***n*-substrate**			
50 nm GOX			
0.01 nC/μm^2	pins floating	no	0.94
0.01 nC/μm^2	pins floating	yes	0.30
0.04 nC/μm^2	pins floating	no	1.65
0.04 nC/μm^2	pins grounded	no	1.02
0.04 nC/μm^2	-5 V	yes	0.33
0.04 nC/μm^2	-5 V	no	0.32
32 nm GOX			
0.04 nC/μm^2	pins grounded	no	0.23
0.04 nC/μm^2	-5 V	no	0.08

With no bias applied to the capacitors, ΔN_{ot} is 3 - 4 times greater when the floodgun is not used than when it is on, consistent with the observation that damage to the 3 μm transistors was minimized by using the floodgun. The net oxide-trap charge increased with ion dose. When the pins were grounded, the trap density was about half of what it was when the leads were electrically floating. When the capacitors were biased, there was a slight reduction in the net oxide-trap charge in the *p*-substrate, but ΔN_{ot} for the *n*-substrate capacitor decreased by almost an order of magnitude. Results under bias were not appreciably altered by using electron flood charge neutralization.

DISCUSSION

The I_d - V_{gs} curves for the 0.5 μm technology CMOS transistors exhibited appreciable subthreshold stretchout following FIB irradiation without charge neutralization, and a small amount of stretchout was observed for the 3 μm technology as well. The stretchout moves V_t to higher values for *n*-channel transistors and to lower (more negative) values for *p*-channel transistors - i.e., both *n*- and *p*-channel transistors move further into enhancement mode. Such stretchout is associated with the creation of interface traps [4,6]. These traps are amphoteric (i.e., can capture either holes or electrons) and capture majority carriers during post-irradiation testing. As a result, the absolute value of V_t increases for both *n*- and *p*-channel transistors, as observed. The decrease in mobility is also consistent with interface trapping of carriers, due to the high effectiveness of interface traps in increasing scattering rates as compared to oxide traps [7]. Moreover, interface-trap buildup can be quite sensitive to transistor geometry [8] and can recover with thermal annealing [6,9], consistent with our results.

The I_d - V_{gs} curves shift to less positive values following irradiation without charge neutralization for both *n*- and *p*-channel MOS transistors in the 1 μm technology. These shifts are consistent with net positive charge buildup in the oxide as the dominant damage mechanism [4]. Also, *n*-channel transistors in the 3 μm technology exhibited a shift to lower voltages as well as subthreshold stretchout. The FIB-induced parameter shifts are smaller for the 1 and 3 μm technologies than for the 0.5 μm technology over the range of doses explored. Whereas the parameter shifts increased linearly with the log of ion dose for the 0.5 μm technology, for the 1 and 3 μm technologies the parameter values are almost constant with increasing dose until an ion dose of ~ 0.1 nC/μm^2 is exceeded, and then a large increase is observed.

One possible mechanism leading to damage of the MOS transistors is FIB-induced charging; the effectiveness of electron flood charge neutralization in preventing damage supports this hypothesis. Energy from the ion beam could be coupled into the gate oxide or oxide/silicon interface during FIB irradiation, through the metal interconnects or via charge buildup in intermediate insulators. A charging mechanism requires that sufficiently high voltage is developed on the gate to produce electron-hole pairs, as well as that the electric field across the oxide is large enough to produce the band-bending needed for electron tunneling [10]. For the 13 nm gate oxide, it is estimated that 6 - 7 V on the gate could be sufficient to create interface traps, whereas > 25 V would be required to produce either oxide-trap or interface-trap charge in the 50 nm gate oxide [10]. The charging experiments described in the previous section indicate that a positive gate voltage develops during FIB irradiation when electron flood charge neutralization is not used. In most cases the V_g measured was only on the order of 0.5 - 1.5 V due to loading of the gate; however, the observed charge contrast suggests that fairly high voltages develop on the transistor gates during FIB irradiation. A charging mechanism would allow greater damage to occur for higher ion doses (as observed) because the electric field stress would be applied to the gate for a longer time and, in addition, a higher gate voltage may occur with longer stress times or higher beam currents. The details of charging in FIB-irradiation are not fully understood at this time, but could be similar to effects observed for plasma damage [11].

A second possible mechanism is ionizing radiation damage. Ionizing radiation-induced shifts in transistor parameters have been extensively studied and are generally attributed to carrier trapping in the gate oxide or at the interface between the gate oxide and the channel region [4,7]. However, in FIB irradiation the ions penetrate only a short distance (~ 30 nm) into the sample and should not produce x-rays that could penetrate into the gate oxide region and cause charge trapping. It is known that a low level of x-rays could be produced in the vicinity of the ion source and the electrostatic focusing lenses [12], but such x-rays would not be focused by the ion optics. Since it is clear that the damage is very localized (test transistors not exposed to the ion beam as little as 200 μm away from those that have received a FIB dose exhibit no parameter shifts), a localized production of an ionizing species is a more likely explanation.

In addition to x-rays, ionizing species include high energy electrons and UV photons. The incident Ga ions are much more efficient at transferring energy to the nucleus (which displaces the atom by a few nm) than to the electrons of atoms in the substrate. It is expected that most electrons produced in the substrate will have relatively low energy (2 - 20 eV, similar to the secondary electrons) and will be absorbed within a relatively short distance (a few nm) [12]. However, rare scattering events that produce electrons with energy > 10 keV, sufficient to penetrate to the gate oxide and cause radiation damage, cannot be ruled out.

It is known that photon emission occurs from excited neutral atoms sputtered from the surface and that the photon energies depend upon the electronic structure of the target atom. In the case of silicon, a low level of photons (~ 6 x 10^{-3} per incident ion) is produced in the ultraviolet range at 288 nm, and there is additional emission at 190 nm [13]. This suggests that during sputtering of SiO_2 or Si_3N_4 passivation layers, UV radiation would be generated near the sample surface, which would provide a more localized source of damage. UV photons with ~250 nm wavelength are typically used for erasure of data stored in UV erasable EPROMS [14], so it is expected that 288 nm UV photons would be able to penetrate to the gate region in the absence of an intervening metal layer. A problem with this explanation is that the bandgap of SiO_2 is 9 eV, while the UV photon energies arising from sputtered Si are only 4.4 and 6.7 eV. However, the gate oxide is surrounded by silicon (polysilicon above and Si substrate below), which could permit the introduction of holes into the oxide via anode hole injection [15].

Radiation effects in the 3 μm technology discussed here have previously been studied. For *p*-substrate capacitors (with 50 nm gate oxide), ΔN_{ot} in the previous work was 2.2 x 10^{11}/cm^2 for a radiation dose of 10 - 15 krad (SiO_2) with a +5 V bias [16]. A similar ΔN_{ot} was observed when the *p*-substrate capacitors received an ion dose of 0.04 nC/μm^2 with a +5 V bias both with and without charge neutralization in the FIB (see Table II), suggesting that ionizing radiation rather than charging may be the primary damage mechanism in this case. Further evidence in support of an ionizing radiation damage mechanism is found by comparing ΔN_{ot} for *p*-substrate capacitors with a thinner (32 nm radiation-hardened) gate oxide with low trapping efficiency (0.055) to the results for the 50 nm non-radiation-hardened gate oxide with high trapping efficiency (0.45) just discussed. If radiation damage has occurred, it is expected that [16]:

$$\frac{\Delta N_{ot(32nm)}}{\Delta N_{ot(50nm)}} = \frac{f_{ot(32nm)} \times t_{ox(32nm)}}{f_{ot(50nm)} \times t_{ox(50nm)}} \cong 0.08$$

where f_{oi} is the trapping efficiency and t_{ox} is the oxide thickness. The measured ratio of ΔN_{ot} for the two cases is 0.09 for +5 V gate bias (Table II), in excellent agreement with the prediction for radiation damage.

A difficulty with attributing charge trapping in the capacitor experiments to UV radiation damage is the top metallization (Al) on the capacitors, which does not transmit UV photons. The damage to

these metallized capacitors means that the production of either high energy electrons or x-rays, although seemingly unlikely, should not be ruled out entirely. Given that the charge on each Ga ion is 1.6 x 10^{-19} C, a dose of 0.04 nC/μm^2 corresponds to ~3 x 10^{16} ions/cm^2. This implies that each ion must create ~ 1.4 x 10^{-5} electron-hole pairs in the 50 nm oxide (the trapping efficiency is ~ 0.45). In other words, because ΔN_{ot} is low compared with the number of incident ions, it is possible that the production of high energy electrons and/or x-rays via low probability scattering events could produce sufficient electron-hole pairs to explain the observed development of oxide-trap charge in the capacitor experiments reported here.

In transistor structures without an overlying metal layer, UV irradiation would still need to be considered as a possible damage mechanism. For example, an ion dose of 0.04 nC/μm^2 corresponds to ~ 3 x 10^{16} ions/cm^2, implying UV photon production of ~2 x 10^{14}/cm^2. If UV is a damage mechanism and if each UV photon produces ~ 2 x 10^{-3} electron-hole pairs in the oxide (again, assuming a trapping efficiency of ~ 0.45 [16]), it would be possible to generate ΔN_{ot} = 2 x 10^{11} in the 50 nm oxide discussed above. The efficiency of UV photons in producing electron-hole pairs is not known for FIB applications, but could be sufficiently high given that UV production occurs close to the sample surface.

The preceding discussion indicates that it is plausible for ionizing radiation generated during FIB irradiation to cause oxide-trap charge damage in the 3 μm technology capacitors, and that the same mechanism could lead to the formation of oxide-trap charge and/or interface traps in transistor gate oxides. Clearly, further study will be required to fully understand the possible ionizing-radiation damage mechanisms related to FIB exposure of transistors and capacitors.

Analysis of the changes in C-V curves for the irradiated capacitors provides arguments for both charging and ionizing radiation as damage mechanisms, at least for the 3 μm technology. When the device pins were floating during FIB exposure, it was found (Table II) that use of electron flood charge neutralization reduced ΔN_{ot}, suggesting that the damage is charging related. However, when the pins were biased, the electron floodgun made very little difference in the C-V curve. This suggests that charging plays a role in oxide degradation of these capacitors unless the pins are biased or grounded, and is consistent with the finding that parameter shifts occurred for packaged transistors when the pins were floating but not when biased or grounded.

It is highly unlikely that mobile ionic charges are the cause of post-FIB parameter shifts. The action of mobile ionic charges would not produce subthreshold stretchout (and so could not explain the effects in the 0.5 and 3 μm technologies) [17]. Further, no significant motion of mobile ions at short times would be expected at +5 or -5 V bias at room temperature [17].

Our findings indicate that the ion dose during navigation should be kept to a minimum if the IC will be tested or used following FIB modification. The ion dose is minimized by using the minimum possible beam current, a short pixel dwell time, and the minimum number of pixels in the image. Figures 5 - 7 show the effectiveness of electron flood charge neutralization in minimizing changes in transistor parameters for ion doses less than 10^{-4} nC/μm^2. This suggests that charge neutralization should be used whenever possible during FIB modification of ICs, particularly when larger beam currents are used. In some cases, it is necessary to obtain an electron mode image (i.e., without charge neutralization) of an area. Under those circumstances, the minimum possible ion dose should be used and other charge neutralization strategies (such as the application of a thin, conductive carbon coating) could be employed. Such approaches have not been considered in this study but are of interest.

The present results indicate an increased ESD susceptibility of packaged transistors (with pins floating) relative to those on a wafer (with substrate grounded). In an IC, these effects would be mitigated by the fact that a given transistor would be connected to other transistors and thus have charge dissipation paths. The different degrees of damage observed for transistors on wafers (substrate grounded) and in packages (pins floating and grounded) are not fully understood, but point to the importance of good sample grounding.

CONCLUSIONS

This work demonstrates that MOS transistors can experience significant parameter shifts when exposed to FIB irradiation. Evidence of both interface-trap and oxide-trap charge generation has been found. The extent of the parameter shifts as well as the type of damage that occurs (interface or oxide-trap charge) depends upon the transistor technology, transistor geometry, processing details, layout, and biasing conditions. Two possible damage mechanisms, charging and ionizing radiation, were discussed. Both oxide-trap charge and interface-trap charge effects are minimized by the use of electron flood charge neutralization. In addition, it has been shown that interface trap charge damage in the 0.5 μm technology can be mitigated by post-FIB annealing.

There are a number of issues that have not yet been fully understood relating to the work presented here, such as the differences in FIB effects on *n*- and *p*-channel transistors in the same technology. The mechanism by which the apparent radiation damage is generated also needs to be more fully explored. Further study will be required to fully characterize the effects and damage mechanisms of FIB-irradiation on transistors and ICs.

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